PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
NXP B.V.	06/28/2011

RECEIVING PARTY DATA

Name:	Nytell Software LLC
Street Address:	2711 Centerville Rd.
Internal Address:	Suite 400, Attn: Dept. 307
City:	Wilmington
State/Country:	DELAWARE
Postal Code:	19808

PROPERTY NUMBERS Total: 20

Property Type	Number
Application Number:	10535591
Application Number:	11719399
Application Number:	11994245
Application Number:	11995091
Application Number:	12518485
Application Number:	12518500
Application Number:	12523388
Application Number:	12531726
Application Number:	12090689
Application Number:	08496630
Application Number:	09009751
Application Number:	08649732
Application Number:	09805384
Application Number:	09887463

CH $800.00 10535591

Application Number:	10136732
Application Number:	10226158
Application Number:	10218074
Application Number:	09868797
Application Number:	10496537
Application Number:	10511512

CORRESPONDENCE DATA

Fax Number: (312)775-8100
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.
Phone: 3127758000
Email: mhmpto@mcandrews-ip.com
Correspondent Name: Peter J. McAndrews
Address Line 1: 500 W. Madison St.
Address Line 2: 34th Floor
Address Line 4: Chicago, ILLINOIS 60661

ATTORNEY DOCKET NUMBER:	24436US02 - 24459US01
NAME OF SUBMITTER:	Peter J. McAndrews

Total Attachments: 20
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Exhibit B

ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, NXP B.V., a company formed in The Netherlands, with an office at High Tech Campus 60, 5656 AG Eindhoven, The Netherlands (***"Assignor"***), does hereby sell, assign, transfer, and convey unto Nytell Software LLC, a Delaware limited liability company, having an address at 2711 Centerville Rd, Suite 400, Attn: Dept. 307, Wilmington, DE 19808 (***"Assignee"***), or its designees, all right, title, and interest that exist today and may exist in the future in and to any and all of the following (collectively, the ***"Patent Rights"***):

(a) the provisional patent applications, patent applications and patents listed in the table below (the "***Patents***");

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
10/535591	US	11/11/2003	Using a cache miss pattern to address a stride prediction table Van De Waerdt, Jan-Willem
11/719399	US	11/15/2005	Cache with prefetch Van De Waerdt, Jan-Willem
11/994245	US	06/30/2006	Multi-phase frequency divider Song, Wenyi
CN200680023846.0	CN	06/30/2006	Multi-phase frequency divider Song, Wenyi
EP06765981.3	EP	06/30/2006	Multi-phase frequency divider Song, Wenyi
11/995091	US	07/14/2006	Using historic load profiles to dynamically adjust operating frequency and available power to a handheld multimedia device processor core Koul, Manoj

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
CN200680025395.4	CN	07/14/2006	Using historic load profiles to dynamically adjust operating frequency and available power to a handheld multimedia device processor core Koul, Manoj
EP06780089.6	EP	07/14/2006	Using historic load profiles to dynamically adjust operating frequency and available power to a handheld multimedia device processor core Koul, Manoj
12/518485	US	12/11/2007	Pipelined processor and compiler/scheduler for variable number branch delay slots Van De Waerdt, Jan-Willem
12/518500	US	12/11/2007	Virtual functional units for VLIW processors Van De Waerdt, Jan-Willem
CN200780045552.2	CN	12/11/2007	Virtual functional units for VLIW processors Van De Waerdt, Jan-Willem
EP07849416.8	EP	12/11/2007	Virtual functional units for VLIW processors Van De Waerdt, Jan-Willem
12/523388	US	01/24/2008	Hardware triggered data cache line pre-allocation Van De Waerdt, Jan-Willem
CN200880002944.5	CN	01/24/2008	Hardware triggered data cache line pre-allocation Van De Waerdt, Jan-Willem
GB2115598	GB	01/24/2008	Hardware triggered data cache line pre-allocation Van De Waerdt, Jan-Willem
FR2115598	GB	01/24/2008	Hardware triggered data cache line pre-allocation Van De Waerdt, Jan-Willem

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
DE602008005851.4	DE	01/24/2008	Hardware triggered data cache line pre-allocation Van De Waerdt, Jan-Willem
12/531726	US	03/26/2008	Electronic device and method determining a workload of an electronic device Burchard, Artur T.
CN200880010262.9	CN	03/26/2008	Electronic device and method determining a workload of an electronic device Burchard, Artur T.
EP08719838.8	EP	03/26/2008	Electronic device and method determining a workload of an electronic device Burchard, Artur T.
12/090689	US	10/18/2006	Cache with high access store bandwidth Van De Waerdt, Jan-Willem
CNZL200680038522.4	CN	10/18/2006	Cache with high access store bandwidth Van De Waerdt, Jan-Willem
EP06809640.3	EP	10/18/2006	Cache with high access store bandwidth Van De Waerdt, Jan-Willem
JP2008-536192	JP	10/18/2006	Cache with high access store bandwidth Van De Waerdt, Jan-Willem
5815701	US	06/29/1995	Computer method and apparatus which maintains context switching speed with a large number of registers and which improves interrupt processing time Slavenburg, Gerrit Ary

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
5978910	US	01/20/1998	Performing pending interrupts or exceptions when interruptible jumps are detected Slavenburg, Gerrit Ary
5826054	US	05/15/1996	Compressed instruction format for use in a VLIW processor Jacobs, Eino
6704859	US	08/04/1998	Compressed instruction format for use in a VLIW processor Jacobs, Eino
10/762863	US	01/22/2004	Compressed instruction format for use in a VLIW processor Jacobs, Eino
DE69728495.6	DE	05/15/1997	VLIW processor which processes compressed instruction format Jacobs, Eino
FR0843848	FR	05/15/1997	VLIW processor which processes compressed instruction format Jacobs, Eino
GB0843848	GB	05/15/1997	VLIW processor which processes compressed instruction format Jacobs, Eino
JP3750821	JP	05/15/1997	VLIW processor which processes compressed instruction format Jacobs, Eino
5862398	US	05/15/1996	Compiler generating swizzled instructions usable in a simplified cache layout Hampapuram, Hari
CNZL97190850.8	CN	05/14/1997	Processor with instruction cache Ang, Michael

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
DE69723804.0	DE	05/14/1997	Processor with an instruction cache Ang, Michael
FR0846291	FR	05/14/1997	Processor with an instruction cache Ang, Michael
GB0846291	GB	05/14/1997	Processor with an instruction cache Ang, Michael
JP3706633	JP	05/14/1997	Processor with an instruction cache Ang, Michael
6643739	US	03/13/2001	Cache way prediction based on instruction base register Van De Waerdt, Jan-Willem
EP02702599.8	EP	02/28/2002	Cache way prediction based on instruction base register Van De Waerdt, Jan-Willem
JP4137641	JP	02/28/2002	Cache way prediction based on instruction base register Van De Waerdt, Jan-Willem
KR10-0831557	KR	02/28/2002	Cache way prediction based on instruction base register Van De Waerdt, Jan-Willem
6678792	US	06/22/2001	Fast and accurate cache way selection Van De Waerdt, Jan-Willem
CNZL02812403.0	CN	06/18/2002	Fast and accurate cache way selection Van De Waerdt, Jan-Willem
EP02735878.7	EP	06/18/2002	Fast and accurate cache way selection Van De Waerdt, Jan-Willem

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
6760818	US	05/01/2002	Memory region based data pre-fetching Van De Waerdt, Jan-Willem
CNZL03809724.9	CN	04/22/2003	Memory region based data pre-fetching Van De Waerdt, Jan-Willem
JP4566737	JP	04/22/2003	Memory region based data pre-fetching Van De Waerdt, Jan-Willem
7162588	US	08/23/2002	Processor prefetch to match memory bus protocol characteristics Van De Waerdt, Jan-Willem
CNZL03819933.5	CN	08/15/2003	Processor prefetch to match memory bus protocol characteristics Van De Waerdt, Jan-Willem
EP03792594.8	EP	08/15/2003	Processor prefetch to match memory bus protocol characteristics Van De Waerdt, Jan-Willem
JP2004-530473	JP	08/15/2003	Processor prefetch to match memory bus protocol characteristics Van De Waerdt, Jan-Willem
7406569	US	08/12/2002	Instruction cache way prediction for jump targets Van De Waerdt, Jan-Willem
EP03784355.4	EP	08/11/2003	Instruction cache way prediction for jump targets Van De Waerdt, Jan-Willem
JP4195006	JP	08/11/2003	Instruction cache way prediction for jump targets Van De Waerdt, Jan-Willem
10/242785	US	09/13/2002	Translation lookaside buffer Stravers, Paulus

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
CNZL03821569.1	CN	09/12/2003	Translation lookaside buffer with partial tag hashed according to page size indicator Stravers, Paulus
EP03795156.3	EP	09/12/2003	Translation lookaside buffer with partial tag hashed according to page size indicator Stravers, Paulus
KR10-2005-7004205	KR	09/12/2003	Translation lookaside buffer with partial tag hashed according to page size indicator Stravers, Paulus
7080235	US	12/21/1999	Device and method for generating and executing compressed programs of a very long instruction word processor Weiss, Matthias
FR1145113	FR	12/21/1999	Device and method for generating and executing compressed programs of a very long instruction word processor Weiss, Matthias
GB1145113	GB	12/21/1999	Device and method for generating and executing compressed programs of a very long instruction word processor Weiss, Matthias
JP4486754	JP	12/21/1999	Device and method for generating and executing compressed programs of a very long instruction word processor Weiss, Matthias
7472257	US	11/20/2002	Rerouting VLIW instructions to accommodate execution units deactivated upon detection by dispatch units of dedicated instruction alerting multiple successive removed NOPs Pessolano, Francesco
CNZL02823521.5	CN	11/20/2002	VLIW architecture with power down instruction Pessolano, Francesco

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
EP02781573.7	EP	11/20/2002	VLIW architecture with power down instruction Pessolano, Francesco
JP2003-548078	JP	11/20/2002	Configurable processor, and instruction set, dispatch method, compilation method for such a processor Pessolano, Francesco
10/511512	US	04/01/2003	Multi-issue processor Leijten, Jeroen Anton Johan
CNZL03808679.4	CN	04/01/2003	Multi-issue processor Leijten, Jeroen Anton Johan
DE60333089.4	DE	04/01/2003	Multi-issue processor Leijten, Jeroen Anton Johan
FR1499960	FR	04/01/2003	Multi-issue processor Leijten, Jeroen Anton Johan
GB1499960	GB	04/01/2003	Multi-issue processor Leijten, Jeroen Anton Johan
JP4194953	JP	04/01/2003	Multi-issue processor Leijten, Jeroen Anton Johan
10/530495	US	10/01/2003	Data processing apparatus address range dependent parallelization of instructions Sethuraman, Ramanathan
CNZL200380101196.3	CN	10/01/2003	Data processing apparatus address range dependent parallelization of instructions Sethuraman, Ramanathan

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
EP03807932.3	EP	10/01/2003	Data processing apparatus address range dependent parallelization of instructions Sethuraman, Ramanathan
JP4283226	JP	10/01/2003	Data processing apparatus address range dependent parallelization of instructions Sethuraman, Ramanathan
7334111	US	01/11/2005	Method and related device for use in decoding executable code King, Colin I.
CNZL200580002293.6	CN	01/11/2005	Method and related device for use in decoding executable code King, Colin I
DE602005008196.8	DE	01/11/2005	Method and device for use in decoding executable code King, Colin I
FR1709533	FR	01/11/2005	Method and device for use in decoding executable code King, Colin I
GB1709533	GB	01/11/2005	Method and device for use in decoding executable code King, Colin I
JP2006-548546	JP	01/11/2005	Method and related device for use in decoding executable code King, Colin I.
CNZL200580017074.5	CN	05/18/2005	Microprocessor and method of instruction alignment Hoogerbrugge, Jan
DE602005007216.0	DE	05/18/2005	Microprocessor and method of instruction alignment Hoogerbrugge, Jan

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
FR1754142	FR	05/18/2005	Microprocessor and method of instruction alignment Hoogerbrugge, Jan
GB1754142	GB	05/18/2005	Microprocessor and method of instruction alignment Hoogerbrugge, Jan
7689975	US	04/13/2004	Processing of a compileable computer program Popp, Ondrej
CNZL200480010025.4	CN	04/13/2004	Regenerating header files out of preprocessed and afterwards modified source files Popp, Ondrej
KR10-2005-7019534	KR	04/13/2004	Regenerating header files out of preprocessed and afterwards modified source files Popp, Ondrej
11/814801	US	01/17/2006	Multi-threaded processor Hoogerbrugge, Jan
CNZL200680002878.2	CN	01/17/2006	Multi-threaded processor Hoogerbrugge, Jan
12/090028	US	10/10/2006	Program executable image encryption King, Colin I.
EP06809557.9	EP	10/10/2006	Program executable image encryption King, Colin I.
7287151	US	03/28/2002	Communication path to each part of distributed register file from functional units in addition to partial communication network Bekooij, Marco Jan Gerrit

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
JP3799041	JP	03/28/2002	VLIW processor Bekooij, Marco Jan Gerrit
KR10-0947446	KR	03/28/2002	VLIW processor Bekooij, Marco Jan Gerrit
12/306605	US	06/27/2007	Decoding sound parameters Szczerba, Marek Zbigniew
CN200780024376.4	CN	06/27/2007	Decoding sound parameters Szczerba, Marek
EP07789815.3	EP	06/27/2007	Decoding sound parameters Szczerba, Marek
JP2009-517552	JP	06/27/2007	Decoding sound parameters Gerrits, Andreas
7269720	US	04/04/2005	Dynamically controlling execution of operations within a multi-operation instruction Tromp, Marcel J. A.
7577827	US	02/28/2001	Data processor with multi-command instruction words Hoogerbrugge, Jan
DE60141807.7	DE	02/12/2001	Data processor with multi-command instruction words Hoogerbrugge, Jan
FR1236095	FR	02/12/2001	Data processor with multi-command instruction words Hoogerbrugge, Jan
GB1236095	GB	02/12/2001	Data processor with multi-command instruction words Hoogerbrugge, Jan

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
JP2001-563991	JP	02/12/2001	Data processor with multi-command instruction words Hoogerbrugge, Jan
7353337	US	02/23/2004	Reducing cache effects of certain code pieces Wester, Rogier
CNZL200480010956.4	CN	02/23/2004	Reducing cache trashing of certain pieces Wester, Rogier
DE602004023372.2	DE	02/23/2004	Reducing cache trashing of certain pieces Wester, Rogier
FR1599803	FR	02/23/2004	Reducing cache trashing of certain pieces Wester, Rogier
GB1599803	GB	02/23/2004	Reducing cache trashing of certain pieces Wester, Rogier
KR10-0985239	KR	02/23/2004	Reducing cache trashing of certain pieces Wester, Rogier
5692139	US	04/19/1995	VLIW processing device including improved memory for avoiding collisions without an excessive number of ports Slavenburg, Gerrit Ary
DE69130723.7	DE	10/03/1991	Processing device including a memory circuit and a group of functional units Slavenburg, Gerrit Ary
FR0479390	FR	10/03/1991	Processing device including a memory circuit and a group of functional units Slavenburg, Gerrit Ary

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
GB0479390	GB	10/03/1991	Processing device including a memory circuit and a group of functional units Slavenburg, Gerrit Ary
JP3687982	JP	10/04/1991	Processor equipped with memory circuit and group of functioning unit Slavenburg, Gerrit Ary
KR10-0242619	KR	10/05/1991	Multiport memory bypass under software control Slavenburg, Gerrit Ary
5450556	US	10/25/1993	VLIW processor which uses path information generated by a branch control unit to inhibit operations which are not on a correct path Slavenburg, Gerrit Ary
5832202	US	12/16/1994	Exception recovery in a data processing system Slavenburg, Gerrit Ary
6370623	US	12/30/1994	Multiport register file to accommodate data of differing lengths Mehra, Vijay K.
6002880	US	03/03/1997	VLIW processor with less instruction issue slots than functional units Slavenburg, Gerrit Ary
6122722	US	03/17/1999	VLIW processor with less instruction issue slots than functional units Slavenburg, Gerrit Ary
DE69129569.7	DE	09/02/1991	Very long instruction word machine for efficient execution of programs with conditional branches Slavenburg, Gerrit Ary

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
DE69325785.7	DE	12/24/1993	Improved very long instruction word processor architecture Slavenburg, Gerrit Ary
DE69525527.4	DE	11/16/1995	Plural multiport register file to accommodate data of differing lengths Mehra, Vijay K.
FR0474297	FR	09/02/1991	Very long instruction word machine for efficient execution of programs with conditional branches Slavenburg, Gerrit Ary
FR0605927	FR	12/24/1993	Improved very long instruction word processor architecture Slavenburg, Gerrit Ary
FR0748477	FR	11/16/1995	Plural multiport register file to accommodate data of differing lengths Mehra, Vijay K.
GB0474297	GB	09/02/1991	Very long instruction word machine for efficient execution of programs with conditional branches Slavenburg, Gerrit Ary
GB0605927	GB	12/24/1993	Improved very long instruction word processor architecture Slavenburg, Gerrit Ary
GB0748477	GB	11/16/1995	Plural multiport register file to accommodate data of differing lengths Mehra, Vijay K.
GB0745241	GB	11/21/1995	Exception recovery in a data processing system Slavenburg, Gerrit Ary
IT0605927	IT	12/24/1993	Improved very long instruction word processor architecture Slavenburg, Gerrit Ary

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
JP3098071	JP	09/05/1991	Computer system for efficiently executing program having conditioned branch Slavenburg, Gerrit Ary
JP3916680	JP	12/28/1993	Processor Slavenburg, Gerrit Ary
JP3591842	JP	11/16/1995	Plural multiport register file to accommodate data of differing lengths Mehra, Vijay K.
KR10-0242617	KR	09/05/1991	Exception recovery in a data processing system Slavenburg, Gerrit Ary
KR10-0290325	KR	12/28/1993	Long instruction word processor architecture Slavenburg, Gerrit Ary
7293258	US	05/17/2000	Data processor and method for using a data processor with debug circuit Vranken, Hendrikus Petrus Elisabeth
DE60012661.7	DE	05/01/2000	Data processor with a debug circuit Vranken, Hendrikus Petrus Elisabeth
FR1099166	FR	05/01/2000	Data processor with a debug circuit Vranken, Hendrikus Petrus Elisabeth
GB1099166	GB	05/01/2000	Data processor with a debug circuit Vranken, Hendrikus Petrus Elisabeth
JP2000-620478	JP	05/01/2000	Data processor with a debug circuit Vranken, Hendrikus Petrus Elisabeth

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
KR10-0705847	KR	05/01/2000	Data processor with a debug circuit Vranken, Hendrikus Petrus Elisabeth
7827372	US	08/17/2004	Intergrated circuit and a method of cache remapping Bink, Adrianus Josephus
CNZL200480025280.6	CN	08/17/2004	Integrated circuit and a method of cache remapping Bink, Adrianus Josephus
DE602004007532.9	DE	08/17/2004	Integrated circuit and a method of cache remapping Bink, Adrianus Josephus
FR1665286	FR	08/17/2004	Integrated circuit and a method of cache remapping Bink, Adrianus Josephus
GB1665286	GB	08/17/2004	Integrated circuit and a method of cache remapping Bink, Adrianus Josephus
11/916328	US	05/31/2006	Data processing system and method for scheduling the use of at least one exclusive resource Dijkstra, Hendrik
CNZL200680019523.4	CN	05/31/2006	Data processing system and method for scheduling the use of at least one exclusive resource Dijkstra, Hendrik
EP06756027.6	EP	05/31/2006	Data processing system and method for scheduling the use of at least one exclusive resource Dijkstra, Hendrik
JP4673408	JP	05/31/2006	Data processing system and method for scheduling the use of at least one exclusive resource Dijkstra, Hendrik

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
12/673898	US	08/15/2008	Data processing with protection against soft errors Hoogerbrugge, Jan
CN200880102796.4	CN	08/15/2008	Data processing with protection against soft errors Hoogerbrugge, Jan
EP08807332.5	EP	08/15/2008	Data processing with protection against soft errors Hoogerbrugge, Jan
12/682789	US	10/16/2008	Circuit and method with cache coherence stress control Karlapalem, Sainath
CN200880111554.1	CN	10/16/2008	Circuit and method with cache coherence stress control Karlapalem, Sainath
EP08840774.7	EP	10/16/2008	Circuit and method with cache coherence stress control Karlapalem, Sainath
6886091	US	06/29/2001	Replacing VLIW operation with equivalent operation requiring fewer issue slots Vissers, Kornelis A.
5852741	US	05/15/1996	VLIW processor which processes compressed instruction format Jacobs, Eino
6131152	US	05/15/1996	Planar cache layout and instruction stream therefor Ang, Michael
CNZL200480037421.6	CN	11/30/2004	Memory-efficient instruction processing scheme Dytrych, Peter
DE602004019346.1	DE	11/30/2004	Memory-efficient instruction processing scheme Dytrych, Peter

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
FR1697830	FR	11/30/2004	Memory-efficient instruction processing scheme Dytrych, Peter
GB1697830	GB	11/30/2004	Memory-efficient instruction processing scheme Dytrych, Peter
JP2006-544614	JP	11/30/2004	Memory-efficient instruction processing scheme Dytrych, Peter
7716456	US	11/30/2004	Memory-efficient instruction processing scheme Dytrych, Peter

(b) all patents and patent applications (i) to which any of the Patents directly or indirectly claims priority, (ii) for which any of the Patents directly or indirectly forms a basis for priority, and/or (iii) that were co-owned applications that incorporate by reference, or are incorporated by reference into, the Patents;

(c) all reissues, reexaminations, extensions, continuations, continuations in part, continuing prosecution applications, requests for continuing examinations, divisions, registrations of any item in any of the foregoing categories (a) and (b);

(d) all foreign patents, patent applications, and counterparts relating to any item in any of the foregoing categories (a) through (c), including, without limitation, certificates of invention, utility models, industrial design protection, design patent protection, and other governmental grants or issuances;

(e) all items in any of the foregoing in categories (b) through (d), whether or not expressly listed as Patents below and whether or not claims in any of the foregoing have been rejected, withdrawn, cancelled, or the like;

(f) inventions, invention disclosures, and discoveries described and enabled in any of the Patents and/or any item in the foregoing categories (b) through (e) that (i) are included in any claim in the Patents and/or any item in the foregoing categories (b) through (e), (ii) are subject matter capable of being reduced to a patent claim in a reissue or reexamination proceeding brought on any of the Patents and/or any item in the foregoing categories (b) through (e), and/or (iii) could have been included as an allowable claim in any

of the Patents and/or any item in the foregoing categories (b) through (e) under applicable patent laws;

(g) all rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections, or other governmental grants or issuances of any type related to any item in any of the foregoing categories (a) through (f), including, without limitation, under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement, or understanding;

(h) all causes of action (whether known or unknown or whether currently pending, filed, or otherwise) and other enforcement rights under, or on account of, any of the Patents and/or any item in any of the foregoing categories (b) through (g), including, without limitation, all causes of action and other enforcement rights for

(1) damages,
(2) injunctive relief, and
(3) any other remedies of any kind

for past, current, and future infringement; and

(i) all rights to collect royalties and other payments under or on account of any of the Patents and/or any item in any of the foregoing categories (b) through (h).

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

The terms and conditions of this Assignment of Patent Rights will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed at Newburgh, NY on 28 June, 2011.

ASSIGNOR:

NXP B.V.

By: _____
Name: Aaron Waxler
Title: Authorized Signatory
(Signature MUST be attested)

ATTESTATION OF SIGNATURE PURSUANT TO 28 U.S.C. § 1746

The undersigned witnessed the signature of Aaron Waxer to the above Assignment of Patent Rights on behalf of NXP B.V. and makes the following statements:

1. I am over the age of 18 and competent to testify as to the facts in this Attestation block if called upon to do so.

2. Aaron Waxer is personally known to me (or proved to me on the basis of satisfactory evidence) and appeared before me on 28 June, 2011 to execute the above Assignment of Patent Rights on behalf of NXP B.V.

3. Aaron Waxer subscribed to the above Assignment of Patent Rights on behalf of NXP B.V.

I declare under penalty of perjury under the laws of the United States of America that the statements made in the three (3) numbered paragraphs immediately above are true and correct.

EXECUTED on 28 June, 2011 (date)

Print Name: Shejieca Brazil