PATENT ASSIGNMENT

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
NXP B.V.	06/28/2011

RECEIVING PARTY DATA

Name:	Nytell Software LLC
Street Address:	2711 Centerville Road
Internal Address:	Suite 400, Att: Dept. 307
City:	Wilmington
State/Country:	DELAWARE
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PROPERTY NUMBERS Total: 23

Property Type	Number
Application Number:	60428285
Application Number:	60627870
Application Number:	60696489
Application Number:	60748335
Application Number:	60874530
Application Number:	60874529
Application Number:	60886598
Application Number:	60728576
Application Number:	08649731
Application Number:	09086696
Application Number:	11597872
Application Number:	09895582
Application Number:	60448871
Application Number:	07290979

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Application Number:	07594534
Application Number:	07654847
Application Number:	08063850
Application Number:	07578976
Application Number:	07998080
Application Number:	08445963
Application Number:	08715060
Application Number:	09090038
Application Number:	60699837

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ATTORNEY DOCKET NUMBER:	24436US01 - 24480US01
NAME OF SUBMITTER:	Peter J. McAndrews

Total Attachments: 14
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Exhibit C

ASSIGNMENT OF RIGHTS IN CERTAIN ASSETS

For good and valuable consideration, the receipt of which is hereby acknowledged, NXP B.V., a company formed in The Netherlands, with an office at High Tech Campus 60, 5656 AG Eindhoven, The Netherlands (***"Assignor"***), does hereby sell, assign, transfer, and convey unto Nytell Software LLC, a Delaware limited liability company, having an address at 2711 Centerville Rd, Suite 400, Attn: Dept. 307, Wilmington, DE 19808 (***"Assignee"***), or its designees, the right, title, and interest in and to any and all of the following provisional patent applications, patent applications, patents, and other governmental grants or issuances of any kind (the "***Certain Assets***") on an as is and where is basis:

Patent or Application No.	**Country**	**Filing Date**	**Title of Patent and First Named Inventor**
60/428285	US	11/22/2002	Using a cache miss pattern to address a stride prediction table Van De Waerdt, Jan-Willem
CN200380103952.6	CN	11/11/2003	Using a cache miss pattern to address a stride prediction table Van De Waerdt, Jan-Willem
EP03772449.9	EP	11/11/2003	Using a cache miss pattern to address a stride prediction table Van De Waerdt, Jan-Willem
JP2004-554787	JP	11/11/2003	Using a cache miss pattern to address a stride prediction table Van De Waerdt, Jan-Willem
PCT/IB2003/005165	WO	11/11/2003	Using a cache miss pattern to address a stride prediction table Van De Waerdt, Jan-Willem
60/627870	US	11/15/2004	Cache with prefetch Van De Waerdt, Jan-Willem
CN200580038887.2	CN	11/15/2005	Cache with prefetch Van De Waerdt, Jan-Willem
EP05804160.9	EP	11/15/2005	Cache with prefetch Van De Waerdt, Jan-Willem
JP2007-540824	JP	11/15/2005	Cache with prefetch Van De Waerdt, Jan-Willem

KR10-2007-7013533	KR	11/15/2005	Cache with prefetch Van De Waerdt, Jan-Willem
PCT/IB2005/053767	WO	11/15/2005	Cache with prefetch Van De Waerdt, Jan-Willem
60/696489	US	06/30/2005	Multi-phase frequency divider Song, Wenyi
PCT/IB2006/052217	WO	06/30/2006	Multi-phase frequency divider Song, Wenyi
60/748335	US	12/06/2005	Using historic load profiles to dynamically adjust operating frequency and available power to a handheld multimedia device processor core Koul, Manoj
JP2008-521026	JP	07/14/2006	Using historic load profiles to dynamically adjust operating frequency and available power to a handheld multimedia device processor core Koul, Manoj
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60/874530	US	12/11/2006	Pipelined processor and compiler/scheduler for variable number branch delay slots Van De Waerdt, Jan-Willem
EP07849414.3	EP	12/11/2007	Pipelined processor and compiler/scheduler for variable number branch delay slots Van De Waerdt, Jan-Willem
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PCT/IB2008/050262	WO	01/24/2008	Hardware triggered data cache line pre-allocation Van De Waerdt, Jan-Willem
EP07105151.0	EP	03/28/2007	Electronic device and method determining a workload of an electronic device Burchard, Artur T.
PCT/IB2008/051124	WO	03/26/2008	Electronic device and method determining a workload of an electronic device Burchard, Artur T.
60/728576	US	10/19/2005	Cache with high access store bandwidth Van De Waerdt, Jan-Willem
PCT/IB2006/053847	WO	10/18/2006	Cache with high access store bandwidth Van De Waerdt, Jan-Willem
DE69621405.9	DE	06/26/1996	Processing system, processor, memory storing instruction stream and compiler Slavenburg, Gerrit, A.
EP0777877	EP	06/26/1996	Processing system, processor, memory storing instruction stream and compiler Slavenburg, Gerrit, A.
FR0777877	FR	06/26/1996	Processing system, processor, memory storing instruction stream and compiler Slavenburg, Gerrit, A.
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EP0843848	EP	05/15/1997	VLIW processor which processes compressed instruction format Jacobs, Eino
PCT/IB1997/000558	WO	05/15/1997	VLIW processor which processes compressed instruction format Jacobs, Eino
EP0846291	EP	05/14/1997	Processor with an instruction cache Ang, Michael
PCT/IB1997/000552	WO	05/14/1997	Processor with an instruction cache Ang, Michael
CN02800633.X	CN	02/28/2002	Cache way prediction based on instruction base register Van De Waerdt, Jan-Willem
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PCT/IB2002/002327	WO	06/18/2002	Fast and accurate cache way selection Van De Waerdt, Jan-Willem
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EP03715258.4	EP	04/22/2003	Memory region based data pre-fetching Van De Waerdt, Jan-Willem
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CN03819241.1	CN	08/11/2003	Instruction cache way prediction for jump targets Van De Waerdt, Jan-Willem
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PCT/IB2003/003915	WO	09/12/2003	Translation lookaside buffer with partial tag hashed according to page size indicator Stravers, Paulus
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EP1145113	EP	12/21/1999	Device and method for generating and executing compressed programs of a very long instruction word processor Weiss, Matthias
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KR10-2004-7007937	KR	11/20/2002	VLIW architecture with power down instruction Pessolano, Francesco
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EP1499960	EP	04/01/2003	Multi-issue processor Leijten, Jeroen A. J.
KR10-2004-7016702	KR	04/01/2003	Multi-issue processor Leijten, Jeroen A. J.
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EP1709533	EP	01/11/2005	Method and device for use in decoding executable code King, Colin I
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EP1754142	EP	05/18/2005	Microprocessor and method of instruction alignment Hoogerbrugge, Jan
JP2007-514241	JP	05/18/2005	Microprocessor and method of instruction alignment Hoogerbrugge, Jan
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JP2006-506834	JP	04/13/2004	Regenerating header files out of preprocessed and afterwards modified source files Popp, Ondrej
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JP2007-551782	JP	01/17/2006	Multi-threaded processor Hoogerbrugge, Jan
PCT/IB2006/050167	WO	01/17/2006	Multi-threaded processor Hoogerbrugge, Jan
CN200680038390.5	CN	10/10/2006	Program executable image encryption King, Colin I.
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EP1236095	EP	02/12/2001	Data processor with multi-command instruction words Hoogerbrugge, Jan
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60/448871	US	02/24/2003	Reducing cache effects of certain code pieces Wester, Rogier
EP1599803	EP	02/23/2004	Reducing cache trashing of certain pieces Wester, Rogier
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07/290979	US	12/28/1988	Video processor system, and also imaging system and image storage system provided with such a video processor system Sluijter, Robert J.
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DE68909425.6	DE	01/05/1989	Video processor system, and also imaging system and image storage system provided with such a video processor system Sluijter, Robert Johannes
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EP0479390	EP	10/03/1991	Processing device including a memory circuit and a group of functional units Slavenburg, Gerrit Ary
ES0325310	ES	01/05/1989	Video processor system, and also imaging system and image storage system provided with such a video processor system Sluijter, Robert Johannes
FI94991	FI	01/06/1989	Video processor system, and also imaging system and image storage system provided with such a video processor system. Sluijter, Robert Johannes
FR0325310	FR	01/05/1989	Video processor system, and also imaging system and image storage system provided with such a video processor system Sluijter, Robert Johannes
GB0325310	GB	01/05/1989	Video processor system, and also imaging system and image storage system provided with such a video processor system Sluijter, Robert Johannes
HK0950202	HK	01/05/1989	Video processor system, and also imaging system and image storage system provided with such a video processor system Sluijter, Robert Johannes
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07/578976	US	09/05/1990	Efficient execution of programs with conditional branches on very long instruction word machines Slavenburg, Gerrit Ary
07/998080	US	12/29/1992	VLIW processor with less instruction issue slots than functional units note: typographical error "vlim processor with less instruction issue slots than functional units" per application data tab of pair Slavenburg, Gerrit Ary
08/445963	US	05/22/1995	VLIW processor with less instruction issue slots than functional units Slavenburg, Gerrit Ary
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EP0745241	EP	11/21/1995	Exception recovery in a data processing system Slavenburg, Gerrit Ary
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KR10-1996-0704551	KR	11/21/1995	Exception recovery in a data processing system Slavenburg, Gerrit Ary
KR10-0389220	KR	11/16/1995	Plural multiport register file to accommodate data of differing lengths Mehra, Vijay K.
PCT/IB1995/001013	WO	11/16/1995	Plural multiport register file to accommodate data of differing lengths Mehra, Vijay K.
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PCT/EP2000/004195	WO	05/01/2000	Data processor with a debug circuit Vranken, Hendrikus Petrus Elisabeth
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EP1665286	EP	08/17/2004	Integrated circuit and a method of cache remapping Bink, Adrianus Josephus
IT1665286	IT	08/17/2004	Integrated circuit and a method of cache remapping Bink, Adrianus Josephus
JP2006-525220	JP	08/17/2004	Integrated circuit and a method of cache remapping Bink, Adrianus Josephus
PCT/IB2004/051465	WO	08/17/2004	Integrated circuit and a method of cache remapping Bink, Adrianus Josephus
EP05110338.0	EP	11/04/2005	Data processing system and method for scheduling the use of at least one exclusive resource Dijkstra, Hendrik
PCT/IB2006/051742	WO	05/31/2006	Data processing system and method for scheduling the use of at least one exclusive resource Dijkstra, Hendrik

EP07114487.7	EP	08/17/2007	Data processing with protection against soft errors Hoogerbrugge, Jan
PCT/IB2008/053284	WO	08/15/2008	Data processing with protection against soft errors Hoogerbrugge, Jan
EP07118763.7	EP	10/18/2007	Circuit and method with cache coherence stress control Karlapalem, Sainath
PCT/IB2008/054251	WO	10/16/2008	Circuit and method with cache coherence stress control Karlapalem, Sainath
60/699837	US	07/14/2005	Historic load profile statistical analysis for reduced/low power consumption in multimedia applications by dynamic computational power scalability Koul, Manoj
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EP02079219.8	EP	10/11/2002	Data processing apparatus address range dependent parallelization of instructions Sethuraman, Ramanathan
EP04102357.3	EP	05/27/2004	Microprocessor and method of instruction alignment Hoogerbrugge, Jan
EP03101032.5	EP	04/16/2003	Processing of a compileable program Popp, Ondrej
EP05100455.4	EP	01/25/2005	Multi-threaded processor Hoogerbrugge, Jan
EP05109642.8	EP	10/17/2005	Program executable image encryption King, Colin I.
EP06116297.0	EP	06/29/2006	Decoding sound parameters Szczerba, Marek

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EP99201568.5	EP	05/19/1999	Data processor and method for using a data processor with a debug circuit Vranken, Hendrikus Petrus Elisabeth
IT0748477	IT	11/16/1995	Plural multiport register file to accommodate data of differing lengths Mehra, Vijay K.
EP04727084.8	EP	4/13/2004	Regenerating header files out of preprocessed and afterwards modified source files Popp, Ondrej
EP03104704.6	EP	12/16/2003	Memory-efficient instruction processing scheme Dytrych, Peter
PCT/IB2004/052595	WO	11/30/2004	Memory-efficient instruction processing scheme Dytrych, Peter
EP1697830	EP	11/30/2004	Memory-efficient instruction processing scheme Dytrych, Peter
JP2008-519121	JP	06/30/2006	Multi-phase frequency divider Song, Wenyi
EP2115598	EP	01/24/2008	Hardware triggered data cache line pre-allocation Van De Waerdt, Jan-Willem
JP2004-535773	JP	09/12/2003	Translation lookaside buffer with partial tag hashed according to page size indicator Stravers, Paulus

Assignor assigns to Assignee all rights to the inventions, invention disclosures, and discoveries in the assets listed above, together, with the rights, if any, to revive prosecution of claims under such assets and to sue or otherwise enforce any claims under such assets for past, present or future infringement.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to make available to Assignee all records regarding the Certain Assets.

The terms and conditions of this Assignment of Rights in Certain Assets will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

DATED this 28th day of June 2011.

ASSIGNOR:

NXP B.V.

By: _____

Name: AARON WAXER

Title: AUTHORIZED SIGNATORY