PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Daniel E. Leckrone	08/11/2011
IntellaSys BEC Ltd.	08/11/2011

RECEIVING PARTY DATA

Name:	Technology Properties Limited LLC
Street Address:	20883 Stevens Creek Boulevard
Internal Address:	Suite 100
City:	Cupertino
State/Country:	CALIFORNIA
Postal Code:	95014

PROPERTY NUMBERS Total: 20

Property Type	Number
Patent Number:	5001367
Patent Number:	5030853
Patent Number:	5105105
Patent Number:	5247212
Patent Number:	5304874
Patent Number:	5305269
Patent Number:	5357480
Patent Number:	5363001
Patent Number:	5365483
Patent Number:	5384730
Patent Number:	5388075
Patent Number:	5391949
Patent Number:	5396457

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Patent Number:	5424980
Application Number:	07940299
Application Number:	08202414
PCT Number:	US9001957
PCT Number:	US9200869
PCT Number:	US9204630
PCT Number:	US9308232

CORRESPONDENCE DATA

Fax Number: (408)446-4690
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Address Line 2: Suite 100
Address Line 4: Cupertino, CALIFORNIA 95014

ATTORNEY DOCKET NUMBER:	TBIRD
NAME OF SUBMITTER:	Mark Salvatore

Total Attachments: 7
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ASSIGNMENT

This instrument of assignment ("Assignment") is entered into by and between Daniel E. Leckrone hereinafter sometimes "DEL", and IntellaSys BEC Ltd. hereinafter sometimes "BEC" on the one hand, and Technology Properties Limited LLC hereinafter sometimes "TPL LLC", the successor-in-interest to Technology Properties Limited on the other hand.

WHEREAS, the Patents and related materials described in the Schedule made a part hereof as Attachment I are commonly known as the "Fast Logic Portfolio" and arose out of the employment of the Inventors by Thunderbird Technology, Inc. ("TTI");

WHEREAS, BEC may have acquired and/or retained certain rights from TTI or others with respect to the sale of products which utilize technology protected by the Fast Logic Portfolio;

WHEREAS, SRAM Products LLC ("SPL") may have acquired and/or retained certain rights from TTI or others with respect to the sale of products which utilize technology protected by the Fast Logic Portfolio; and,

WHEREAS, DEL was the sole Member of SPL at the time of its dissolution/cancellation in 2010 and accordingly, is the successor-in-interest to any residual rights to the Fast Logic Portfolio which may have been owned by SPL at the time of its said dissolution/cancellation.

NOW THEREFORE, for and in consideration of the mutual covenants herein contained as well as of other good and valuable consideration the receipt and sufficiency of which is hereby acknowledged, it is covenanted and agreed by and between the parties hereto that:

1. By these presents, BEC hereby grants, sets over, assigns, transfers, conveys, and acquits unto TPL all of its right, title, and interest of whatsoever kind or nature in and to the Patents and related materials described in the Schedule made a part hereof as Attachment I commonly known as the "Fast Logic Portfolio".

2. By these presents, DEL hereby grants, sets over, assigns, transfers, conveys, and acquits unto TPL all of his

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right, title, and interest of whatsoever kind or nature in and to the Patents and related materials described in the Schedule made a part hereof as Attachment I commonly known as the "Fast Logic Portfolio".

IN WITNESS WHEREOF, the parties have hereunto set their hands and seals this 11th day of August, 2011.

DANIEL E. LECKRONE

by: _____
Daniel E. Leckrone

INTELLASYS BEC LTD

by: _____
Daniel E. Leckrone
Chmn & Sole Shareholder

Attachments:

I. Schedule of Fast Logic Patents

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ATTACHMENT I
Schedule of Fast Logic Patents

Title	App. #	Country	Patent
Random Access Memory Architecture Including Primary and Signal Bit Lines and Coupling Means Therefor	08/201,858	US	5,365,483
Data Input Register for Random Access Memory	08/202,296	US	5,363,001
Address Change Detecting System for a Memory	08/201,982	US	5,357,480
Differential Latching Inverter Circuit	08/287,713	US	5,391,949
Differential Latching Inverter and Random Access Memory Using Same	08/202,414	US	
Complementary Logic Input Parallel (CLIP) Logic Circuit Family	07/648,219	US	5,247,212
Self-Timing Random Access Memory	08/202,041	US	5,424,980
Differential Latching Inverter and Random Access Memory Using Same	07/742,649	US	5,305,269
High Speed Logic and Memory Family Using Ring Segment Buffer	07/497,103	US	5,030,853
High Speed Complementary Field Effect Transistor Logic Circuits	07/338,280	US	5,001,367
Coincident Activation of Pass Transistors in a Random Access Memory	08/216,776	US	5,384,730

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Schedule of Fast Logic Patents

Coincident Activation of Pass Transistors in a Random Access Memory	07/940,299	US	
High Speed Logic and Memory Family Using Ring Segment Buffer	07/687,756	US	5,105,105
Read and Write Timing System for Random Access Memory	08/201,640	US	5,388,075
Random Access Memory Including or Gate Sensing Networks	08/202,531	US	5,396,457
Differential Latching Inverter and Random Access Memory Using Same	07/708,459	US	5,304,874
Coincident Activation of Pass Transistors in a Random Access Memory	2141860	Canada	
Complementary Logic Input Parallel (CLIP) Logic Circuit Family	2101559	Canada	2101559
Differential Latching Inverter and Random Access Memory Using Same	2109835	Canada	2109835
High Speed Complementary Field Effect Transistor Logic Circuits	2051103	Canada	2051103
High Speed Complementary Field Effect Transistor Logic Circuits	90906650.8	EPO	EP 0467971
Complementary Logic Input Parallel (CLIP) Logic Circuit Family	92906350.1	EPO	EP 0569540

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Schedule of Fast Logic Patents

Differential Latching Inverter and Random Access Memory Using Same	92913329.6	EPO	EP 0587753
Differential Latching Inverter and Random Access Memory Using Same	92913329.6	EPO	EP 0587753
Coincident Activation of Pass Transistors in a Random Access Memory	93921284.1	EPO	
Differential Latching Inverter and Random Access Memory Using Same	92913329.6	France	0587753
High Speed Complementary Field Effect Transistor Logic Circuits	90906650.8	France	0467971
Complementary Logic Input Parallel (CLIP) Logic Circuit Family	92906350.1	France	0569540
High Speed Complementary Field Effect Transistor Logic Circuits	90906650.8	Germany	DE 69013498
Complementary Logic Input Parallel (CLIP) Logic Circuit Family	92906350.1	Germany	DE 69204659
Differential Latching Inverter and Random Access Memory Using Same	92913329.6	Germany	69205682.3
High Speed Complementary Field Effect Transistor Logic Circuits	90906650.8	Italy	0467971
Complementary Logic Input Parallel (CLIP) Logic Circuit Family	92906350.1	Italy	0569540

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Schedule of Fast Logic Patents

High Speed Complementary Field Effect Transistor Logic Circuits	1990-506467	Japan	JP 2839368
Complementary Logic Input Parallel (CLIP) Logic Circuit Family	505756	Japan	JP 3242650
Differential Latching Inverter and Random Access Memory Using Same	500623/1993	Japan	
Coincident Activation of Pass Transistors in a Random Access Memory	507418/94	Japan	
Complementary Logic Input Parallel (CLIP) Logic Circuit Family	1993-702251	Korea	0221565
Coincident Activation of Pass Transistors in a Random Access Memory	700835/95	Korea	
Differential Latching Inverter and Random Access Memory Using Same	1993-0703674	Korea	0264139
High Speed Complementary Field Effect Transistor Logic Circuits	90906650.8	Netherlands	0467971
Complementary Logic Input Parallel (CLIP) Logic Circuit Family	92906350.1	Netherlands	0569540
Differential Latching Inverter and Random Access Memory Using Same	92913329.6	Netherlands	0587753
Coincident Activation of Pass Transistors in a Random Access Memory	PCT/US1993/008232	PCT	

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Schedule of Fast Logic Patents

Differential Latching Inverter and Random Access Memory Using Same	PCT/US1992/004630	PCT	
Complementary Logic Input Parallel (CLIP) Logic Circuit Family	PCT/US1992/000869	PCT	
High Speed Complementary Field Effect Transistor Logic Circuits	PCT/US1990/001957	PCT	
Differential Latching Inverter and Random Access Memory Using Same	92913329.6	United Kingdom	0587753
High Speed Complementary Field Effect Transistor Logic Circuits	90906650.8	United Kingdom	0467971
Complementary Logic Input Parallel (CLIP) Logic Circuit Family	92906350.1	United Kingdom	0569540

This Schedule of Patents shall be deemed to include the items listed above, as well as all progenitors and progeny thereof and all additions, changes, amendments, modifications, actions, counterparts, continuations, continuations-in-part, extensions, reissues, divisionals and/or renewals of such progenitors and progeny, as well as all inventions disclosed in any such patents, progenitors, or progeny.

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