PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE BY SECURED PARTY

CONVEYING PARTY DATA

Name	Execution Date
Silicon Valley Bank	08/26/2011

RECEIVING PARTY DATA

Name:	NetLogic Microsystems, Inc.
Street Address:	3975 Freedom Circle, 9th Floor
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PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	10329246

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CH $40.00 10329246

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NAME OF SUBMITTER:	Katayoun Ghazian

Total Attachments: 20
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RELEASE OF INTELLECTUAL PROPERTY SECURITY AGREEMENT
COVERING INTERESTS IN PATENTS

Reference is made to the Intellectual Property Security Agreement, dated as of July 17, 2009, (the "Agreement") between SILICON VALLEY BANK ("Secured Party") and NETLOGIC MICROSYSTEMS, INC., NETLOGIC MICROSYSTEMS INTERNATIONAL LIMITED and NETLOGIC MICROSYSTEMS CAYMANS LIMITED and recorded with the U.S. Department of Commerce, United States Patent and Trademark Office on July 17, 2009, (reel/frame 022973/0710). As of the date hereof, Secured Party, without recourse, representation, warranty or other assurance of any kind, hereby releases and terminates its security interest in the Intellectual Property Collateral (as defined in the Agreement) set forth on ***Schedule 1*** attached hereto.

Dated: August 26, 2011

SILICON VALLEY BANK

By: Rick Freeman
Name: RICK FREEMAN
Title: RELATIONSHIP MANAGER

A/74494438.2

SCHEDULE 1

INTELLECTUAL PROPERTY COLLATERAL RELEASED

Patents

(SEE ATTACHED)

No.	Serial or Patent No.	Issued Patent No.	Filing Date	Jurisdiction	Title
1.	09/999,798	6,944,709	10/31/2001	US	Content Adressable Memory With Range Compare Function
2.	10/024/609	6,690,309	12/17/2001	US	HIGH SPEED TRANSMISSION SYSTEM WITH CLOCK INCLUSIVE BALANCED CODING
3.	10/026,142	6,515,884	12/18/2001	US	CONTENT ADDRESSABLE MEMORY HAVING REDUCED CURRENT CONSUMPTION
4.	10/026,141	6,697,275	12/18/2001	US	METHOD AND APPARATUS FOR CONTENT ADDRESSABLE MEMORY TEST MODE
5.	10/027,553	6,721,202	12/21/2001	US	Bit Encoded Ternary Content Addressable Memory Cell
6.	10/061,941	6,934,796	2/1/2002	US	Content Addressable Memory With Hashing Function
7.	10/081,643	6,661,716	2/21/2002	US	WRITE METHOD AND CRICUIT FOR CONTENT ADDRESSABLE MEMORY
8.	10/093,580	6,772,279	3/7/2002	US	METHOD AND APPARATUS FOR MONITORING THE STATUS OF CAM COMPARAND REGISTERS USING A FREE LIST AND A BUSY
9.	10/109,364	6,763,426	3/28/2002	US	CASCADABLE CONTENT ADDRESSABLE MEMORY (CAM) DEVICE AND ARCHITECTURE
10.	10/165,560	6,892,273	6/7/2002	US	METHOD AND APPARATUS FOR STORING MASK VALUES IN A CONTENT ADDRESSABLE MEMORY (CAM) DEVICE
11.	10/176,495		6/21/2002	US	Methods and Apparatus for Clock and Data Recovery Using Transmission Lines
12.	10/180,357	7,272,684	6/26/2002	US	RANGE COMPARE CIRCUIT FOR SEARCH ENGINE
13.	10/197,298		7/16/2002	US	SEARCH METHOD AND APPARATUS FOR SEARCH ENGINE DEVICE
14.	10/199,225	6,954,823	7/19/2002	US	SEARCH ENGINE DEVICE AND METHOD FOR GENERATING OUTPUT SEARCH RESPONSES FROM MULTIPLE INPUT SEARCH
15.	10/202,526	7,111,123	7/24/2002	US	A CIRCUIT AND METHOD TO ALLOW SEARCHING BEYOND A DESIGNATED ADDRESS OF A CONTENT ADDRESSABLE
16.	10/208,226	6,971,053	7/30/2002	US	Method For Initiating Internal Parity Operations In A Cam Device
17.	10/213,484	6,788,103	8/6/2002	US	Activ Shunt-Peaked Logic Gates
18.	10/217,746	7,206,212	8/13/2002	US	CONTENT ADDRESSABLE MEMORY (CAM) DEVICE WITH ENTRIES HAVING TERNARY MATCH AND RANGE COMPARE
19.	10/243,076	6,718,433	9/12/2002	US	Match And Priority Encoding Logic Circuit

No.	Serial or Patent No.	Issued Patent No.	Filing Date	Jurisdiction	Title
20.	10/264,667	7,401,180	10/4/2002	US	CONTENT ADDRESSABLE MEMORY (CAM) DEVICE HAVING SELECTABLE ACCESS AND METHOD THEREFOR
21.	10/246,883	6,876,558	10/4/2002	US	METHOD AND APPARATUS FOR IDENTIFYING CONTENT ADDRESSABLE MEMORY DEVICE RESULTS FOR MULTIPLE
22.	10/266,953	7,403,407	10/8/2002	US	A MAGNITUDE COMPARATOR CIRCUIT FOR CONTENT ADDRESSABLE MEMORY WITH PROGRAMMABLE PRIORITY
23.	10/271,660	7,185,141	10/16/2002	US	APPARATUS AND METHOD FOR ASSOCIATING INFORMATION VALUES WITH PORTIONS OF A CONTENT ADDRESSABLE
24.	10/281,814	7,117,300	10/28/2002	US	METHOD AND APPARATUS FOR RESTRICTED SEARCH OPERATION IN CONTENT ADDRESSABLE MEMORY (CAM)
25.	10/286,223	6,933,757	10/31/2002	US	TIMING METHOD AND APPARATUS FOR INTEGRATED CIRCUIT DEVICE
26.	10/286,198	6,903,951	10/31/2002	US	CONTENT ADDRESSABLE MEMORY (CAM) DEVICE DECODER CIRCUIT
27.	10/300,361	6,879,523	11/20/2002	US	RANDOM ACCESS MEMORY (RAM) METHOD OF OPERATION AND DEVICE FOR SEARCH ENGINE SYSTEMS
28.	10/317,918	6,845,024	12/12/2002	US	RESULT COMPARE CIRCUIT AND METHOD FOR CONTENT ADDRESSABLE MEMORY (CAM) DEVICE
29.	10/320,588	6,988,164	12/16/2002	US	COMPARE CIRCUIT AND METHOD FOR CONTENT ADDRESSABLE MEMORY (CAM) DEVICE
30.	10/320,053	7,000,066	12/16/2002	US	PRIORITY ENCODER CIRCUIT FOR CONTENT ADDRESSABLE MEMORY (CAM) DEVICE
31.	10/320,049	6,906,936	12/16/2002	US	DATA PRECLASSIFIER METHOD AND APPARATUS FOR CONTENT ADDRESSABLE MEMORY (CAM) DEVICE
32.	10/329,146	7,117,301	12/23/2002	US	PACKET-BASED COMMUNICATION FOR CONTENT ADDRESSABLE MEMORY (CAM) DEVICES AND SYSTEMS
33.	10/364,147	6,711,041	2/11/2003	US	Content Addressable Memory With Configurable Class-Based Storage Partition
34.	10/370,833	7,005,885	2/21/2003	US	Methods and Apparatus for Injecting an External Clock into a Circuit
35.	10/402,887	7,426,518	3/28/2003	US	System And Method For Efficiently Searching A Forwarding Database That Is Split Into A Bounded Number Of Sub-Databases Having A

No.	Serial or Patent No.	Issued Patent No.	Filing Date	Jurisdiction	Title
36.	10/453,719	6,728,124	6/3/2003	US	Content Addressable Memory With Error Detection Signaling
37.	10/613,629	7,342,886	7/2/2003	US	Method And Apparatus For Managing Individual Traffic Flows
38.	10/613,347	7,349,332	7/2/2003	US	Apparatus For Queuing Different Traffic Types
39.	10/613,628	7,346,000	7/2/2003	US	Method And Apparatus For Throttling Selected Traffic Flows
40.	10/613,892	7,289,442	7/2/2003	US	Method And Apparatus For Terminating Selected Traffic Flows
41.	10/613,776	7,257,084	7/2/2003	US	Rollover Bits For Packet Departure Time Calculator
42.	10/613,891		7/2/2003	US	Method And Apparatus For Calculating Packet Departure Times
43.	10/615,093	7,075,363	7/7/2003	US	Title:
44.	10/622,862	6,901,000	7/18/2003	US	Content Addressable Memory With Multi-Ported Compare And Word Length Selection
45.	10/639,153	6,967,855	8/11/2003	US	Concurrent Searching Of Different Tables Within A Content Addressable Memory
46.	10/639,187	7,257,763	8/11/2003	US	Content Addressable Memory With Error Signaling
47.	10/644,454	6,865,121	8/19/2003	US	Programmable Delay Circuit Within A Content Addressable Memory
48.	10/679,067	6,813,174	10/2/2003	US	Content Addressable Memory Having Dynamic Match Resolution
49.	10/679,073	6,898,099	10/2/2003	US	Content Addressable Memory Having Dynamic Match Resolution
50.	10/681,525	7,019,999	10/8/2003	US	Content Addressable Memory With Latching Sense Amplifier
51.	10/685,026	7,254,748	10/14/2003	US	Error Correcting Content Addressable Memory
52.	10/700,722		11/3/2003	US	Multiple String Searching Using Content Addressable Memory
53.	10/713,185	7,133,302	11/15/2003	US	Low Power Content Addressable Memory Device
54.	10/716,140	6,831,850	11/18/2003	US	Content Addressable Memory With Configurable Class-Based Storage Partition
55.	10/719,099	7,193,874	11/22/2003	US	Content Addressable Memory Device
56.	10/734,666	6,914,795	12/12/2003	US	Content Addressable Memory With Selective Error Logging
57.	10/734,464	6,944,039	12/12/2003	US	Content Addressable Memory With Mode-Selectable Match-Detect Timing
58.	10/739,246	6,903,953	12/17/2003	US	Content Addressable Memory With Cascaded Array
59.	10/743,962	6,961,810	12/22/2003	US	Synchronous Content Addressable Memory
60.	10/746,899	6,958,925	12/24/2003	US	STAGGERED COMPARE ARCHITECTURE FOR CONTENT ADDRESSABLE MEMORY (CAM)
61.	10/752,889	7,002,823	1/7/2004	US	Content Addressable Memory Device With Simultaneous Write And Compare Function
62.	10/774,168	7,251,707	2/6/2004	US	Content Based Content Addressable Memory Block Enabling Using Search Key

No.	Serial or Patent No.	Issued Patent No.	Filing Date	Jurisdiction	Title
63.	10/773,591	7,219,188	2/6/2004	US	Segmented Content Addressable Memory Array And Priority Encoder
64.	10/775,526	6,804,135	2/9/2004	US	Content Addressable Memory Having Column Redundancy
65.	10/776,441	7,337,267	2/10/2004	US	Hierarchical, Programmable-Priority Content Addressable Memory System
66.	10/778,635	7,009,425	2/13/2004	US	Methods and Apparatus for Improving Large Signal Performance for Active Shunt-peaked Circuits
67.	10/789,299	7,272,027	2/26/2004	US	Priority Circuit For Content Addressable Memory
68.	10/789,705	7,228,378	2/27/2004	US	Entry Location In A Content Addressable Memory
69.	10/794,945	6,943,060	3/5/2004	US	Method For Fabricating Integrated Circuit Package With Solder Bumps
70.	10/801,462	7,412,561	3/15/2004	US	Transposing Of Bits In Input Data To Form A Comparand Within A Content Addressable Memory
71.	10/809,244		3/25/2004	US	Network Device, Carrier Medium And Methods For Incrementally Updating A Forwarding Database That Is Split Into A Bounded Number Of
72.	10/810,176		3/26/2004	US	Cost-Based Technology And Manufacturing Exchange
73.	10/841,607	7,437,354	5/7/2004	US	Architecture For Algorithmic Network Search Engines With Fixed Latency, High Capacity And High Throughput
74.	10/855,580	7,325,091	5/26/2004	US	Disabling Defective Blocks In A Partitioned Cam Device
75.	10/859,477	7,113,415	6/1/2004	US	Match Line Pre-Charging In A Content Addressable Memory Having Configurable Rose
76.	10/866,353		6/11/2004	US	Circuit, Apparatus, And Method For Extracting Multiple Matching Entries From A Content Addressable Memory (Cam) Device
77.	10/873,608	7,084,672	6/24/2004	US	SENSE AMPLIFIER CIRCUIT FOR CONTENT ADDRESSABLE MEMORY DEVICE
78.	10/883,160	7,505,295	7/1/2004	US	Content Addressable Memory With Multi-Row Write Function
79.	10/883,158	7,319,602	7/1/2004	US	Content Addressable Memory With Twisted Data Lines
80.	10/883,161	7,215,004	7/1/2004	US	Integrated Circuit Device With Electronically Accessible Device Identifier
81.	10/897,062		7/22/2004	US	RANGE CODE COMPRESSION METHOD AND APPARATUS FOR TERNARY CONTENT ADDRESSABLE MEMORY (CAM) DEVICES
82.	10/930,539	7,126,834	8/30/2004	US	SENSE AMPLIFIER ARCHITECTURE FOR CONTENT ADDRESSABLE MEMORY DEVICE

No.	Serial or Patent No.	Issued Patent No.	Filing Date	Jurisdiction	Title
83.	10/931,960	7,173,837	8/31/2004	US	CONTENT ADDRESSABLE MEMORY (CAM) CELL BIT LINE ARCHITECTURE
84.	10/938,028	6,944,040	9/10/2004	US	Programmable Delay Circuit Within A Content Addressable Memory
85.	10/940,129	7,099,170	9/14/2004	US	REDUCED TURN-ON CURRENT CONTENT ADDRESSABLE MEMORY (CAM) DEVICE AND METHOD
86.	10/948,050	7,451,267	9/22/2004	US	METHOD AND APPARATUS FOR LEARN AND RELATED OPERATIONS IN NETWORK SEARCH ENGINE
87.	10/950,323	7,461,200	9/23/2004	US	METHOD AND APPARATUS FOR OVERLAYING FLAT AND/OR TREE BASED DATAT SETS ONTO CONTENT ADDRESSABLE
88.	10/957,060	7,050,318	10/1/2004	US	Selective Match Line Pre-Charging In A Cam Device Using Pre-Compare Operations
89.	10/963,473	7,016,243	10/11/2004	US	Content Addressable Memory Having Column Redundancy
90.	10/964,121	7,230,840	10/12/2004	US	Content Addressable Memory With Configurable Class-Based Storage Partition
91.	10/977,516		10/29/2004	US	CONTENT ADDRESSABLE MEMORY (CAM) DEVICE AND METHOD FOR FLEXIBLE SUPPRESSION OF HIT INDICATION
92.	11/000,568		11/30/2004	US	CONTENT ADDRESSABLE MEMORY (CAM) DEVICE AND METHOD FOR UPDATING DATA
93.	11/011,464		12/13/2004	US	FULL-TERNARY CONTENT ADDRESSABLE MEMORY (CAM) CONFIGURABLE FOR PSEUDO-TERNARY OPERATION
94.	11/014,123	7,149,101	12/15/2004	US	METHOD AND APPARATUS FOR SMOOTHING CURRENT TRANSIENTS IN ACONTENT ADDRESSABLE MEMORY (CAM)
95.	11/022,267	7,382,637	12/24/2004	US	Block-Writable Content Addressable Memory Device
96.	11/043,391		1/25/2005	US	METHOD FOR ON-THE-FLY ERROR CORRECTION IN ACONTENT ADDRESSABLE MEMORY (CAM) AND DEVICE THEREFOR
97.	11/043,750	7,213,101	1/25/2005	US	Classless Interdomain Routing Using Binary Content Addressable Memory
98.	11/045,575	7,392,349	1/26/2005	US	Table Management Within A Policy-Based Routing System
99.	11/044,478	7,532,697	1/27/2005	US	Methods and Apparatus for Clock and Data Recovery Using a Single Source
100.	11/047,793		1/31/2005	US	METHOD AND DEVICE FOR VIRUTALIZATION OF MULTIPLE DATA SETS ON SAME ASSOCIATIVE MEMORY

No.	Serial or Patent No.	Issued Patent No.	Filing Date	Jurisdiction	Title
101.	11/061,259	7,230,841	2/18/2005	US	Content Addressable Memory Having Dynamic Match Resolution
102.	11/085,399	7,277,983	3/21/2005	US	METHOD AND APPARATUS FOR SMOOTHING CURRENT TRANSIENTS IN A CONTENT ADDRESSABLE MEMORY (CAM)
103.	11/088,150	7,042,748	3/22/2005	US	Content Addressable Memory With Cascaded Array
104.	11/090,116	7,126,837	3/24/2005	US	INTERLOCKING MEMORYLOGIC CELL LAYOUT AND METHOD OF MANUFACTURE
105.	11/089,837		3/24/2005	US	DEVICE AND METHOD FOR ENSURING CURRENT CONSUMPTION IN SEARCH ENGINE SYSTEM
106.	11/101,873	7,154,764	4/9/2005	US	Bit Line Control Circuit For A Content Addressable Memory
107.	11/104,077	7,379,352	4/11/2005	US	RANDOM ACCESS MEMORY(RAM) METHOD OF OPERATION AND DEVICE FOR SEARCH ENGINE SYSTEMS
108.	12/150,146	7,474,586	4/11/2005	US	RANDOM ACCESS MEMORY(RAM) METHOD OF OPERATION AND DEVICE FOR SEARCH ENGINE SYSTEMS
109.	11/138,512	7,283,380	5/25/2005	US	Content Addressable Memory With Selective Error Logging
110.	11/146,639	7,251,147	6/7/2005	US	TERNARY CONTENT COMPARATOR CELLS
111.	11/154,066	7,246,198	6/15/2005	US	Content Addressable Memory With Programmable Word Width And Programmable Priority
112.	11/194,067	7,461,295	7/29/2005	US	Timing Failure Analysis In A Semiconductor Device Having A Pipelined Architecture
113.	11/207,323		8/18/2005	US	METHOD AND SYSTEM FOR FINDING MAXIMAL STRIPES IN CACHE MEMORY WITH CONTENT ADDRESSABLE MEMORY
114.	11/218,366	7,366,830	9/1/2005	US	ROW EXPANSION REDUCTION BY INVERSION FOR RANGE REPRESENTATION IN TERNARY CONTENT ADDRESSABLE
115.	11/219,109		9/1/2005	US	PARTIAL ROW EXPANSION BY ORING FOR RANGE REPRESENTATION IN CONTENT ADDRESSABLE MEMORY
116.	11/240,160	7,277,307	9/30/2005	US	Column Defect Detection In A Content Addressable Memory
117.	11/256,066	7,193,877	10/21/2005	US	Content Addressable Memory With Reduced Test Time
118.	11/257,255	7,317,628	10/24/2005	US	Memory Device And Sense Amplifier Circuit With Faster Sensing Speed And Improved Insensitivities To Fabrication Process Variations

No.	Serial or Patent No.	Issued Patent No.	Filing Date	Jurisdiction	Title
119.	11/281,227	7,221,575	11/17/2005	US	PSEUDO TERNARY CONTENT ADDRESSABLE MEMORY DEVICE HAVING ROW REDUNDANCY AND METHOD THEREFOR
120.	11/296,786	7,432,750	12/7/2005	US	Methods and Apparatus for Frequency Synthesis with Feedback Interpolation
121.	11/298,206		12/8/2005	US	Re-Entrant Processing In A Content Addressable Memory
122.	11/321,412	7,323,916	12/29/2005	US	Methods and Apparatus for Generating Multiple Clocks Using Feedback Interpolation
123.	11/344,788		1/31/2006	US	Simultaneous Multi-Threading In A Content Addressable Memory
124.	11/366,040	7,324,362	3/1/2006	US	CONTENT ADDRESSABLE MEMORY CELL CONFIGURABLE BETWEEN MULTIFLE MODES AND METHOD THEREFOR
125.	11/367,253		3/2/2006	US	Methods and Circuits for Driving Large Off-Chip Loads
126.	11/376,764	7,298,635	3/15/2006	US	CONTENT ADDRESSABLE MEMORY (CAM) WITH SINGLE ENDED WRITE MULTIPLEXING
127.	11/384,736	7,450,409	3/20/2006	US	CONTENT ADDRESSABLE MEMORY (CAM) CELL HAVING COLUMN-WISE CONDITIONAL DATA PRE-WRITI
128.	12/288,764		3/20/2006	US	CONTENT ADDRESSABLE MEMORY (CAM) CELL HAVING COLUMN-WISE CONDITIONAL DATA PRE-WRITI
129.	11/388,785		3/24/2006	US	Memory Optimized Pattern Searching
130.	11/397,308		4/3/2006	US	Signature Searching System
131.	11/429,705	7,436,688	5/8/2006	US	PRIORITY ENCODER CIRCUIT AND METHOD
132.	11/438,185		5/22/2006	US	TERNARY CONTENT ADDRESSABLE MEMORY (TCAM) CELLS WITH LOW SIGNAL LINE NUMBERS
133.	11/453,164	7,474,545	6/13/2006	US	SOFT PRIORITY CIRCUIT AND METHOD FOR CONTENT ADDRESSABLE MEMORY (CAM) DEVICES
134.	11/426,011	7,389,377	6/22/2006	US	Access Control List Processor
135.	11/478,234		6/29/2006	US	BLOCK MAPPING CIRCUIT AND METHOD FOR MEMORY DEVICE
136.	11/428,381		6/30/2006	US	Range Representation In A Content Addressable Memory (Cam) Using An Improved Encoding Scheme
137.	11/460,615		7/27/2006	US	Controlling A Searchable Range Within A Network Search Engine
138.	11/499,021	7,447,052	8/4/2006	US	METHOD AND DEVICE FOR LIMITING CURRENT RATE CHANGES IN BLOCK SELECTABLE SEARCH ENGINE
139.	11/501,584	7,362,602	8/18/2006	US	SENSE AMPLIFIER CIRCUIT AND METHOD

No.	Serial or Patent No.	Issued Patent No.	Filing Date	Jurisdiction	Title
140.	11/524,351	7,539,032	9/19/2006	US	Regular Expression Searching Of Packet Contents Using Dedicated Search Circuits
141.	11/524,026	7,539,031	9/19/2006	US	Inexact Pattern Searching Using Bitmap Contained In A Bitcheck Command
142.	11/523,958	7,529,746	9/19/2006	US	Search Circuit Having Individually Selectable Search Engines
143.	11/533,204		9/19/2006	US	Improved Multiple String Searching Using Content Addressable Memory
144.	11/524,024		9/19/2006	US	Search Engine Having Multiple Co-Processors For Performing Inexact Pattern Search Operations
145.	11/523,881		9/19/2006	US	Method And Apparatus For Managing Multiple Data Flows In a Content Search System
146.	11/525,274	7,417,882	9/21/2006	US	CONTENT ADDRESSABLE MEMORY DEVICE
147.	11/585,460	7,277,309	10/23/2006	US	INTERLOCKING MEMORY/LOGIC CELL LAYOUT AND METHOD OF MANUFACTURE
148.	11/557,098	7,417,881	11/6/2006	US	Low Power Content Addressable Memory
149.	11/638,649		12/13/2006	US	METHOD FOR SCALABLE MULTIPLE MATCH EXTRACTION USING TERNARY CAMs AND RAMs
150.	11/614,075		12/20/2006	US	Network Search Engine (Nse) And Method For Performing Interval Location Using Prefix Matching
151.	11/647,696	7,307,861	12/28/2006	US	CONTENT ADDRESSABLE MEMORY (CAM) CELL BIT LINE ARCHITECTURE
152.	11/670,924	7,391,200	2/2/2007	US	P-Channel Power Chip
153.	11/675,928		2/16/2007	US	Content Addressable Memory With Error Detection
154.	11/713,258		3/2/2007	US	FAULT DETECTION IN CAMS USING BIST BY PROGRAMMING ADDRESS SPACE
155.	11/689,421		3/21/2007	US	Method And Apparatus For Optimizing String Search Operations
156.	11/689,429		3/21/2007	US	Optimizing Search Trees By Increasing Failure Size Parameter
157.	11/689,437		3/21/2007	US	Optimizing Search Trees by Increasing Success Size Parameter
158.	11/689,446		3/21/2007	US	Iterative Compare Operations Using Next Success Size Bitmap
159.	11/742,997		5/1/2007	US	Content Addressable Memory Having Dynamic Match Resolution
160.	11/745,415		5/7/2007	US	Integrated Circuit Device With Electronically Accessible Device Identifier
161.	11/746,016		5/8/2007	US	Transistor With Spatially Integrated Schottky Diode
162.	11/756,139		5/31/2007	US	Low Power Serial Link
163.	11/764,157		6/15/2007	US	Configurable Non-Volatile Logic Structure For Characterizing An Integrated Circuit Device

No.	Serial or Patent No.	Issued Patent No.	Filing Date	Jurisdiction	Title
164.	11/768,129		6/25/2007	US	Method And Apparatus For Terminating Selected Traffic Flows
165.	11/780,391	7,440,304	7/19/2007	US	Multiple String Searching Using Ternary Content Addressable Memory
166.	11/781,712		7/23/2007	US	Programmable Delay Clock Buffer
167.	11/830,360		7/30/2007	US	Method And Apparatus For Constructing A Failure Tree From A Search Tree
168.	11/830,397		7/30/2007	US	Assigning Encoded State Values To A Search Tree According To Failure Chains
169.	11/844,836		8/24/2007	US	Method and Apparatus for Shaping Electronic Pulses
170.	11/861,690	7,436,229	9/26/2007	US	Title: Methods and Apparatus for Minimizing Jitter in a Clock Synthesis Circuit that Uses Feedback Interpolation
171.	11/869,595		10/9/2007	US	A Digital Linear Voltage Regulator
172.	11/974,714		10/15/2007	US	LEVEL SHIFTING CIRCUIT AND METHOD
173.	11/876,118		10/22/2007	US	Content Addressable Memory With Twisted Data Lines
174.	11/930,978		10/31/2007	US	Methods and Apparatus for Clock and Data Recovery Using Transmission Lines
175.	11/935,270		11/5/2007	US	Packet Classification Device
176.	11/935,286		11/5/2007	US	Method For Combining And Storing Access Control Lists
177.	11/938,164	7,443,215	11/9/2007	US	Methods And Apparatus To Increase The Resolution Of A Clock Synthesis Circuit That Uses Feedback Interpolation
178.	11/983,382		11/15/2007	US	METHOD FOR ON-THE-FLY ERROR CORRECTION IN A CONTENT ADDRESSABLE MEMORY (CAM) AND DEVICE THEREFOR
179.	12/006,972	7,433,217	1/7/2008	US	CONTENT ADDRESSABLE MEMORY CELL CONFIGURABLE BETWEEN MULTIPLE MODES AND METHOD THEREFOR
180.	12/012,663		2/4/2008	US	CONTENT ADDRESSABLE MEMORY (CAM) HAVING DIFFUSED MATCH LINE STRUCTURE
181.	12/012,660		2/4/2008	US	CONTENT ADDRESSABLE MEMORY HAVING BLOCK SELECTABLE LOW POWER MODE
182.	12/012,618		2/4/2008	US	DEVICE AND METHOD FOR SAME COMMAND PARTIAL SEARCH KEY UPDATE AND SEARCH START IN CONTENT ADDRESSABLE
183.	12/012,672		2/4/2008	US	CONFIGURABLE I/O
184.	12/069,093		2/6/2008	US	CONTENT ADDRESSABLE MEMORY HAVING ASYNCHRONOUS MATCH LINE PRECHARGE DISABLE
185.	12/028,774		2/8/2008	US	Multi-Phase Power System With Redundancy

No.	Serial or Patent No.	Issued Patent No.	Filing Date	Jurisdiction	Title
186.	12/072,361		2/25/2008	US	ROW EXPANSION REDUCTION BY INVERSION FOR RANGE REPRESENTATION IN TERNARY CONTENT ADDRESSABLE
187.	12/049,904		3/17/2008	US	Increased Throughput for Management Data Input/Output
188.	12/130,732		5/30/2008	US	Methods and Apparatus for Frequency Synthesis with Feedback Interpolation
189.	12/131,992		6/3/2008	US	Content Addressable Memory Having Programmable Interconnect Structure
190.	12/132,053		6/3/2008	US	Content Addressable Memory Having Selectively Interconnected Shift Register Circuits
191.	12/214,952		6/23/2008	US	METHOD AND APPARATUS FOR OVERLAYING FLAT AND/OR TREE BASED DATAT SETS ONTO CONTENT ADDRESSABLE
192.	12/215,747		6/27/2008	US	METHODS AND CIRCUITS FOR PLACING UNUSED CONTENT ADDRESSABLE MEMORY (CAM) CELLS INTO LOW CURRENT
193.	12/215,875		6/27/2008	US	BIT LINE CURRENT REDUCTION ARCHITECTURE
194.	12/215,748		6/27/2008	US	MATCH LINE CURRENT REDUCTION ARCHITECTURE
195.	12/165,541		6/30/2008	US	Packet Switching Method And System
196.	12/168,600		7/7/2008	US	Transposing Of Bits In Input Data To Form A Comparand Within A Content Addressable Memory
197.	12/171,099		7/10/2008	US	System And Method For Efficiently Searching A Forwarding Database That Is Split Into a Bounded Number Of Sub-Databases Having A
198.	12/175,272		7/17/2008	US	Low Power Content Addressable Memory
199.	61/082,051		7/18/2008	US	Determining Regular Expression Match Lengths
200.	61/087,581		8/8/2008	US	Counter Circuit For Regular Expression Search Engines
201.	12/195,299		8/20/2008	US	Dynamic Random Access Memory Based Content Addressable Memory Cell With Concurrent Read and Compare
202.	12/211,565		9/16/2008	US	Multiple String Searching Using Ternary Content Addressable Memory
203.	12/275,160		11/20/2008	US	Dynamically Partitioned Cam Array
204.	12/313,868		11/24/2008	US	STRING SEARCH IN CAM DEVICE UTILIZING PARALLEL SHIFTED SEARCH KEYS
205.	12/335,506		12/15/2008	US	Character Encoding Schemes For Search Engines
206.	12/341,284		12/22/2008	US	Regular Expression Search Engine
207.	12/341,754		12/22/2008	US	Content Addressable Memory Having Selectively Interconnected Counter Circuits

No.	Serial or Patent No.	Issued Patent No.	Filing Date	Jurisdiction	Title
208.	12/341,949		12/22/2008	US	Content Addressable Memory Having Programmable Combinational Logic Circuits
209.	12/352,528		1/12/2009	US	Row Redundancy For Content Addressable Memory Having Programmable Interconnect Structure
210.	12/367,233		2/6/2009	US	Packet Processing System Having Selectively Loadable Search Engine
211.	61/168,120		4/9/2009	US	Spin Torque Transfer Content Addressable Memory Device
212.	12/386,128		4/13/2009	US	SUBSTRATE BIASING CIRCUIT AND METHOD
213.	12/185,750		8/4/2008	US	Methods And Apparatus To Increase The Resolution Of A Clock Synthesis Circuit That Uses Feedback Interpolation

Issued Patents

	Title	Juris.	Patent No.	Issue Date	Application #	Filing Date
1.	Content Addressable Memory (CAM) Arrays And Cells Having Low Power Requirements	US	USRE39227	8/8/2006	10/403,581	3/31/2003
2.	Content Addressable Memory (CAM) Devices That Can Identify Highest Priority Matches In Non-Sectored Cam Arrays And Methods Of Operating Same	US	US6665202	12/16/2003	09/962,737	9/25/2001
3.	Compact Ternary Content Addressable Memory Cell	US	US6496399	12/17/2002	09/941,372	8/28/2001
4.	Content Addressable Memory (CAM) Devices Having Dedicated Mask Cell Sub-Arrays Therein And Methods Of Operating Same	US	US6839256	1/4/2005	10/386,400	3/11/2003
5.	Content Addressable Memory (CAM) Devices That Support Power Saving Longest Prefix Match Operations And Methods Of Operating Same	US	US7050317	5/23/2006	10/927,453	8/26/2004
6.	Content Addressable Memory (CAM) Devices Having Priority Class Detectors Therein That Perform Local Encoding Of Match Line Signals	US	US7095641	8/22/2006	11/393,336	3/30/2006
7.	Content Addressable Memory (CAM) Devices Having Bidirectional Interface Circuit Therein That Support Passing Word Line And Match Signals On Global Word Lines	US	US7301850	11/27/2007	11/393,493	3/30/2006
8.	Content Addressable Memory (CAM) Devices That Utilize Priority Class Detectors To Identify Highest Priority Matches In Multiple CAM Arrays And Methods Of Operating Same	US	US7092311	8/15/2006	10/386,399	3/11/2003
9.	Content Addressable Memory (CAM) Devices Having CAM Array Blocks Therein That Conserve Bit Line Power During Staged Compare Operations	US	US6804134	10/12/2004	10/410,569	4/9/2003
10.	Content Addressable And Random Access Memory Devices Having High Speed Sense Amplifiers Therein With Low Power Consumption Requirements	US	US6879532	4/12/2005	10/934,209	9/3/2004
11.	Multi-Bank Content Addressable Memory (CAM) Devices Having Segment-Based Priority Resolution Circuits Therein And Methods Of Operating Same	US	US6937491	8/30/2005	10/263,223	10/2/2002
12.	Multi-Bank Content Addressable Memory (CAM) Devices Having Staged Segment-To-Segment Soft And Hard Priority Resolution Circuits Therein And Methods Of Operating Same	US	US7069378	6/27/2006	10/263,258	10/2/2002

	Title	Juris.	Patent No.	Issue Date	Application #	Filing Date
13.	Content Addressable Memories Having Entries Stored Therein With Independently Searchable Weight Fields And Methods Of Operating Same	US	US6745280	6/1/2004	10/109,328	3/28/2002
14.	Content Addressable Memory With Programmable Priority Weighting And Low Cost Match Detection	US	US6577520	6/10/2003	10/274,659	10/21/2002
15.	Content Addressable Memory (CAM) Devices That Utilize Dual-Capture Match Line Signal Repeaters To Achieve Desired Speed/Power Tradeoff And Methods Of Operating Same	US	US6965519	11/15/2005	10/464,598	6/18/2003
16.	Dram-Based CAM Cell With Shared Bitlines	US	US7016211	3/21/2006	10/921760	8/18/2004
17.	Low Power Content Addressable Memory Array (CAM) and Method of Operating Same	US	US7486531	2/3/2009	11/203,058	8/12/2005
18.	Content Addressable Memory (CAM) Devices Having Reliable Column Redundancy Characteristics And Methods Of Operating Same	US	US6657878	12/2/2003	10/084,842	2/27/2002
19.	CAM Circuit With Radiation Resistance	US	US6560156	5/6/2003	10/099,913	3/14/2002
20.	CAM Circuit With Radiation Resistance	US	US6924995	8/2/2005	10/845,654	5/13/2004
21.	CAM Circuit With Radiation Resistance	US	US6754093	6/22/2004	10/165,506	6/6/2002
22.	CAM Circuit With Separate Memory And Logic Operating Voltages	US	US6661687	12/9/2003	10/350,991	1/23/2003
23.	CAM Circuit With Separate Memory And Logic Operating Voltages	US	US6512685	1/28/2003	10/164,981	6/6/2002
24.	Hardware Hashing Of An Input Of A Content Addressable Memory (CAM) To Emulate A Wider CAM	US	US7136960	11/14/2006	10/173516	6/14/2002
25.	Use Of Hashed Content Addressable Memory (CAM) To Accelerate Content-Aware Searches	US	US7171439	1/30/2007	10/173,206	6/14/2002
26.	Fast Collision Detection For A Hashed Content Addressable Memory (CAM) Using A Random Access Memory	US	US7290084	10/30/2007	10/980,858	11/2/2004
27.	CAM Circuit With Error Correction	US	US6700827	3/2/2004	10/226,512	8/23/2002
28.	Content Addressable Memory (CAM) Devices Having Error Detection And Correction Control Circuits Therein And Methods Of Operating Same	US	US6879504	4/12/2005	10/619,638	7/15/2003
29.	Content Addressable Memory (CAM) Devices That Support Distributed CAM Control And Methods Of Operating Same	US	US7058757	6/6/2006	10/620161	7/15/2003
30.	Content Addressable Memory (CAM) Devices That Utilize Multi-Port CAM Cells And Control Logic To Support Multiple Overlapping Search Cycles That	US	US6781857	8/24/2004	10/306,799	11/27/2002

	Title	Juris.	Patent No.	Issue Date	Application #	Filing Date
	Are Asynchronously Timed Relative To Each Other					
31.	Multiple Match Detection Logic And Gates For Content Addressable Memory (CAM) Devices	US	US6859378	2/22/2005	10/869,387	6/16/2004
32.	Content Addressable Memory (CAM) Devices Having Scalable Multiple Match Detection Circuits Therein	US	US6924994	8/2/2005	10/385,155	3/10/2003
33.	Content Addressable Memory (CAM) Devices Having CAM Array Blocks Therein That Perform Pipelined And Interleaved Search, Write And Read Operations And Methods Of Operating Same	US	US6829153	12/7/2004	10/622,396	7/18/2003
34.	Content Addressable Memory (CAM) Devices Having Adjustable Match Line Precharge Circuits Therein	US	US6775168	8/10/2004	10/622,408	7/18/2003
35.	Content Addressable Memory (CAM) Devices Having Speed Adjustable Match Line Signal Repeaters Therein	US	US6760242	7/6/2004	10/323,236	12/18/2002
36.	Content Addressable Memory (CAM) Devices That Utilize Segmented Match Lines And Word Lines To Support Pipelined Search And Write Operations And Methods Of Operating Same	US	US6967856	11/22/2005	10/701,048	11/4/2003
37.	Content Addressable Memory Devices With Virtual Partitioning And Methods Of Operating Same	US	US6867991	3/15/2005	10/613,245	7/3/2003
38.	Content Addressable Memory (CAM) Arrays Having Memory Cells Therein With Different Susceptibilities To Soft Errors	US	US7193876	3/20/2007	11/181534	7/14/2005
39.	Content Addressable Memory (CAM) Devices Having Multi-Block Error Detection Logic And Entry Selective Error Correction Logic Therein	US	US6987684	1/17/2006	10/738,264	12/17/2003
40.	Content Addressable Memory (CAM) Devices With Dual-Function Check Bit Cells That Support Column Redundancy And Check Bit Cells With Reduced Susceptibility To Soft Errors	US	US6870749	3/22/2005	10/619,635	7/15/2003
41.	Ternary Content Addressable Memory (Tcam) Cells With Small Footprint Size And Efficient Layout Aspect Ratio	US	US6900999	5/31/2005	10/609,756	6/30/2003
42.	Content Addressable Memory (CAM) Devices With Block Select And Pipelined Virtual Sector Look-Up Control And Methods Of Operating Same	US	US6972978	12/6/2005	10/663,860	9/16/2003

	Title	Juris.	Patent No.	Issue Date	Application #	Filing Date
43.	CAM-Based Search Engines That Support Pipelined Multi-Database Search Operations Using Encoded Multi-Database Identifiers	US	US7260675	8/21/2007	11/532,746	9/18/2006
44.	CAM-Based Search Engines That Support Pipelined Multi-Database Search Operations Using Replacement Search Key Segments	US	US7120731	10/10/2006	10/688,353	10/17/2003
45.	Content Addressable Memories (CAM) Having Low Power Dynamic Match Line Sensing Circuits Therein	US	US7471537	12/30/2008	11/751,900	5/22/2007
46.	High Speed Nand-Type Content Addressable Memory (CAM)	US	US7110275	9/19/2006	11/137,163	5/25/2005
47.	CAM Based Search Engines And Packet Co-Processors Having Results Status Signaling For Completed Contexts	US	US7082493	7/25/2006	10/698,246	10/31/2003
48.	CAM-Based Search Engine Devices Having Advanced Search And Learn Instruction Handling	US	US7194573	3/20/2007	10/721,036	11/21/2003
49.	CAM-Based Search Engines Having Per Entry Age Reporting Capability	US	US7120733	10/10/2006	10/714,680	11/14/2003
50.	Binary And Ternary Non-Volatile CAM	US	US7499303	3/3/2009	10/950,186	9/24/2004
51.	CAM-Based Search Engine Devices Having Index Translation Capability	US	US7185172	2/27/2007	10/743,597	12/22/2003
52.	Method And Apparatus For CAM With Reduced Cross-Coupling Interference	US	US7522438	4/21/2009	11/931,573	10/31/2007
53.	Method And Apparatus For CAM With Reduced Cross-Coupling Interference	US	US7248492	7/24/2007	11/393,985	3/30/2006
54.	Method And Apparatus For CAM With Reduced Cross-Coupling Interference	US	US7187571	3/6/2007	10/821,601	4/9/2004
55.	Content Addressable Memory (CAM) Devices That Support Background Bist And Bisr Operations And Methods Of Operating Same	US	US7304875	12/4/2007	11/184,414	7/19/2005
56.	Content Addressable Memory (CAM) Devices Having Nand-Type Compare Circuits	US	US7355890	4/8/2008	11/553,202	10/26/2006
57.	Complementary Data Line Driver Circuits With Conditional Charge Recycling Capability That May Be Used In Random Access And Content Addressable Memory Devices And Method Of Operating Same	US	US6549042	4/15/2003	10/004,456	10/19/2001
58.	Switching circuit implementing variable string matching	US	US7353332	4/1/2008	11/248,901	10/11/2005
59.	Method and Apparatus for Source Synchronous Testing	US	US7548105	6/16/2009	11/395,079	3/31/2006

Patent Applications

	Title	Juris.	Application #	Filing Date	Status
60.	Content addressable memory (CAM) devices that perform pipelined multi-cycle look-up operations using cam sub-arrays and longest match detection	US	10/285,031	10/31/2002	Filed
61.	Content Addressable Memory (CAM) Devices Having Soft Priority Resolution Circuits Therein And Methods Of Operating Same	US	10/613,542	7/3/2003	Filed
62.	CAM Arrays Having CAM Cells Therein With Match Line And Low Match Line Connections And Methods Of Operating Same (Reissue)	US	10/106,420	3/26/2002	Filed
63.	Method And Apparatus For CAM With Selective Parallel Match Lines	US	10/821,556	4/9/2004	Filed
64.	Content Addressable Memory Having Redundant Row Isolated Noise Circuit and Method of Use	US	11/764,668	6/18/2007	Filed
65.	Method And Apparatus For CAM With Reduced Cross-Coupling Interference	US	11/765,326	6/19/2007	Filed
66.	Method And Apparatus For CAM With Reduced Cross-Coupling Interference	US	11/931,662	10/31/2007	Filed
67.	Method And Apparatus For CAM With Reduced Cross-Coupling Interference	US	11/931,764	10/31/2007	Filed
68.	Method And Apparatus For CAM With Reduced Cross-Coupling Interference	US	11/931,868	10/31/2007	Filed
69.	Method And Apparatus For CAM With Reduced Cross-Coupling Interference	US	11/931,920	10/31/2007	Filed
70.	Integrated Search Engine Devices That Utilize Hierarchical Memories Containing B-Trees And Span Prefix Masks To Support Longest Prefix Match Search Operations	US	11/184,243	7/19/2005	Filed
71.	Integrated Search Engine Devices Having Pipelined Search And B-Tree Maintenance Sub-Engines Therein	US	11/674,474	2/13/2007	Filed
72.	Integrated Search Engine Devices Having Pipelined Search And Tree Maintenance Sub-Engines Therein That Support Variable Tree Height	US	11/674,487	2/13/2007	Filed
73.	Search Engine Devices That Support High Speed Parallel Decoding Of Digital Search Tries	US	11/395,097	3/31/2006	Filed
74.	Handle Allocation Managers and Methods for Integrated Circuit Search Engine Devices	US	11/962,716	12/21/2007	Filed
75.	Integrated Search Engine Devices Having A Plurality Of Multi-Way Trees Of Search Keys Therein That Share A Common Root Node	US	11/858,441	9/20/2007	Filed

	Title	Juris.	Application #	Filing Date	Status
76.	Integrated Search Engine Devices That Support LPM Search Operations Using Span Prefix Masks That Encode Key Prefix Length	US	11/768,646	6/26/2007	Filed
77.	Integrated Search Engine Devices That Support Multi-Way Search Trees Having Multi-Column Nodes	US	11/864,290	9/28/2007	Filed
78.	Integrated Search Engine Devices That Support Efficient Default Route Match Detection And Handle Management in Multi-Way Trees	US	11/934,240	11/2/2007	Filed
79.	Integrated Search Engine Devices Having Pipelined Search And Tree Maintenance Sub-Engines Therein That Maintain Search Coherence During Multi-Cycle Update Operations	US	11/685,982	3/14/2007	Filed
80.	Integrated Search Engine Devices and Methods of Updating Same Using Node Splitting and Merging Operations	US	11/532,225	9/15/2006	Filed
81.	Dual-Port Content Addressable Memory Circuit and Method of Use	US	12/340,467	12/19/2008	Filed
82.	System And Method To Improve Reliability In Memory Word Line	US	12/052,334	3/20/2008	Filed
83.	Integrated Circuit Search Engine Devices Having Priority Sequencer Circuits Therein That Sequentially Encode Multiple Match Signals	US	11/554,958	10/31/2006	Filed
84.	Handle Memory Access Managers and Methods for Integrated Circuit Search Engine Devices	US	12/102,282	4/14/2008	Filed
85.	Integrated Search Engine Devices Having Pipelined Node Maintenance Sub-Engines Therein That Support Database Flush Operations	US	11/963,142	12/21/2007	Filed
86.	Combined Processor Access And Built In Self Test In Hierarchical Memory Systems	US	11/959,705	12/19/2007	Filed
87.	Integrated Search Engine Devices That Support Database Key Dumping And Methods of Operating Same	US	11/963,041	12/21/2007	Filed
88.	Integrated Search Engine Devices That Utilize SPM-Linked Bit Maps to Reduce Handle Memory Duplication And Methods of Operating Same	US	12/336,565	12/17/2008	Filed
89.	Longest Matching Prefix Search Engine with Hierarchical Decoders	US	12/110,103	4/25/2008	Filed
90.	Content Addressable Memory (CAM) Array Capable of Implementing Read or Write Operations During Search Operations	US	12/405,154	3/16/2009	Filed
91.	Content Addressable Memory Having Bidirectional Lines That Support Passing Read/Write Data And Search Data	US	12/405,000	3/16/2009	Filed

	Title	Juris.	Application #	Filing Date	Status
92.	Separate CAM Core Power Supply For Power Saving	US	12/197,549	8/25/2008	Filed
93.	Ternary Content Addressable Memory Having Reduced Leakage Effects	US	12/431,332	4/28/2009	Filed
94.	Switching Circuit Implementing Variable String Matching	US	12/028,668	2/28/2008	Filed
95.	Method and apparatus for memory array with asymmetrical memory cells	US	10/852,874	5/25/2004	Filed