PATENT ASSIGNMENT

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NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Hynix Semiconductor Inc.	08/22/2011

RECEIVING PARTY DATA

Name:	658868 N.B. Inc.
Street Address:	44 Chipman Hill
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PROPERTY NUMBERS Total: 17

Property Type	Number
Patent Number:	5846887
Patent Number:	5869404
Patent Number:	5923080
Patent Number:	6060399
Patent Number:	6091106
Patent Number:	6150870
Patent Number:	6154073
Patent Number:	6207496
Patent Number:	6034392
Patent Number:	6242316
Patent Number:	6288586
Patent Number:	6291865
Patent Number:	6313029
Patent Number:	6306743

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Patent Number:	6342425
Patent Number:	6507062

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Total Attachments: 17
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Exhibit B

ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, Hynix Semiconductor Inc., a Korean corporation, having an address at San 136-1, Ami-Li Bubal-Up Icheon-Si, Kyungki-Do, Korea [Address of Seller] (***"Assignor"***) does hereby sell, assign, transfer, and convey unto 658868 N.B Inc , a Canadian corporation (***"Assignee"***), or its designees, all right, title, and interest that exists today and may exist in the future in and to any and all of the following (collectively, the ***"Patent Rights"***):

(a) the provisional patent applications, patent applications and patents listed in the table below (the ***"Patents"***);

Representative US Patent	Country	Patent Number	Application Number	Filing Date	Title of Patent	First Named Inventor
US5427980	US	5530294	08/421793	4/14/1995	Method of making a contact of a semiconductor memory device	Kim; Jae K.
	US	5427980	08/159551	12/1/1993		
	KR	10-0098415	10-1992-0023045	12/2/1992		
	JP	2558058	05-299803	11/30/1993		
US5441904	US	5441904	08/341892	11/15/1994	Method for forming a two-layered polysilicon gate electrode in a semiconductor device using grain boundaries	Kim; Jong C.
	KR	10-0116196	10-1993-0024301	11/16/1993		
	JP		06-281936	11/16/1994		
	GB	2300298	9507837.4	4/18/1995		
	DE	4440857	4440857.9	11/15/1994		
	CN	1076865	95104684.5	4/28/1995		
US5509995	US	5509995	08/248754	5/25/1994	Process for anisotropically etching semiconductor material	Park; Hae S.
	KR	10-0115705	10-1993-0009164	5/26/1993		
	JP	2690860	06-110900	5/25/1994		
US5656860	US	6057232	08/862926	5/27/1997	Wiring structure for semiconductor device and fabrication method therefor	Lee; Chang-Jae
	US	5656860	08/494645	6/23/1995		
	KR	10-0179822	10-1995-0007653	4/1/1995		
	JP	2915828	07-217297	8/25/1995		
US5696012	US	5696012	08/772851	12/24/1996	Fabrication method of semiconductor memory device containing CMOS transistors	Son; Jeong-Hwan
	KR	10-0214468	10-1995-0067325	12/29/1995		
	JP	3008180	08-348077	12/26/1996		
	DE	19654738	19654738.5	12/30/1996		
US5703406	US	5883438	08/854069	5/8/1997	Interconnection structure for attaching a semiconductor device to a substrate	Kang; Dae Soon
	US	5703406	08/587744	1/19/1996		
	KR	10-0157899	10-1995-0031431	9/22/1995		
	JP		08-003453	1/12/1996		
	CN	1072840	96109653.5	9/11/1996		
US5714402	US	5714402	08/757246	11/27/1996	Method for fabricating a capacitor of a semiconductor device and the structure of the same	Choi; Kyeong Keun
	TW	142603 (454294)	085114568	11/26/1996		
	KR	10-0200299	10-1995-0045483	11/30/1995		
	JP	2820930	08-321927	12/2/1996		
	GB	2307789	9624828.1	11/28/1996		
	DE	19649670	19649670.5	11/29/1996		
	CN	1065658	96120755.8	11/28/1996		
US5757692	US	5757692	08/727852	10/4/1996	Semiconductor memory device	Suh; Jung Won
	TW	086250 (302536)	085112185	10/5/1996		
	KR	10-0166046	10-1995-0034288	10/6/1995		
	JP	3048936	08-266275	10/7/1996		

	GB	2306028	9620871.5	10/7/1996		
	DE	19641237	19641237.4	10/7/1996		

US5759900	US	5759900	08/708742	9/5/1996	Method for manufacturing MOSFET	Suh; Jai Bum
	KR	10-0156156	10-1995-0049773	12/14/1995		
	JP	2852901	08-170688	6/11/1996		
US5781041	US	5781041	08/669746	6/26/1996	Sense amplifier with low power in a semiconductor device	Lee; Jong Hyeop
	TW	089243 (315542)	085107801	6/28/1996		
	KR	10-0144017	10-1995-0017887	6/28/1995		
	GB	2302750	9613545.4	6/27/1996		
US5781500	DE	29724263	29724263.6	5/6/1997	Method and circuit for generating internal pulse signals in synchronous memory	Oh; Jong Hoon
	DE	29724147	29724147.8	5/6/1997		
	US	5781500	08/850247	5/2/1997		
	TW	119068 (400519)	086106099	5/6/1997		
	KR	10-0218734	10-1996-0014688	5/6/1996		
	JP	2985831	09-130554	5/6/1997		
	GB	2312977	9709078.1	5/2/1997		
	DE	19719116	19719116.9	5/6/1997		
US5796675	US	5796675	08/796219	2/7/1997	Synchronous memory device having dual input registers of pipeline structure in data path	Jang; Seong Jun
	KR	10-0190373	10-1996-0003078	2/8/1996		
	GB	2310062	9702686.8	2/10/1997		
US5835439	US	5835439	08/887280	7/2/1997	Sub word line driving circuit and a semiconductor memory device using the same	Suh; Jung Won
	US	5781498	08/764083	12/6/1996		
	KR	10-0170903	10-1995-0048041	12/8/1995		
	JP		2000-177294	12/6/1996		
	JP	3181845	08-327065	12/6/1996		
	GB	2348724	0015127.4	12/9/1996		
	GB	2307998	9625569.0	12/9/1996		
	DE	19655409	19655409.8	12/6/1996		
	DE	19650715	19650715.4	12/6/1996		
US5846887	US	5846887	08/757161	11/27/1996	Method for removing defects by ion implantation using medium temperature oxide layer	Lee; Kil Ho
	TW	102773 (358229)	085114813	11/30/1996		
	KR		10-1995-0045482	11/30/1995		
	KR	10-0170901	10-1995-0050433	12/15/1995		
	KR	10-0235962	10-1996-0054802	11/18/1996		
	JP	3249753	08-320430	11/29/1996		
	GB	2307790	9624883.6	11/29/1996		
	DE	19649701	19649701.9	11/29/1996		
	CN	1103494	96123096.7	11/29/1996		
US5859961	US	5859961	08/656164	5/31/1996	Renumbered array architecture for multi-array memories	Proebsting; Robert J.
	TW	097153 (340218)	086106770	5/17/1997		
	KR	10-0272398	10-1997-0021284	5/28/1997		
	JP		09-143749	6/2/1997		
	EP		97108267.2	5/22/1997		
	CN	1093662	97112165.6	5/29/1997		
US5864497	US	5864497	08/961544	10/30/1997	Memory device having divided global bit lines	Suh; Jung Won
	US		08/652333	5/22/1996		
	TW	102689 (358210)	085106202	5/24/1996		
	KR	10-0147708	10-1995-0012759	5/22/1995		
	JP		08-151737	5/22/1996		
	GB	2301212	9610754.5	5/22/1996		
	CN	1104727	96108472.3	5/22/1996		
US5869404	US	5869404	08/847811	4/25/1997	Method for forming contact hole of semiconductor device	Kim; Jeong Ho
	KR	10-0244793	10-1996-0014113	5/1/1996		

US5875149	PCT		PCT/US1999/023694	10/12/1999	Word line driver for semiconductor memories	Oh; Jong-Hoon
	US	6011746	09/182943	10/29/1998		
	US	5875149	08/828817	2/6/1997		
	KR	10-0592548	10-2001-7005250	4/26/2001		
	JP		2000-580231	10/12/1999		
	AU		2000-0013127	10/12/1999		
	DE		19983711.2	10/12/1999		
US5882968	US	5882968	08/576752	12/21/1995	Semiconductor device fabrication method	Jun; Young Kwon
	KR	10-0141950	10-1994-0036063	12/22/1994		
	JP	2988862	07-332310	12/20/1995		
	[redacted]					
US5904538	US	5904538	08/923141	9/4/1997	Method for developing shallow trench isolation in a semiconductor memory device	Son; Jeong-Hwan
	KR	10-0230817	10-1997-0010083	3/24/1997		
	JP	2914950	10-053037	3/5/1998		
US5923080	US	5923080	08/960081	10/24/1997	Semiconductor apparatus having a leadframe with coated leads	Chun; Heung Sup
	US		08/631153	4/12/1996		
	KR	10-0157905	10-1995-0036165	10/19/1995		
	JP	2753696	08-003280	1/11/1996		
	CN	1071493	96119946.6	10/4/1996		
US5937293	US	6078081	09/326694	6/7/1999	Method of fabricating a source/drain with LDD and halo	Lee; Sang Don
	US	5937293	09/057537	4/9/1998		
	KR	10-0223846	10-1997-0021319	5/28/1997		
	JP	2905808	10-109258	4/20/1998		
US5994200	US	5994200	08/898574	7/22/1997	Trench isolation structure of a semiconductor device and a method for thereof	Kim; Young-Gwan
	KR	10-0226488	10-1996-0072490	12/26/1996		
	JP		09-331399	12/2/1997		
US6002625	US	6002625	08/991618	12/16/1997	Cell array and sense amplifier structure exhibiting improved noise characteristic and reduced size	Ahn; Jin-Hong
	KR	10-0242998	10-1996-0077508	12/30/1996		
	JP		09-359109	12/26/1997		
	DE	19756929	19756929.3	12/19/1997		
US6017801	US	6017801	09/006479	1/13/1998	Method for fabricating field effect transistor	Youn; Kang-Sik
	KR	10-0344818	10-1997-0048550	9/24/1997		
	JP		10-034553	2/17/1998		
US6060399	US	6060399	08/923108	9/4/1997	Method for isolating semiconductor devices	Kim; Young-Gwan
	KR	10-0230816	10-1997-0009087	3/18/1997		
	JP	2914951	10-053038	3/5/1998		
US6060778	US	6060778	09/060981	4/15/1998	Ball grid array package	Jeong; Tae Sung
	TW	137986 (449844)	087103626	3/12/1998		
	KR	10-0220249	10-1997-0019144	5/17/1997		
	KR		10-1997-0019145	5/17/1997		
	JP	3407184	10-100428	3/27/1998		
	GB	2373924	0213162.1	3/20/1998		
	GB		0212903.9	3/20/1998		
	GB	2325340	9806078.3	3/20/1998		
	DE	19821715	19821715.3	5/14/1998		
	CN	100365804	98107932.6	5/6/1998		
US6064619	US	6064619	09/106308	6/29/1998	Synchronous dynamic random access memory in a semiconductor memory device	Ahn; Seung Han
	TW	123347 (411477)	087110345	6/26/1998		
	KR	10-0265589	10-1997-0030229	6/30/1997		
	JP	3466088	10-184542	6/30/1998		

US6066540	US	6066540	09/143096	8/28/1998	Method for manufacturing a capacitor of a semiconductor device	Yeom; Seung Jin
	TW	135032 (437067)	087114157	8/27/1998		
	KR	10-0250480	10-1997-0044618	8/30/1997		
US6080594	US	6080594	09/336698	6/21/1999	Method for fabricating a capacitor of a semiconductor device	Choi; Kyeong Keun
	US	5953576	08/925060	9/9/1997		
	US	5702970	08/670592	6/26/1996		
	TW	089751 (315506)	085107601	6/25/1996		
	KR	10-0159013	10-1995-0017479	6/26/1995		
	KR	10-0330572	10-1995-0018911	6/30/1995		
	KR	10-0360150	10-1995-0018912	6/30/1995		
	JP	2802262	08-166338	6/26/1996		
	CN	1122306	99123981.4	6/26/1996		
	CN	1054702	96107006.4	6/26/1996		
US6087857	US	6087857	08/943184	10/3/1997	Clock signal phase comparator	Wang; Sung-Ho
	KR	10-0244466	10-1997-0015777	4/26/1997		
	JP	3492899	09-333396	12/4/1997		
	DE	19749115	19749115.4	11/6/1997		
US6091106	US	6091106	08/957781	10/24/1997	Low voltage transistor structure having a grooved gate	Park; Sung Kye
	KR	10-0277878	10-1996-0052735	11/8/1996		
	JP	3122876	09-258198	9/24/1997		
	DE	19719156	19719156.8	5/6/1997		
US6103603	US	6103603	09/065487	4/24/1998	Method of fabricating gate electrodes of twin-well CMOS device	Han; Suk-Bin
	KR	10-0268923	10-1997-0049796	9/29/1997		
US6107138	US	6107138	08/744805	11/6/1996	Method for fabricating a semiconductor device having a tapered contact hole	Jeong; Ei Sam
	KR	10-0212419	10-1995-0039934	11/6/1995		
	JP	3007305	08-294244	11/6/1996		
US6117787	US	6117787	09/013095	1/26/1998	Planarization method for a semiconductor device	Park; Jin-Won
	KR	10-0253311	10-1997-0045517	9/2/1997		
	JP	2991695	10-178375	6/25/1998		
US6121682	US	6121682	09/469131	12/21/1999	Multi-chip package	Kim; Jae Myun
	KR	10-0470386	10-1998-0058915	12/26/1998		
US6124208	US	6124208	09/186354	11/5/1998	Method of preventing bowing in a via formation process	Park; Jae-Hyun
	KR	10-0258875	10-1998-0000967	1/15/1998		
	JP	4147361	11-007134	1/14/1999		
US6140700	US	6214648	09/604762	6/26/2000	Semiconductor chip package and method for fabricating the same	Shin; Myeong Jin
	US	6140700	08/966703	11/10/1997		
	KR	10-0232221	10-1996-0079246	12/31/1996		
	JP	3084520	09-359361	12/26/1997		
	DE	19743766	19743766.4	10/2/1997		
	CN	1170315	97118438.0	9/11/1997		
US6144230	US	6144230	09/317113	5/24/1999	Sense amplifier driving device	Kim; Moo Suk
	KR	10-0335397	10-1998-0018884	5/25/1998		
US6150870	US	6150870	09/195202	11/18/1998	Adjustable substrate voltage applying circuit of a semiconductor device	Kang; Dong Keum
	KR	10-0300034	10-1998-0003576	2/7/1998		
	JP	4241974	10-322288	11/12/1998		
US6154073	US	6154073	09/196121	11/20/1998	Delay locked loop device of the semiconductor circuit	Choi; Jae Myoung
	TW	164014 (502502)	087119356	11/21/1998		
	KR	10-0264077	10-1997-0062077	11/21/1997		
	JP		10-343634	11/18/1998		
	US	6162664	09/168886	10/9/1998	Method for fabricating a surface	
	US		08/970419	11/14/1997		

US6162664	KR	10-0239406	10-1996-0073492	12/27/1996	mounting type semiconductor chip package	Kim; Jin-Sung
	JP	2986095	09-219430	8/14/1997		
	DE	19743767	19743767.2	10/2/1997		
US6198667	US	6198667	09/290399	4/13/1999	Plural memory banks device that can simultaneously read from or write to all of the memory banks during testing	Joo; Yang-Sung
	KR	10-0313503	10-1999-0005021	2/12/1999		
US6201760	US	6201760	09/461718	12/16/1999	Apparatus and method for performing data read operation in DDR SDRAM	Yun; Mi-Kyung
	TW	139858 (454189)	088122563	12/21/1999		
	KR	10-0291194	10-1998-0061071	12/30/1998		
	JP		11-367763	12/24/1999		
	DE	19963497	19963497.1	12/28/1999		
US6207496	US	6207496	09/362210	7/28/1999	Method of forming capacitor of semiconductor device	Kang; Tae Woong
	KR	10-0277907	10-1998-0055605	12/17/1998		
US6207997	US	6207997	09/127443	7/31/1998	Thin film transistor for antistatic circuit and method for fabricating the same	Jeong; Jae Goan
	US	5807728	08/774824	12/27/1996		
	KR	10-0211539	10-1995-0066053	12/29/1995		
	JP		2003-314606	9/5/2003		
	JP	3516565	08-346144	12/25/1996		
	GB	2309588	9627040.0	12/30/1996		
	CN	1106044	96114100.X	12/30/1996		
US6209056	US	6209056	08/885035	6/30/1997	Semiconductor memory device having a plurality of bank sections distributed in a plurality of divided memory cell arrays	Suh; Jung Won
	TW	103468 (358179)	086106866	5/22/1997		
	KR	10-0203145	10-1996-0025753	6/29/1996		
	JP		09-172281	6/27/1997		
	GB	2314654	9712293.1	6/12/1997		
	DE	19723432	19723432.1	6/4/1997		
US6239641	US	6239641	09/476380	1/3/2000	Delay locked loop using bidirectional delay	Lee; Joong Ho
	KR	10-0336750	10-1999-0030900	7/28/1999		
US6242316	US	6242316	09/457340	12/8/1999	Semiconductor device having capacitor and method of fabricating the same	Joo; Jae-Hyun
	US	6034392	09/151601	9/11/1998		
	KR	10-0292689	10-1998-0020528	6/3/1998		
US6262467	US	6262467	09/410613	10/1/1999	Etch barrier structure of a semiconductor device and method for fabricating the same	Hahn; Dae Hee
	US	5985734	08/979235	11/26/1997		
	KR	10-0228773	10-1996-0080242	12/31/1996		
	JP	3104666	09-366223	12/25/1997		
US6288586	US	6288586	09/243469	2/3/1999	Circuit for standby current reduction	Ahn; Jin Hong
	TW	124417 (415079)	088100584	1/15/1999		
	KR	10-0252844	10-1998-0004191	2/12/1998		
	JP	3883319	11-034140	2/12/1999		
	GB	2334391	9903237.7	2/12/1999		
	DE	19905749	19905749.4	2/11/1999		
US6291865	US	6291865	09/217574	12/21/1998	Semiconductor device having improved on-off current characteristics	Lee; Hyung Joo
	KR	10-0268933	10-1997-0075403	12/27/1997		
	JP		10-351265	12/10/1998		
US6292042	US	6292042	09/295403	4/21/1999	Phase splitter	Kim; Ha Soo
	KR	10-0263485	10-1998-0014845	4/25/1998		
US6297091	US	6297091	09/397136	9/16/1999	Method for fabricating contact pad for semiconductor device	Roh; Jae Sung
	KR	10-0331848	10-1999-0029330	7/20/1999		
	JP	4346782	2000-063029	3/8/2000		
US6306743	US	6306743	09/798942	3/6/2001	Method for forming a gate electrode on a semiconductor substrate	Lee; Byung Hak
	KR	10-0351907	10-2000-0068405	11/17/2000		

	JP	4484392	2001-120618	4/19/2001	a semiconductor substrate	
US6313029	US	6313029	09/606874	6/28/2000	Method for forming multi-layer interconnection of a semiconductor device	Kim; Jang Geun
	KR	10-0303366	10-1999-0025254	6/29/1999		
US6329678	US	6329678	09/451852	12/1/1999	Semiconductor memory array	Jung; Tae-Hyung
	KR	10-0302597	10-1998-0053130	12/4/1998		
US6333527	US	6333527	09/867584	5/31/2001	Semiconductor device and method for fabricating the same	Kim; Jae Kap
	US	6261882	08/773174	12/27/1996		
	US		08/468958	6/6/1995		
	KR	10-0131722	10-1994-0012822	6/8/1994		
	KR	10-0140473	10-1994-0012823	6/8/1994		
	JP		07-141733	6/8/1995		
	GB	2290167	9511673.7	6/8/1995		
	DE	19521006	19521006.9	6/8/1995		
	CN	1049070	95106326.X	6/8/1995		
US6337256	US		10/015665	12/17/2001	Impurity ion segregation precluding layer, fabrication method thereof, isolation structure for semiconductor device using the impurity ion segregation precluding layer and fabricating method thereof	Shim; Hyun Sook
	US	6337256	09/441206	11/16/1999		
	KR	10-0319620	10-1999-0016624	5/10/1999		
US6342441	US	6342441	09/434520	11/5/1999	Method for fabricating semiconductor device	Park; Ji Soo
	KR	10-0313510	10-1999-0011590	4/2/1999		
US6350650	US	6350650	09/710958	11/14/2000	Method for fabricating a semiconductor memory device	Lee; Pyung Woo
	KR	10-0364798	10-2000-0017401	4/3/2000		
	JP		2001-080326	3/21/2001		
US6355579	US	6355579	09/442736	11/18/1999	Method for forming gate oxide film in semiconductor device	Ra; Sa Kyun
	KR	10-0281135	10-1999-0005853	2/22/1999		
	JP		2000-039864	2/17/2000		
US6363451	US	6363451	09/329263	6/28/1999	Data bus line control circuit	Kim; Tae Yun
	KR	10-0308066	10-1998-0024836	6/29/1998		
US6380607	US	6380607	09/216874	12/21/1998	Semiconductor device and method for reducing parasitic capacitance between data lines	Seo; Won Cheul
	KR		10-1997-0080698	12/31/1997		
	KR	10-0351888	10-1998-0030314	7/28/1998		
	JP	4657237	2007-087378	3/29/2007		
	JP	3964066	10-373267	12/28/1998		
US6385121	US	6385121	09/750228	12/29/2000	Semiconductor memory device having a plurality of banks sharing a column control unit	Lee; Byung Jae
	KR	10-0520179	10-1999-0066395	12/30/1999		
US6392456	US	6392456	09/427272	10/26/1999	Analog mixed digital DLL	Pyeon; Hong Beom
	KR	10-0295674	10-1999-0000565	1/12/1999		
	JP	4337108	2000-003752	1/12/2000		
	DE		19934226.1	7/21/1999		
US6407448	US	6407448	09/922103	8/6/2001	Stackable ball grid array semiconductor package and fabrication method thereof	Chun; Dong Seok
	US	6291259	09/239152	1/28/1999		
	KR	10-0266693	10-1998-0020098	5/30/1998		
	JP	3063032	11-094767	4/1/1999		
	DE	19845316	19845316.7	10/1/1998		
US6436775	US	6436775	09/884052	6/20/2001	MOSFET device fabrication method capable of allowing application of self-aligned contact process while maintaining metal gate to have uniform thickness	Kim; Tae Kyun
	KR	10-0336574	10-2000-0034318	6/21/2000		
	KR	10-0333373	10-2000-0034322	6/21/2000		
	JP	4239188	2001-188094	6/21/2001		
	US	6437618	09/888905	6/25/2001		

US6437618	TW	170876 (518594)	090115781	6/28/2001	Delay locked loop incorporating a ring type delay and counting elements	Lee; Seong-Hoon
	KR	10-0362199	10-2000-0036728	6/30/2000		
	JP	4504581	2001-049134	2/23/2001		
US6451649	US	6451649	09/751842	1/2/2001	Method for fabricating semiconductor device having a capacitor	An; Jun Kwon
	KR	10-0359163	10-1999-0067978	12/31/1999		
US6472303	US	6472303	10/034242	12/28/2001	Method of forming a contact plug for a semiconductor device	Weon; Dae Hee
	TW	177497 (530383)	090133285	12/31/2001		
	KR	10-0455724	10-2001-0061885	10/8/2001		
	JP	4646174	2001-399958	12/28/2001		
US6489822	US	6489822	09/747886	12/22/2000	Delay locked loop with delay control unit for noise elimination	Han; Jong-Hee
	TW	162739 (501347)	090103026	2/12/2001		
	KR	10-0533984	10-1999-0066913	12/30/1999		
	JP	4411504	2001-000035	1/4/2001		
US6506676	US	6506676	10/033509	12/27/2001	Method of manufacturing semiconductor devices with titanium aluminum nitride work function	Park; Dae Gyu
	TW	164869 (507330)	090129826	12/3/2001		
	KR	10-0387259	10-2000-0085449	12/29/2000		
	JP	4753510	2001-375358	12/10/2001		
US6507062	US	6507062	10/013402	12/13/2001	Capacitor for semiconductor memory device	Joo; Jae-Hyun
	US	6342425	09/417775	10/14/1999		
	KR	10-0324316	10-1999-0010529	3/26/1999		
	JP	4344900	11-356418	12/15/1999		
US6511875	US	6664160	10/298564	11/19/2002	Method for making high K dielectric gate for semiconductor device	Park; Dae-Gyu
	US	6511875	09/883188	6/19/2001		
	KR	10-0545706	10-2000-0035965	6/28/2000		
US6514826	US	6514826	09/721636	11/27/2000	Method of forming a gate electrode in a semiconductor device	Park; Dae Gyu
	KR	10-0351254	10-1999-0060557	12/22/1999		
US6519188	US	6519188	10/005877	12/7/2001	Circuit and method for controlling buffers in semiconductor memory device	Ryoo; Ki Hyung
	KR	10-0546187	10-2000-0077738	12/18/2000		
	KR	10-0400310	10-2001-0039028	6/30/2001		
	GB	2373905	0129792.8	12/12/2001		
US6521960	US	6521960	09/750017	12/29/2000	Column transistor for semiconductor devices	Lee; Kyoung Soo
	TW	149442 (465108)	089127177	12/19/2000		
	KR	10-0313151	10-1999-0066307	12/30/1999		
	JP		2001-000037	1/4/2001		
	GB	2400732	0416099.0	12/20/2000		
	GB	2364171	0031248.8	12/20/2000		
	DE		10065703.6	12/29/2000		
	CN	1207788	00136917.2	12/28/2000		
US6525581	US	6525581	10/033989	12/28/2001	Duty correction circuit and a method of correcting a duty	Choi; Young Bae
	KR	10-0401522	10-2001-0058153	9/20/2001		
	JP	3896451	2001-401848	12/28/2001		
US6534810	US	6534810	09/749621	12/28/2000	Semiconductor memory device having capacitor structure formed in proximity to corresponding transistor	Baek; Yong-Ku
	KR		10-1999-0064053	12/28/1999		
	JP		2000-361112	11/28/2000		
US6555454	US	6555454	09/742170	12/19/2000	Semiconductor memory device incorporating therein ruthenium electrode and method for the manufacture thereof	Park; Sung-Eon
	TW	156612 (489521)	089128300	12/29/2000		
	KR	10-0316027	10-1999-0063639	12/28/1999		
	JP		2000-399602	12/27/2000		
	CN	1201397	00120681.8	12/28/2000		
US6556488	US	6556488	09/742816	12/19/2000	Delay locked loop for use in	Han; Jong-Hee

[illegible]	KR	10-0521418	10-1999-0066815	12/30/1999	semiconductor memory device	[illegible]
US6566188	US	6566188	10/177950	6/21/2002	Method of forming contact holes in semiconductor devices and method of forming capacitors using the same	Kim; Dong Hyun
	TW	I265592	091113618	6/21/2002		
	KR	10-0604555	10-2001-0035569	6/21/2001		
	JP	4171249	2002-178445	6/19/2002		
	DE	10227344	10227344.8	6/19/2002		
US6586288	US	6586288	09/982841	10/18/2001	Method of forming dual-metal gates in semiconductor device	Kim; Tae Kyun
	KR	10-0361521	10-2000-0067946	11/16/2000		
	KR	10-0384774	10-2000-0067947	11/16/2000		
	JP		2001-318490	10/16/2001		
US6593236	US	6593236	09/874505	6/5/2001	Method of forming a metal wiring in a semiconductor device with copper seed	Pyo; Sung Gyu
	TW	171041 (518715)	090114708	6/18/2001		
	KR	10-0407680	10-2000-0033984	6/20/2000		
	JP	4790162	2001-184675	6/19/2001		
US6593786	US	6593786	10/180528	6/27/2002	Register controlled DLL reducing current consumption	Jung; Hea-Suk
	KR	10-0399941	10-2001-0038871	6/30/2001		
	JP		2002-183183	6/24/2002		
US6596629	US	6596629	10/116941	4/5/2002	Method for forming wire in semiconductor device	Cho; Young-a
	KR	10-0400248	10-2001-0018402	4/6/2001		
	JP	4071029	2002-105153	4/8/2002		
US6597614	US	6597614	09/892550	6/28/2001	Self refresh circuit for semiconductor memory device	Nam; Jong Ki
	KR	10-0631935	10-2000-0036896	6/30/2000		
US6597622	US	6597622	10/046174	1/16/2002	Apparatus and method for operation of multi-bank semiconductor memory device with an up/down counter	Lee; Joo-Sang
	KR	10-0379339	10-2001-0002391	1/16/2001		
US6603337	US	6603337	10/035082	12/28/2001	Duty cycle correction circuit	Cho; Seong Ik
	KR	10-0384781	10-2000-0085580	12/29/2000		
	JP		2001-395449	12/26/2001		
	GB	2373384	0130605.9	12/21/2001		
US6642132	US	6768179	10/663910	9/17/2003	Cmos of semiconductor device and method for manufacturing the same	Cho; Heung Jae
	US	6642132	10/253779	9/25/2002		
	TW	I221019	091121312	9/18/2002		
	KR	10-0426441	10-2001-0067848	11/1/2001		
	JP		2002-255975	8/30/2002		
US6657920	US	6657920	10/028704	12/28/2001	Circuit for generating internal address in semiconductor memory device	Lee; Jae Youl
	KR	10-0424178	10-2001-0058148	9/20/2001		
	JP		2002-078788	3/20/2002		
US6686788	US	6686788	10/140280	5/6/2002	Delay circuit of clock synchronization device using delay cells having wide delay range	Kim; Se Jun
	KR	10-0400317	10-2001-0039015	6/30/2001		
US6744090	US	7432151	10/799877	3/15/2004	Damascene capacitor formed in metal interconnection layer	Kim; Si-Bum
	US	6744090	10/260624	10/1/2002		
	TW	I292202	091132780	11/7/2002		
	KR	10-0422597	10-2001-0074336	11/27/2001		
	JP	4328501	2002-218465	7/26/2002		
US6756261	US	6756261	10/247398	9/19/2002	Method for fabricating capacitors in semiconductor devices	Hong; Kwon
	KR		10-2001-0058831	9/22/2001		
	JP		2002-218475	7/26/2002		
US6760806	US	6760806	10/024366	12/21/2001	Low power semiconductor memory device having a normal mode and a	Jeon; Byung

US6766800	KR	10-0437610	10-2001-0058146	9/20/2001	device having a normal mode and a partial array self refresh mode	Deuk
US6767788	US		10/876481	6/28/2004	Semiconductor device having a metal insulator metal capacitor	Kim; Si Bum
	US	6767788	10/152843	5/23/2002		
	KR	10-0531419	10-2001-0032906	6/12/2001		
	JP		2002-155296	5/29/2002		
US6818537	US	6818537	10/034504	12/28/2001	Method of manufacturing a contact plug for a semiconductor device	Cheong; Woo Seock
	KR	10-0455725	10-2001-0061887	10/8/2001		
	JP		2001-401846	12/28/2001		
US6844259	US	6844259	10/331724	12/31/2002	Method for forming contact plug in semiconductor device	Cheong; Woo-Seock
	KR	10-0446316	10-2002-0017679	3/30/2002		
	CN	100338736	03101730.4	1/21/2003		
US6855604	US	6855604	10/617683	7/14/2003	Method for fabricating metal-oxide semiconductor transistor	Lee; Sang-Don
	KR	10-0507856	10-2002-0086465	12/30/2002		
US6856011	US	6856011	10/232652	9/3/2002	Semiconductor chip package and method of fabricating same	Choi; Kwang Sung
	US	6458627	09/415267	10/12/1999		
	KR	10-0319624	10-1999-0018251	5/20/1999		
US6859081	US	6859081	10/638994	8/11/2003	Duty cycle correction circuit and delay locked loop having the same	Hong; Sang-Hoon
	TW	I282665	092119402	7/16/2003		
	KR	10-0490655	10-2002-0066425	10/30/2002		
	CN	100505545	200310102661.7	10/28/2003		
US6859404	US	6859404	10/883099	6/30/2004	Apparatus and method of compensating for phase delay in semiconductor device	Kim; Kyung-Hoon
	KR	10-0543923	10-2003-0057854	8/21/2003		
	JP		2004-196856	7/2/2004		
	DE		102004031449.7	6/29/2004		
US6894942	US	6894942	10/334298	12/31/2002	Refresh control circuit and method for semiconductor memory device	Cho; Jin Hee
	KR	10-0479821	10-2002-0027519	5/17/2002		
US6920068	US	6920068	10/749892	12/31/2003	Semiconductor memory device with modified global input/output scheme	Ku; Kie-Bong
	TW	I312158	092137420	12/30/2003		
	KR	10-0492907	10-2003-0034876	5/30/2003		
	JP		2004-103091	3/31/2004		
US6930535	US	6930535	10/653578	9/2/2003	High voltage supply circuit and a method of supplying high voltage	Kim; Kwan Weon
	TW	I279084	092127681	10/6/2003		
	KR	10-0549345	10-2003-0058630	8/25/2003		
	JP		2003-345766	10/3/2003		
US6943602	US	6943602	11/026970	12/30/2004	Delay locked loop and locking method thereof	Lee; Hyun-Woo
	TW	I293520	093141578	12/31/2004		
	KR	10-0639616	10-2004-0087313	10/29/2004		
	JP	4192273	2005-070772	3/14/2005		
	CN	100470670	200510073043.3	5/30/2005		
US6944833	US	6944833	10/329936	12/26/2002	Delay model circuit for use in delay locked loop	Jeon; Young-Jin
	KR	10-0482736	10-2002-0055263	9/12/2002		
	JP		2002-374690	12/25/2002		
US6964930	US	6964930	10/739620	12/18/2003	Method of fabricating dielectric layer	Park; Dong Su
	TW	I234226	092135666	12/16/2003		
	KR	10-0541675	10-2003-0027511	4/30/2003		
	JP	4566555	2003-421694	12/18/2003		
US6982924	US	6982924	10/875387	6/25/2004	Data output control circuit	Na; Kwang-Jin
	KR	10-0540487	10-2003-0076835	10/31/2003		
US7022599	US	7022599	10/306335	11/27/2002	Method of manufacturing semiconductor devices	Yoo; Kyong Sik
	TW		091133038	11/11/2002		
	KR	10-0432785	10-2001-0081929	12/20/2001		
	JP		2002-277261	9/24/2002		
	US	7042799	10/880381	6/29/2004	Write circuit of double data rate	

US7042799	TW	I264725	093119299	6/30/2004	Write circuit of double data rate synchronous DRAM	Cho; Yong Deok
	KR	10-0521049	10-2003-0100162	12/30/2003		
US7057951	US	7057951	10/877038	6/24/2004	Semiconductor memory device for controlling write recovery time	Im; Jae-Hyuk
	TW	I267081	093118421	6/25/2004		
	KR	10-0543930	10-2003-0076796	10/31/2003		
US7057964	US	7057964	11/015421	12/20/2004	Semiconductor memory device with efficient multiplexing of I/O pad in multi-chip package	Hong; Sang-Hoon
	KR	10-0551072	10-2003-0098509	12/29/2003		
US7068558	US	7068558	10/877037	6/24/2004	Semiconductor memory device having row path control circuit and operating method thereof	Cho; Jin-Hee
	KR	10-0540488	10-2003-0076848	10/31/2003		
US7095668	US	7095668	11/032381	1/10/2005	Main amplifier and semiconductor device	Cho; Yong Deok
	TW	I287248	094101017	1/13/2005		
	KR	10-0611404	10-2004-0058803	7/27/2004		
US7099228	US	7099228	11/004806	12/7/2004	Semiconductor memory device	Koo; Cheul Hee
	KR	10-0610439	10-2004-0071647	9/8/2004		
US7101791	US	7101791	10/879133	6/30/2004	Method for forming conductive line of semiconductor device	Jin; Sung Gon
	TW	I302726	093118336	6/24/2004		
	KR	10-0576464	10-2003-0096378	12/24/2003		
	CN	100336187	200410061945.0	6/29/2004		
US7119015	US	7119015	10/879220	6/30/2004	Method for forming polysilicon plug of semiconductor device	Park; Hyung Soon
	KR	10-0596834	10-2003-0096072	12/24/2003		
US7138324	US	7138324	11/293124	12/5/2005	Method of inhibiting degradation of gate oxide film	Yoo; Kyung Dong
	US		10/878364	6/29/2004		
	TW	I240317	093119274	6/30/2004		
	KR	10-0610436	10-2003-0095301	12/23/2003		
	JP		2004-194143	6/30/2004		
	CN	100338737	200410062127.2	7/2/2004		
US7145821	US	7145821	11/025800	12/28/2004	Semiconductor memory device for low power system	Kang; Hee-Bok
	TW	I280584	093140004	12/22/2004		
	KR	10-0673898	10-2004-0087660	10/30/2004		
	JP	4348545	2004-378210	12/27/2004		
	CN	100479060	200410081794.5	12/31/2004		
US7154808	US	7154808	11/125380	5/9/2005	Semiconductor memory device for simultaneously testing blocks of cells	Shim; Young Bo
	TW	I263218	094113171	4/26/2005		
	KR	10-0551430	10-2004-0063057	8/11/2004		
US7157359	US	7157359	10/036156	12/26/2001	Method of forming a metal gate in a semiconductor device using atomic layer deposition process	Park; Dae Gyu
	TW	170233 (516131)	090132016	12/24/2001		
	KR		10-2000-0085582	12/29/2000		
	JP		2001-393197	12/26/2001		
	CN	1180458	01144786.9	12/28/2001		
US7170815	US	7170815	10/879274	6/30/2004	Memory apparatus having multi-port architecture for supporting multi processor	Kang; Hee Bok
	KR	10-0596821	10-2003-0094567	12/22/2003		
US7193906	US	7193906	11/008672	12/10/2004	Voltage regulating circuit and method of regulating voltage	Jang; Ji Eun
	KR	10-0570076	10-2004-0008025	2/6/2004		
US7196966	US	7196966	10/879650	6/28/2004	On die termination mode transfer circuit in semiconductor memory device and its method	Jin; Seung-Eon
	TW	I253084	093118720	6/28/2004		
	KR	10-0528164	10-2004-0009501	2/13/2004		
	JP	4693089	2004-195037	6/30/2004		
	CN	100476999	200410088904.0	11/4/2004		
	US	7212465	11/077612	3/11/2005	Clock signal generation apparatus for use	
	TW	I277977	094105221	2/22/2005		

US7212465	KR	10-0638747	10-2004-0113615	12/28/2004	in semiconductor memory device and its method	Kang; Tae-Jin
	JP	4707461	2005-158771	5/31/2005		
	DE		102005010906.3	3/9/2005		
US7236420	US		11/809244	5/30/2007	Memory chip architecture having non-rectangular memory banks and method for arranging memory banks	Chun; Jun-Hyun
	US	7236420	10/511253	4/25/2005		
	PCT		PCT/KR2003/000722	4/10/2003		
	CN	100580801	03808109.1	4/10/2003		
	DE		10392539.2	4/10/2003		
	JP	4559738	2003-582770	4/10/2003		
	AU		2003-0219596	4/10/2003		
	TW	I318410	092108267	4/10/2003		
	KR		10-2002-0019395	4/10/2002		
	KR		10-2002-0019394	4/10/2002		
	KR		10-2002-0019444	4/10/2002		
	KR	10-0552654	10-2003-0018104	3/24/2003		
US7276451	US	7276451	11/321628	12/30/2005	Method for manufacturing semiconductor device	Hong; Jae Ok
	KR	10-0673117	10-2005-0069411	7/29/2005		
US7307913	US	7307913	11/476597	6/29/2006	Clock control device for toggling an internal clock of a synchronous DRAM for reduced power consumption	Do; Chang-Ho
	TW	I304219	095123711	6/30/2006		
	KR		10-2005-0091673	9/29/2005		
	KR	10-0798766	10-2005-0117137	12/2/2005		
US7316973	US	7316973	11/002706	12/3/2004	Method for fabricating semiconductor device	Roh; Jai-Sun
	KR	10-0533978	10-2004-0050189	6/30/2004		
US7348255	US		11/999466	12/4/2007	Semiconductor device and method for fabricating a semiconductor device	Cho; Jun-Hee
	US	7348255	11/321925	12/28/2005		
	KR	10-0637692	10-2005-0055863	6/27/2005		
	JP		2006-014546	1/24/2006		
US7351652	US	7351652	11/444064	5/30/2006	Method of manufacturing semiconductor device	Park; Shin Seung
	KR	10-0739252	10-2005-0046857	6/1/2005		
	JP		2006-133513	5/12/2006		
	CN	100452351	200610081351.5	5/18/2006		
US7355913	US	7355913	11/396193	3/30/2006	Semiconductor memory device	Kang; Hee-Bok
	KR	10-0571650	10-2005-0027382	3/31/2005		
	JP		2006-093578	3/30/2006		
US7372294	US	7372294	11/478084	6/30/2006	On-die termination apparatus	Kim; Yong-Mi
	KR		10-2005-0091657	9/29/2005		
	KR	10-0753035	10-2005-0117640	12/5/2005		
US7382671	US	7382671	10/882442	7/1/2004	Method for detecting column fail by controlling sense amplifier of memory device	Lee; Geun Il
	KR	10-0587080	10-2004-0034897	5/17/2004		
US7396772	US	7396772	11/582638	10/17/2006	Method for fabricating semiconductor device having capacitor	Lee; Sang-Do
	TW	I312554	095134575	9/19/2006		
	KR	10-0799125	10-2006-0049007	5/30/2006		
	CN	100539078	200610137622.4	10/31/2006		
US7410866	US	7790546	12/168823	7/7/2008	Method for forming storage node of capacitor in semiconductor device	Sun; Jun-Hyeub
	US	7410866	11/204660	8/15/2005		
	TW	I281231	094119760	6/15/2005		
	KR	10-0721548	10-2004-0108694	12/20/2004		
	KR	10-0623599	10-2004-0110083	12/22/2004		
	KR	10-0733458	10-2004-0112821	12/27/2004		
	JP		2005-175980	6/16/2005		
	CN	100423269	200510117259.5	10/31/2005		
US7411839	US	7411839	11/480877	7/6/2006	Data input circuit of semiconductor memory device and data input method	Cha; Jae Hoon
	TW	I307513	095125170	7/11/2006		

	KR	10-0650844	10-2005-0118980	12/7/2005	thereof	
US7428168	US	7428168	11/478527	6/30/2006	Semiconductor memory device sharing a data line sense amplifier and a write driver in order to reduce a chip size	Kim; Seung-Lo
	TW	I311760	095123952	6/30/2006		
	KR	10-0668513	10-2005-0134011	12/29/2005		
	KR		10-2005-0090844	9/28/2005		
	JP		2006-182714	6/30/2006		
	CN		200610128058.X	9/1/2006		
US7436036	US	7436036	11/502920	8/11/2006	PMOS transistor of semiconductor device, semiconductor device comprising the same, and method for manufacturing the same	Lee; Jung Suk
	KR	10-0762239	10-2006-0040110	5/3/2006		
US7449403	US	7449403	11/122718	5/5/2005	Method for manufacturing semiconductor device	Kim; Dong Seok
	KR	10-0608368	10-2004-0061933	8/6/2004		
US7449965	US	7859347	12/255074	10/21/2008	Self refresh oscillator and oscillation signal generation method of the same	Jang; Ji-Eun
	US	7449965	11/319718	12/29/2005		
	KR	10-0631167	10-2004-0116671	12/30/2004		
US7450448	US	7450448	11/321877	12/30/2005	Semiconductor memory device	Do; Chang-Ho
	TW		094147407	12/30/2005		
	KR	10-0673903	10-2005-0036593	4/30/2005		
	JP		2006-001080	1/6/2006		
	CN	1855293	200610002104.1	1/16/2006		
US7459358	US		12/323391	11/25/2008	Method for fabricating a semiconductor device	Lee; Sang Don
	US	7459358	11/414353	5/1/2006		
	KR	10-0720238	10-2006-0006966	1/23/2006		
	JP		2006-153562	6/1/2006		
US7479676	US	7776711	12/331830	12/10/2008	Transistor of semiconductor memory device	Kim; Hyun Jung
	US	7479676	11/450096	6/9/2006		
	KR	10-0642384	10-2005-0086497	9/15/2005		
US7489586	US	7746723	12/354158	1/15/2009	Semiconductor memory device and driving method thereof	Oh; Young-Hoon
	US	7489586	11/647402	12/29/2006		
	KR	10-0832021	10-2006-0059735	6/29/2006		
US7495469	US	7847584	12/356514	1/20/2009	On-die termination circuit and driving method thereof	Park; Jung-Hoon
	US	7495469	11/824165	6/28/2007		
	KR	10-0772533	10-2006-0094052	9/27/2006		
US7547600	US	7547600	11/476261	6/27/2006	Five channel fin transistor and method for fabricating the same	Kim; Kwang-Ok
	TW	I323942	095118349	5/24/2006		
	KR	10-0792384	10-2005-0130534	12/27/2005		
	JP		2006-221172	8/14/2006		
	CN	100563028	200610150790.7	10/26/2006		
USRE37960	US	RE37960	08/824879	3/26/1997	Method for forming an oxynitride film in a semiconductor device	Cho; Byung-Jin
	US	5541141	08/394607	2/27/1995		
	KR	10-0115675	10-1993-0029790	12/27/1993		
	US	5631199	08/499241	7/7/1995		
	CN	1047877	95109344.5	7/7/1995		
	GB		9513226.2	6/29/1995		
	KR	10-0187674	10-1994-0016248	7/7/1994		

(b) all patents and patent applications (i) to which any of the Patents directly or indirectly claims priority, (ii) for which any of the Patents directly or indirectly forms a basis for priority, and/or (iii) that were co-owned applications that incorporate by reference, or are incorporated by reference into, the Patents;

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categories (a) and (b);

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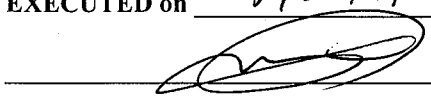

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The terms and conditions of this Assignment of Patent Rights will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed at San Francisco, California on 8/22/11.

ASSIGNOR:

HYNIX SEMICONDUCTOR INC.

By: [signature]
Name: ET Kim
Title: Vice President
(Signature MUST be attested)

ATTESTATION OF SIGNATURE PURSUANT TO 28 U.S.C. § 1746

The undersigned witnessed the signature of ET KIM to the above Assignment of Patent Rights on behalf of Hynix Semiconductor Inc. and makes the following statements:

1. I am over the age of 18 and competent to testify as to the facts in this Attestation block if called upon to do so.

2. ET KIM is personally known to me (or proved to me on the basis of satisfactory evidence) and appeared before me on 8 22, 2011 to execute the above Assignment of Patent Rights on behalf of Hynix Semiconductor Inc..

3. ET KIM subscribed to the above Assignment of Patent Rights on behalf of Hynix Semiconductor Inc.

I declare under penalty of perjury under the laws of the United States of America that the statements made in the three (3) numbered paragraphs immediately above are true and correct.

CALIFORNIA JURAT WITH AFFIANT STATEMENT

☑ See Attached Document (Notary to cross out lines 1–6 below)
☐ See Statement Below (Lines 1–5 to be completed only by document signer[s], *not* Notary)

1
2
3
4
5
6

Signature of Document Signer No. 1

Signature of Document Signer No. 2 (if any)

State of California

County of San Francisco

Subscribed and sworn to (or affirmed) before me on this

22d day of August, 2011, by
Date Month Year

(1) Eun Tae Kim,
Name of Signer

proved to me on the basis of satisfactory evidence to be the person who appeared before me.) ~~(.)~~

(and

(2) _____,
Name of Signer

proved to me on the basis of satisfactory evidence to be the person who appeared before me.)

Signature Doreen B. Bordessa
Signature of Notary Public

DOREEN B. BORDESSA
Commission # 1788655
Notary Public - California
San Francisco County
My Comm. Expires Feb 9, 2012

Place Notary Seal Above

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Though the information below is not required by law, it may prove valuable to persons relying on the document and could prevent fraudulent removal and reattachment of this form to another document.

Further Description of Any Attached Document

Title or Type of Document: Assignment of Patent Rights - Exhibit B

Document Date: 8/22/11 Number of Pages: 16

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