

Form PTO-1595 (Rev. 03-11)  
OMB No. 0651-0027 (exp. 03/31/2012)

U.S. DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office

## RECORDATION FORM COVER SHEET PATENTS ONLY

To the Director of the U.S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

### 1. Name of conveying party(ies):

Micron Technology Inc.

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

### 2. Name and address of receiving party(ies)

Name: Round Rock Research, LLC

Internal Address: \_\_\_\_\_

Street Address: \_\_\_\_\_

P. O. Box 1042

City: Mount Kisco

State: New York

Country: United States of America Zip: 10549

Additional name(s) & address(es) attached? ☐ Yes ☒ No

### 3. Nature of conveyance/Execution Date(s):

Execution Date(s): December 30, 2009

☐ Assignment ☐ Merger ☐ Change of Name

☐ Security Agreement ☐ Joint Research Agreement

☐ Government Interest Assignment

☐ Executive Order 9424, Confirmatory License

☒ Other In response to the Notice of Non-Recordation  
Statement under 37 CFR 3.73(b) is removed  
from submission

### 4. Application or patent number(s):

A. Patent Application No.(s)

☐ This document is being filed together with a new application.

B. Patent No.(s)

8,054,703

Additional numbers attached? ☐ Yes ☒ No

### 5. Name and address to whom correspondence concerning document should be mailed:

Name: Richard J. Botos  
LERNER, DAVID, LITTENBERG,  
KRUMHOLZ & MENTLIK, LLP

Internal Address: Atty. Dkt.:

Street Address: 600 South Avenue West

City: Westfield

State: NJ Zip: 07090

Phone Number: 908-654-5000

Fax Number: 908-654-7866

Email Address: ataylor@ldlkm.com

### 6. Total number of applications and patents involved:

1

### 7. Total fee (37 CFR 1.21(h) & 3.41) \$ 40.00

☒ Authorized to be charged to deposit account

☐ Enclosed


☐ None required (government interest not affecting title)

### 8. Payment Information

Deposit Account Number 12-1095

Authorized User Name Richard J. Botos

### 9. Signature:



Signature

December 1, 2011

Date

Richard J. Botos - 32,016

Name of Person Signing

Total number of pages including cover sheet, attachments, and documents: 7

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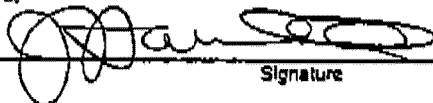
☐ None required (government interest not affecting title)

**8. Payment Information**

Deposit Account Number 12-1095

Authorized User Name John J. Farrell

**9. Signature:**



Signature

November 2, 2011

Date

John J. Farrell, 57,291

Name of Person Signing

Total number of pages including cover sheet, attachments, and documents:

8

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**EXHIBIT A****CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS**

This Confirmatory Assignment of Patent Rights (the "Agreement") is entered into this 30th day of December, 2009 (the "Closing Date"), by and between Micron Technology, Inc., a Delaware corporation ("Assignor"), and Round Rock Research, LLC, a Delaware limited liability company ("Assignee").

WHEREAS, Assignor and Assignee are party to that certain Patent Sale and Transfer Agreement dated on or about the date hereof (as in effect from time to time, the "Patent Sale and Transfer Agreement"); capitalized terms used but not otherwise defined in this Agreement shall have the respective meaning assigned thereto in the Patent Sale and Transfer Agreement;

WHEREAS, pursuant to the Patent Sale and Transfer Agreement, Assignor has agreed to sell, convey, transfer, assign and deliver to Assignee all of Assignor's (and its Subsidiaries') right, title and interest, including Patent Rights, in and to the Patents listed on Schedule A hereto (collectively, the "Assigned Patents");

WHEREAS, Assignee is now desirous of acquiring the entire and exclusive right, title and interest in and to the Assigned Patents in the United States and throughout the world; and

WHEREAS, Assignor is now willing to assign to Assignee all rights, title and interest in and to the Assigned Patents in the United States and throughout the world; and

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged by Assignor, Assignor hereby assigns, transfers and conveys to Assignee, its successors, legal representatives and assigns, and Assignee hereby accepts, all of Assignor's right, title and interest in the United States and throughout the world in and to the Assigned Patents and any and all Letters Patent that are or may be granted thereon, and any legal equivalent thereof that may be granted in any country or countries foreign to the United States, in each case including without limitation any extensions, substitutes, continuations, continuations-in-part, divisions, reissues, reexaminations, and renewals thereof, or other equivalents thereof, and further, all rights and privileges pertaining to the Assigned Patents and any and all Letters Patent that are or may be granted thereon, and any legal equivalent thereof that may be granted in any country or countries foreign to the United States, including, without limitation, the right, if any, to petition, sue or otherwise seek and recover damages, profits and any other remedy (monetary, injunctive, declaratory or other) in the United States and anywhere throughout the world for any past, present and future infringement thereof, conversion or misappropriation of, or other injury, offense, violation, breach of duty or wrong relating to, any of the Assigned Patents, or any license, agreement, contract or other matter relating thereto.

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks of the United States of America and the appropriate officers of all other jurisdictions in which the Assigned Patents are or may be registered or in which applications included among the Assigned Patents are pending, to record the title of Assignee, its successors, legal representatives and assigns, as owner of all right, title and interest in and to the Assigned Patents, and to issue to Assignee, its successors, legal representatives and assigns, all Letters Patent and any legal

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**PATENT**  
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equivalent thereof that may be granted in any country or countries foreign to the United States and recordings of patent rights resulting from any application included among the Assigned Patents, in accordance with the terms of this instrument.

Except to the extent that federal law preempts state law with respect to the matters covered hereby, this Agreement shall be governed by and construed in accordance with the laws of the State of Delaware, without giving effect to any of the principles of conflicts of laws thereof that would result in the application of the laws of another jurisdiction to this Agreement.

This Agreement shall be binding on, and shall inure to the benefit of, the parties hereto and their respective successors and assigns, and may be executed in two or more counterparts, each of which shall be deemed to be an original, but all of which shall constitute one and the same agreement. Each of the parties hereto agrees to accept and be bound by facsimile signatures hereto.

Each party represents that it has taken all necessary action to authorize the execution and delivery of this Agreement.

[The remainder of this page has been intentionally left blank.]

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PATENT  
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IN WITNESS WHEREOF, the parties hereto have caused this Agreement to be executed by their respective duly authorized officers, as of the date first written above.

**ASSIGNOR:**

MICRON TECHNOLOGY, INC.

By: [Signature]  
 Name: Steven R. Appleton  
 Title: Chairman and CEO

**ASSIGNEE:**

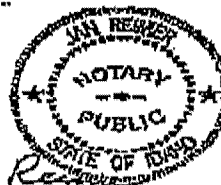
ROUND ROCK RESEARCH, LLC

By: [Signature]  
 Name: John Desmarais  
 Title: Managing

On this 23rd day of December, 2009, before me appeared Steven R. Appleton, the person who signed this instrument, who acknowledged that he/she signed it as a free act on his/her own behalf or on behalf of the Assignor with authority to do so.

State of IDAHO )

ss. )

County of Ada )

[Note that federal patent assignments must also include a cover sheet. See 37 C.F.R. 3.28]

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## Schedule A Patents

2001-0942.00/EP	EP	20-Nov-02	ACTIVE TERMINATION CIRCUIT AND METHOD FOR CONTROLLING THE IMPEDANCE OF EXTERNAL INTEGRATED CIRCUIT TERMINALS	Pending		02789818.8
2001-0942.00/KR	KR	20-Nov-02	ACTIVE TERMINATION CIRCUIT AND METHOD FOR CONTROLLING THE IMPEDANCE OF EXTERNAL INTEGRATED CIRCUIT TERMINALS	Issued	11-Feb-09 10-884226	2004-7008892
2001-0942.00/TW	TW	19-Nov-02	ACTIVE TERMINATION CIRCUIT AND METHOD FOR CONTROLLING THE IMPEDANCE OF EXTERNAL INTEGRATED CIRCUIT TERMINALS	Issued	11-Oct-07 1288527	091133709
2001-0942.00/US	US	28-Nov-01	ACTIVE TERMINATION CIRCUIT AND METHOD FOR CONTROLLING THE IMPEDANCE OF EXTERNAL INTEGRATED CIRCUIT TERMINALS	Issued	02-Dec-03 8657906	09/997,156
2001-0942.01/US	US	26-Feb-03	ACTIVE TERMINATION CIRCUIT AND METHOD FOR CONTROLLING THE IMPEDANCE OF EXTERNAL INTEGRATED CIRCUIT TERMINALS	Issued	23-Mar-04 8711073	10/375,639
2001-0942.02/US	US	21-Jan-04	ACTIVE TERMINATION CIRCUIT AND METHOD FOR CONTROLLING THE IMPEDANCE OF EXTERNAL INTEGRATED CIRCUIT TERMINALS	Issued	13-Sep-05 6944071	10/782,805
2001-0942.03/US	US	29-Nov-04	ACTIVE TERMINATION CIRCUIT AND METHOD FOR CONTROLLING THE IMPEDANCE OF EXTERNAL INTEGRATED CIRCUIT TERMINALS	Issued	12-Sep-06 7106638	10/999,771
2001-0942.04/US	US	29-Nov-04	ACTIVE TERMINATION CIRCUIT AND METHOD FOR CONTROLLING THE IMPEDANCE OF EXTERNAL INTEGRATED CIRCUIT TERMINALS	Issued	06-Mar-07 7187601	10/999,770
2001-0942.05/US	US	10-Jan-06	ACTIVE TERMINATION CIRCUIT AND METHOD FOR CONTROLLING THE IMPEDANCE OF EXTERNAL INTEGRATED CIRCUIT TERMINALS	Pending		11/328,596
2001-0942.06/US	US	10-Jan-06	ACTIVE TERMINATION CIRCUIT AND METHOD FOR CONTROLLING THE IMPEDANCE OF EXTERNAL INTEGRATED CIRCUIT TERMINALS	Issued	03-Jun-06 7382667	11/328,482
2001-0949.00/IT	IT	18-Mar-02	FLASH MEMORY PROGRAMMING	Issued	22-Mar-06 1333053	rm2002a000 148
2001-0949.00/US	US	13-Jan-03	FLASH MEMORY PROGRAMMING	Issued	13-Jun-06 7062599	10/341,314
2001-0949.01/US	US	07-Mar-06	FLASH MEMORY PROGRAMMING	Issued	09-Jan-07 7162570	11/369,348
2001-0950.00/IT	IT	09-Jul-02	DUAL BUS FAST MEMORY ARCHITECTURE	Issued	11-Apr-06 1333309	rm2002a000 369
2001-0950.00/US	US	14-Feb-03	DUAL BUS MEMORY BURST ARCHITECTURE	Issued	12-Jul-05 6917545	10/367,587
2001-0950.01/US	US	01-Jun-05	DUAL BUS MEMORY BURST ARCHITECTURE	Issued	16-Jan-07 7164607	11/142,114
2001-0968.00/US	US	30-May-02	DYNAMICALLY CENTERED SETUP-TIME AND HOLD-TIME WINDOW	Issued	09-Dec-03 6661717	10/156,807
2001-0973.00/US	US	19-Apr-02	INTEGRATED CIRCUIT PACKAGE HAVING REDUCED INTERCONNECTS	Issued	27-Dec-05 6979904	10/126,067
2001-0973.01/US	US	01-Sep-05	INTEGRATED CIRCUIT PACKAGE HAVING REDUCED INTERCONNECTS	Pending		11/218,998
2001-0979.00/US	US	11-Feb-02	SYSTEM AND METHOD FOR POWER SAVING DELAY LOCKED LOOP CONTROL BY SELECTIVELY LOCKING DELAY INTERVAL	Issued	17-Jan-06 6988218	10/074,298
2001-0979.01/US	US	07-Dec-05	SYSTEM AND METHOD FOR POWER SAVING DELAY LOCKED LOOP CONTROL BY SELECTIVELY LOCKING DELAY INTERVAL	Issued	09-Sep-08 7424835	11/297,087
2001-0979.02/US	US	05-Sep-08	SYSTEM AND METHOD FOR POWER SAVING DELAY LOCKED LOOP CONTROL	Pending		12/205,629
2001-0980.00/US	US	09-Oct-02	THROUGH WAFER PLATING FOR SILICON INTERPOSER TECHNOLOGY	Issued	30-Aug-05 6936536	10/287,822
2001-0980.01/US	US	16-Jul-05	METHODS OF CONDUCTING THROUGH-WAFER VIAS	Issued	04-Sep-07 7265052	11/183,441
2001-0980.02/US	US	21-Feb-07	DEVICE WITH NOVEL CONDUCTIVE VIA STRUCTURE	Pending		11/677,257