PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Palmchip Corporation	09/15/2011

RECEIVING PARTY DATA

Name:	NetVinci, Inc.
Street Address:	P.O. Box 2804
Internal Address:	Scotia Centre, 4th Floor
City:	George Town
State/Country:	CAYMAN ISLANDS
Postal Code:	KY1-1112

PROPERTY NUMBERS Total: 6

Property Type	Number
Patent Number:	6769046
Patent Number:	7062587
Patent Number:	7124376
Patent Number:	5978954
Patent Number:	6601126
Patent Number:	6917997

OP $240.00 6769046

CORRESPONDENCE DATA

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ATTORNEY DOCKET NUMBER:	AF-1 THRU AF-6
NAME OF SUBMITTER:	David Lewis

Total Attachments: 16
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INTELLECTUAL PROPERTY TRANSFER AGREEMENT

This Intellectual Property Transfer Agreement ("Agreement") is entered into as of September 15, 2011 (hereinafter the "Effective Date") by and between:

PalmChip Corporation (hereinafter "Assignor"), a corporation organized under the laws of Delaware; and

NetVinci, Inc. (hereinafter "Assignee"), an exempted corporation organized under the laws of Cayman Islands.

WHEREAS Assignor is the owner and right holder of the Assigned Technology, as defined below;

WHEREAS Assignee is a company involved in the design and manufacture of various integrated circuits ("ICs") and devices embedding those ICs, including but not limited to storage IC, communication IC, controller IC;

WHEREAS Assignee is desirous of acquiring the entire right, title and interests of the Assignor in and to the Assigned Technology and Assignor is willing to assign and transfer all right and interest in and to Assigned Technology on the terms and conditions set forth below;

NOW THEREFORE, in view of the above premises and the following mutual covenants and promises, the parties hereto agree as follows:

Redacted

Redacted

2. IP TRANSFER

2.1 Assignment. Assignor hereby assigns to the Assignee, the Assignee's heirs, executors, administrators, all the Assignor's rights, titles and interests in and to Assigned Technology, and benefits accruing or belonging thereto. Redacted

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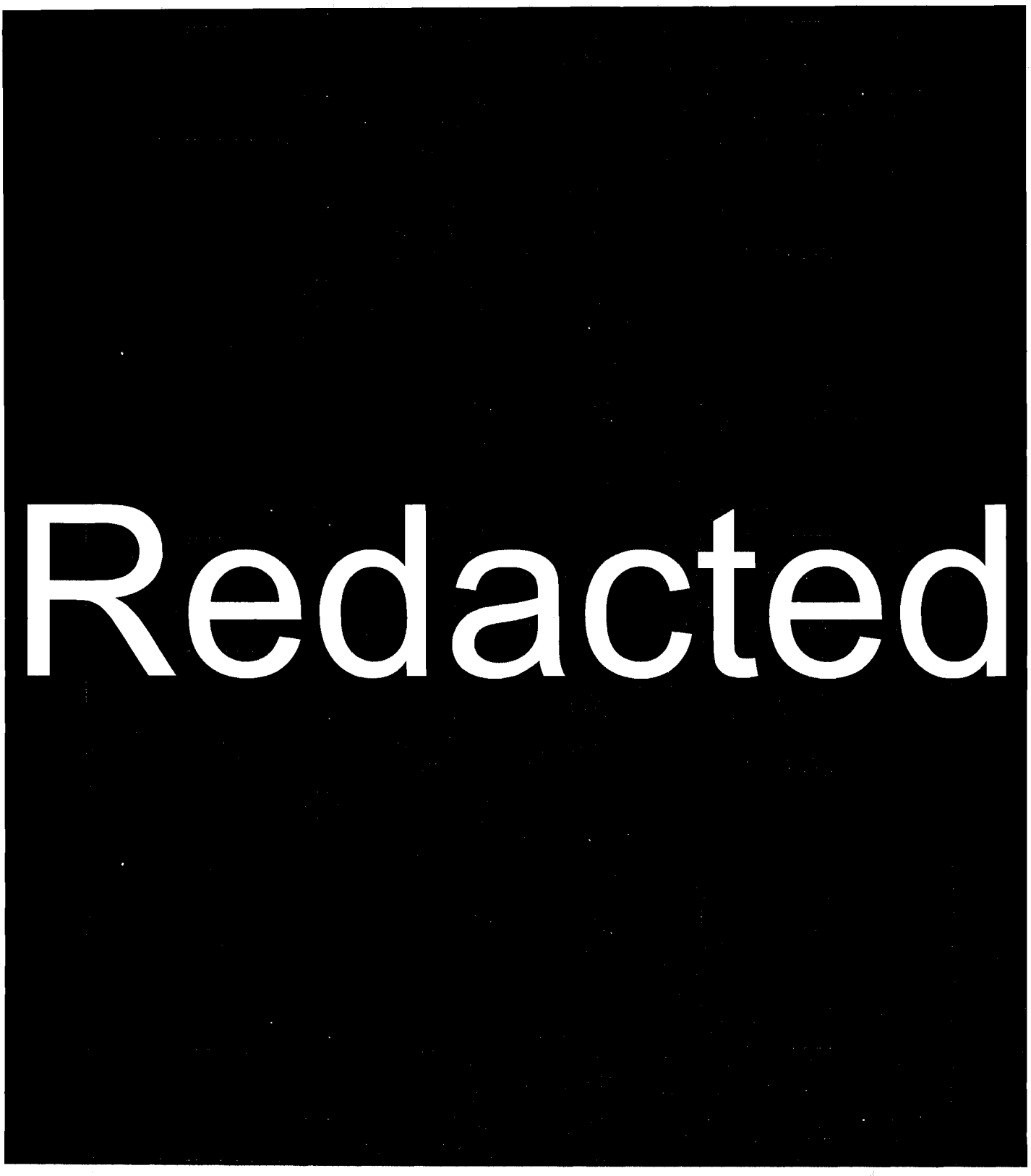
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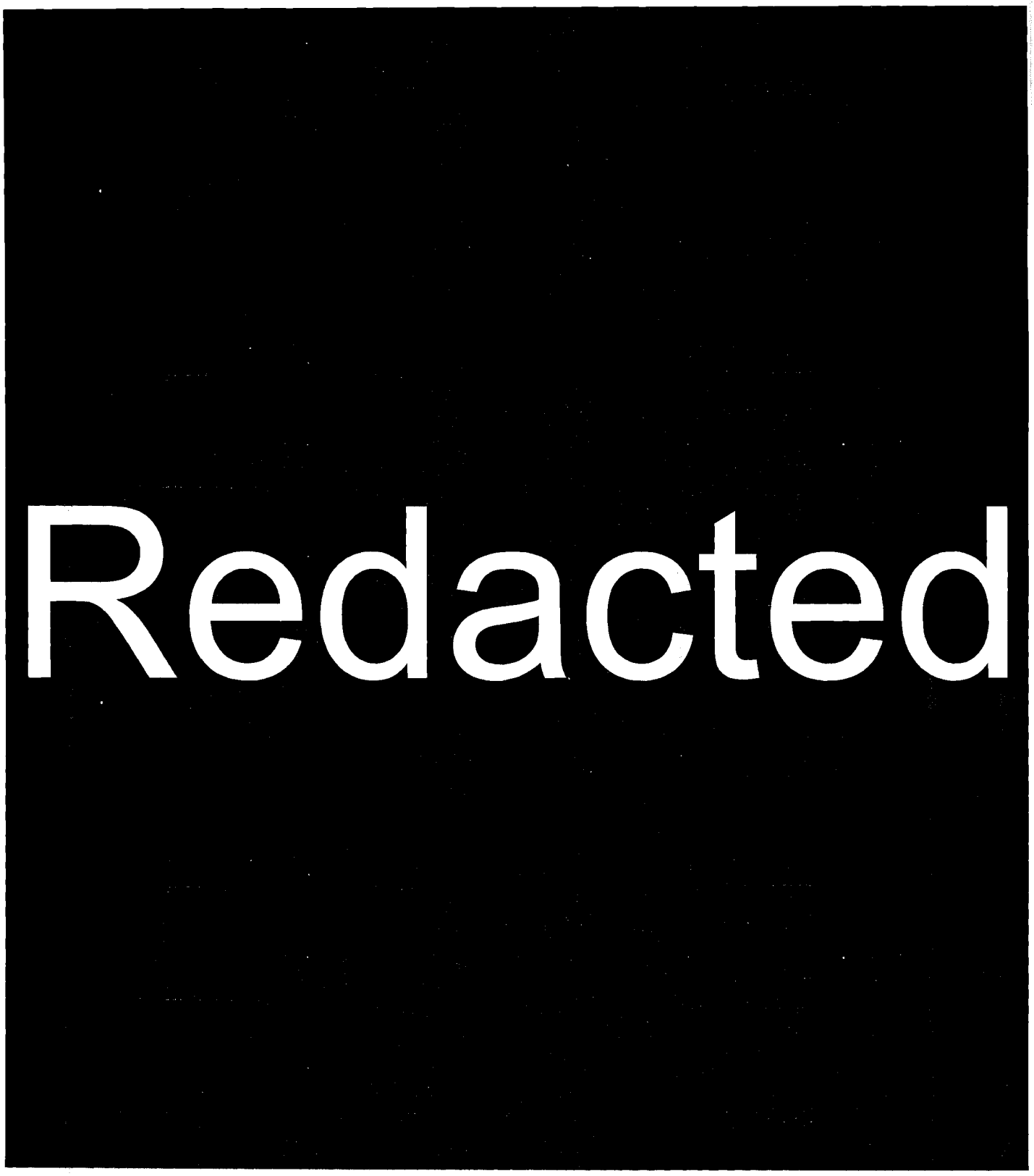
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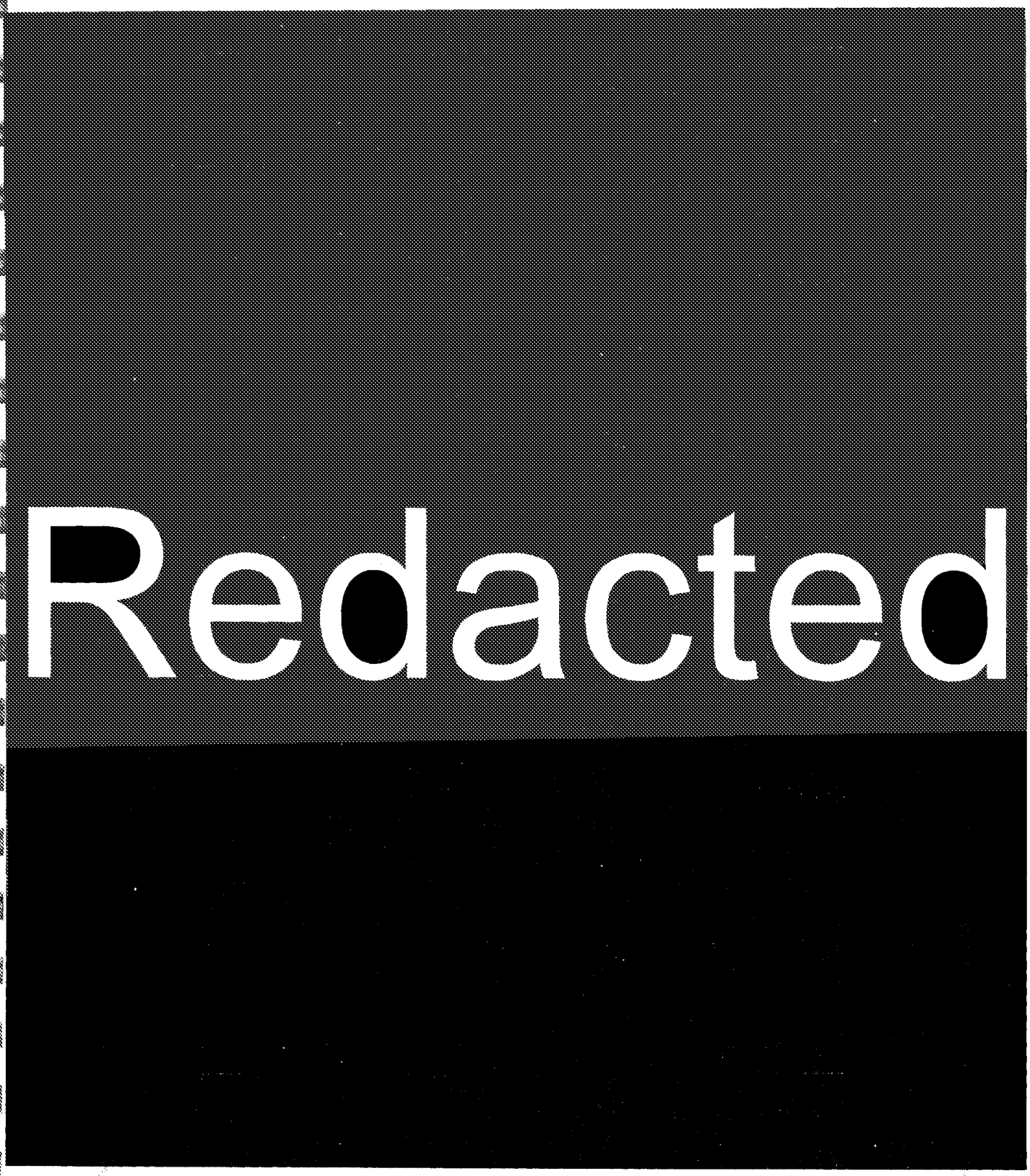
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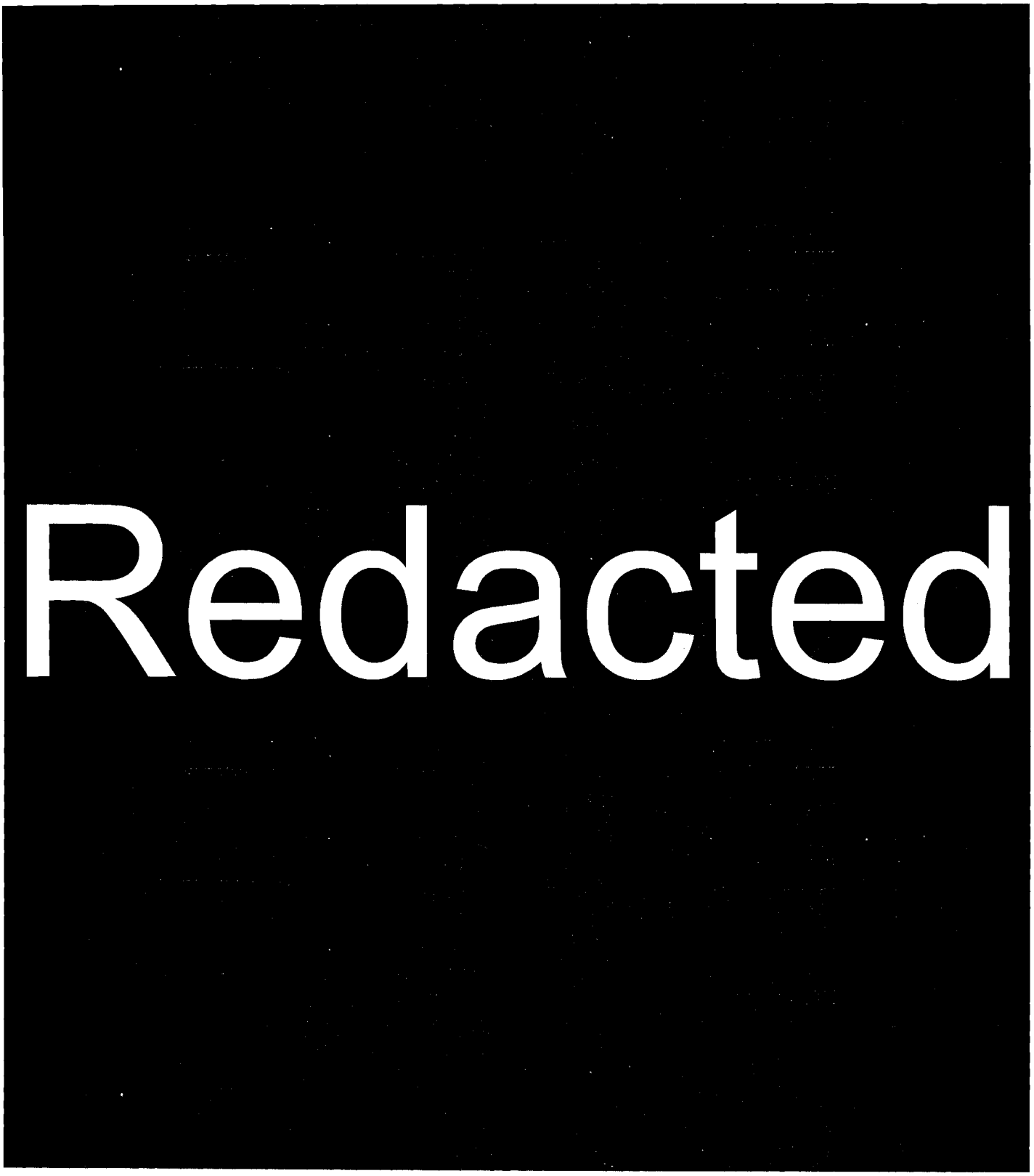
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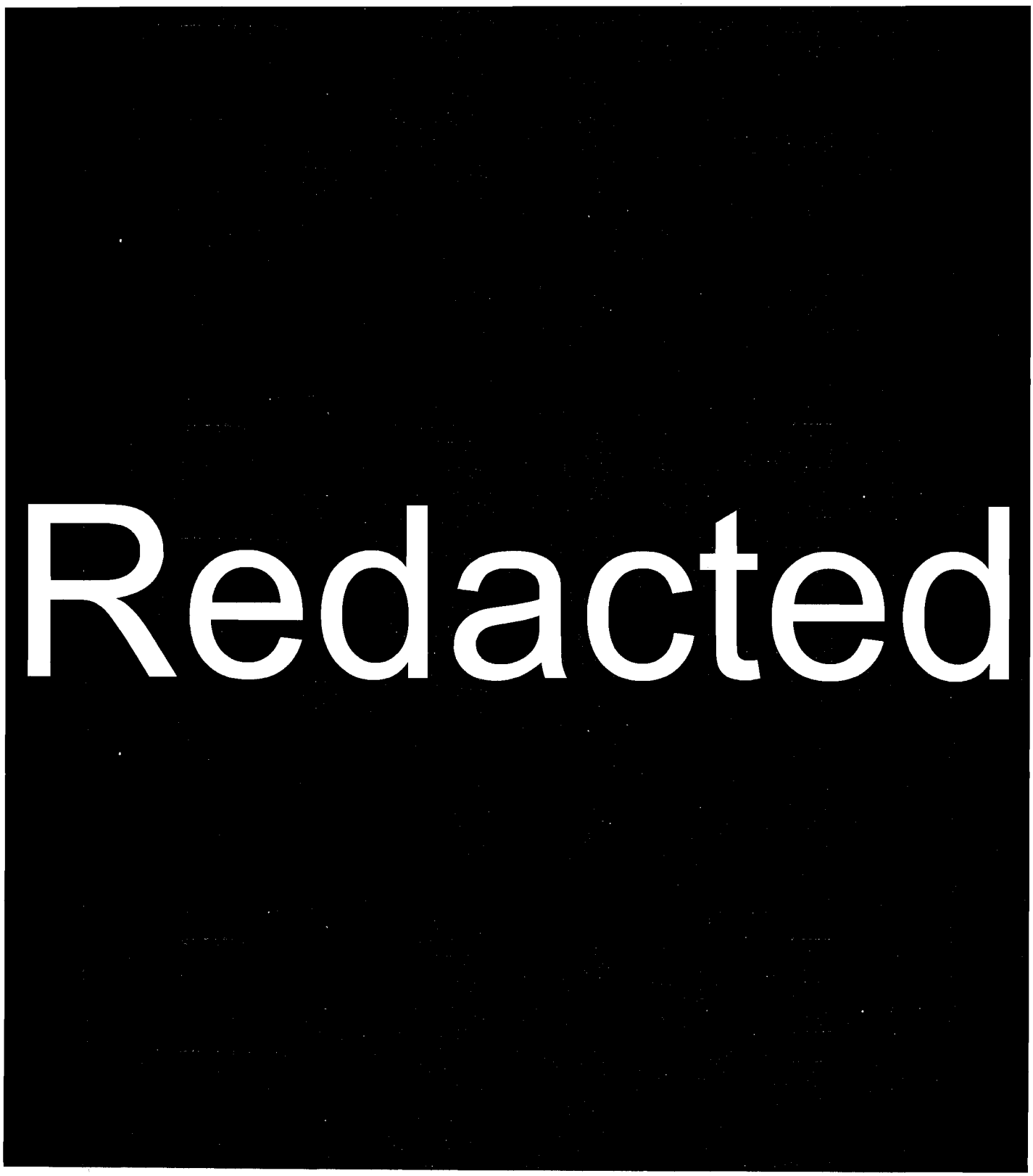
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IN WITNESS THEREOF, the parties have executed this Agreement.

ASSIGNOR:

By _____

(Signature)

Maha Zaid

(Typed or Printed Name)

Title CEO

Date Signed 9/15/2011

ASSIGNEE:

By _____

(Signature)

JAVIER ZAYAS

(Typed or Printed Name)

Title CEO

Date Signed Sep 15, 2011

Exhibit A

Exhibit A-1 Palmchip Patents

1. US Patent No. 5,978,954 – On-the-fly error detection and correction buffer processor
2. US Patent No. 6,601,126 – Chip-core framework for systems-on-a-chip
3. US Patent No. 6,769,046 – System-resource router
4. US Patent No. 7,062,587 – Unidirectional bus architecture for SoC applications
5. US Patent No. 7,124,376 – Design tool for systems-on-a-chip
6. US Patent No. 6,917,997 – Integrated circuit including interrupt controller with shared preamble execution and global-disable control bit

Patent Summary

Patent 1:

•United States Patent **5,978,954**

•**Ou , et al. November 2, 1999**

•Assignee:***Palmchip*** **Corporation** (San Jose, CA)

•On-the-fly error detection and correction buffer processor

Abstract:

An on-the-fly error detection and correction hardware core for a mass storage hard disk drive comprises a microcode machine optimized and limited to doing Galois Field arithmetic (GF[2.sub.8]) in support of Reed-Solomon error detection and correction (RS-EDC). The microcode machine is implemented as a hardware core in a system-on-a-chip design that includes a general purpose core RISC-processor. A dual-input arithmetic logic unit (ALU) includes a set of basic arithmetic blocks necessary to support the RS-EDC operations, i.e., a multiplier, a dedicated adder, a general purpose adder, a divider, a log unit, a quadratic solution lookup, a cubic solution lookup, and a move datapath. The operations and outputs of all the basic arithmetic blocks are presented in parallel to an op-code selector. The selected output is routed back for deposit to one of eight general purpose registers (R0-R7). A set of up to eight syndrome registers (S0-S7) can be selectively routed along with R0-R7 through a pair of

ALU-input selectors. A microinstruction register allows a destination register decoder to be controlled, instruction-by-instruction, as well as the ALU input and output selectors. The microcode program is stored in a ROM-type structure that is indexed by a program counter. A flow control selector allows either the next microprogram address (+1) to be selected from an incrementer, or a branch address to be selected from a jump table.

Patent 2: The most important patent for System on chip bus architecture.

•United States Patent **6,601,126**

•**Zaidi , et al. July 29, 2003**

•Chip-core framework for systems-on-a-chip

•Assignee:***Palmchip*** **Corporation** (San Jose, CA)

Abstract:

A system-on-chip interconnection structure and method uses unidirectional buses only, central shared memory controllers, separate interconnects for high-speed and low-speed peripherals, zero wait-state register accesses, application-specific memory map and peripherals, application-specific test methodology, allowances for cache controllers, and good fits with standard ASIC flow and tools.

Patent 3:

•United States Patent 6,769,046

•**Adams , et al. July 27, 2004**

•System-resource router

•Assignee:***Palmchip*** **Corporation** (San Jose, CA)

Abstract :

A system resource router interfaces initiators through protocol-adapting sockets to a plurality of sub-buses. A switch matrix allows at least some of the sockets to be connected to two or more of the sub-buses. Each sub-bus interfaces through a channel controller to target devices like memory and peripherals. A graphical user interface, assembly program, and computer-aided design platform allow users to customize system resource router configurations for particular applications. At least one embodiment

produces Verilog or other hardware description language intellectual property technology libraries. It implements the optimal mix of sub-buses, switches, sockets, and controllers that will be needed for a particular user application.

Patent 4:

•United States Patent **7,062,587**

•**Zaidi , et al. June 13, 2006**

•Unidirectional bus architecture for SoC applications

•Assignee:***Palmchip*** **Corporation** (San Jose, CA)

Abstract:

The System-on-Chip apparatus and integration methodology disclosed includes a single semiconductor integrated circuit having one or more processor subsystems, one or more DMA-type peripherals, and a Memory Access Controller (MAC) on a first internal unidirectional bus. The first internal unidirectional bus controls transactions between the processor subsystem(s) and the DMA peripheral(s) using a Memory Access Controller (MAC) and unidirectional, positive-edge clocked address and transaction control signals. The first internal unidirectional bus can support burst operation, variable-speed pipelined memory transactions, and hidden arbitration. The SoC may include a second internal unidirectional bus that controls transactions between the processor subsystem(s) and non-DMA peripherals. The second internal unidirectional bus controls transactions between the processor subsystem(s) and the non-DMA peripheral(s) using unidirectional address and transaction control signals. Peripherals may be synchronous or asynchronous to their respective buses.

Patent 5:

•United States Patent 7,124,376

•**Zaidi , et al. October 17, 2006**

•Design tool for systems-on-a-chip

•Assignee:***Palmchip*** **Corporation** (San Jose, CA)

Abstract:

A pre-designed system-on-chip architecture and method includes several standard library devices, HDL source code, simulation environment and regression, synthesis scripts, software header files, software libraries, ASIC verification test suites, and makefiles. The standard library devices comprise an integrated CPU, a shared memory controller, a peripheral controller, system peripherals, a DMA controller, embedded memory, and general system control. CPU bridges are used to accommodate a variety of processor types and to insulate users from the complexities of interfacing to different kinds of processors. Such CPU bridges further allow the latest processors to be rapidly integrated into existing integration platforms and designs.

Patent 6:

•United States Patent **6,917,997**

•**Bhagat. July 12, 2005**

•Integrated circuit including interrupt controller with shared preamble execution and global-disable control bit

•Assignee:***Palmchip*** **Corporation** (San Jose, CA)

Abstract:

A interrupt controller includes specialized interfaces and controls for ARM7TDMI-type microcontroller cores. Such sends interrupt vectors and IRQ or FIQ interrupt requests to the processor depending on particular interrupts received. Wherein, THUMB program execution is more economical with program code space, and an interrupt service routine preamble is coded in ARM program code to cause a switch to THUMB program execution. The interrupt service routine preamble is shared amongst all the interrupt service routines to further economize on program code space.

Modified Form **PTO-1595**

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United States Patent and Trademark Office

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Palmchip Corporation

Signature Date of Assignment (Execution Date):

September 15, 2011

Additional name(s) of conveying party(ies) attached? ☐ Yes ☑ No

2. Name and address of receiving party(ies)

Name: NetVinci, Inc.

Internal Address: Scotia Centre, 4th Floor

Street Address: P.O. Box 2804

City: George Town

State: Grand Cayman

Country: Cayman Islands Zip: KY1-1112

Additional name(s) & address(es) attached? ☐ Yes ☑ No

3. Nature of conveyance

☑ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☐ Government Interest Assignment
☐ Executive Order 9424, Confirmatory License
☐ Other

4. Application or patent number(s): ☐ This document is being filed together with a new application.

A. Patent Application No.(s)

B. Patent No.(s)

(1) 6,769,046
(2) 7,062,587
(3) 7,124,376
(4) 5,978,954
(5) 6,601,126
(6) 6,917,997

Additional numbers attached? ☐ Yes ☑ No

5. Name and address to whom correspondence concerning document should be mailed:

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State: California Zip: 95110

Phone Number: 408-993-1800

Fax Number: 408-993-1800

Email Address: davidlewisnmn@yahoo.com

6. Total number of applications and patents involved: 6

7. Total fee (37 CFR 1.21(h) & 3.41) $ 240.00

☐ Authorized to be charged by credit card
☑ Authorized to be charged to deposit account
☐ Enclosed (PAYMENT MADE BY EFT)
☐ None required (government interest not affecting title)

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Expiration Date

b. Deposit Account Number 503345

Authorized User Name David Lewis

9. Signature:

David Lewis — Signature

March 14, 2012 — Date

David Lewis
Name of Person Signing

Documents to be recorded (including cover sheet) should be faxed to (703) 306-5995, or mailed to:
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☐ Security Agreement ☐ Change of Name
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Name: David Lewis

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Phone Number: 408-993-1800

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March 14, 2012 — Date

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