PATENT ASSIGNMENT

Electronic Version v1.1
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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY AGREEMENT

CONVEYING PARTY DATA

Name	Execution Date
Ramtron International Corporation	02/29/2012

RECEIVING PARTY DATA

Name:	Silicon Valley Bank
Street Address:	3003 Tasman Drive
City:	Santa Clara
State/Country:	CALIFORNIA
Postal Code:	05954

PROPERTY NUMBERS Total: 13

Property Type	Number
Patent Number:	5909624
Patent Number:	5608246
Patent Number:	7176824
Patent Number:	7271744
Patent Number:	7120220
Patent Number:	7142627
Patent Number:	7116572
Patent Number:	7313010
Patent Number:	7570090
Patent Number:	7652909
Patent Number:	7672151
Patent Number:	7924599
Patent Number:	8081500

CORRESPONDENCE DATA

CH $520.00 5909624

Fax Number:	
Email:	trent.martinet@dgslaw.com
Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent via US Mail.	
Correspondent Name:	Trent Martinet
Address Line 1:	1550 17th Street
Address Line 4:	Denver, COLORADO 80202

NAME OF SUBMITTER:	Trent Martinet

Total Attachments: 5
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AMENDED AND RESTATED INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Amended and Restated Intellectual Property Security Agreement (this "Agreement") is entered into as of the Effective Date by and between SILICON VALLEY BANK ("Bank") and RAMTRON INTERNATIONAL CORPORATION, a Delaware corporation ("Grantor").

RECITALS

A. Bank has agreed to make certain advances of money and to extend certain financial accommodation to Grantor (the "Loans") in the amounts and manner set forth in that certain Amended and Restated Loan and Security Agreement by and between Bank and Grantor dated the Effective Date (as the same may be amended, modified or supplemented from time to time, the "Loan Agreement"; capitalized terms used herein are used as defined in the Loan Agreement). Bank is willing to make the Loans to Grantor, but only upon the condition, among others, that Grantor shall grant to Bank a security interest in certain Copyrights, Trademarks, Patents, and Mask Works to secure the obligations of Grantor under the Loan Agreement. This Agreement amends and restates that certain Intellectual Property Security Agreement of Grantor dated as of August 18, 2009.

B. Pursuant to the terms of the Loan Agreement, Grantor has granted to Bank a security interest in all of Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of its obligations under the Loan Agreement, Grantor hereby represents, warrants, covenants and agrees as follows:

AGREEMENT

To secure its obligations under the Loan Agreement, Grantor grants and pledges to Bank a security interest in all of Grantor's right, title and interest in, to and under its Intellectual Property Collateral (including without limitation those Copyrights, Patents, Trademarks and Mask Works listed on Schedules A, B, C, and D hereto), and including without limitation all proceeds thereof (such as, by way of example but not by way of limitation, license royalties and proceeds of infringement suits), the right to sue for past, present and future infringements, all rights corresponding thereto throughout the world and all re-issues, divisions continuations, renewals, extensions and continuations-in-part thereof.

This security interest is granted in conjunction with the security interest granted to Bank under the Loan Agreement. The rights and remedies of Bank with respect to the security interest granted hereby are in addition to those set forth in the Loan Agreement and the other Loan Documents, and those which are now or hereafter available to Bank as a matter of law or equity. Each right, power and remedy of Bank provided for herein or in the Loan Agreement or any of the Loan Documents, or now or hereafter existing at law or in equity shall be cumulative and concurrent and shall be in addition to every right, power or remedy provided for herein and the exercise by Bank of any one or more of the rights, powers or remedies provided for in this Agreement, the Loan Agreement or any of the other Loan Documents, or now or hereafter existing at law or in equity, shall not preclude the simultaneous or later exercise by any person, including Bank, of any or all other rights, powers or remedies.

IN WITNESS WHEREOF, the parties have caused this Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

Address of Grantor:

1850 Ramtron Drive
Colorado Springs, CO 80921

Attn: Gery Richards

Address of Bank:

3003 Tasman Drive
Santa Clara, CA 95054-1191

Attn: Chris Ennis

GRANTOR:

RAMTRON INTERNATIONAL CORPORATION

By: _____

Title: CEO

BANK:

SILICON VALLEY BANK

By: _____

Title: Relationship Manager

EXHIBIT B

Patents

SEE ATTACHED SCHEDULE B

RAM No.	Tech.	Short Title	Patent No.	Issued	Expires	Inventor	Assignee	
ISSUED PATENTS	TOTAL ISSUED:	95						
Application:	America USA							
RAM 352 FWC	FRAM	Semiconductor Device	5,523,595	6/4/1996	6/4/2013	Takenaka		
RAM 357 FWC	FRAM	Semiconductor Device	5,866,926	2/2/1999	2/2/2016	Takenaka		
RAM 358 FWC 2	FRAM	Semiconductor Device	5,475,248	12/12/1995	12/13/2013	Takenaka		
RAM 360	FRAM	Non-Volatile Ferroelectric Memory	5,371,699	12/6/1994	11/17/2012	Larson		
RAM 368 DIV	FRAM/RFID	Integration of High Value Cap w/FE	5,909,624	6/1/1999	9/8/2015	Yeager		
RAM 368 FWC	FRAM/RFID	Integration of High Value Cap w/FE	5,608,246	3/4/1997	2/10/2014	Yeager		
RAM 370	FRAM	High Speed Ferroelectric Based	5,530,668	6/25/1996	4/12/2015	Chern		
RAM 371	FRAM	Voltage Reference for FE 1T/1C	5,572,459	11/5/1996	9/16/2014	Wilson		
RAM 378	FRAM	Passivation Method/Structure Using	5,438,023	8/1/1995	3/11/2014	Argos		
RAM 378 DIV	FRAM	Passivation Method/Structure Using	5,578,867	11/26/1996	3/11/2014	Argos		
RAM 384	FRAM	Circuit Method for Reducing	5,592,410	1/7/1997	4/10/2015	Verhaeghe		
RAM 384 DIV	FRAM	Circuit Method for Reducing	5,815,430	9/29/1998	4/10/2015	Verhaeghe		
RAM 386	FRAM	Low Loss, Regulated Charge Pump	5,889,428	3/30/1999	3/30/2016	Young, D		
RAM 387	FRAM	Ferroelectric Nonvolatile Random	5,598,366	1/28/1997	8/16/2015	Kraus		
RAM 396	FRAM	The Use of Calcium and Strontium	5,969,935	10/19/1999	3/15/2016	Kammerdiner		
RAM 396 DIV	FRAM	The Use of Calcium and Strontium	5,800,683	9/1/1998	3/15/2016	Kammerdiner		
RAM 397	FRAM	A Method of Measuring Retention	6,008,659	12/28/1999	3/15/2016	Traynor		
RAM 399 DIV	FRAM	Yield Enhancement Technique	6,190,926	2/20/2001	2/20/2017	Mitra/Argos		
RAM 405	FRAM	Bandgap Reference Based	5,852,376	12/22/1998	8/23/2016	Kraus		
RAM 407	FRAM	Partially or Completely	5,920,453	7/6/1999	8/20/2016	Evans		
RAM 407 CIP	FRAM	Partially or Completely	5,864,932	2/2/1999	8/20/2016	Evans		
RAM 407CIP2	FRAM	Partially or Completely	6,027,947	2/22/2000	10/11/2016	Evans		
RAM 407CIP2 DIV	FRAM	Method of Fabricating Partially	6,150,184	11/21/2000	11/21/2016	Evans		
RAM 407CIP3	FRAM	Completely Encapsulated TE	6,211,542	4/3/2001	4/3/2017	Eastep/Evans		
RAM 409	FRAM	Semiconductor Memory Device	5,818,771	10/6/1998	9/30/2016	Yoshihiko		
RAM 414	FRAM	Sensing Methodology for a 1T/1C	5,880,989	3/9/1999	11/14/2017	Wilson		
RAM 415	FRAM	Dual-Level Metalization Method	5,902,131	5/11/1999	5/9/2017	Argos		
RAM 415CIP2	FRAM	Multi-Layer approach for Optimizing	6,287,637	9/11/2001	9/11/2017	Fan Chu		
RAM 422	FRAM	Integrated Circuit Memory Device	6,263,398	7/17/2001	7/17/2017	Taylor		
RAM 425	FRAM	Voltage Boost Circuit and Operation	5,854,568	12/29/1998	8/20/2017	Moscaluk		
RAM 433	FRAM	Reference Cell for a 1T/1C	5,956,266	9/21/1999	11/14/2017	Wilson		
RAM 434	FRAM	Memory Cell Config for a 1T/1C	6,028,783	2/22/2000	11/14/2017	Allen/Kraus		
RAM 434CON	FRAM	Memory Cell Config for a 1T/1C	6,185,123	2/6/2001	2/6/2018	Allen/Kraus		
RAM 435	FRAM	Reference Cell Configuration for a	5,986,919	11/16/1999	11/14/2017	Allen		
RAM 435CON	FRAM	Reference Cell Configuration for a	6,252,793	6/26/2001	6/26/2018	Allen/Kraus		
RAM 436	FRAM	Sense Amplifier Configuration for a	5,969,980	10/19/1999	11/14/2017	Allen		
RAM 436CON	FRAM	Sense Amplifier Configuration for a	6,560,137	5/6/2003	5/25/2018	Allen		
RAM 437	FRAM	Column Decoder Configuration for	5,892,728	4/6/1999	11/14/2017	Allen		
RAM 437CON	FRAM	Column Decoder Configuration for	6,856,573	2/15/2005	2/15/2018	Allen/Wilson/Perkalis		
RAM 438	FRAM	Plate Line Driver Circuit for	5,978,251	11/2/1999	11/14/2017	Kraus		
RAM 440	FRAM	Plate Line Driver Circuit for	5,995,406	11/30/1999	11/14/2017	Kraus		
RAM 442	FRAM	FE Thin Films and Solutions	6,203,608	3/20/2001	3/20/2018	Sun/DH/TD		
RAM 444	FRAM	Method of Manufacturing FE Mem	6,174,735	1/16/2001	1/16/2019	Evans		
RAM 444 DIV	FRAM	FE Memory Device Structure Use	6,201,726	3/13/2001	10/23/2018	Evans		
RAM 444 DIV 2	FRAM	FE Memory Device Structure Use	6,358,755	3/19/2002	3/19/2019	Evans		
RAM 446	FRAM	Hydrogen Barrier Encapsulation	6,249,014	6/19/2001	6/10/2018	Bailey		
RAM 446 DIV	FRAM	Hydrogen Barrier Encapsulation	6,613,586	9/2/2003	9/2/2020	Bailey		
RAM 454	FRAM	Barrier Layer to Protect a FE	6,242,299	6/5/2001	6/5/2019	Hickert		
RAM 455	FRAM	FE Non-Volatile Latch Circuit	6,141,237	10/31/2000	10/31/2018	Eliason/Kraus		
RAM 462	FRAM	Nonvolatile Octal Latch & D-Type	6,362,675	3/26/2002	3/26/2019	Alwais		
RAM 466 CIP (FUJ99-228CIP)	FRAM	Semiconductor Device Having a	6,964,873	11/15/2005	11/15/2022	Fox/Chu	FUJ/RIC	
RAM 467	FRAM/Ulvac	High Temperature Deposition of	6,682,772	1/27/2004	1/27/2021	Fox	RIC	
RAM 469 (FUJ99-02886)	FRAM/FUJ RIC	Ferroelectric Thin Film Capacitors	6,627,930	9/30/2003	9/30/2020	Glen Fox, Sun, Chu	FUJ/RIC	
RAM 477	FRAM	Two Stage Low Voltage FE Boost	6,535,446	3/18/2003	6/28/2021	Moscaluk		
RAM 478	FRAM	FE Voltage Boost Circuits	6,275,425	8/14/2001	11/16/2020	Eliason		

RAM 479	FRAM	Process and Structure for Masking	6,495,413	12/17/2002	12/17/2019	Sun, et al		
RAM 480	FRAM	Capacitively Coupled FE Random	6,597,028	7/22/2003	7/22/2020	Glen Fox		
RAM 482	FRAM	Method for Mfg a FE Mem Cell	6,376,259	4/23/2002	4/21/2021	Chu/Fox		
RAM 483	FRAM	Ferroelectric Random Access	6,445,608	9/3/2002	9/10/2018	Schwartz/Alwais		
RAM 485 CON	FRAM	Ferroelectric Random Access	6,661,696	12/9/2003	12/9/2020	Schwartz/Alwais		
RAM 488	FRAM/FUJ-RIC	Process for Producing High Qual	6,887,716	5/3/2005	5/3/2022	Fox/Chu/Easter	FUJ/RIC	
RAM 490	FRAM/FUJ-RIC	Process for Producing a Strontium	6,674,633	1/6/2004	1/6/2021	Sun	FUJ/RIC	
RAM 493	FRAM	Ferroelectric Non-Volatile Logic	6,650,158	11/18/2003	11/18/2020	Eliason		
RAM 493DIV	FRAM	Ferroelectric Non-Volatile Logic	6,894,549	5/17/2005	5/17/2022	Eliason		
RAM 495	FRAM	CMOS Boosting Circuit Utilizing	6,430,093	8/6/2002	8/6/2019	Eliason/Kraus		
RAM 497	FRAM	FE Memory w/Bit-Plate Parallel	6,538,914	3/25/2003	3/25/2020	YB Chung		
RAM 498 (FUJ-41246)	FRAM/FUJ-RIC	FE Semiconductor Memory	6,617,626	9/9/2003	9/9/2020	Fan Chu/Shan Sun	FUJ/RIC	
RAM 498 DIV (FUJ-41246DIV)	FRAM/FUJ-RIC	FE Semiconductor Memory	6,777,287	8/17/2004	8/17/2021	Shan Sun/Fan Chu	FUJ/RIC	
RAM 500	FRAM	Self Referencing 1T/1C FE	6,459,609	10/1/2002	12/13/2018	Xiao Hong DU		
RAM 502	FRAM	Method for Producing Crystall	6,853,535	2/8/2005	10/26/2022	Glen Fox/Tom D.		
RAM 503	FRAM	Method for Producing Crystall	6,728,093	4/27/2004	4/27/2021	Glen Fox		
RAM 506	TI	CMOS Voltage Booster Circuits	6,864,738	3/8/2005	5/8/2022	DU/Eliason/Kraus	TI	
RAM 507	FRAM	Bit-Line Shielding Method for FE	6,717,839	4/6/2004	4/6/2021	Xiao Hong DU		
RAM 508	FRAM/TI	Programmable Reference for 1T1C	6,819,601	11/16/2004	11/16/2021	Eliason/Kraus	TI	
RAM 509	FRAM/TI	Method for Improving Retention	6,830,938	12/14/2004	12/14/2021	Shan Sun (Rodriquez)	TI	
RAM 510	FRAM/TI	Local Interconnect Using the Elec	6,730,950	5/4/2004	5/4/2021	Eliason	TI	
RAM 511	FRAM	Imprint-Free Coding for Ferroelectric	7,176,824	2/13/2007	5/7/2024	Du/Young		
RAM 511 CON	FRAM	Imprint-Free Coding for Ferroelectric	7,271,744	9/18/2007	9/18/2024	Du/Young		
RAM 514	FRAM	Non-Volatile Counter	7,120,220	10/10/2006	10/10/2023	Du/Taylor		
RAM 514 CIP	FRAM	Counting Scheme with Automatic	7,142,627	11/28/2006	2/10/2025	Du/Taylor		
RAM 515	FRAM	Circuit for Generating a Centered	7,116,572	10/3/2006	10/3/2023	Sun/Du/Chu/Sommervold		
RAM 515DIV	FRAM	Circuit for Generating a Centered	7,313,010	12/25/2007	12/25/2024	Sun/Du/Chu/Sommervold		
RAM 522	FRAM/TI	High Reliability Area Efficient	7,038,932	5/2/2006	5/2/2023	Eliason	TI	
RAM 533	GOAL PATENT	Non-Contacating Temp Sensing Device	6,222,454	4/24/2001	4/24/2018	Harling, et. al	GOAL	
RAM 527	FRAM	Fast Power-On Detect Circuit	7,570,090	8/4/2009	12/19/2027	Du		
RAM 528	FRAM	2T2C Ferroelectric RAM with Complementary	7,652,909	10/21/2007	7/17/2028	Du		
RAM 555	FRAM	Method for Reading Non-Volatile Ferroele	7,672,151	3/2/2010	3/2/2027	Evans, et al.		
RAM 556	FRAM	Non-Volatile Memory Circuit Using Ferro	7,924,599	4/12/2011	4/12/2028	Evans, et al.		
RAM 531	FRAM	Method for Mitigating Imprint in a Ferro	8,081,500	11/30/2011	8/28/2029	Taylor/Chu		
Total: 87	**America, U.S.**							
Application:	**CHINA**							
RAM 502/503 CHN	FRAM	Method for Producing Crystallographically	ZL03123976.5	9/12/2007	5/29/2023	Davenport/Fox		
RAM 502/503 CHN DIV	FRAM	Method for Producing Crystallographically	ZL0200710137	10/21/2009	5/29/2023	Davenport/Fox		
Total: 2	**CHINA**							
Application:	**Germany**							
Total: 0	**Germany**							
Application:	**Japan**							
RAM 407 JPN	FRAM	Completely Encapsulated Top Electrode	4,511,642	8/20/1997	8/20/2017	Evans, et al.		
RAM 415 JPN	FRAM	Dual-Level Metalization Method	2,962,475	8/6/1999	5/11/2018	Argos		
RAM 414 JPN	FRAM	Sensing Methodology for a 1T/1C	4,188,472	9/19/2008	11/16/2018	Wilson/Kraus/Lehman		
Total: 3	**Japan**							
Application:	**Korea**							
RAM 442 KOR (MMC)	FRAM	Ferroelectric Thin Films and Sol	453,416	10/8/2004		Shan Sun		
Total: 1	**Korea**							