PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Intel Corporation	03/25/2008

RECEIVING PARTY DATA

Name:	Numonyx B.V.
Street Address:	A-1 Business Centre
Internal Address:	Z.A. Vers la Piece, Rte de l'Etraz
City:	Rolle
State/Country:	SWITZERLAND
Postal Code:	1180

PROPERTY NUMBERS Total: 2

Property Type	Number
Patent Number:	6035401
Patent Number:	6643169

CH $80.00 6035401

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Total Attachments: 23

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ASSIGNMENT

For good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, Intel Corporation, a Delaware Corporation, having an address of 2200 Mission College Boulevard, Santa Clara, CA 95052, U.S.A. ("Assignor"), hereby sells, assigns, transfers and conveys to Numonyx B.V., Acting Through its Swiss Branch, having an address of A-1 Business Centre, Z.A. Vers la Piece, Rte de l'Etraz, 1180 Rolle, Switzerland ("Assignee"), its successors, assigns and legal representatives, Assignor's entire right, title and interest in and to:

1. the U.S. Letters Patents listed on Exhibit A,

2. the U.S. Patent Applications listed on Exhibit B,

3. the foreign patents and patent applications listed on Exhibit C,

and any and all causes of action for past, present, and future infringement of any of said Letters Patents, subject to prior encumbrances,

each and every of the foregoing rights, titles and interests herein assigned to be held and enjoyed by Assignee, its successors, assigns and legal representatives, as fully and entirely as the same would have been held and enjoyed by Assignor had this Assignment not been made.

IN TESTIMONY WHEREOF, Assignor and Assignee having caused this Assignment to be duly executed in their respective names and behalves by affixing their hands thereto by their respective designated officer, director, or agent, whose names and titles appear below.

Executed at SANTA CLARA, CA, this 25TH day of MARCH, 2008

Signature: _____ Signature: _____

Name: Cary I. Klafter Name: _____

(Intel Corporation) (Numonyx B.V.)

VICE PRESIDENT, LEGAL + CORPORATE SECRETARY

LEGAL OK KM KM

For recording

CALIFORNIA ALL-PURPOSE ACKNOWLEDGMENT

State of California
County of SANTA CLARA }

On MARCH 25, 2008 (Date) before me, ANN CUNNINGHAM, NOTARY PUBLIC (Here Insert Name and Title of the Officer),

personally appeared CARY I. KLAFTER (Name(s) of Signer(s))

who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/~~are~~ subscribed to the within instrument and acknowledged to me that he/~~she/they~~ executed the same in his/~~her/their~~ authorized capacity(ies), and that by his/~~her/their~~ signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

Signature _____ (Signature of Notary Public)

ANN CUNNINGHAM
Commission # 1759138
Notary Public - California
Santa Clara County
My Comm. Expires Jul 26, 2011

Place Notary Seal Above

OPTIONAL

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Title or Type of Document: ASSIGNMENT

Document Date: MARCH 25, 2008 Number of Pages: ONE

Signer(s) Other Than Named Above: NUMONYX B.V.

Capacity(ies) Claimed by Signer(s)

Signer's Name: CARY I. KLAFTER
☐ Individual
☒ Corporate Officer — Title(s): VICE PRESIDENT LEGAL + CORP. SECRETARY
☐ Partner — ☐ Limited ☐ General
☐ Attorney in Fact
☐ Trustee
☐ Guardian or Conservator
☐ Other: _____
Signer Is Representing: _____

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Signer's Name: _____
☐ Individual
☐ Corporate Officer — Title(s): _____
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Exhibit A

Country	Patent Number	Publication Number	Serial Number	Title
US	4,841,482		07/157,364	LEAKAGE VERIFICATION FOR FLASH EPROM
US	4,858,186		07/144,569	LOAD LINE FOR FLASH EPROM
US	4,860,261		07/323,310	LEAKAGE VERIFICATION FOR FLASH EPROM
US	4,875,188		07/144,567	VOLTAGE MARGINING CIRCUIT FOR FLASH EPROM
US	4,885,262		07/320,763	CHEMICAL MODIFICATION OF SPIN-ON-GLASS FOR IMPROVED PERFORMANCE IN IC FABRICATION
US	4,932,062		07/351,393	METHOD AND APPARATUS FOR FREQUENCY ANALYSIS OF TELEPHONE SIGNALS
US	4,937,476		07/462,879	SELF-BIASED, HIGH-GAIN DIFFERENTIAL AMPLIFIER WITH FEEDBACK
US	4,947,141		07/335,087	OSCILLATOR NETWORK FOR RADIO RECEIVER
US	4,957,877		07/274,420	PROCESS FOR SIMULTANEOUSLY FABRICATING EEPROM CELL AND FLASH EPROM CELL
US	4,979,214		07/351,785	METHOD AND APPARATUS FOR IDENTIFYING SPEECH IN TELEPHONE SIGNALS
US	4,992,980		07/390,159	A NOVEL ARCHITECTURE FOR VIRTUAL GROUND HIGH DENSITY EPROMS
US	5,023,844		07/486,408	SIX-WAY ACCESS PORTED RAM ARRAY CELL
US	5,046,088		07/429,849	CONVERTER FOR IN-BAND ROUTING AND/OR ORIGINATION INFORMATION
US	5,048,195		07/563,560	APPARATUS AND METHOD FOR ALIGNMENT OF ADJACENT SURFACES
US	5,050,066		07/257,857	QUEUE BLOCK ARCHITECTURE
US	5,050,123		07/612,452	RADIATION SHIELD FOR EPROM CELLS
US	5,061,190		07/567,123	DOUBLE DENSITY BACKWARD AND FORWARD COMPATIBLE CARD EDGE CONNECTOR SYSTEM
US	5,073,969		07/227,078	MICROPROCESSOR BUS INTERFACE UNIT WHICH CHANGES SCHEDULED DATA TRANSFER INDICATIONS UPON SENSING CHANGE IN ENABLE SIGNALS BEFORE RECEIVING READY SIGNAL
US	5,077,738		07/707,241	TEST MODE ENABLE SCHEME FOR MEMORY
US	5,102,814		07/609,192	METHOD FOR IMPROVING DEVICE SCALABILITY OF BURIED BIT LINE FLASH EPROM DEVICES
US	5,123,097		08/294,529	APPARATUS AND METHOD FOR SIMULTANEOUS EXECUTION OF A WRITE INSTRUCTION AND A SUCCEEDING READ INSTRUCTION IN A DATA PROCESSING SYSTEM WITH A STORE THROUGH CACHE STRATEGY
US	5,125,080		07/436,200	LOGIC SUPPORT CHIP FOR AT-TYPE COMPUTER WITH IMPROVED BUS ARCHITECTURE
US	5,126,029		07/635,662	APPARATUS AND METHOD FOR ACHIEVING VIA STEP COVERAGE SYMMETRY
US	5,128,895		07/658,184	APPARATUS AND METHOD FOR IMPROVED READING/PROGRAMMING OF VIRTUAL GROUND EPROM ARRAYS
US	5,131,083		07/333,980	METHOD OF TRANSFERRING BURST DATA IN A MICROPROCESSOR
US	5,136,177		07/747,642	MULTI-QUADRANT CHARGE DOMAIN SYNAPSE CELL
US	5,136,544		07/589,388	COMPUTER MEMORY WITH STATUS CELL
US	5,139,971		07/712,116	ANNEAL TO DECREASE MOISTURE ABSORBANCE OF INTERMETAL DIELECTRICS
US	5,155,377		07/821,634	CHARGE DOMAIN DIFFERENTIAL CONDUCTANCE SYNAPSE CELL FOR NEURAL NETWORKS
US	5,164,330		07/686,683	ETCHBACK PROCESS FOR TUNGSTEN UTILIZING A NF3/AR CHEMISTRY
US	5,168,178		07/752,780	HIGH SPEED NOR'ING, INVERTING, MUX'ING AND LATCHING CIRCUIT WITH TEMPERATURE COMPENSATED OUTPUT NOISE CONTROL
US	5,175,126		07/635,686	IMPROVED TITANIUM NITRIDE BARRIER LAYER

Exhibit A

US	5,177,745	07/589,391	MEMORY DEVICE WITH A TEST MODE
US	5,185,763	07/683,359	DATA BIT TO CONSTELLATION SYMBOL MAPPER
US	5,185,786	07/612,572	AUTOMATIC CALL CENTER OVERFLOW RETRIEVAL SYSTEM
US	5,185,872	07/486,407	SYSTEM FOR EXECUTING DIFFERENT CYCLE INSTRUCTIONS BY SELECTIVELY BYPASSING SCOREBOARD REGISTER AND CANCELING THE EXECUTION OF CONDITIONALLY ISSUED INSTRUCTION IF NEEDED RESOURCES ARE BUSY
US	5,212,910	07/727,829	COMPOSITE POLISHING PAD FOR SEMICONDUCTOR PROCESS
US	5,222,046	07/601,012	PROCESSOR CONTROLLED COMMAND PORT ARCHITECTURE FOR FLASH MEMORY
US	5,237,535	07/773,228	METHOD OF REPAIRING OVERERASED CELLS IN A FLASH MEMORY
US	5,243,700	07/898,190	PORT EXPANDER ARCHITECTURE FOR EPROM
US	5,244,843	07/809,971	NOVEL PROCESS FOR FORMING A THIN OXIDE LAYER
US	5,282,140	07/904,001	PARTICLE FLUX SHADOWING FOR THREE-DIMENSIONAL TOPOGRAPHY SIMULATION
US	5,349,608	08/038,323	VITERBI ACS UNIT WITH RENORMALIZATION
US	5,414,669	08/119,719	METHOD AND APPARATUS FOR PROGRAMMING AND ERASING FLASH EEPROM MEMORY ARRAYS UTILIZING A CHARGE PUMP CIRCUIT
US	5,421,001	07/877,409	COMPUTER METHOD AND APPARATUS FOR A TABLE DRIVEN FILE INTERFACE
US	5,430,674	08/252,850	IMPROVED METHOD AND APPARATUS FOR SEQUENTIAL PROGRAMMING OF A FLASH EEPROM MEMORY
US	5,430,677	08/239,939	ARCHITECTURE FOR READING INFORMATION FROM A MEMORY ARRAY
US	5,448,712	08/201,044	CIRCUITRY AND METHOD FOR PROGRAMMING AND ERASING A NON-VOLATILE SEMICONDUCTOR MEMORY
US	5,488,257	08/384,629	MULTILAYER MOLDED PLASTIC PACKAGE USING MESIC TECHNOLOGY
US	5,508,958	08/315,292	METHOD AND APPARATUS FOR SENSING THE STATE OF FLOATING GATE MEMORY CELLS BY APPLYING A VARIABLE GATE VOLTAGE
US	5,509,134	08/086,186	METHOD AND APPARATUS FOR EXECUTION OF OPERATIONS IN A FLASH MEMORY ARRAY SYSTEM AND METHOD
US	5,513,333	08/100,508	CIRCUITRY AND METHOD FOR PROGRAMMING AND ERASING A NON-VOLATILE SEMICONDUCTOR MEMORY
US	5,515,317	08/252,920	ADDRESSING MODES FOR A DYNAMIC SINGLE BIT PER CELL TO MULTIPLE BIT PER CELL MEMORY
US	5,519,847	08/085,969	METHOD OF PIPELINING SEQUENTIAL WRITES IN A FLASH MEMORY
US	5,532,915	08/217,095	METHOD AND APPARATUS FOR PROVIDING AN ULTRA LOW POWER REGULATED NEGATIVE CHARGE PUMP
US	5,537,350	08/119,520	A COST EFFICIENT SERIES BITS PROGRAMMING FOR THE FLASH MEMORY
US	5,537,357	08/266,132	METHOD FOR PRECONDITIONING A NONVOLATILE MEMORY ARRAY
US	5,539,690	08/252,747	WRITE VERIFY SCHEMES FOR FLASH MEMORY WITH MULTILEVEL CELL
US	5,556,807	08/140,070	ADVANCED MULTILAYER MOLDED PLASTIC PACKAGE USING MESIC TECHNOLOGY
US	5,586,230	08/148,181	SURFACE SWEEPING METHOD FOR SURFACE MOVEMENT IN THREE-DIMENSIONAL TOPOGRAPHY SIMULATION

Exhibit A

US	5,588,728	08/580,489	PORTABLE DISK DRIVE CARRIER AND CHASSIS
US	5,592,435	08/575,339	PIPELINED READ ARCHITECTURE FOR MEMORY
US	5,594,686	08/578,175	METHOD AND APPARATUS FOR PROTECTING DATA STORED IN FLASH MEMORY
US	5,602,794	08/537,233	VARIABLE STAGE CHARGE PUMP
US	5,604,880	08/643,990	COMPUTER SYSTEM WITH A MEMORY IDENTIFICATION SCHEME
US	5,608,669	08/599,123	FAST INTERNAL REFERENCE CELL TRIMMING FOR FLASH EEPROM MEMORY
US	5,608,679	08/594,415	FAST INTERNAL REFERENCE CELL TRIMMING FOR FLASH EEPROM MEMORY
US	5,654,978	08/146,490	PULSE POSITION MODULATION WITH SPREAD SPECTRUM
US	5,663,918	08/575,177	METHOD AND APPARATUS FOR DETECTING AND SELECTING VOLTAGE SUPPLIES FOR FLASH MEMORY
US	5,666,379	08/468,802	BEST-OF-M PULSE POSITION MODULATION DETECTOR
US	5,669,783	08/342,379	IC SOCKET PERMITTING CHECKING CONNECTED STATE BETWEEN IC SOCKET AND PRINTED WIRING BOARD
US	5,684,752	08/724,270	PIPELINED READ ARCHITECTURE FOR MEMORY
US	5,699,612	08/618,686	METHOD OF CHECKING CONNECTED STATE BETWEEN IC SOCKET AND PRINTED WIRING BOARD
US	5,701,272	08/723,666	NEGATIVE VOLTAGE SWITCHING CIRCUIT
US	5,719,436	08/402,933	PACKAGE HOUSING MULTIPLE SEMICONDUCTOR DIES
US	5,732,039	08/720,876	VARIABLE STAGE CHARGE PUMP
US	5,736,777	08/581,436	METHOD AND APPARATUS FOR FAST SELF-DESTRUCTION OF A CMOS INTEGRATED CIRCUIT
US	5,748,546	08/827,670	SENSING SCHEME FOR FLASH MEMORY WITH MULTILEVEL CELLS
US	5,761,054	08/917,988	INTEGRATED CIRCUIT ASSEMBLY PREVENTING INTRUSIONS INTO ELECTRONIC CIRCUITRY
US	5,767,735	08/720,943	VARIABLE STAGE CHARGE PUMP
US	5,781,473	08/720,944	VARIABLE STAGE CHARGE PUMP
US	5,793,101	08/781,358	PACKAGE HOUSING MULTIPLE SEMICONDUCTOR DIES
US	5,809,558	08/819,688	METHOD AND DATA STORAGE SYSTEM FOR STORING DATA IN BLOCKS WITHOUT FILE REALLOCATION BEFORE ERASURE
US	5,822,246	08/723,270	METHOD AND APPARATUS FOR DETECTING THE VOLTAGE ON THE VCC PIN
US	5,824,571	08/575,295	MULTI-LAYERED CONTACTING FOR SECURING INTEGRATED CIRCUITS
US	5,828,616	08/801,004	SENSING SCHEME FOR FLASH MEMORY WITH MULTILEVEL CELLS
US	5,835,413	08/771,445	METHOD FOR IMPROVED DATA RETENTION IN A NONVOLATILE WRITEABLE MEMORY BY SENSING AND REPROGRAMMING CELL VOLTAGE LEVELS
US	5,854,632	08/731,635	APPARATUS AND METHOD FOR SIMULATING SPECULAR REFLECTION IN A COMPUTER GRAPHICS/IMAGING SYSTEM
US	5,892,710	08/910,866	METHOD AND CIRCUITRY FOR STORING DISCRETE AMOUNTS OF CHARGE IN A SINGLE MEMORY ELEMENT
US	5,898,610	08/775,796	METHOD AND APPARATUS FOR BIT CELL GROUND CHOKING FOR IMPROVED MEMORY WRITE MARGIN
US	5,901,358	08/893,938	MOBILE STATION LOCATING SYSTEM AND METHOD
US	5,926,550		PERIPHERAL DEVICE PREVENTING POST-SCAN MODIFICATION

Exhibit A

US	5,933,026	08/834,026	SELF-CONFIGURING INTERFACE ARCHITECTURE ON FLASH MEMORIES
US	5,942,805	08/771,275	A FIDUCIAL FOR ALIGNING AN INTEGRATED CIRCUIT DIE
US	5,974,310	08/823,234	COMMUNICATION CONTROL FOR A USER OF A CENTRAL COMMUNICATION CENTER
US	5,978,591	09/028,367	PERSONAL INFORMATION DEVICE AND METHOD FOR DOWNLOADING REPROGRAMMING DATA FROM A COMPUTER TO THE PERSONAL INFORMATION DEVICE VIA THE PCMCIA PORT OR THROUGH A DOCKING STATION WITH BAUD RATE CONVERSION MEANS
US	5,994,939	09/006,649	VARIABLE DELAY CELL WITH A SELF-BIASING LOAD
US	5,999,593	09/009,561	SYSTEM AND METHOD FOR AUTOMATIC PBX DETECTION
US	6,001,703	08/978,535	METHOD OF FORMING A FIDUCIAL FOR ALIGNING AN INTEGRATED CIRCUIT DIE
US	6,002,721	09/119,479	CARRIER FREQUENCY ESTIMATOR FOR A SIGNAL RECEIVER
US	6,009,497	09/189,000	METHOD AND APPARATUS FOR UPDATING FLASH MEMORY RESIDENT FIRMWARE THROUGH A STANDARD DISK DRIVE INTERFACE
US	6,031,283	08/708,857	INTEGRATED CIRCUIT PACKAGE
US	6,035,401	08/794,283	BLOCK LOCKING APPARATUS FOR FLASH MEMORY
US	6,092,154	08/966,771	METHOD OF PRE-CACHING OR PRE-FETCHING DATA UTILIZING THREAD LISTS AND MULTIMEDIA EDITING SYSTEMS USING SUCH PRE-CACHING
US	6,192,079	09/074,556	METHOD AND APPARATUS FOR INCREASING VIDEO FRAME RATE
US	6,202,209	09/368,878	PERSONAL INFORMATION DEVICE AND METHOD FOR DOWNLOADING REPROGRAMMING DATA FROM A COMPUTER TO THE PERSONAL INFORMATION DEVICE VIA THE PCMCIA PORT OR THROUGH A DOCKING STATION WITH BAUD RATE CONVERSION MEANS
US	6,223,233	09/189,572	WALLET FOR PERSONAL INFORMATION DEVICE
US	6,256,492	09/354,926	COMMUNICATION CONTROL FOR A USER OF A CENTRAL COMMUNICATION CENTER
US	6,272,540	09/224,030	ARRANGEMENT AND METHOD FOR PROVIDING FLEXIBLE MANAGEMENT OF A NETWORK
US	6,304,645	09/518,966	CALL PROCESSING SYSTEM WITH RESOURCES ON MULTIPLE PLATFORMS
US	6,308,073	09/282,281	MOBILE STATION LOCATING AND TRACKING SYSTEM AND METHOD
US	6,342,848	09/518,107	SYSTEM FOR DATA DEPENDENT VOLTAGE BIAS LEVEL
US	6,356,062	09/670,850	DEGENERATIVE LOAD TEMPERATURE CORRECTION FOR CHARGE PUMPS
US	6,396,305	09/823,191	DIGITAL LEAKAGE COMPENSATION CIRCUIT
US	6,438,825	09/008,968	METHOD TO PREVENT INTRUSIONS INTO ELECTRONIC CIRCUITRY
US	6,442,069	09/752,345	DIFFERENTIAL SIGNAL PATH FOR HIGH SPEED DATA TRANSMISSION IN FLASH MEMORY
US	6,449,735	08/672,983	METHOD AND APPARATUS FOR PROVIDING IMPROVED DIAGNOSTIC FUNCTIONS IN A COMPUTER SYSTEM
US	6,469,482	09/607,483	INDUCTIVE CHARGE PUMP CIRCUIT FOR PROVIDING VOLTAGES USEFUL FOR FLASH MEMORY AND OTHER APPLICATIONS
US	6,477,091	09/823,463	METHOD, APPARATUS, AND SYSTEM TO ENHANCE NEGATIVE VOLTAGE SWITCHING
US	6,501,731	09/344,820	CBR/VBR TRAFFIC SCHEDULER
US	6,564,285	09/595,327	SYNCHRONOUS INTERFACE FOR A NONVOLATILE MEMORY

Exhibit A

US	6,577,695		09/526,794	EMULATING NARROW BAND PHASE-LOCKED LOOP BEHAVIOR ON A WIDE BAND PHASE-LOCKED LOOP
US	6,601,179		09/307,324	CIRCUIT AND METHOD FOR CONTROLLING POWER AND PERFORMANCE BASED ON OPERATING ENVIRONMENT
US	6,643,169		09/955,282	VARIABLE LEVEL MEMORY
US	6,650,589		09/997,809	LOW VOLTAGE OPERATION OF STATIC RANDOM ACCESS MEMORY
US	6,657,959		09/335,223	SYSTEMS AND METHODS FOR IMPLEMENTING ABR WITH GUARANTEED MCR
US	6,677,233		10/039,095	MATERIAL DEPOSITION FROM A LIQUEFIED GAS SOLUTION
US	6,725,247		09/846,609	TWO-DIMENSIONAL PYRAMID FILTER ARCHITECTURE
US	6,735,418		09/527,314	ANTENNA INTERFACE
US	6,744,669		10/174,193	MEMORY CIRCUIT INCLUDING BOOSTER PUMP FOR PROGRAMMING VOLTAGE GENERATION
US	6,751,456	20010021650	09/819,460	COMMUNICATION CONTROL FOR A USER OF A CENTRAL COMMUNICATION CENTER
US	6,788,584		10/078,106	METHOD, APPARATUS, AND SYSTEM TO ENHANCE NEGATIVE VOLTAGE SWITCHING
US	6,795,501		08/965,637	MULTI-LAYER CODER/DECODER FOR PRODUCING QUANTIZATION ERROR SIGNAL SAMPLES
US	6,804,317		10/040,689	DIGITAL FRAME DETERMINATION METHOD AND APPARATUS
US	6,822,535	US-2003-0112097-A1	10/109,811	FILM BULK ACOUSTIC RESONATOR STRUCTURE AND METHOD OF MAKING
US	6,833,615		09/751,614	VIA-IN-PAD WITH OFF-CENTER GEOMETRY
US	6,842,133		10/427,163	STROBE THROUGH DIFFERENTIAL SIGNALING
US	6,845,455		09/834,167	WALLET DETACHABLE RETAINING A PERSONAL INFORMATION DEVICE AND RECEIVING A WAKE SIGNAL AND A STAY AWAKE SIGNAL FROM THE PERSONAL INFORMATION DEVICE
US	6,870,767	US-2004-0057355-A1	10/666,988	VARIABLE LEVEL MEMORY
US	6,944,065	US-2004-0228192-A1	10/877,634	METHOD, APPARATUS, AND SYSTEM TO ENHANCE NEGATIVE VOLTAGE SWITCHING
US	6,985,709		09/887,595	NOISE DEPENDENT FILTER
US	7,000,126		10/126,274	METHOD FOR MEDIA CONTENT PRESENTATION IN CONSIDERATION OF SYSTEM POWER
US	7,010,706		09/834,408	APPARATUS HAVING A FIRST CIRCUIT SUPPLYING A POWER POTENTIAL TO A SECOND CIRCUIT UNDER A FIRST OPERATING MODE OTHERWISE DECOUPLING THE POWER POTENTIAL
US	7,047,495		09/607,592	METHOD AND APPARATUS FOR GRAPHICAL DEVICE MANAGEMENT USING A VIRTUAL CONSOLE
US	7,050,663	US-2006-0029323-A1	09/982,227	AN INTEGRATED OPTICAL CIRCUIT HAVING AN INTEGRATED ARRAYED WAVEGUIDE GRATING (AWG) AND OPTICAL AMPLIFIER(S)
US	7,065,327		09/762,720	A SINGLE-CHIP CMOS DIRECT-CONVERSION TRANSCEIVER
US	7,078,912	US-2004-0246006-A1	10/456,076	TECHNIQUES TO TEST SIGNAL PROPAGATION MEDIA
US	7,136,813		09/963,177	PROBABILISTIC NETWORKS FOR DETECTING SIGNAL CONTENT
US	7,141,448		09/874,666	CONTROLLED COLLAPSE CHIP CONNECTION (C4) INTEGRATED CIRCUIT PACKAGE WHICH HAS TWO DISSIMILAR UNDERFILL MATERIALS
US	7,149,883		09/539,734	METHOD AND APPARATUS SELECTIVELY TO ADVANCE A WRITE POINTER FOR A QUEUE BASED ON THE INDICATED VALIDITY OR INVALIDITY OF AN INSTRUCTION STORED WITHIN THE QUEUE
US	7,154,358	US-2005-0030128	10/942,147	FILM BULK ACOUSTIC RESONATOR STRUCTURE AND METHOD OF MAKING
US	7,187,068	US-2006-0033193-A1	10/917,142	METHODS AND APPARATUS FOR PROVIDING STACKED-DIE DEVICES
US	7,194,071		09/749,745	ENHANCED MEDIA GATEWAY CONTROL PROTOCOL

Exhibit A

US	7,268,425	US-2004-0173901-A1	10/382,680	THERMALLY ENHANCED ELECTRONIC FLIP-CHIP PACKAGING WITH EXTERNAL-CONNECTOR-SIDE DIE AND METHOD
US	7,289,525	US-2003-0156535-A1	10/080,329	INVERSE MULTIPLEXING OF MANAGED TRAFFIC FLOWS OVER A MULTI-STAR NETWORK
US	7,289,557	US-2005-0053125-A1	10/660,228	ADAPTIVE EQUALIZATION USING A CONDITIONAL UPDATE SIGN-SIGN LEAST MEAN SQUARE ALGORITHM
US	7,308,713		09/721,785	LINK-LOCK DEVICE AND METHOD OF MONITORING AND CONTROLLING A LINK FOR FAILURES AND INTRUSIONS
US	7,323,360	WWN	10/003,238	ELECTRONIC ASSEMBLY WITH FILLED NO-FLOW UNDERFILL AND METHODS OF MANUFACTURE

Exhibit B

Country	Patent Number	Publication Number	Serial Number	Title
US			09/079,065	POSITION SENSITIVE DISPLAY CONTROLLER
US			09/261,849	CONTROLLED COLLAPSE CHIP CONNECTION (C4) INTEGRATED CIRCUIT PACKAGE WHICH HAS TWO DISSIMILAR UNDERFILL MATERIALS
		US 2002-0014688 A1		
US			09/409,791	CARRIER FREQUENCY ESTIMATOR FOR A SIGNAL RECEIVER
US			09/584,520	REMOTELY MANAGING AND CONTROLLING A CONSUMER APPLIANCE
US			09/733,289	MICROELECTRONIC PACKAGE HAVING AN INTEGRATED HEAT SINK AND BUILD-UP LAYERS
		US 2002-0070443 A1		
US		US-2002-0135563-A1	09/817,719	ENABLING MANUAL ADJUSTMENT OF POINTING DEVICE CURSOR SPEED
US			10/109,313	INTEGRATED OPTOELECTRICAL CIRCUIT PACKAGE WITH OPTICAL WAVEGUIDE INTERCONNECTS
		US 2003-0185484 A1		
US			10/128,373	ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT HAVING A RING OSCILLATOR TIMER CIRCUIT
		US 2003-0202299 A1		
US		US-2004-0128132-A1	10/330,537	PRONUNCIATION NETWORK
US			10/369,933	SYSTEM AND METHOD OF EFFICIENTLY MODULATING DATA USING SYMBOLS HAVING MORE THAN ONE PULSE
		US 2004-0161051 A1		
US			10/396,659	IMPROVED FLOURINE DOPED SIO2 FILM AND METHOD OF FABRICATION
		US 2003-0209805 A1		
US			10/435,347	APPARATUS AND METHOD TO PROVIDE MULTITHREADED COMPUTER PROCESSING
		US 2004-0225840 A1		
US		US-2004-0247024-A1	10/457,092	TECHNIQUES TO PERFORM LINE QUALIFICATION
US		US-2006-0143544-A1	11/015,964	REMOTE STATUS FORWARDING OPERATING IN A DISTRIBUTED SYSTEM
US		US 2006-0133366 A1	11/016,197	CASCADED CONNECTION MATRICES IN A DISTRIBUTED CROSS-CONNECTION SYSTEM
US		US-2006-0153179-A1	11/025,420	TECHNIQUES FOR TRANSMITTING AND RECEIVING TRAFFIC OVER ADVANCED SWITCHING COMPATIBLE SWITCH FABRICS
US		US-2006-0035409-A1	11/212,015	METHODS AND APPARATUSES FOR PROVIDING STACKED-DIE DEVICES
US		US-2007-0127578-A1	11/292,569	LOW DELAY AND SMALL MEMORY FOOTPRINT PICTURE BUFFERING
US		US-2007-0139445-A1	11/303,117	METHOD AND APPARATUS FOR DISPLAYING ROTATED IMAGES
US			60/099,723	A SINGLE-CHIP CMOS DIRECT-CONVERSION TRANSCEIVER
US			60/135,467	ANTENNA INTERFACE

Exhibit C

Country	Patent Number	Publication Number	Serial Number	Title
AU	668379		35952/93	COMPUTER METHOD AND APPARATUS FOR A TABLE DRIVEN FILE PARSER
AU			37233/95	METHOD OF PRE-CACHING DATA UTILIZING THREAD LISTS AND MULTIMEDIA EDITING SYSTEM USING SUCH PRE-CACHING
BE	0251296		87109409.0	PORTABLE COMMUNICATION TERMINAL FOR REMOTE DATABASE QUERY
BR	PI9509921-2	1654	PI9509921-2	PORTABLE DISK DRIVE CARRIER AND CHASSIS
CA			2432906	ENHANCED MEDIA GATEWAY CONTROL PROTOCOL
CA			2463627	AN INTEGRATED OPTICAL CIRCUIT HAVING AN INTEGRATED ARRAYED WAVEGUIDE GRATING (AWG) AND OPTICAL AMPLIFIER(S)
CA	2185333	2185333AA	2185333	METHOD AND APPARATUS FOR PROVIDING AN ULTRA LOW POWER REGULATED NEGATIVE CHARGE PUMP
CA			2355881	ARRANGEMENT AND METHOD FOR PROVIDING FLEXIBLE MANAGEMENT OF A NETWORK
CA			2371945	ANTENNA INTERFACE
CA	2132108		2132108	COMPUTER METHOD AND APPARATUS FOR A TABLE DRIVEN FILE INTERFACE
CA			2408276	REMOTELY MANAGING AND CONTROLLING A CONSUMER APPLIANCE
CA	2318450		2318450	SYSTEM AND METHOD FOR AUTOMATIC PBX DETECTION
CL			1000-96	BEST-OF-M PULSE POSITION MODULATION DETECTOR
CN		CN 1518688A	01822961.1	SYSTEM AND METHOD FOR PROVIDING AUTHENTICATION AND VERIFICATION SERVICES IN AN ENHANCED MEDIA GATEWAY
CN			01822925.5	ENHANCED MEDIA GATEWAY CONTROL PROTOCOL
CN	ZL01821582.3		1821582.3	VIA-IN-PAD WITH OFF-CENTER GEOMETRY AND METHODS OF MANUFACTURE
CN			02813257.2	MATERIAL DEPOSITION FROM A LIQUEFIED GAS SOLUTION
CN		CN 1596449A	02823658.0	LOW VOLTAGE OPERATION OF STATIC RANDOM ACCESS MEMORY
CN		1269082T	98808744.8	MOBILE STATION LOCATING SYSTEM AND METHOD
CN		1589480	02822880.4	VARIABLE LEVEL MEMORY
CN	ZL02821250.9	1575519	2821250.9	ELECTRONIC ASSEMBLY WITH FILLED NO-FLOW UNDERFILL AND METHODS OF MANUFACTURE
CN			02826724.9	DIGITAL FRAME DETERMINATION METHOD AND APPARATUS
CN	ZL 02818839.X	CN 1559067A	02818839.X	PROBABILISTIC NETWORKS FOR DETECTING SIGNAL CONTENT
CN			02828164	FILM BULK ACOUSTIC RESONATOR STRUCTURE AND METHOD OF MAKING
CN		1734424A	200510098094.1	SYSTEM AND METHOD TO DETECT ERRORS AND PREDICT POTENTIAL FAILURES
CN		CN1662870A	03813976.6	METHOD FOR MEDIA CONTENT PRESENTATION IN CONSIDERATION OF SYSTEM POWER
CN		CN1647471A	03808970.X	INVERSE MULTIPLEXING OF MANAGED TRAFFIC FLOWS OVER A MULTI-STAR NETWORK
CN		1732511A	200380107684.5	PRONUNCIATION NETWORK
CN		1792049A		SYSTEM AND METHOD OF EFFICIENTLY MODULATING DATA USING SYMBOLS HAVING MORE THAN ONE PULSE

Exhibit C

CN			200480005928.3	THERMALLY ENHANCED ELECTRONIC FLIP-CHIP PACKAGING WITH EXTERNAL-CONNECTOR-SIDE DIE AND METHOD
CN		CN1902940A	200480039698.2	ANNOTATING MEDIA CONTENT WITH USER-SPECIFIED INFORMATION
CN		1812123	200510023017.X	RESONANT TUNNELING DEVICE USING METAL OXIDE SEMICONDUCTOR PROCESSING
CN		101075422	200610064091.0	METHOD AND APPARATUS FOR DISPLAYING ROTATED IMAGES
CN	ZL95196684.7	1169204	95196684.7	VOLTAGE SUPPLIES FOR FLASH MEMORY
CN	ZL96199936.5	1134825	96199936.5	SECURE SEMICONDUCTOR DEVICE
CN	ZL97181414.7	1110059	97181414.7	METHOD AND APPARATUS FOR DOCKING AND UNDOCKING A NOTEBOOK COMPUTER
CN	ZL00819034.8	1046605a	00819034.8	METHOD AND APPARATUS FOR PERFORMING VIDEO IMAGE DECODING
CN	ZL 99815589.6	1333949	99815589.6	CIRCUIT FOR DATA DEPENDENT VOLTAGE BIAS LEVEL
CN	ZL00816502.5		00816502.5	IMPROVED FLOURINE DOPED SIO2 FILM AND METHOD OF FABRICATION
CN	ZL00804578.X	1350702	00804578.X	A CONTROLLED COLLAPSE CHIP CONNECTION (C4) INTEGRATED CIRCUIT PACKAGE WHICH HAS TWO DISSIMILAR UNDER FILL MATERIALS
CN		1483204	01814712.7	INDUCTIVE CHARGE PUMP CIRCUIT FOR PROVIDING VOLTAGES USEFUL FOR FLASH MEMORY AND OTHER APPLICATIONS
CN		1555573	1820255.1	MICROELECTRONIC PACKAGE HAVING AN INTEGRATED HEAT SINK AND BUILD-UP LAYERS
CN		CN 1531810A	01819255.6	LINK-LOCK DEVICE AND METHOD OF MONITORING AND CONTROLLING A LINK FOR FAILURES AND INTRUSIONS
CN			01806003.X	CALL PROCESSING SYSTEM WITH RESOURCES ON MULTIPLE PLATFORM
CN	ZL01816419.6	1466807	01816419.6	DEGENERATIVE LOAD TEMPERATURE CORRECTION FOR CHARGE PUMPS
CN	ZL99804084.3	CN 1140095C	99804084.3	SYSTEM AND METHOD FOR AUTOMATIC PBX DETECTION
DE	4024930		P4024930.1-53	A NOVEL ARCHITECTURE FOR VIRTUAL GROUND HIGH DENSITY EPROMS
DE	1436648	1436648	02795533.5	AN INTEGRATED OPTICAL CIRCUIT HAVING AN INTEGRATED ARRAYED WAVEGUIDE GRATING (AWG) AND OPTICAL AMPLIFIER(S)
DE	1430525	1430525	02768930.6	DUAL-DAMASCENE INTERCONNECTS WITHOUT AN ETCH STOP LAYER BY ALTERNATING ILDS
DE	1396081	1396081	02725662.7	TWO-DIMENSIONAL PYRAMID FILTER ARCHITECTURE
DE	695 33 487.5-08		9594294.2	PORTABLE DISK DRIVE CARRIER AND CHASSIS
DE	0852799	DE 696 20 774 T2	696 20 774.5-08	VARIABLE STAGE CHARGE PUMP
DE	0815615	0815615	969087568-2308	PACKAGE HOUSING MULTIPLE SEMICONDUCTOR DIES
DE	696 29 925.9-08	DE 696 29 925 T2	96918382.1	NEGATIVE VOLTAGE SWITCHING CIRCUIT
DE	196 81 689		196 81 689.0-33	MULTI-LAYERED CONTACTING FOR SECURING INTEGRATED CIRCUITS
DE	0909416	DE 697 30 430 T2	697 30 430.2	METHOD AND APPARATUS FOR PROVIDING IMPROVED DIAGNOSTIC FUNCTIONS IN A COMPUTER SYSTEM
DE	197 82 133		197 82 133.2	METHOD AND APPARATUS FOR DOCKING AND UNDOCKING A NOTEBOOK COMPUTER
DE	19781978	DE 19781978 T1	197 81 978.8-33	INTEGRATED CIRCUIT PACKAGE
DE		DE 198 82 312 T1	198 82 312.6	SELF-CONFIGURING INTERFACE ARCHITECTURE ON FLASH MEMORIES

Exhibit C

DE	0251296		87103170.0	PORTABLE COMMUNICATION TERMINAL FOR REMOTE DATABASE QUERY
DE		DE 199 86 726 T1	199 83 726.0-42	METHOD AND CIRCUIT FOR DATA DEPENDENT VOLTAGE BIAS LEVEL
DE		DE 100 85 212 T1	100 85 212.2-33	IMPROVED FLOURINE DOPED SIO2 FILM AND METHOD OF FABRICATION
DE	968568	968568	98911466.5	EMULATING NARROW BANK PHASE-LOCKED LOOP BEHAVIOR ON A WIDE BAND PHASE-LOCKED LOOP
DE	697 23 798.2-08		97308183.9	APPARATUS AND METHOD FOR SIMULATING SPECULAR REFLECTION IN A COMPUTER GRAPHICS/IMAGING SYSTEM
DE	0781432	0781432	95935071.1	THREAD LIST EXPLICT CACHING SYSTEM
EP			1273026.3	SYSTEM AND METHOD FOR PROVIDING AUTHENTICATION AND VERIFICATION SERVICES IN AN ENHANCED MEDIA GATEWAY
EP	1436648	1436648	02795533.5	AN INTEGRATED OPTICAL CIRCUIT HAVING AN INTEGRATED ARRAYED WAVEGUIDE GRATING (AWG) AND OPTICAL AMPLIFIER(S)
EP		1346613	1273027.1	VIA-IN-PAD WITH OFF-CENTER GEOMETRY AND METHODS OF MANUFACTURE
EP			02792542.9	MATERIAL DEPOSITION FROM A LIQUEFIED GAS SOLUTION
EP	1396081	1396081	02725662.7	TWO-DIMENSIONAL PYRAMID FILTER ARCHITECTURE
EP		1428221	02757016.7	VARIABLE LEVEL MEMORY
EP		1440469	02802225.9	ELECTRONIC ASSEMBLY WITH FILLED NO-FLOW UNDERFILL AND METHODS OF MANUFACTURE
EP		1468514	02798607.4	DIGITAL FRAME DETERMINATION METHOD AND APPARATUS
EP		1433163	02757625.5	PROBABILISTIC NETWORKS FOR DETECTING SIGNAL CONTENT
EP		1456946	02805206.6	FILM BULK ACOUSTIC RESONATOR STRUCTURE AND METHOD OF PRODUCING IT
EP			05768522.4	SYSTEM AND METHOD TO DETECT ERRORS AND PREDICT POTENTIAL FAILURES
EP		1476994	03717887.8	MULTIPLEXING OF MANAGED AND UNMANAGED TRAFFIC FLOWS OVER A MULTI-STAR NETWORK
EP		1514386	03724240.1	ESTABLISHING AN AD HOC NETWORK
EP		1 595 343	04700900.6	SYSTEM AND METHOD OF EFFICIENTLY MODULATING DATA USING SYMBOLS HAVING MORE THAN ONE PULSE
EP		1604400	04709509.6	THERMALLY ENHANCED ELECTRONIC FLIP-CHIP PACKAGING WITH EXTERNAL-CONNECTOR-SIDE DIE AND METHOD
EP		1 680 926	04 796 692.4	ANNOTATING MEDIA CONTENT WITH USER-SPECIFIED INFORMATION
EP	292791	EP 0 292 791 B1	88107610.3	MICROPROGRAMMED SYSTEMS SOFTWARE INSTRUCTION UNDO
EP	0794717	0794717	95942924.2	PORTABLE DISK DRIVE CARRIER AND CHASSIS
EP	0815615	0815615	96908756.8-2308	A PACKAGE HOUSING MULTIPLE SEMICONDUCTOR DIES
EP		1029416	98946118.1	MULTI-LAYER CODER/DECODER
EP		1048108	99901331.1	VARIABLE DELAY CELL WITH A SELF-BIASING LOAD
EP		1240785	00989714.1	METHOD AND APPARATUS FOR PERFORMING VIDEO IMAGE DECODING
EP	1142202	1142202	99967807.1	ARRANGEMENT AND METHOD FOR PROVIDING FLEXIBLE MANAGEMENT OF A NETWORK
EP		1180267	00932547.3	ANTENNA INTERFACE

Exhibit C

EP	968568	968568	98911466.5	EMULATING NARROW BANK PHASE-LOCKED LOOP BEHAVIOR ON A WIDE BAND PHASE-LOCKED LOOP
EP			99946859.8	A SINGLE-CHIP CMOS DIRECT-CONVERSION TRANSCEIVER
EP		1297530	01941818.5	INDUCTIVE CHARGE PUMP CIRCUIT FOR PROVIDING VOLTAGES USEFUL FOR FLASH MEMORY AND OTHER APPLICATIONS
EP	638188		93904673.6	COMPUTER METHOD AND APPARATUSFOR A TABLE DRIVEN FILE INTERFACE
EP			01948405.4	METHOD AND APPARATUS FOR GRAPHICAL DEVICE MANAGEMENT USING A VIRTUAL CONSOLE
EP		1285384	01935694.8	REMOTELY MANAGING AND CONTROLLING A CONSUMER APPLIANCE
EP		1354354	1992286.3	MICROELECTRONIC PACKAGE HAVING AN INTEGRATED HEAT SINK AND BUILD-UP LAYERS
EP			01995179.7	LINK-LOCK DEVICE AND METHOD OF MONITORING AND CONTROLLING A LINK FOR FAILURES AND INTRUSIONS
EP	0837429	DE 697 23 798 T2	97308183.9	APPARATUS AND METHOD FOR SIMULATING SPECULAR REFLECTION IN A COMPUTER GRAPHICS/IMAGING SYSTEM
EP		1323226	01975434.0	DEGENERATIVE LOAD TEMPERATURE CORRECTION FOR CHARGE PUMPS
EP	0781432	0781432	95935071.1	THREAD LIST EXPLICT CACHING SYSTEM
EP			99904159.3	SYSTEM AND METHOD FOR AUTOMATIC PBX DETECTION
FR	9006713		9006713	A NOVEL ARCHITECTURE FOR VIRTUAL GROUND HIGH DENSITY EPROMS
FR	9208358		9208358	COMPOSITE POLISHING PAD FOR SEMICONDUCTOR PROCESS
FR	1436648	1436648	02795533.5	AN INTEGRATED OPTICAL CIRCUIT HAVING AN INTEGRATED ARRAYED WAVEGUIDE GRATING (AWG) AND OPTICAL AMPLIFIER(S)
FR	1396081	1396081	02725662.7	TWO-DIMENSIONAL PYRAMID FILTER ARCHITECTURE
FR	0830686		96918382.1	NEGATIVE VOLTAGE SWITCHING CIRCUIT
FR	0837429		97308183.9	APPARATUS AND METHOD FOR SIMULATING SPECULAR REFLECTION IN A COMPUTER GRAPHICS/IMAGING SYSTEM
GB	2214380		8820080.3	LOAD LINE FOR FLASH EPROM
GB	2227582		8924745.6	PORT EXPANDER ARCHITECTURE FOR EPROM
GB	2234834		9004859.6	ELECTRICALLY PROGRAMMABLE MEMORY DEVICE
GB	2266796		9314259.4	METHOD OF ACCESSING AN ELECTRICALLY PROGRAMMABLE MEMORY DEVICE
GB	2257382		9203649.0	IMPROVED COMPOSITE POLISHING PAD FOR SEMICONDUCTOR PROCESS
GB	603158		94101294.0	ADVANCED MULTILAYER MOLDED PLASTIC PACKAGE USING MESIC TECHNOLOGY
GB	1436648	1436648	02795533.5	AN INTEGRATED OPTICAL CIRCUIT HAVING AN INTEGRATED ARRAYED WAVEGUIDE GRATING (AWG) AND OPTICAL AMPLIFIER(S)
GB	1396081	1396081	02725662.7	TWO-DIMENSIONAL PYRAMID FILTER ARCHITECTURE
GB	2369702	2369702	0202551.8	PERSONAL INFORMATION DEVICE AND METHOD FOR DOWNLOADING REPROGRAMMING DATA FROM A COMPUTER
GB	292791		881077610.3	METHOD AND APPARATUS FOR BACKING OUT OF A SOFTWARE INSTRUCTION AFTER EXECUTION HAS BEGUN
GB	0794717	0794717	9594294.2	PORTABLE DISK DRIVE CARRIER AND CHASSIS

Exhibit C

GB	0815615	0815615	969087568-2308	PACKAGE HOUSING MULTIPLE SEMICONDUCTOR DIES
GB	2323212	2323212	9811429.1	MULTI-LAYERED CONTACTING FOR SECURING INTEGRATED CIRCUITS
GB	2340973	2340973	9911695.6	METHOD AND APPARATUS FOR DOCKING AND UNDOCKING A NOTEBOOK COMPUTER
GB	2333182	2333182	9905399.3	INTEGRATED CIRCUIT PACKAGE
GB	0251296		87109409.0	PORTABLE COMMUNICATION TERMINAL FOR REMOTE DATABASE QUERY
GB	2353912	2353912	0026721.1	METHOD AND APPARATUS FOR INCREASING VIDEO FRAME RATE
GB	2373372	2373372	0212404.8	IMPROVED FLOURINE DOPED SIO2 FILM
GB	638188		93904673.6	COMPUTER METHOD AND APPARATUS FOR A TABLE DRIVEN FILE PARSER
GB	0781432	0781432	95935071.1	THREAD LIST EXPLICT CACHING SYSTEM
HK	1000475		97102060.5	PORT EXPANDER ARCHITECTURE FOR EPROM
HK			3109116.7	VIA-IN-PAD WITH OFF-CENTER GEOMETRY AND METHODS OF MANUFACTURE
HK		1065662	04108409.4	DIGITAL FRAME DETERMINATION METHOD AND APPARATUS
HK		1063099A	04105864.8	PROBABILISTIC NETWORKS FOR DETECTING SIGNAL CONTENT
HK		1067806	04108659.1	FILM BULK ACOUSTIC RESONATOR STRUCTURE AND METHOD OF PRODUCING IT
HK		1069269	05102495.1	ESTABLISHING AN AD HOC NETWORK
HK		1077946A	05112185.5	SYSTEM AND METHOD OF EFFICIENTLY MODULATING DATA USING SYMBOLS HAVING MORE THAN ONE PULSE
HK		1077124A	05111716.5	THERMALLY ENHANCED ELECTRONIC FLIP-CHIP PACKAGING WITH EXTERNAL-CONNECTOR-SIDE DIE AND METHOD
HK	HK1003252		98102243.4	PORTABLE DISK DRIVE CARRIER AND CHASSIS
HK	HK1002790	1002790A	981015020.2	METHOD AND APPARATUS FOR DETECTING AND SELECTING VOLTAGE SUPPLIES FOR FLASH MEMORY
HK	HK1015520	1015520	99100215.1	VARIABLE STAGE CHARGE PUMP
HK	HK 10098978	10098978	98110789.7	NEGATIVE VOLTAGE SWITCHING CIRCUIT
HK	1016341	1016341	99101098.1	MULTI-LAYERED CONTACTING FOR SECURING INTEGRATED CIRCUITS
HK	HK1017451		99102071	METHOD AND APPARATUS FOR PROVIDING IMPROVED DIAGNOSTIC FUNCTIONS IN A COMPUTER SYSTEM
HK	1027403	1027403	00105429.0	METHOD AND APPARATUS FOR DOCKING AND UNDOCKING A NOTEBOOK COMPUTER
HK	HK1031968	1031968b	01102410.7	METHOD AND APPARATUS FOR INCREASING VIDEO FRAME RATE
HK		1046605A	02108033.0	METHOD AND APPARATUS FOR PERFORMING VIDEO IMAGE DECODING
HK	HK1046331	1046331B	02107701.3	IMPROVED FLOURINE DOPED SIO2 FILM
HK		1052576A	03104815.2	INDUCTIVE CHARGE PUMP CIRCUIT FOR PROVIDING VOLTAGES USEFUL FOR FLASH MEMORY AND OTHER APPLICATIONS
HK			03107859.2	MICROELECTRONIC PACKAGE HAVING AN INTEGRATED HEAT SINK AND BUILD-UP LAYERS
HK			03106719.4	LINK-LOCK DEVICE AND METHOD OF MONITORING AND CONTROLLING A LINK FOR FAILURES AND INTRUSIONS

Exhibit C

HK			03103974.1	CALL PROCESSING SYSTEM WITH RESOURCES ON MULTIPLE PLATFORMS
HK	1005524	1005524A	98194475.9	APPARATUS AND METHOD FOR SIMULATING SPECULAR REFLECTION IN A COMPUTER GRAPHICS/IMAGING SYSTEM
HK		1034154	01103490.8	SYSTEM AND METHOD FOR AUTOMATIC PBX DETECTION
IL	130,563		130,563	METHOD AND APPARATUS FOR BIT CELL GROUND CHOKING FOR IMPROVED MEMORY WRITE MARGIN
IN	195131		675/KOLNP/2003	VIA-IN-PAD WITH OFF-CENTER GEOMETRY AND METHODS OF MANUFACTURE
IN	200061		IN/PCT/2001,01042/MU	CONTROLLED COLLAPSE CHIP CONNECTION (C4) INTEGRATED CIRCUIT PACKAGE WHICH HAS TWO DISSIMILAR UNDERFILL MATERIALS
IN	199364		IN/PCT/2002/01358-C	A METHOD AND SYSTEM FOR PROVIDING INTERNET SERVICES TO A CONSUMER THROUGH REMOTE MANAGEMENT AND CONTROL
IN			540/KOLNP/2003	MICROELECTRONIC PACKAGE HAVING AN INTEGRATED HEAT SINK AND BUILD-UP LAYERS
IR	66126		921103	COMPOSITE POLISHING PAD FOR SEMICONDUCTOR PROCESS
IT	1242497		21015 A/90	A NOVEL ARCHITECTURE FOR VIRTUAL GROUND HIGH DENSITY EPROMS
IT	292791		88107610.3	METHOD AND APPARATUS FOR BACKING OUT OF A SOFTWARE INSTRUCTION AFTER EXECUTION HAS BEGUN
IT			97308183.9	APPARATUS AND METHOD FOR SIMULATING SPECULAR REFLECTION IN A COMPUTER GRAPHICS/IMAGING SYSTEM
JP	3213820		122983/92	ETCHBACK PROCESS FOR TUNGSTEN UTILIZING A NF3/AR CHEMISTRY
JP	317963	5-190808	324108/91	RADIATION SHIELD FOR EPROM CELLS
JP	3099209	5212669A2	154196/92	COMPOSITE POLISHING PAD FOR SEMICONDUCTOR PROCESS
JP		6507275T2	514358/93	ADVANCED MULTILAYER MOLDED PLASTIC PACKAGE USING MESIC TECHNOLOGY
JP	3,416,894	76,023/1994	121,723/1993	A COMPUTER-CONTROLLED DISPLAY SYSTEM
JP	3,365,565	52,269/1994	121,605/1993	PARTICLE FLUX SHADOWING FOR THREE-DIMENSIONAL TOPOGRAPHY SIMULATION
JP		2004-527816	2002-554833	SYSTEM AND METHOD FOR PROVIDING AUTHENTICATION AND VERIFICATION SERVICES IN AN ENHANCED MEDIA GATEWAY
JP		2005-504448	2002-555069	ENHANCED MEDIA GATEWAY CONTROL PROTOCOL
JP			2003-536786	AN INTEGRATED OPTICAL CIRCUIT HAVING AN INTEGRATED ARRAYED WAVEGUIDE GRATING (AWG) AND OPTICAL AMPLIFIER(S)
JP			2002-555593	VIA-IN-PAD WITH OFF-CENTER GEOMETRY AND METHODS OF MANUFACTURE
JP		P2005-512261A	P2003-550231	LOW VOLTAGE OPERATION OF STATIC RANDOM ACCESS MEMORY
JP		2004-525460	2002-575882	ENABLING MANUAL ADJUSTMENT OF POINTING DEVICE CURSOR SPEED
JP			2002-586286	TWO-DIMENSIONAL PYRAMID FILTER ARCHITECTURE
JP		2003-506787A	2001-516051	PERSONAL INFORMATION DEVICE AND METHOD FOR DOWNLOADING REPROGRAMMING DATA FROM A COMPUTER TO THE PERSONAL INFORMATION DEVICE VIA THE PCMCIA PORT OR THROUGH A DOCKING STATION WITH BAUD RATE CONVERSION MEANS
JP			2003-553708	FILM BULK ACOUSTIC RESONATOR STRUCTURE AND METHOD OF MAKING

Exhibit C

JP			586733/2003	METHOD FOR MEDIA CONTENT PRESENTATION IN CONSIDERATION OF SYSTEM POWER
JP			2004-500440	ESTABLISHING AN AD HOC NETWORK
JP		P2006-522385A		APPARATUS AND METHOD TO PROVIDE MULTITHREADED COMPUTER PROCESSING
JP			2006-538272	ANNOTATING MEDIA CONTENT WITH USER-SPECIFIED INFORMATION
JP	3,667,786		71270/94	IC SOCKET PERMITTING CHECKING CONNECTED STATE BETWEEN IC SOCKET AND PRINTED WIRING BOARD
JP	3688710		524718/95	METHOD AND APPARATUS FOR PROVIDING AN ULTRA LOW POWER REGULATED NEGATIVE CHARGE PUMP
JP	1865189		121665/88	METHOD AND APPARATUS FOR BACKING OUT OF A SOFTWARE INSTRUCTION AFTER EXECUTION HAS BEGUN
JP			514005/96	METHOD AND APPARATUS FOR DETECTING AND SELECTING VOLTAGE SUPPLIES FOR FLASH MEMORY
JP	3766101		513766/97	VARIABLE STAGE CHARGE PUMP
JP	3717937		527776/96	A PACKAGE HOUSING MULTIPLE SEMICONDUCTOR DIES
JP			501941/97	NEGATIVE VOLTAGE SWITCHING CIRCUIT
JP			523636/98	METHOD AND APPARATUS FOR DOCKING AND UNDOCKING A NOTEBOOK COMPUTER
JP			530079/98	METHOD AND APPARATUS FOR BIT CELL GROUND CHOKING FOR IMPROVED MEMORY WRITE MARGIN
JP			541666/98	A PERIPHERAL DEVICE PREVENTING POST-SCAN MODIFICATION
JP			2000-519556	MULTI-LAYER CODER/DECODER
JP			2000-540619	A VARIABLE DELAY CELL WITH A SELF-BIASING LOAD
JP			2000-547785	METHOD AND APPARATUS FOR INCREASING VIDEO FRAME RATE
JP			2000-583167	METHOD AND CIRCUIT FOR DATA DEPENDENT VOLTAGE BIAS LEVEL
JP			2000-603092	CONTROLLED COLLAPSE CHIP CONNECTION (C4) INTEGRATED CIRCUIT PACKAGE WHICH HAS TWO DISSIMILAR UNDERFILL MATERIALS
JP	3786419		519231/93	COMPUTER METHOD AND APPARATUSFOR A TABLE DRIVEN FILE INTERFACE
JP			2002-548782	MICROELECTRONIC PACKAGE HAVING AN INTEGRATED HEAT SINK AND BUILD-UP LAYERS
JP	3813873	2003-526285	2001-565629	CALL PROCESSING SYSTEM WITH RESOURCES ON MULTIPLE PLATFORM
JP		10-134206	195011/1997	APPARATUS AND METHOD FOR SIMULATING SPECULAR REFLECTION IN A COMPUTER GRAPHICS/IMAGING SYSTEM
KR	214163		92-4336	COMPOSITE POLISHING PAD FOR SEMICONDUCTOR PROCESS
KR		10-2005-0037411	10-2004-7005595	AN INTEGRATED OPTICAL CIRCUIT HAVING AN INTEGRATED ARRAYED WAVEGUIDE GRATING (AWG) AND OPTICAL AMPLIFIER(S)
KR	10-0603879	10-2003-0067738	10-2003-7008832	VIA-IN-PAD WITH OFF-CENTER GEOMETRY AND METHODS OF MANUFACTURE
KR		10-2005-0058249	10-2004-7008174	LOW VOLTAGE OPERATION OF STATIC RANDOM ACCESS MEMORY
KR	0550676	2004-0015207	10-2003-7014161	TWO-DIMENSIONAL PYRAMID FILTER ARCHITECTURE
KR		10-2004-0044938	10-2004-7003885	VARIABLE LEVEL MEMORY

Exhibit C

KR		10-2004-0066919	10-2004-7009478	FILM BULK ACOUSTIC RESONATOR STRUCTURE AND METHOD OF PRODUCING IT
KR		10-2004-101489	10-2004-7016496	METHOD FOR MEDIA CONTENT PRESENTATION IN CONSIDERATION OF SYSTEM POWER
KR		10-2006-0023963	2005-7021223	APPARATUS AND METHOD TO PROVIDE MULTITHREADED COMPUTER PROCESSING
KR	263275		1996-705254	METHOD AND APPARATUS FOR PROVIDING AN ULTRA LOW POWER REGULATED NEGATIVE CHARGE PUMP
KR	95/10128		95/10128	PORTABLE DISK DRIVE CARRIER AND CHASSIS
KR	292832	1999-0022544	1997-709025	NEGATIVE VOLTAGE SWITCHING CIRCUIT
KR	307895	10-0307895	1998-704709	MULTI-LAYERED CONTACTING FOR SECURING INTEGRATED CIRCUITS
KR	387336	2000-69050	1999-7004461	VARIOUS APPARATUS FOR DOCKING AND UNDOCKING A NOTEBOOK COMPUTER
KR	343029		1999-7005947	METHOD AND APPARATUS FOR BIT CELL GROUND CHOKING FOR IMPROVED MEMORY WRITE MARGIN
KR	488324		1999-7001953	AN INTEGRATED CIRCUIT PACKAGE
KR	387338	2001-6234	1999-7009316	SELF-CONFIGURING 108 AND 3.0 VOLT INTERFACE ARCHITECTURE ON FLASH MEMORIES
KR	0367110	2001-0034112	10-2000-7007725	A VARIABLE DELAY CELL WITH A SELF-BIASING LOAD
KR	430139	2001-43403	2000-7012436	POSITION SENSITIVE DISPLAY CONTROLLER
KR	0569749	2001-0080431	10-2001-7006012	METHOD AND CIRCUIT FOR DATA DEPENDENT VOLTAGE BIAS LEVEL
KR	0522383	2001-0108306	2001-7011227	CONTROLLED COLLAPSE CHIP CONNECTION (C4) INTEGRATED CIRCUIT PACKAGE WHICH HAS TWO DISSIMILAR UNDERFILL MATERIALS
KR	0498675	10-2005-0019917	10-2005-7001212	CONTROLLED COLLAPSE CHIP CONNECTION (C4) INTEGRATED CIRCUIT PACKAGE WHICH HAS TWO DISSIMILAR UNDERFILL MATERIALS
KR		10-2004-14432	10-2003-7007506	MICROELECTRONIC PACKAGE HAVING AN INTEGRATED HEAT SINK AND BUILD-UP LAYERS
KR	0548910	2003-0043974	10-2003-7004397	DEGENERATIVE LOAD TEMPERATURE CORRECTION FOR CHARGE PUMPS
MX			PA/A/2001/008580	CONTROLLED COLLAPSE CHIP CONNECTION (C4) INTEGRATED CIRCUIT PACKAGE WHICH HAS TWO DISSIMILAR UNDERFILL MATERIALS
MY	MY-130278-A		PI20015604	VIA-IN-PAD WITH OFF-CENTER GEOMETRY AND METHODS OF MANUFACTURE
MY	MY - 122780 - A		PI 20020207	DIGITAL LEAKAGE COMPENSATION CIRCUIT
MY			PI 2022322	NOISE DEPENDENT FILTER
MY			PI20024718	FILM BULK ACOUSTIC RESONATOR STRUCTURE AND METHOD OF MAKING
MY			PI 20041684	APPARATUS AND METHOD TO PROVIDE MULTITHREADED COMPUTER PROCESSING
MY	MY-124,460-A		9600858	PACKAGE HOUSING MULTIPLE SEMICONDUCTOR DIES
MY	MY-116966-A		9704164	AN INTEGRATED CIRCUIT PACKAGE
MY	MY-122,261-A		9801913	SELF-CONFIGURING 1.8 AND 3.0 VOLT INTERFACE ARCHITECTURE ON FLASH MEMORIES
MY			PI20015198	MICROELECTRONIC PACKAGE HAVING AN INTEGRATED HEAT SINK AND BUILD-UP LAYERS
NL	1396081	1396081	02725662.7	TWO-DIMENSIONAL PYRAMID FILTER ARCHITECTURE
PCT		WO 92/022086	PCT/US92/04145	ANNEAL TO DECREASE MOISTURE ABSORBANCE OF INTERMETAL DIELECTRICS

Exhibit C

PCT	WO02/054201A2	PCT/US01/44675	SYSTEM AND METHOD FOR PROVIDING AUTHENTICATION AND VERIFICATION SERVICES IN AN ENHANCED MEDIA GATEWAY
PCT	WO 00/01167	PCT/US99/14500	SYSTEMS AND METHODS FOR IMPLEMENTING ABR WITH GUARANTEED MCR
PCT	WO 00/01120	PCT/US99/14268	CBR/VBR TRAFFIC SCHEDULER
PCT	WO02/054707A2	PCT/US01/49779	ENHANCED MEDIA GATEWAY CONTROL PROTOCOL
PCT	WO 02/054838	PCT/US01/44721	VIA-IN-PAD WITH OFF-CENTER GEOMETRY AND METHODS OF MANUFACTURE
PCT		PCT/US02/41705	MATERIAL DEPOSITION FROM A LIQUEFIED GAS SOLUTION
PCT	WO 02/080179	PCT/US02/03633	DIGITAL LEAKAGE COMPENSATION CIRCUIT
PCT	WO 02/084468	PCT/US02/10816	APPARATUS AND CIRCUIT HAVING REDUCED LEAKAGE CURRENT AND METHOD THEREFOR
PCT	02/077916	PCT/US02/02110	ENABLING MANUAL ADJUSTMENT OF POINTING DEVICE CURSOR SPEED
PCT	WO 96/42137A1	PCT/US96/06811	BEST-OF-M PULSE POSITION MODULATION DETECTOR
PCT	WO 98/042111	PCT/US98/04864	COMMUNICATION CONTROL FOR A USER OF A CENTRAL COMMUNICATION CENTER
PCT	WO 03/025948	PCT/US02/25092	VARIABLE LEVEL MEMORY
PCT	WO 03/036692	PCT/US02/34516	ELECTRONIC ASSEMBLY WITH FILLED NO-FLOW UNDERFILL AND METHODS OF MANUFACTURE
PCT	WO 01/11467	PCT/US99/27132	PERSONAL INFORMATION DEVICE AND METHOD FOR DOWNLOADING REPROGRAMMING DATA FROM A COMPUTER
PCT	WO 00/28426	PCT/US99/26626	WALLET FOR PERSONAL INFORMATION DEVICE
PCT	WO 03/061169	PCT/US02/41548	DIGITAL FRAME DETERMINATION METHOD AND APPARATUS
PCT	WO 03/028008	PCT/US02/28358	PROBABILISTIC NETWORKS FOR DETECTING SIGNAL CONTENT
PCT		PCT/US03/04584	INTEGRATED OPTOELECTRICAL CIRCUIT PACKAGE WITH OPTICAL WAVEGUIDE INTERCONNECTS
PCT	2006/014400	PCT/US05/23733	SYSTEM AND METHOD TO DETECT ERRORS AND PREDICT POTENTIAL FAILURES
PCT	WO 03/090056	PCT/US03/11345	METHOD FOR MEDIA CONTENT PRESENTATION IN CONSIDERATION OF SYSTEM POWER
PCT	WO 03/073708A1	PCT/US03/03691	INVERSE MULTIPLEXING OF MANAGED TRAFFIC FLOWS OVER A MULTI-STAR NETWORK
PCT		PCT/US03/09535	ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT HAVING A RING OSCILLATOR TIMER CIRCUIT
PCT	WO 03/092205	PCT/US03/12902	ESTABLISHING AN AD HOC NETWORK
PCT	WO 2005/027446 A1	PCT/US04/29175	ADAPTIVE EQUALIZATION USING A CONDITIONAL UPDATE SIGN-SIGN LEAST MEAN SQUARE ALGORITHM
PCT	WO 2004/061821	PCT/US03/39108	PRONUNCIATION NETWORK
PCT	WO 2004/102376	PCT/US2004/012020	APPARATUS AND METHOD TO PROVIDE MULTITHREADED COMPUTER PROCESSING
PCT	WO 2004/079823	PCT/US04/03817	THERMALLY ENHANCED ELECTRONIC FLIP-CHIP PACKAGING WITH EXTERNAL-CONNECTOR-SIDE DIE AND METHOD
PCT	WO 2004/112366 A1	PCT/US2004/016583	TECHNIQUES TO PERFORM LINE QUALIFICATION
PCT	WO 2004/099169 A2	PCT/US2004/011645	METHOD AND APPARATUS USING DIFFERENTIAL SIGNALING AND COMMON MODE SIGNALING

Exhibit C

PCT	WO 2004/111666 A1	PCT/US2004/016587	TECHNIQUES TO TEST SIGNAL PROPAGATION MEDIA
PCT	WO 2006/020438	PCT/US2005/027103	METHODS AND APPARATUS FOR PROVIDING STACKED-DIE DEVICES
PCT	WO 2006/066276	PCT/US05/46571	UNIFYING CASCADED CONNECTION MATRICES IN A DISTRIBUTED CROSS-CONNECTION SYSTEM
PCT	WO 2006/066165	PCT/US05/45850	REMOTE STATUS FORWARDING OPERATING IN A DISTRIBUTED SYSTEM
PCT	wo2006/072053	PCT/US2005/047581	TECHNIQUES FOR TRANSMITTING AND RECEIVING TRAFFIC OVER ADVANCED SWITCHING COMPATIBLE SWITCH FABRICS
PCT	WO 2006/062730	PCT/US05/42254	AIRFLOW CONTROL SYSTEM
PCT	WO 2006/050283	PCT/US2005/039310	RESONANT TUNNELING TRANSISTOR USING CONVENTIONAL MOSFET PROCESSING
PCT	WO 2006/086129	PCT/US06/01918	ADVANCED TCA CHASSIS WITH A MOVABLE FAN TRAY
PCT	WO 2007/075294	PCT/US2006/046778	METHOD AND APPARATUS FOR DISPLAYING ROTATED IMAGES
PCT	WO 2007/065008 A1	PCT/US2006/046260	LOW DELAY AND SMALL MEMORY FOOTPRINT PICTURE BUFFERING
PCT		PCT/US95/15443	PORTABLE DISK DRIVE CARRIER AND CHASSIS
PCT		PCT/US96/03331	PACKAGE HOUSING MULTIPLE SEMICONDUCTOR DIES
PCT	WO 97/22990	PCT/US96/19808	SECURE SEMICONDUCTOR DEVICE
PCT	WO 98/22968	PCT/US97/17491	METHOD AND APPARATUS FOR DOCKING AND UNDOCKING A NOTEBOOK COMPUTER
PCT	WO 97/024765	PCT/US96/20808	METHOD AND APPARATUS FOR FAST SELF-DESTRUCTION OF A CMOS INTEGRATED CIRCUIT
PCT	WO 98/28748	PCT/US97/18694	METHOD AND APPARATUS FOR IMPROVED DATA RETENTION IN NONVOLATILE MEMORY VIA EQUALIZATION OF CELL VOLTAGE LEVELS
PCT	WO 98/10466	PCT/US97/11890	INTEGRATED CIRCUIT PACKAGE
PCT	WO 98/30913	PCT/US97/22690	A FIDUCIAL FOR ALIGNING AN INTEGRATED CIRCUIT DIE
PCT	WO 98/44676	PCT/US98/05010	A PERIPHERAL DEVICE PREVENTING POST-SCAN MODIFICATION
PCT	WO 99/23826	PCT/US98/19536	MULTI-LAYER CODER/DECODER
PCT			CIRCUIT AND METHOD FOR CONTROLLING POWER AND PERFORMANCE BASED ON OPERATING ENVIRONMENT
PCT		PCT/US98/07759	A CIRCUIT AND METHOD FOR CONTROLLING POWER AND PERFORMANCE BASED ON OPERATING ENVIRONMENT
PCT	WO 99/37024	PCT/US99/00191	A VARIABLE DELAY CELL WITH A SELF-BIASING LOAD
PCT	WO 99/58935	PCT/US99/08034	POSITION SENSITIVE DISPLAY CONTROLLER
PCT	WO 99/57906	PCT/US99/05436	METHOD AND APPARATUS FOR INCREASING VIDEO FRAME RATE
PCT	WO 2001/077821	PCT/US01/08104	METHOD AND APPARATUS FOR WRITING INSTRUCTIONS INTO A BUFFER QUEUE INCLUDING OVERWRITING INVALID ENTRIES
PCT		PCT/US00/28164	IMPROVED FLOURINE DOPED SIO2 FILM
PCT	WO 00/52756	PCT/US00/03242	CONTROLLED COLLAPSE CHIP CONNECTION (C4) INTEGRATED CIRCUIT PACKAGE WHICH HAS TWO DISSIMILAR UNDERFILL MATERIALS
PCT	WO 00/072457	PCT/US00/13606	ANTENNA INTERFACE

Exhibit C

PCT		WO 98/39847	PCT/US98/04175	EMULATING NARROW BANK PHASE-LOCKED LOOP BEHAVIOR ON A WIDE BAND PHASE-LOCKED LOOP
PCT		WO 00/16492	PCT/US99/20792	A SINGLE-CHIP CMOS DIRECT-CONVERSION TRANSCEIVER
PCT		WO 96/002973	PCT/US94/07957	VITERBI ACS UNIT WITH RENORMALIZATION
PCT		WO 00/005834	PCT/US99/10464	CARRIER FREQUENCY ESTIMATOR FOR A SIGNAL RECEIVER
PCT		WO 93/022734	PCT/US93/00732	COMPUTER METHOD AND APPARATUS FOR A TABLE DRIVEN FILE INTERFACE
PCT		WO 02/03201	PCT/US01/19280	METHOD AND APPARATUS FOR GRAPHICAL DEVICE MANAGEMENT USING A VIRTUAL CONSOLE
PCT		WO 01/93155	PCT/US01/16135	REMOTELY MANAGING AND CONTROLLING A CONSUMER APPLIANCE
PCT		WO 02/47162	PCT/US01/49898	MICROELECTRONIC PACKAGE HAVING AN INTEGRATED HEAT SINK AND BUILD-UP LAYERS
PCT		WO 02/43342	PCT/US01/43615	LINK-LOCK DEVICE AND METHOD OF MONITORING AND CONTROLLING A LINK FOR FAILURES AND INTRUSIONS
PCT		WO 01/67728	PCT/US01/02323	CALL PROCESSING SYSTEM WITH RESOURCES ON MULTIPLE PLATFORM
PCT		WO 02/080182	PCT/US02/08751	METHOD, APPARATUS, AND SYSTEM TO ENHANCE NEGATIVE VOLTAGE SWITCHING
PCT		WO 99/037076	PCT/US99/01202	SYSTEM AND METHOD FOR AUTOMATIC PBX DETECTION
PH	1-1999-00064	1048108	1-1999-00064	A VARIABLE DELAY CELL WITH A SELF-BIASING LOAD
RU	2272308		2004114867	AN INTEGRATED OPTICAL CIRCUIT HAVING AN INTEGRATED ARRAYED WAVEGUIDE GRATING (AWG) AND OPTICAL AMPLIFIER(S)
RU	2172525	23,2001	98108548	VARIABLE STAGE CHARGE PUMP
SG	95907556		9203649.0	COMPOSITE POLISHING PAD FOR SEMICONDUCTOR PROCESS
SG	96977		200302974-1	VIA-IN-PAD WITH OFF-CENTER GEOMETRY AND METHODS OF MANUFACTURE
SG	101681		200307522-3	MATERIAL DEPOSITION FROM A LIQUEFIED GAS SOLUTION
SG	104206		200402809-8	LOW VOLTAGE OPERATION OF STATIC RANDOM ACCESS MEMORY
SG	103418		200400973-4	VARIABLE LEVEL MEMORY
SG	105264		200403602-6	DIGITAL FRAME DETERMINATION METHOD AND APPARATUS
SG	103034		200401398-3	PROBABILISTIC NETWORKS FOR DETECTING SIGNAL CONTENT
SG	117627		200406094-3	ESTABLISHING AN AD HOC NETWORK
SG	63591		9605497-8	METHOD AND APPARATUS FOR PROGRAMMING AND ERASING FLASH EEPROM MEMORY ARRAYS UTILIZING A CHARGE PUMP CIRCUIT
SG			200504905-1	SYSTEM AND METHOD OF EFFICIENTLY MODULATING DATA USING SYMBOLS HAVING MORE THAN ONE PULSE
SG	41086		9702174-5	PORTABLE DISK DRIVE CARRIER AND CHASSIS
SG	39320		9701544-0	METHOD AND APPARATUS FOR DETECTING AND SELECTING VOLTAGE SUPPLIES FOR FLASH MEMORY
SG	49445		9800988-9	VARIABLE STAGE CHARGE PUMP
SG	45876		9704852-4	METHOD TO PREVENT INTRUSIONS INTO ELECTRONIC CIRCUITRY
SG	45806		9704782-3	PACKAGE HOUSING MULTIPLE SEMICONDUCTOR DIES

Exhibit C

SG	61079		9806364-7	METHOD AND APPARATUS FOR PROVIDING IMPROVED DIAGNOSTIC FUNCTIONS INA COMPUTER SYSTEM
SG	65368		9902175-0	METHOD AND APPARATUS FOR DOCKING AND UNDOCKING A NOTEBOOK COMPUTER
SG	66110	200203A	9902870-6	METHOD AND APPARATUS FOR BIT CELL GROUND CHOKING FOR IMPROVED MEMORY WRITE MARGIN
SG	64145		9900858-3	INTEGRATED CIRCUIT PACKAGE
SG	89071		200202938-7	IMPROVED FLOURINE DOPED SIO2 FILM AND METHOD OF FABRICATION
SG	84929	1180267	200107090-3	ANTENNA INTERFACE
SG	67712		9904271.5	EMULATING NARROW BANK PHASE-LOCKED LOOP BEHAVIOR ON A WIDE BAND PHASE-LOCKED LOOP
SG	200207831-9		200207831-9	INDUCTIVE CHARGE PUMP CIRCUIT FOR PROVIDING VOLTAGES USEFUL FOR FLASH MEMORY AND OTHER APPLICATIONS
SG	97371		200303042-6	MICROELECTRONIC PACKAGE HAVING AN INTEGRATED HEAT SINK AND BUILD-UP LAYERS
SG	74026		9703726-1	APPARATUS AND METHOD FOR SIMULATING SPECULAR REFLECTION IN A COMPUTER GRAPHICS/IMAGING SYSTEM
SG	95375		200301211-9	DEGENERATIVE LOAD TEMPERATURE CORRECTION FOR CHARGE PUMPS
TH		55989	70821	VIA-IN-PAD WITH OFF-CENTER GEOMETRY AND METHODS OF MANUFACTURE
TH			77522	ELECTRONIC ASSEMBLY WITH FILLED NO-FLOW UNDERFILL AND METHODS OF MANUFACTURE
TH		52607	70155	MICROELECTRONIC PACKAGE HAVING AN INTEGRATED HEAT SINK AND BUILD-UP LAYERS
TW	65102		81102503	IMPROVED COMPOSITE POLISHING PAD FOR SEMICONDUCTOR PROCESS
TW	I241355		91138032	MATERIAL DEPOSITION FROM A LIQUEFIED GAS SOLUTION
TW	NI-180769	541797	091105913	DIGITAL LEAKAGE COMPENSATION CIRCUIT
TW	I235909		91104263	APPARATUS AND CIRCUIT HAVING REDUCED LEAKAGE CURRENT AND METHOD THEREFOR
TW	I 277100		091132888	LOW VOLTAGE OPERATION OF STATIC RANDOM ACCESS MEMORY
TW	203147	589566	91100508	ENABLING MANUAL ADJUSTMENT OF POINTING DEVICE CURSOR SPEED
TW	NI-187516	556120	091104602	TWO-DIMENSIONAL PYRAMID FILTER ARCHITECTURE
TW	I268511		91119529	VARIABLE LEVEL MEMORY
TW	I 266510			DIGITAL FRAME DETERMINATION METHOD AND APPARATUS
TW			091121741	PROBABILISTIC NETWORKS FOR DETECTING SIGNAL CONTENT
TW			92105182	INTEGRATED OPTOELECTRICAL CIRCUIT PACKAGE WITH OPTICAL WAVEGUIDE INTERCONNECTS
TW	196797	200301577	91136074	FILM BULK ACOUSTIC RESONATOR STRUCTURE AND METHOD OF MAKING
TW		200608188	94122531	SYSTEM AND METHOD TO DETECT ERRORS AND PREDICT POTENTIAL FAILURES
TW			92108929	METHOD FOR MEDIA CONTENT PRESENTATION IN CONSIDERATION OF SYSTEM POWER

Exhibit C

TW		200303670	92103629	INVERSE MULTIPLEXING OF MANAGED TRAFFIC FLOWS OVER A MULTI-STAR NETWORK
TW		200305989	092103764	ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT HAVING A RING OSCILLATOR TIMER CIRCUIT
TW			93127272	ADAPTIVE EQUALIZATION USING A CONDITIONAL UPDATE SIGN-SIGN LEAST MEAN SQUARE ALGORITHM
TW		200425439	93103221	THERMALLY ENHANCED ELECTRONIC FLIP-CHIP PACKAGING WITH EXTERNAL-CONNECTOR-SIDE DIE AND METHOD
TW	I 244854	200501726	93115087	TECHNIQUES TO PERFORM LINE QUALIFICATION
TW			93110830	STROBE THROUGH DIFFERENTIAL SIGNALING
TW	I 245503	200428801	93115086	TECHNIQUES TO TEST SIGNAL PROPAGATION MEDIA
TW			93132733	ANNOTATING MEDIA CONTENT WITH USER-SPECIFIED INFORMATION
TW		200618253	94125491	METHODS AND APPARATUSES FOR PROVIDING STACKED-DIE DEVICES
TW		200637275	94144718	CASCADED CONNECTION MATRICES IN A DISTRIBUTED CROSS-CONNECTION SYSTEM
TW		200635267	94144719	REMOTE STATUS FORWARDING OPERATING IN A DISTRIBUTED CROSS-CONNECTION SYSTEM
TW		200704036	94147137	TECHNIQUES FOR TRANSMITTING AND RECEIVING TRAFFIC OVER ADVANCED SWITCHING COMPATIBLE SWITCH FABRICS
TW		200629556	94137898	RESONANT TUNNELING TRANSISTOR USING CONVENTIONAL MOSFET PROCESSING
TW	107586		85102352	IC SOCKET AND METHOD OF CHECKING CONNECTED STATE BETWEEN IC SOCKET AND PRINTED WIRING BOARD
TW			95146490	METHOD AND APPARATUS FOR DISPLAYING ROTATED IMAGES
TW			95144673	LOW DELAY AND SMALL MEMORY FOOTPRINT PICTURE BUFFERING
TW	NI 147686	471144	84114065	A METHOD TO PREVENT INTRUSIONS INTO ELECTRONIC CIRCUITRY
TW	93868		86101070	MULTI-LAYERED CONTACTING FOR SECURING INTEGRATED CIRCUITS
TW	105201		86115173	METHOD AND APPARATUS FOR DOCKING AND UNDOCKING A NOTEBOOK COMPUTER
TW	101313		86119800	A METHOD AND APPARATUS FOR BIT CELL GROUND CHOKING FOR IMPROVED MEMORY WRITE MARGIN
TW	NI-138833	451121	87106806	CIRCUIT AND METHOD FOR CONTROLLING POWER AND PERFORMANCE BASED ON OPERATING ENVIRONMENT
TW	NI-132638	437158	88100466	VARIABLE DELAY CELL WITH A SELF-BIASING LOAD
TW	NI-137397	448693	88107420	METHOD AND APPARATUS FOR INCREASING VIDEO FRAME RATE
TW	NI-162716	502541	089125882	METHOD AND APPARATUS FOR PERFORMING VIDEO IMAGE DECODING
TW	NI-172931	522339	090103910	METHOD AND APPARATUS FOR WRITING UOPS INTO A BUFFER QUEUE INCLUDING OVERWRITING ENTRIES THAT ARE INDICATED TO CONTAIN INVALID UOPS
TW	I226100	I226100	089124269	IMPROVED FLOURINE DOPED SIO2 FILM AND METHOD OF FABRICATION
TW	147310	466839	89109929	ANTENNA INTERFACE
TW	138262	444439	88115667	A SINGLE-CHIP CMOS DIRECT-CONVERSION TRANSCEIVER

Exhibit C

TW			90112533	INDUCTIVE CHARGE PUMP CIRCUIT FOR PROVIDING VOLTAGES USEFUL FOR FLASH MEMORY AND OTHER
TW	I242733	I242733	90113072	REMOTELY MANAGING AND CONTROLLING A CONSUMER APPLIANCE
TW	NI - 189923		090128857	LINK-LOCK DEVICE AND METHOD OF MONITORING AND CONTROLLING A LINK FOR FAILURES AND INTRUSIONS
TW	096578	338141	86109133	APPARATUS AND METHOD FOR SIMULATING SPECULAR REFLECTION IN A COMPUTER GRAPHICS/IMAGING SYSTEM
TW	NI-179952	538574	090123932	DEGENERATIVE LOAD TEMPERATURE CORRECTION FOR CHARGE PUMPS
TW	NI-199496	583684	091104064	METHOD, APPARATUS, AND SYSTEM TO ENHANCE NEGATIVE VOLTAGE SWITCHING
US	7,208,348	US-2005-0090040-A1	10/994,995	VIA-IN-PAD WITH OFF-CENTER GEOMETRY AND METHODS OF MANUFACTURE