PATENT ASSIGNMENT

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
SemiSouth Laboratories, Inc.	08/08/2011

RECEIVING PARTY DATA

Name:	SS SC IP, LLC
Street Address:	1401 Livingston Lane
City:	Jackson
State/Country:	MISSISSIPPI
Postal Code:	39213

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	13463031

CORRESPONDENCE DATA

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CH $40.00 13463031

ATTORNEY DOCKET NUMBER:	17388/83703
NAME OF SUBMITTER:	Christopher W. Raimund

Total Attachments: 5
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ASSIGNMENT OF PATENTS AND PATENT APPLICATIONS

THIS ASSIGNMENT OF PATENTS AND PATENT APPLICATIONS is entered into and shall be effective as of the 19th day of July, 2011, by and between SemiSouth Laboratories, Inc., a Mississippi corporaton (the "Assignor") and SS SC IP, LLC, a Mississippi limited liability company (the "Assignee").

FOR GOOD AND VALUABLE CONSIDERATION, the receipt of which is hereby expressly acknowledged, Assignor does hereby assign and transfer unto Assignee the Assignor's entire right, title and interest, for all countries in and to certain issued patents and patent applications, as listed on the attached *Exhibit A*, together with all invention(s) and improvement(s) set forth therein, any and all continuations, continuations-in-part, divisionals, and renewals of and substitutes for said applications and their equivalents in U.S. and/or foreign jurisdictions, all applications claiming priority to or the benefit of said applications, including patent applications filed in U.S. and/or foreign jurisdictions or under any international convention, and all the rights and privileges under any and all Patent that may be granted therefore in any country, and any reissues, or reexaminations, or extensions of patent granted from any of the above and their equivalents in any jurisdiction. Assignor requests that any and all patents issuing from said applications be issued to said Assignee, its successors, assigns and legal representatives, or to such nominees as it may designate.

Assignor agrees that, when requested, it will, without charge to said Assignee but at its expense, sign all papers, take all rightful oaths, and do all acts which may be necessary, desirable or convenient for securing and maintaining patents for said inventions in any and all countries and for vesting title thereto in said Assignee, its successors, assigns and legal representatives or nominees.

Assignor authorizes and empowers said Assignee, its successors, assigns and legal representatives or nominees, to invoke and claim for any application for patent or other form of protection for said inventions filed by it or them, the benefit of the right of priority provided by the International Convention for the Protection of Industrial Property, as amended, or by any convention which may henceforth be substituted for it, and to invoke and claim such right of priority without further written or oral authorization from Assignor.

Assignor hereby consents that a copy of this assignment shall be deemed a full legal and formal equivalent of any assignment, consent to file or like document which may be required in any country for any purpose and more particularly in proof of the right of said Assignee or nominee to claim the aforesaid benefit of the right of priority provided by the International Convention for the Protection of Industrial Property, as amended, or by any convention which may henceforth be substituted for it.

IN WITNESS WHEREOF, I have hereunto set my hand effective as of the date set forth above.

SEMISOUTH LABORATORIES, INC.

By: Robert Maddox

Its: Chief Financial Officer

8/8/2011

STATE OF Mississippi)
) SS
COUNTY OF Oktibbeha)

I, the undersigned, a notary public in and for said county in said state, hereby certify that Robert Maddox, whose name individually and as Chief Financial Officer of SemiSouth Laboratories, Inc., a Mississippi corporation, is signed to the foregoing instrument, and who is known to me, acknowledged before me on this day that, being informed of the contents of such instrument, he, individually and in his capacity as Chief Financial Officer, executed the same voluntarily on the day the same bears date.

Given under my hand and official seal this 8th day of August, 2011.

Alexis P. Nordin
NOTARY PUBLIC

My Commission Expires: 1/3/2015

[NOTARIAL SEAL]

STATE OF MISSISSIPPI NOTARY PUBLIC ID # 97940 ALEXIS P. NORDIN Commission Expires Jan. 3, 2015 OKTIBBEHA COUNTY

7/2656527.2

EXHIBIT A

U.S. Patent No.	Title
6,815,304	SILICON CARBIDE BIPOLAR JUNCTION TRANSISTOR WITH OVERGROWN BASE REGION
6,693,308	POWER SIC DEVICES HAVING RAISED GUARD RINGS
7,119,380	LATERAL TRENCH FIELD-EFFECT TRANSISTORS IN WIDE BANDGAP SEMICONDUCTOR MATERIALS, METHODS OF MAKING, AND INTEGRATED CIRCUITS INCORPORATING THE TRANSISTORS
7,242,040	LATERAL TRENCH FIELD-EFFECT TRANSISTORS IN WIDE BANDGAP SEMICONDUCTOR MATERIALS, METHODS OF MAKING, AND INTEGRATED CIRCUITS INCORPORATING THE TRANSISTORS
7,202,528	NORMALLY-OFF INTEGRATED JFET POWER SWITCHES IN WIDE BANDGAP SEMICONDUCTORS AND METHODS OF MAKING
7,556,994	NORMALLY-OFF INTEGRATED JFET POWER SWITCHES IN WIDE BANDGAP SEMICONDUCTORS AND METHODS OF MAKING
7,820,511	NORMALLY-OFF INTEGRATED JFET POWER SWITCHES IN WIDE BANDGAP SEMICONDUCTORS AND METHODS OF MAKING
7,470,967	SELF-ALIGNED SILICON CARBIDE SEMICONDUCTOR DEVICES AND METHODS OF MAKING THE SAME
7,510,921	SELF-ALIGNED SILICON CARBIDE SEMICONDUCTOR DEVICES AND METHODS OF MAKING THE SAME
7,294,860	MONOLITHIC VERTICAL JUNCTION FIELD EFFECT TRANSISTOR AND SCHOTTKY BARRIER DIODE FABRICATED FROM SILICON CARBIDE AND METHOD FOR FABRICATING THE SAME
7,416,929	MONOLITHIC VERTICAL JUNCTION FIELD EFFECT TRANSISTOR AND SCHOTTKY BARRIER DIODE FABRICATED FROM SILICON CARBIDE AND METHOD FOR FABRICATING THE SAME
7,638,379	VERTICAL-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS HAVING BURIED GATES AND METHODS OF MAKING
7,314,799	SELF-ALIGNED TRENCH FIELD EFFECT TRANSISTORS WITH REGROWN GATES AND BIPOLAR JUNCTION TRANSISTORS WITH REGROWN BASE CONTACT REGIONS AND METHODS OF MAKING
7,274,083	SEMICONDUCTOR DEVICE WITH SURGE CURRENT PROTECTION AND METHOD OF MAKING THE SAME
7,960,198	METHOD OF MAKING A SEMICONDUCTOR DEVICE WITH SURGE CURRENT PROTECTION
7,602,228	HALF-BRIDGE CIRCUITS EMPLOYING NORMALLY ON SWITCHES AND METHODS OF PREVENTING UNINTENDED CURRENT FLOW THEREIN
7,907,001	HALF-BRIDGE CIRCUITS EMPLOYING NORMALLY ON SWITCHES AND METHODS OF PREVENTING UNINTENDED CURRENT FLOW THEREIN
7,560,325	METHODS OF MAKING LATERAL JUNCTION FIELD EFFECT TRANSISTORS USING SELECTIVE EPITAXIAL GROWTH
7,821,015	SILICON CARBIDE AND RELATED WIDE-BANDGAP TRANSISTORS ON SEMI-INSULATING EPITAXY
U.S. Patent App. No.	
12/826,033	NORMALLY-OFF INTEGRATED JFET POWER SWITCHES IN WIDE BANDGAP SEMICONDUCTORS AND METHODS OF MAKING SAME
11/198,298	VERTICAL-CHANNEL JUNCTION FIELD-EFFECT TRANSISTORS HAVING BURIED GATES AND METHODS OF MAKING

11/934,805	SELF-ALIGNED TRENCH FIELD EFFECT TRANSISTORS WITH REGROWN GATES AND BIPOLAR JUNCTION TRANSISTORS WITH REGROWN BASE CONTACT REGIONS AND METHODS OF MAKING
11/836,994	VERTICAL JUNCTION FIELD EFFECT TRANSISTOR WITH MESA TERMINATION AND METHOD OF MAKING THE SAME
12/146,580	JUNCTION BARRIER SCHOTTKY RECTIFIERS HAVING EPITAXIALLY GROWN P+-N JUNCTIONS AND METHODS OF MAKING
13/021,132	HALF-BRIDGE CIRCUITS EMPLOYING NORMALLY ON SWITCHES AND METHODS OF PREVENTING UNINTENDED CURRENT FLOW THEREIN
12/055,725	EPITAXIAL GROWTH ON LOW DEGREE OFF-AXIS SIC SUBSTRATES AND SEMICONDUCTOR DEVICES MADE THEREBY
12/117,121	SEMICONDUCTOR DEVICES WITH NON-PUNCH-THROUGH SEMICONDUCTOR CHANNELS HAVING ENHANCED CONDUCTION AND METHODS OF MAKING
13/108,505	SEMICONDUCTOR DEVICES WITH NON-PUNCH-THROUGH SEMICONDUCTOR CHANNELS HAVING ENHANCED CONDUCTION AND METHODS OF MAKING
12/170,599	SEMICONDUCTOR DEVICES WITH NON-PUNCH-THROUGH SEMICONDUCTOR CHANNELS HAVING ENHANCED CONDUCTION AND METHODS OF MAKING
12/818,281	METHODS OF MAKING VERTICAL JUNCTION FIELD-EFFECT TRANSISTORS AND BIPOLAR JUNCTION TRANSISTORS WITHOUT ION-IMPLANTATION AND DEVICES MADE THEREWITH
12/818,232	VERTICAL CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR WITH GRADED (BURIED OR NON-BURIED) P-N JUNCTION GATE
12/962,823	METHODS OF MAKING SEMICONDUCTOR DEVICES HAVING IMPLANTED SIDEWALLS AND DEVICES MADE THEREBY
12/613,065	VERTICAL JUNCTION FIELD EFFECT TRANSISTORS HAVING SLOPED SIDEWALLS AND METHODS OF MAKING
12/896,130	VERTICAL JUNCTION FIELD EFFECT TRANSISTORS HAVING SLOPED SIDEWALLS AND METHODS OF MAKING
12/881,771	SILICON CARBIDE AND RELATED WIDE-BANDGAP TRANSISTORS ON SEMI-INSULATING EPITAXY
11/764,606	OPTICALLY CONTROLLED SILICON CARBIDE AND RELATED WIDE-BANDGAP TRANSISTORS AND THYRISTORS
12/437,173	HIGH TEMPERATURE GATE DRIVERS FOR WIDE BANDGAP SEMICONDUCTOR POWER JFETS AND INTEGRATED CIRCUITS INCLUDING THE SAME
13/105,543	HIGH TEMPERATURE GATE DRIVERS FOR WIDE BANDGAP SEMICONDUCTOR POWER JFETS AND INTEGRATED CIRCUITS INCLUDING THE SAME
12/777,961	GATE DRIVER FOR ENHANCEMENT-MODE AND DEPLETION-MODE WIDE BANDGAP SEMICONDUCTOR JFETS
61/347,928	SELF-ALIGNED STRUCTURE AND PROCESS FOR IMPROVED POWER SEMICONDUCTOR DEVICE – EXPIRED -
13/112,075	SELF-ALIGNED STRUCTURE AND PROCESS FOR IMPROVED POWER SEMICONDUCTOR DEVICE
13/085,648	CASCODE SWITCHES INCLUDING NORMALLY-OFF AND NORMALLY-ON DEVICES AND CIRCUITS COMPRISING THE SWITCHES
61/476,534	VERTICAL JUNCTION FIELD EFFECT TRANSISTORS WITH IMPROVED THERMAL CHARACTERISTICS AND METHODS OF MAKING
PCT App No.	
PCT/US09/50021	SEMICONDUCTOR DEVICES WITH NON-PUNCH-THROUGH SEMICONDUCTOR CHANNELS HAVING ENHANCED CONDUCTION AND METHODS OF MAKING
PCT/US10/39114	METHODS OF MAKING VERTICAL JUNCTION FIELD-EFFECT TRANSISTORS AND BIPOLAR JUNCTION TRANSISTORS WITHOUT ION-IMPLANTATION AND DEVICES MADE THEREWITH
PCT/US10/39106	VERTICAL CHANNEL JUNCTION FIELD-EFFECT TRANSISTOR WITH GRADED (BURIED OR NON-BURIED) P-N JUNCTION GATE

PCT/US2010/059374	METHODS OF MAKING SEMICONDUCTOR DEVICES HAVING IMPLANTED SIDEWALLS AND DEVICES MADE THEREBY
PCT/US09/63391	VERTICAL JUNCTION FIELD EFFECT TRANSISTORS HAVING SLOPED SIDEWALLS AND METHODS OF MAKING
PCT/US2010/033982	HIGH TEMPERATURE GATE DRIVERS FOR WIDE BANDGAP SEMICONDUCTOR POWER JFETS AND INTEGRATED CIRCUITS INCLUDING THE SAME
PCT/US10/34399	GATE DRIVER FOR ENHANCEMENT-MODE AND DEPLETION-MODE WIDE BANDGAP SEMICONDUCTOR JFETS
PCT/US2011/37275	SELF-ALIGNED SEMICONDUCTOR DEVICES WITH REDUCED GATE-SOURCE LEAKAGE UNDER REVERSE BIAS AND METHODS OF MAKING