PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Virage Logic Corporation	09/02/2010
VL C.V.	09/02/2010
ARC Cores Limited	09/02/2010
ARC International I.P., Inc.	09/02/2010
ARC International Intellectual Property, Inc.	09/02/2010
ARC International Limited, Formerly ARC International PLC ARC Cores Limited	09/02/2010
ARC International (UK) Limited	09/02/2010

RECEIVING PARTY DATA

Name:	Synopsys, Inc.
Street Address:	700 East Middlefield Road
City:	Mountain View
State/Country:	CALIFORNIA
Postal Code:	94043

PROPERTY NUMBERS Total: 2

Property Type	Number
Application Number:	13508537
PCT Number:	IB2009055014

CH $80.00 13508537

CORRESPONDENCE DATA

Fax Number: (650)938-5200
Phone: (650)335-7291
Email: dahn@fenwick.com
Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent via US Mail.
Correspondent Name: Dohyun Ahn
Address Line 1: Fenwick & West LLP
Address Line 2: 801 California Street
Address Line 4: Mountain View, CALIFORNIA 94041

ATTORNEY DOCKET NUMBER:	22524-19801
NAME OF SUBMITTER:	Dohyun Ahn

Total Attachments: 47
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VIRAGE LOGIC PATENT ASSIGNMENT

This Virage Logic Patent Assignment (the "Assignment") is made and entered into on September 2, 2010, effective prior to Virage Logic Corporation's conversion from a corporation to an LLC pursuant to the certificate of conversion filed on even date herewith with the Delaware secretary of state. This Assignment is made by and between those entities listed in the signature pages as assignors (collectively, the "Assignors") and Synopsys, Inc., a corporation organized and existing under the laws of the state of Delaware, USA ("Assignee").

RECITALS

WHEREAS, pursuant to that certain Agreement and Plan of Merger dated June 9, 2010 by and between Virage Logic Corporation ("VIRL") and Assignee, VIRL has assigned and/or agreed to assign to Assignee, all right, title and interest in and to the Transferred Patents (as defined below) effective as of the Closing Date;

WHEREAS, the Transferred Patents are currently owned by the Assignors, with different Assignors owning different patents and/or patent applications included in the Transferred Patents;

WHEREAS, all of the Assignors are owned or controlled by VIRL;

WHEREAS, the Assignors and Assignee desire to execute and record this Assignment, in order to effect and/or confirm the assignment of the Transferred Patents to Assignee.

NOW, THEREFORE, the parties hereby agree as follows:

1. Each Assignor does hereby sell, assign, and transfer to Assignee, for itself and its successors, transferees, and assignees, its entire worldwide legal right, title, and interest in and to (a) those patents and patent applications listed in Schedule 1 of this Assignment, (b) all patents and patent applications that claim priority to any of the foregoing, including all continuations, divisionals, reexaminations, reissues, extensions, and foreign counterparts of the foregoing; (c) all patents and patent applications from which any of the foregoing claims priority; (d) all patents that issue from any of the foregoing; and (e) the right to sue in its own name and to recover for past infringement of any applications or patents issuing therefrom together with all rights to recover damages for infringement of provisional rights (collectively, the "Transferred Patents").

2. Each Assignor agrees to execute all oaths, assignments, powers of attorney, applications, and other papers necessary or desirable to fully secure to Assignee the legal rights, titles and interests herein conveyed, when requested, and without further consideration, in order to carry out the intent of this Assignment.

3. Each Assignor grants the attorney of record the power to insert on this Assignment (including in Schedule 1) any further information identifying the Transferred Patents or Assignors that may be necessary or desirable in order to comply with the rules of the relevant patent office for recordation of this document. Without limiting the foregoing, the attorney of record is hereby granted the power to insert missing serial numbers, to correct typographical errors, to identify which Assignor is assigning which Transferred Patent, and to add to Schedule 1 any Transferred Patents that currently are not expressly listed on Schedule 1.

Duly Authorized Representative of ASSIGNOR

Date of Signature

9/2, 2010

Brian Sereda
Chief Financial Officer
Virage Logic Corporation
47100 Bayside Parkway
Fremont, CA 94538

State of California
County of Alameda

On September 2, 2010 before me, Victoria Gregorio personally appeared Brian J. Sereda personally known to me or proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

V. GREGORIO
COMM. # 1830922
NOTARY PUBLIC-CALIFORNIA
ALAMEDA COUNTY
MY COMM. EXP. JAN. 13, 2013

Notary

Notary Seal

Duly Authorized Representative of ASSIGNOR Date of Signature

VL C.V.
High Tech Campus 46
5656 AE, Eindhoven,
The Netherlands

By: ~~VIRAGE LOGIC~~ INTERNATIONAL, its Managing Partner
By: _____ 9/2, 2010
Brian Sereda
Chief Financial Officer

State of California
County of Alameda

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_____
Notary

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Date of Signature

9/2, 2010

Brian Sereda
Chief Financial Officer
ARC Cores Limited
Verulam Point, Station Way
St Albans, Herts AL15HE
United Kingdom

State of California
County of Alameda

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Date of Signature

9/2, 2010

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State of California
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WITNESS my hand and official seal.

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COMM.# 1830922
NOTARY PUBLIC-CALIFORNIA
ALAMEDA COUNTY
MY COMM. EXP. JAN. 13, 2013

Notary Seal

Notary

Duly Authorized Representative of ASSIGNOR

Date of Signature

9/2/2010

Brian Sereda
Chief Financial Officer
ARC International Limited, formerly ARC International PLC
ARC Cores Limited
Verulam Point, Station Way
St Albans, Herts AL15HE
United Kingdom

State of California
County of Alameda

On September 2, 2010 before me, Victoria Gregorio personally appeared Brian J. Sereda personally known to me or proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

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WITNESS my hand and official seal.

Notary Seal

V. GREGORIO
COMM. # 1830922
NOTARY PUBLIC-CALIFORNIA
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MY COMM. EXP. JAN. 13, 2013

Notary

Duly Authorized Representative of ASSIGNOR

Date of Signature

9/2, 2010

Brian Sereda
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United Kingdom

State of California
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NOTARY PUBLIC-CALIFORNIA
ALAMEDA COUNTY
MY COMM. EXP. JAN. 13, 2013

Notary

Notary Seal

VIRAGE LOGIC PATENT ASSIGNMENT SIGNATURE PAGE FOR ASSIGNEES

Duly Authorized Representative of ASSIGNEE

Date of Signature

Sept 2, 2010

Erika Varga McEnroe
Assistant Secretary
Synopsys, Inc., a Delaware corporation
700 East Middlefield Road
Mountain View, CA 94043

State of California
County of Santa clara

On September 2, 2010 before me Christina Kertes [NOTARY PUBLIC] personally appeared Erika Varga McEnroe [REPRESENTATIVE] personally known to me or proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that [he/she] executed the same in [his/her] authorized capacity, and that by [his/her] signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

Notary

Notary Seal

CHRISTINA DANIELLE KERTES
Commission # 1773762
Notary Public - California
Santa Clara County
My Comm. Expires Oct 16, 2011

List of Patents and Patent Applications

Rutan Ref No.	Serial No.	Patent No.	Issue Date	Country I	Assignee	VIRP#
0002P (P002)	09/810,817	6396760	5/28/2002	United States of America	Virage Logic Corporation	VIRP21
0003P	09/895,896	6519202	2/11/2003	United States of America	Virage Logic Corporation	VIRP29
0003PDV (P003D)	10/210,525	6646933	11/11/2003	United States of America	Virage Logic Corporation	VIRP29D
0005P (P005)	09/962,761	7127647	10/24/2006	United States of America	Virage Logic Corporation	VIRP31
0006P (P006)	10/083,241	7237154	6/26/2007	United States of America	Virage Logic Corporation	VIRP34
0008P (P008)	10/295,742	6788574	9/7/2004	United States of America	Virage Logic Corporation	VIRP36
0008PC (P008C)	10/897,185	7095076	8/22/2006	United States of America	Virage Logic Corporation	VIRP36C
0009P (P009)	10/226,380	6850446	2/1/2005	United States of America	Virage Logic Corporation	VIRP40

Rutan Ref No.	Serial No.	Patent No.	Issue Date	Country I	Assignee	VIRP#
0009PDV (P009D)	11/029,916	7184346	2/27/2007	United States of America	Virage Logic Corporation	VIRP40D
0010P (P010)	10/236,555	7149921	12/12/2006	United States of America	Virage Logic Corporation	VIRP41
0011P (P011)	10/236,248	7149924	12/12/2006	United States of America	Virage Logic Corporation	VIRP42
0012P (P012)	10/313,650	6842375	1/11/2005	United States of America	Virage Logic Corporation	VIRP59
0013P (P013)	10/313,199	7130213	10/31/2006	United States of America	Virage Logic Corporation	VIRP60
0013PDV (P013D)	11/590,695	7355914	4/8/2008	United States of America	Virage Logic Corporation	VIRP60D
0014P (P014)	10/313,075	6992938	1/31/2006	United States of America	Virage Logic Corporation	VIRP61
0015P (P015)	10/377,845	6853572	2/8/2005	United States of America	Virage Logic Corporation	VIRP62

Rutan Ref No.	Serial No.	Patent No.	Issue Date	Country I	Assignee	VIRP#
0016P (P016)	10/364,261	7002827	2/21/2006	United States of America	Virage Logic Corporation	VIRP63
0017P (P017)	08/795,580	6051031	4/18/2000	United States of America	Virage Logic Corporation	VIRP01
0019P (P019)	10/664,190	7290186	10/30/2007	United States of America	Virage Logic Corporation	VIRP68
0020P (P020)	10/684,793	7415640	8/19/2008	United States of America	Virage Logic Corporation	VIRP67
0021P (P021)	10/779,194	7219324	5/15/2007	United States of America	Virage Logic Corporation	VIRP71
0021PDV (P021D)	11/734,202	NA	NA	United States of America	Virage Logic Corporation	VIRP71D
0022P (P022)	10/856,520	7069522	6/27/2006	United States of America	Virage Logic Corporation	VIRP73
0022PDV (P022D)	11/401,806	7603634	10/13/2009	United States of America	Virage Logic Corporation	VIRP73D

Rutan Ref No.	Serial No.	Patent No.	Issue Date	Country I	Assignee	VIRP#
0023P (P023)	10/856,191	7149142	12/12/2006	United States of America	Virage Logic Corporation	VIRP78
0025P (P025)	11/147,790	7263016	8/28/2007	United States of America	Virage Logic Corporation	VIRP80
0026P (P026)	11/146,829	7139204	11/21/2006	United States of America	Virage Logic Corporation	VIRP79
0027P (P027)	11/077,654	7142452	11/28/2006	United States of America	Virage Logic Corporation	VIRP74
0028P (P028)	11/147,791	7298659	11/20/2007	United States of America	Virage Logic Corporation	VIRP75
0029P (P029)	11/147,928	7251186	7/31/2007	United States of America	Virage Logic Corporation	VIRP76
0031P (P031)	09/351,767	6838713	1/4/2005	United States of America	Virage Logic Corporation	VIRP56
0031PC (P031C)	10/956,689	7129562	10/31/2006	United States of America	Virage Logic Corporation	VIRP56C 1

Rutan Ref No.	Serial No.	Patent No.	Issue Date	Country I	Assignee	VIRP#
0032P (P032)	11/340,147	7616036	11/10/2009	United States of America	Virage Logic Corporation	VIRP86
0033P (P033)	11/499,829	7519888	4/14/2009	United States of America	Virage Logic Corporation	VIRP90
0034P (P034)	11/520,200	7653849	1/26/2010	United States of America	Virage Logic Corporation	VIRP91
0034PDV (P034D1)	11/520,344	NA	NA	United States of America	Virage Logic Corporation	VIRP91D 1
0034PDV2 (P034D2)	11/520,276	NA	NA	United States of America	Virage Logic Corporation	VIRP91D 2
0034PDV3 (P034D3)	11/520,480	NA	NA	United States of America	Virage Logic Corporation	VIRP91D 3
0035P (P035)	08/917,006	5923060	7/13/1999	United States of America	Virage Logic Corporation	VIRP48
0036P (P036)	08/933,552	6091090	7/18/2000	United States of America	Virage Logic Corporation	VIRP50

Rutan Ref No.	Serial No.	Patent No.	Issue Date	Country I	Assignee	VIRP#
0042P (P042)	09/588,804	6445065	9/3/2002	United States of America	Virage Logic Corporation	VIRP57
0043P (P043)	09/588,802	6617621	9/9/2003	United States of America	Virage Logic Corporation	VIRP58
0054P (P054)	08/557,474	5723883	3/3/1998	United States of America	Virage Logic Corporation	VIRP44
0054PDV (P054D)	08/853,875	5898194	4/27/1999	United States of America	Virage Logic Corporation	VIRP46
0054PX (P054X)	08/747,858	5923059	7/13/1999	United States of America	Virage Logic Corporation	VIRP45
0057P (P057)	11/657,228	NA	NA	United States of America	Virage Logic Corporation	VIRP93
0058P (P058)	11/520,282	NA	NA	United States of America	Virage Logic Corporation	VIRP95
0058PDV (P058D1)	11/520,530	NA	NA	United States of America	Virage Logic Corporation	VIRP95D 1

Rutan Ref No.	Serial No.	Patent No.	Issue Date	Country I	Assignee	VIRP#
0058PDV2 (P058D2	11/520,423	7590902	9/15/2009	United States of America	Virage Logic Corporation	VIRP95D2
0059P (P059)	11/510,035	7598726	10/6/2009	United States of America	Virage Logic Corporation	VIRP98
0060P (P060)	11/870,330	NA	NA	United States of America	Virage Logic Corporation	VIRP101
0061P (P061)	11/847,047	NA	NA	United States of America	Virage Logic Corporation	VIRP108
0062P	12/249,085	NA	NA	United States of America	Virage Logic Corporation	VIRP113
0063P	12/194,454	NA	NA	United States of America	Virage Logic Corporation	VIRP114
0064M	9418663	6862563	3/1/2005	United States of America	ARC Cores Limited	VIRP22
0065M	10371830	6985976	1/10/2006	United States of America	ARC Internati onal I.P., Inc.	VIRP133

Rutan Ref No.	Serial No.	Patent No.	Issue Date	Country I	Assignee	VIRP#
0066M	10371681	7320044	1/15/2008	United States of America	ARC Internati onal I.P., Inc.	VIRP134
0067M	10371829	7039772	5/2/2006	United States of America	ARC Internati onal I.P., Inc.	VIRP135
0068M	10425286	7130936	10/31/2006	United States of America	ARC Internati onal I.P., Inc.	VIRP136
0069M	10669542	7451447	11/11/2008	United States of America	ARC Internati onal IP, Inc.	VIRP137
0070M	10937726	7219315	5/15/2007	United States of America	ARC Internati onal (UK) Limited	VIRP142
0071M	11328926	7478350	1/13/2009	United States of America	ARC Internati onal (UK) Limited	VIRP143
0072M	9886701	6606734	8/12/2003	United States of America	ARC Internati onal (UK) Limited	VIRP144

Rutan Ref No.	Serial No.	Patent No.	Issue Date	Country I	Assignee	VIRP#
0073M	9801241	6988154	1/17/2006	United States of America	ARC Internati onal PLC	VIRP145
0074M	9523871	6560754	5/6/2003	United States of America	ARC Cores Limited	VIRP146
0074MDV	10420299	7171631	1/30/2007	United States of America	ARC Cores Limited	VIRP153
0076M	9808469	7051189	5/23/2006	United States of America	ARC Internati onal PLC	VIRP164
0077M	10125816	7010558	3/7/2006	United States of America	ARC Internati onal (UK) Limited	VIRP166
0078M	10165146	6718504	4/6/2004	United States of America	ARC Internati onal	VIRP167
0079M	10818735	7185260	2/27/2007	United States of America	ARC Internati onal	ARC.030 C1
0080M	9886300	6848074	1/25/2005	United States of America	ARC Internati onal (UK) Limited	VIRP169
0081M	10313548	7493470	2/17/2009	United States of America	ARC Internati onal	VIRP170

Rutan Ref No.	Serial No.	Patent No.	Issue Date	Country I	Assignee	VIRP#
0082M	10330632	7278137	10/2/2007	United States of America	ARC Internati onal PLC	VIRP174
0083M	10358495	7043682	5/9/2006	United States of America	ARC Internati onal PLC	VIRP171
0084M	11430478	7398458	7/8/2008	United States of America	ARC Internati onal PLC	VIRP174
0085M	10423745	7475000	1/6/2009	United States of America	ARC Internati onal PLC	VIRP177
0086M	9805423	7162713	1/9/2007	United States of America	ARC Internati onal I.P., Inc.	VIRP181
0087M	9808612	7133820	11/7/2006	United States of America	ARC Internati onal I.P., Inc.	VIRP182
0088M	8080156	6178547	1/23/2001	United States of America	ARC Internati onal Property Inc.	VIRP183
0089M	09/226777	6084820	7/4/2000	United States of America	Virage Logic Corporat ion	VIRP02
0090M	09/227501	6104663	8/15/2000	United States of America	Virage Logic Corporat ion	VIRP03

Rutan Ref No.	Serial No.	Patent No.	Issue Date	Country I	Assignee	VIRP#
0091M	09/347955	6091620	7/18/2000	United States of America	Virage Logic Corporation	VIRP04
0091MDE	00952143.6	60013295.1	8/25/2004	Germany	Virage Logic Corporation	VIRP04EP
0091MFR	00952143.6	1194930	8/25/2004	France	Virage Logic Corporation	VIRP04EP
0091MGB	00952143.6	1194930	8/25/2004	Great Britain/ UK	Virage Logic Corporation	VIRP04EP
0091MNL	00952143.6	1194930	8/25/2004	Netherlands	Virage Logic Corporation	VIRP04EP
0092M	09/347372	6084819	7/4/2000	United States of America	Virage Logic Corporation	VIRP05
0093M	09/439837	6269036	7/31/2001	United States of America	Virage Logic Corporation	VIRP06
0094M	09/528660	6310817	10/30/2001	United States of America	Virage Logic Corporation	VIRP09

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0095M	09/728377	6392957	5/21/2002	United States of America	Virage Logic Corporation	VIRP20
0096M	09/957098	6738279	5/18/2004	United States of America	Virage Logic Corporation	VIRP32
0097M	10/142523	6711067	3/23/2004	United States of America	Virage Logic Corporation	VIRP33
0098M	*09/408,137*	*6377194*	*4/23/2002*	United States of America	***Caltech licensed patent***	Caltech patents do not have any VIRP number

Virage Logic/ARC International Patent Matters

VIRL FILE NUMBER	ROPES & GRAY FILE NUMBER	PATENT NUMBER	SERIAL NUMBER	TITLE	INVENTORS	STATUS	FAMILY INFORMATION	ISSUE DATE	FILING DATE	EXPIRATION DATE
VIRP122	ARCU-001-101	6862563	9418663	Method and Apparatus for Managing the Configuration and Functionality of a Semi-Conductor Design	Edward Plowman, James Robert, Howard Hakewill, Mohammed Noshad Khan	Issued	UTILITY	1-Mar-05	14-Oct-99	14-Oct-19
VIRP123	ARCU-001-103		12639911	Method and Apparatus for Managing the Configuration and Functionality of a Semi-Conductor Design	Edward Plowman, James Robert, Howard Hakewill, Mohammed Noshad Khan	Pending	CON of ARCU-001-101 (issued), ARCU-001-102 (abandoned)		16-Dec-09	
VIRP124	ARCU-001-IL1	142342	142342	Method and Apparatus for Managing the Configuration and Functionality of a Semi-Conductor Design	James Hakewill, Mohammed Khan, Edward Plowman	Issued	FOREIGN COUNTERPART TO ARCU-001-101	19-Mar-06	14-Oct-99	14-Oct-19
VIRP125	ARCU-001-IN1	206703	INPCT2001420	Method and Apparatus for Managing the Configuration and Functionality of a Semi-Conductor Design	James Hakewill, Mohammed Khan, Edward Plowman	Issued	FOREIGN COUNTERPART TO ARCU-001-101	10-May-07	14-Oct-99	14-Oct-19
VIRP126	ARCU-015-101		11973173	Interprocessor Communication Method	Carl Norman Graham, Kar-Lik Wong, Simon Jones	Pending			5-Oct-07	
VIRP127	ARCU-015-GB1	2442609	7194798	Interprocessor Communication Method	Carl Norman Graham, Kar-Lik Wong, Simon Jones	Issued	FOREIGN COUNTERPART TO ARCU-015-101	11-Feb-09	5-Oct-07	5-Oct-27
VIRP128	ARCU-017-103		11132424	Microprocessor Architecture Having Extendible Logic	James Hakewill, Rich Fuhler	Pending			19-May-05	
VIRP129	ARCU-021-101		11528327	Systems and Methods for Performing Deblocking in Microprocessor-Based Video Codec Applications	Aris Aristodemou, Carl Norman Graham, Kar-Lik Wong, Simon Jones, Yazid Nemouchi	Notice of Allowance received			28-Sep-06	
VIRP130	ARCU-023-101		11528338	Systems and Methods for Recording Instruction Sequences in a Microprocessor Having a Dynamically Decoupleable Extended Instruction Pipeline	Aris Aristodemou, Carl Norman Graham, Kar-Lik Wong, Seow Chuan Lim, Simon Jones, Yazid Nemouchi	Pending			28-Sep-06	
VIRP131	ARCU-024-101		11528325	Systems and Methods for Accelerating Sub-Pixel Interpolation in Video Processing Applications	Aris Aristodemou, Carl Norman Graham, Kar-Lik Wong, Simon	Pending			28-Sep-06	
VIRP132	ARCU-025-101		11528432	Systolic-Array Based Systems and Methods for Performing Block Matching in Motion Compensation	Nigel Topham	Pending			28-Sep-06	

VIRL FILE NUMBER	ROPES & GRAY FILE NUMBER	PATENT NUMBER	SERIAL NUMBER	TITLE	INVENTORS	STATUS	FAMILY INFORMATION	ISSUE DATE	FILING DATE	EXPIRATION DATE
VIRP133	ARCU-031-101	6985976	10371830	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR MEMORY MANAGEMENT	Akash R. Deshpande, Marco Zandonadi, Roberto Attias	Issued		10-Jan-06	20-Feb-03	20-Feb-23
VIRP134	ARCU-033-101	7320044	10371681	SYSTEM, METHOD, AND COMPUTER PRODUCT FOR INTERRUPT SCHEDULING IN PROCESSING COMMUNICATION	Akash R. Deshpande, Marco Zandonadi, Roberto Attias	Issued		15-Jan-08	20-Feb-03	
VIRP135	ARCU-034-101	7039772	10371829	SYSTEM, METHOD, AND COMPUTER PROGRAM FOR PROCESSING REFLECTIVE STATE MACHINES	Akash R. Deshpande, Marco Zandonadi, Roberto Attias	Issued		2-May-06	20-Feb-03	
VIRP136	ARCU-038-101	7130936	10425286	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR SHARED MEMORY QUEUE	Akash R. Deshpande, Mandeep S. Baines, Shamit D. Kapadia	Issued		31-Oct-06	28-Apr-03	31-Oct-23
VIRP137	ARCU-039-102	7451447	10669542	METHOD, COMPUTER PROGRAM AND APPARATUS FOR OPERATING DYNAMIC EVENT MANAGEMENT AND TASK SCHEDULING USING FUNCTION CALLS	Akash R. Deshpande	Issued		11-Nov-08	23-Sep-03	7-Aug-19
VIRP138	ARCU-040-101		11607474	STRUCTURED BLOCK TRANSFER MODULE, SYSTEM ARCHITECTURE AND METHOD FOR TRANSFERRING	Akash Renukadas Deshpande, Bryon Irwin Moyer, Navendu Sinha, Roberto Attias, Shobhit Sonakiya, Stephen John Joseph Fricke, Vineet Gupta, William Charles Jordan	Pending			1-Dec-06	
VIRP139	ARCU-042-101		11607429	PACKET INGRESS/EGRESS BLOCK AND SYSTEM AND METHOD FOR RECEIVING, TRANSMITTING, AND MANAGING PACKETIZED DATA	Akash Renukadas Deshpande, Bryon Irwin Moyer, Navendu Sinha, Roberto Attias, Shobhit Sonakiya, Stephen John Joseph Fricke, Vineet Gupta, William	Pending			1-Dec-06	
VIRP140	ARCU-043-101		11607452	SYSTEM AND METHOD FOR GENERATING HARDWARE ACCELERATORS AND PROCESSOR OFFLOADS	Akash Renukadas Deshpande, Bryon Irwin Moyer, Navendu Sinha, Roberto Attias, Shobhit Sonakiya, Stephen John Joseph Fricke, Vineet Gupta, William Charles Jordan	Pending			1-Dec-06	
VIRP141	ARCU-047-102		10665875	Apparatus, Method and Computer Program for Dynamic Slip Control in Real-Time Scheduling	Akash R. Deshpande	Pending			19-Sep-03	

VIRL FILE NUMBER	ROPES & GRAY FILE NUMBER	PATENT NUMBER	SERIAL NUMBER	TITLE	INVENTORS	STATUS	FAMILY INFORMATION	ISSUE DATE	FILING DATE	EXPIRATION DATE
VIRP142	ARCU-051-101	7219315	10937726	Comparison of Semiconductor Circuitry Simulations	Robert Mark Murray, William Robert Stoye	Issued		15-May-07	9-Sep-04	9-Sep-24
VIRP143	ARCU-053-101	7478350	11328926	Methods for Simulating Hardware	Daryl Stewart, David J. Greaves	Issued		13-Jan-09	9-Jan-06	9-Jan-26
VIRP144	ARCU-054-101	6806734	9886701	Imperative Modelling and Cycle Semantic of almost Arbitrary Netlists	David J. Greaves	Issued		12-Aug-03	21-Jun-01	21-Jun-21
VIRP145	ARCU-058-101	6988154	9801241	MEMORY INTERFACE AND METHOD OF INTERFACING BETWEEN FUNCTIONAL	David Latta	Issued	UTILITY	17-Jan-06	7-Mar-01	7-Mar-21
VIRP146	ARCU-058-103		12143351	MEMORY INTERFACE AND METHOD OF INTERFACING BETWEEN FUNCTIONAL ENTITIES	David Latta	Pending	CON of ARCU-058-101 (issued), ARCU-058-102 (abandoned)		20-Jun-08	
VIRP147	ARCU-059-CN1	808460.2	8084602	Method and Apparatus for Jump Delay Slot Control in a Pipelined Processor	Carl Graham, Peter Warnes	Issued		30-Jun-04	12-May-00	12-May-20
VIRP148	ARCU-059-DE1	60005830.1-08	60005830108	Method and Apparatus for Jump Delay Slot Control in a Pipelined Processor	Carl Graham, Peter Warnes	Issued		8-Oct-03	12-May-00	
VIRP149	ARCU-059-EP1	1190305	9324146	Method and Apparatus for Jump Delay Slot Control in a Pipelined Processor	Carl Graham, Peter Warnes	Issued		8-Oct-03	12-May-00	
VIRP150	ARCU-059-GB1	1190305	9324146	Method and Apparatus for Jump Delay Slot Control in a Pipelined Processor	Carl Graham, Peter Warnes	Issued		8-Oct-03	12-May-00	
VIRP151	ARCU-059-TW1	169646	89109196	Method and Apparatus for Jump Delay Slot Control in a Pipelined Processor	Carl Graham, Peter Warnes	Issued		11-Dec-02	12-May-00	4-Jun-20
VIRP152	ARCU-060-101	6560754	9523871	Method and Apparatus for Jump Control in a Pipelined Processor	James Robert Howard Hakewill, John Sanders	Issued	UTILITY	6-May-03	13-Mar-00	13-Mar-20
VIRP153	ARCU-060-102	7171631	10420299	Method and Apparatus for Jump Control in a Pipelined Processor	James Robert Howard Hakewill, John Sanders	Issued	CON of ARCU-060-101	30-Jan-07	21-Apr-03	21-Apr-23
VIRP154	ARCU-060-CN1	CN 1197006C	8084599	Method and Apparatus for Jump Control in a Pipelined Processor	James Robert Howard Hakewill, Jon Sanders	Issued		15-Sep-04	12-May-00	11-May-20
VIRP155	ARCU-060-DE1	60007312.2-08	9289703	Method and Apparatus for Jump Control in a Pipelined Processor	James Robert Howard Hakewill, Jon Sanders	Issued		17-Dec-03	12-May-00	
VIRP156	ARCU-060-EP1	1190303	9289703	Method and Apparatus for Jump Control in a Pipelined Processor	James Robert Howard Hakewill, Jon Sanders	Issued		17-Dec-03	12-May-00	
VIRP157	ARCU-060-FR1	1190303	9289703	Method and Apparatus for Jump Control in a Pipelined Processor	James Robert Howard Hakewill, Jon Sanders	Issued		17-Dec-03	12-May-00	
VIRP158	ARCU-060-GB1	1190303	9289703	Method and Apparatus for Jump Control in a Pipelined Processor	James Robert Howard Hakewill, Jon Sanders	Issued		17-Dec-03	12-May-00	
VIRP159	ARCU-060-TW1	527563	89109197	Method and Apparatus for Jump Control in a Pipelined Processor	James Hakewill, Radlett Hertx	Issued		11-Apr-03	12-May-00	4-Jul-20
VIRP160	ARCU-061-CN1	CN 1217261C	8045560	Method and Apparatus for Jump Control in a Pipelined Processor	James Robert Howard Hakewill, John Sanders	Issued		31-Aug-05	12-May-00	11-May-20

VIRL FILE NUMBER	ROPES & GRAY FILE NUMBER	PATENT NUMBER	SERIAL NUMBER	TITLE	INVENTORS	STATUS	FAMILY INFORMATION	ISSUE DATE	FILING DATE	EXPIRATION DATE
VIRP161	ARCU-062-CN1	ZL00808462.9	80084629	Method and Apparatus for Loose Register Encoding within a Pipelined Processor	Carl Graham, Peter Warnes	Issued	UTILITY	20-Apr-05	12-May-00	11-May-20
VIRP162	ARCU-062-CN2	CN 100351782C	2.0051E+12	Method and Apparatus for Loose Register Encoding within a Pipelined Processor	Carl Graham, Peter Warnes	Issued	CON of ARCU-062-CN1	28-Nov-07	12-May-00	11-May-20
VIRP163	ARCU-062-TW1	482978	89109199	Method and Apparatus for Loose Register Encoding within a Pipelined Processor	Carl Graham, Peter Warnes	Issued		11-Apr-02	12-May-00	4-Jul-20
VIRP164	ARCU-063-101	7051189	9808469	Method and Apparatus for Processor Code Optimization Using Code Compression	Peter Warnes	Issued	UTILITY	23-May-06	14-Mar-01	14-Mar-21
VIRP165	ARCU-063-102		11438930	Method and Apparatus for Processor Code Optimization Using Code Compression	Peter Warnes	Pending	CON of ARCU-063-101		22-May-06	
VIRP166	ARCU-064-101	7010558	10125616	Data Processor with Enhanced Instruction Execution and Method	Chris Morris	Issued		7-Mar-06	18-Apr-02	
VIRP167	ARCU-065-101	6718504	10165146	Turbo QACS	Alexander Worm, Jonathan Talbot, Robert Coombs	Issued	UTILITY	6-Apr-04	5-Jun-02	
VIRP168	ARCU-065-102	7185260	10818735	Method and Apparatus for Implementing a Data Processor Adapted for Turbo Decoding	Alexander Worm, Jonathan Talbot, Robert Coombs	Issued	CON of ARCU-065-101	27-Feb-07	5-Apr-04	5-Jun-22
VIRP169	ARCU-066-101	6848074	9886300	Method and Apparatus for Implementing a Single Cycle Operation in a Data Processing System [QACS2]	Robert Anthony Coombs	Issued		25-Jan-05	21-Jun-01	21-Jun-21
VIRP170	ARCU-067-101	7493470	10313548	Processor Apparatus and Methods Optimized for Control Applications	Rene Cumplido, Roger Goodall, Simon Jones	Issued		17-Feb-09	6-Dec-02	6-Dec-22
VIRP171	ARCU-068-101	7278137	10330632	Methods and Apparatus for Compiling Instructions for a Data Processor	Michael Lee Jalkut, Peter Warnes, Richard A. Fuhler, Thomas J. Pennello	Issued	UTILITY	2-Oct-07	26-Dec-02	26-Dec-22
VIRP172	ARCU-068-102		11906519	Methods and Apparatus for Compiling Instructions for a Data Processor	Michael Lee Jalkut, Peter Warnes, Richard A. Fuhler, Thomas J. Pennello	Pending	CON of ARCU-068-101		1-Oct-07	
VIRP173	ARCU-071-KR1	10-0718754	20047011897	Configurable Data Processor With Multi-Length Instruction Set Architecture	Jonathan Ferguson, Mohammed Noshad Khan, Peter Warnes, Richard A. Fuhler, Robbie Temple, Simon Davidson	Issued		9-May-07	31-Jan-03	31-Jan-23
VIRP174	ARCU-072-101	7043682	10358495	METHOD AND APPARATUS FOR IMPLEMENTING DECODE OPERATIONS IN A DATA PROCESSOR	Jonathan Ferguson	Issued	UTILITY	9-May-06	4-Feb-03	4-Feb-23
VIRP175	ARCU-072-102	7398458	11430478	METHOD AND APPARATUS FOR IMPLEMENTING DECODE OPERATIONS IN A DATA PROCESSOR	Jonathan Ferguson	Issued	CON of ARCU-072-101	8-Jul-08	8-May-06	

VIRL FILE NUMBER	ROPES & GRAY FILE NUMBER	PATENT NUMBER	SERIAL NUMBER	TITLE	INVENTORS	STATUS	FAMILY INFORMATION	ISSUE DATE	FILING DATE	EXPIRATION DATE
VIRP176	ARCU-072-103		12143250	METHOD AND APPARATUS FOR IMPLEMENTING DECODE OPERATIONS IN A DATA PROCESSOR	Jonathan Ferguson	Pending	CON of ARCU-072-102		20-Jun-08	
VIRP177	ARCU-073-101	7475000	10423745	Apparatus and Method for Managing Integrated Circuit Designs	Benjamin Segust Wimpory, Lee Hewitt, Mark Bilton, Mark Farr, Simon Broadley, Stephen Anthony Cook, Tim Glover	Issued	UTILITY	6-Jan-09	25-Apr-03	
VIRP178	ARCU-073-GN1		38152231	Apparatus and Method for Managing Integrated Circuit Designs	Benjamin Segust Wimpory, Lee Hewitt, Mark Bilton, Mark Farr, Simon Broadley, Stephen	Pending	FOREIGN COUNTERPART TO		25-Apr-03	
VIRP179	ARCU-073-KR1	10-0818826	20047017409	Apparatus and Method for Managing Integrated Circuit Designs	Benjamin Segust Wimpory, Lee Hewitt, Mark Bilton, Mark Farr, Simon Broadley, Stephen	Issued		26-Mar-08	25-Apr-03	
VIRP180	ARCU-074-IN1		751KOLNP06	Improved Computerized Extension Apparatus And Methods	Chao Dong, Lee Hewitt, Mark Farr, Simon Broadley	Pending			27-Aug-04	
VIRP181	ARCU-077-101	7162713	9805423	Difference Engine Method and Apparatus	Thomas J. Pennello	Issued		9-Jan-07	13-Mar-01	13-Mar-21
VIRP182	ARCU-078-101	7133820	9808612	Method and Apparatus for Debugging Programs in a Distributed Environment	Henry A. Davis, Thomas J. Pennello	Issued		7-Nov-06	14-Mar-01	14-Mar-21
VIRP183	ARCU-079-101	6178547	8080156	Method and Apparatus for Generating Non-Redundant Symbolic Debug Information in Computer Programs	Tom Pennello	Issued		23-Jan-01	17-Jun-93	23-Jan-18
VIRP184	ARCU-081-101		12154783	ADAPTIVE VIDEO ENCODING APPARATUS AND METHODS	Aris Aristodemou, Carl Norman Graham, John R.M. Mason, Kar-Lik Wong, Seow Chuan Lim, Tim Hall, Yazid Nemouchi	Pending			27-May-08	
VIRP185	ARCU-081-EP1		PCTUS2008006705 EP TBA	ADAPTIVE VIDEO ENCODING APPARATUS AND METHODS	Aris Aristodemou	Pending			27-May-08	
					Carl Norman Graham					
					John R.M. Mason					
					Kar-Lik Wong					
					Seow Chuan Lim					
					Thomas J. Pennello					
					Tim Hall					
					Yazid Nemouchi					
VIRP186	ARCU-084-101		10516907	ACOUSTICAL VIRTUAL REALITY ENGINE AND ADVANCED TECHNIQUES FOR ENHANCING DELIVERED SOUND	James Barber	Pending			9-Aug-05	
					Thomas Paddock					
VIRP187	ARCU-084-AU1	2003251403	2003251403	ACOUSTICAL VIRTUAL REALITY ENGINE AND ADVANCED TECHNIQUES FOR ENHANCING DELIVERED SOUND	James Barber	Issued		28-May-09	5-Jun-03	5-Jun-23
					Thomas Paddock					

VIRL FILE NUMBER	ROPES & GRAY FILE NUMBER	PATENT NUMBER	SERIAL NUMBER	TITLE	INVENTORS	STATUS	FAMILY INFORMATION	ISSUE DATE	FILING DATE	EXPIRATION DATE
VIRP188	ARCU-084-CA1		2488689	ACOUSTICAL VIRTUAL REALITY ENGINE AND ADVANCED TECHNIQUES FOR ENHANCING DELIVERED SOUND	James Barber	Pending			5-Jun-03	
					Thomas Paddock					
VIRP189	ARCU-084-CN1	ZL03818449.4	38184494	ACOUSTICAL VIRTUAL REALITY ENGINE AND ADVANCED TECHNIQUES FOR ENHANCING DELIVERED SOUND	James Barber	Issued		22-Apr-09	5-Jun-03	5-Jun-23
					Thomas Paddock					
VIRP190	ARCU-084-EP1		37573615	ACOUSTICAL VIRTUAL REALITY ENGINE AND ADVANCED TECHNIQUES FOR ENHANCING DELIVERED SOUND	James Barber	Pending			5-Jun-03	
					Thomas Paddock					
VIRP191	ARCU-084-IN1		2752CHENP2004	ACOUSTICAL VIRTUAL REALITY ENGINE AND ADVANCED TECHNIQUES FOR ENHANCING DELIVERED SOUND	James Barber	Pending			5-Jun-03	
					Thomas Paddock					
VIRP192	ARCU-084-JP1		2004511932	ACOUSTICAL VIRTUAL REALITY ENGINE AND ADVANCED TECHNIQUES FOR ENHANCING DELIVERED SOUND	James Barber	Pending			5-Jun-03	
					Thomas Paddock					
VIRP193	ARCU-084-KR1		1020047019885	ACOUSTICAL VIRTUAL REALITY ENGINE AND ADVANCED TECHNIQUES FOR ENHANCING DELIVERED SOUND	James Barber	Pending			5-Jun-03	
					Thomas Paddock					
VIRP194	ARCU-084-TW1	I318531	092115246	ACOUSTICAL VIRTUAL REALITY ENGINE AND ADVANCED TECHNIQUES FOR ENHANCING DELIVERED SOUND	James Barber	Granted		11-Dec-09	5-Jun-03	
					Thomas Paddock					
VIRP195	ARCU-084-TW2		92134187	ACOUSTICAL VIRTUAL REALITY ENGINE AND ADVANCED TECHNIQUES FOR ENHANCING DELIVERED SOUND	James Barber	Pending	DIV of ARCU-084-TW1		4-Dec-03	
					Thomas Paddock					

Virage Logic Patent/Application Portfolio

CAM NUMBER / DOCKET NUMBER	VIRAGE REF.	ORIGINAL FILING?	NXP REF.	PAT TYPE	INVENTORS	APPL. NO.	FILED	TITLE	STATUS	EXPIRATION DATE	MAINTENANCE FEE DUE
802915-999022 / 12291-029-999	VIRP206	Yes		U.S. Utility	Niranjan Behera; Deepak Sabharwal; Yong Zhang	12/558,816	10/14/2009	SYSTEMS AND METHODS FOR REDUCING MEMORY ARRAY LEAKAGE IN HIGH CAPACITY MEMORIES BY SELECTIVE BIASING	Pending		
802915-999023 / 12291-030-999	VIRP306	Yes	81369458US01	U.S. Utility	Peter Struik	12/347,008	12/31/2008	DISTRIBUTED TABLE-DRIVEN POWER MODE COMPUTATION FOR CONTROLLING OPTIMAL CLOCK AND H32VOLTAGE SWITCHING	Pending		
802915-228023 / 12291-030-228	VIRP307	No		Patent Cooperation Treaty		PCT/US09/69829	12/30/2009		Pending		
802915-999026 / 12291-034-999	VIRP308	No	004923US1	U.S. Utility	Andy Negoi; Michael Zecri	12/299,305	4/24/2007	VERY LOW POWER ANALOG COMPENSATION CIRCUIT	Pending		
802915-146026 / 12291-034-146	VIRP308CN	No	004923CN1	China		200780025006.20	4/24/2007		Pending		Not due until grant
802915-227026 / 12291-034-227	VIRP308EP	No	004923EP2	Europe (EPO)		07728424.8 (Pub no. 2018704)	4/24/2007		Pending		4/30/2010
802915-012026 / 12291-034-012	VIRP308JP	No	004923JP1	Japan		2009-508312	4/24/2007		Pending		Not due until grant
802915-187026 / 12291-034-187	VIRP308SK	No	004923KR1	South Korea		2008-7029458	4/24/2007		Pending		Not due until grant
802915-055026 / 12291-034-055	VIRP308SG	No	0049235G1	Singapore		200808099-6	4/24/2007		Pending		Not due until grant
802915-185026 / 12291-034-185	VIRP308TW	No	004923TW1	Taiwan		096113022 (Pub no. 200810355)	4/24/2007		Pending		Not due until grant
802915-228026 / 12291-034-228		Yes (claiming priority to an unpublished expired original European filing now abandoned)	004923WO1	Patent Cooperation Treaty		PCT/EP2007/053968	4/24/2007		Abandoned		
802915-999025 / 12291-032-999	VIRP309	No	005850US1	U.S. Utility	Andy Negoi	12/299,726	5/2/2007	ELECTRONIC CIRCUIT AND METHOD THEREFOR	Pending		
802915-146025 / 12291-032-146	VIRP309CN	No	005850CN1	China		200780025263.6 (pub no. 101485089-A	5/2/2007		Pending		Not due until grant
802915-227025 / 12291-032-227	VIRP309EP	No	005850EP2	Europe (EPO)		07735730.9	5/2/2007		Pending		5/31/2010

CAM NUMBER / DOCKET NUMBER	VIRAGE REF.	ORIGINAL FILING?	NXP REF.	PAT TYPE	INVENTORS	APPL. NO.	FILED	TITLE	STATUS	EXPIRATION DATE	MAINTENANCE FEE DUE
802915-012025 / 12291-032-012	VIRP309JP	No	005850JP1	Japan		2009-508604	5/2/2007		Pending		Not due until grant
12291-032-228	VIRP309	Yes (claiming priority to an unpublished expired orignal European filing now abandoned)	005850WO1	Patent Cooperation Treaty		PCT/IB2007/051630 (pub no. 2007/129259)	5/2/2007		Abandoned		
802915-999027 / 12291-033-999	VIRP310	No	004842US1	U.S. Utility	Calin Ciordas; Kees G.W. Goossens; Andrei Radulescu	12/307,411	7/3/2007	ELECTRONIC DEVICE, SYSTEM ON CHIP AND METHOD FOR MONITORING DATA FLOW	Pending		
802915-146027 / 12291-033-146	VIRP310CN	No	004842CN1	China		200780025493.2 (pub no. 101484880-A)	7/3/2007		Pending		Not due until grant
802915-227027 / 12291-033-227	VIRP310EP	No	004842EP2	Europe (EPO)		07789875.7 (pub no. 2041661-A)	7/3/2007		Pending		7/31/2010
802915-012027 / 12291-033-012	VIRP310JP1	No	004842JP1	Japan		2009-517582	7/3/2007		Pending		Not due until grant
802915-228027 / 12291-033-228		Yes (claiming priority to an unpublished expired orignal European filing now abandoned)	004842WO1	Patent Cooperation Treaty		PCT/IB2007/052595 (pub no. 2008/004188)	7/3/2007		Abandoned		
802915-999024 / 12291-031-999	VIRP311	No	007342US1	U.S. Utility	Dharmaray M. Nedalgi	12/532,201	3/26/2008	ELECTRONIC DEVICE WITH A HIGH VOLTAGE TOLERANT UNIT	Pending		
802915-146024 / 12291-031-146	VIRP311CN	No	007342CN1	China		200880009746	3/26/2008		Pending		Not due until grant
802915-227024 / 12291-031-227	VIRP311EP	No	007342EP2	Europe (EPO)		08719837.0	3/26/2008		Pending		3/31/2011
802915-228024 / 12291-031-228		Yes (claiming priority to an unpublished expired orignal European filing now abandoned)	007342WO1	Patent Cooperation Treaty		PCT/IB2008/051123	3/26/2008		Abandoned		

CAM NUMBER / DOCKET NUMBER	VIRAGE REF.	ORIGINAL FILING?	NXP REF.	PAT TYPE	INVENTORS	APPL. NO.	FILED	TITLE	STATUS	EXPIRATION DATE	MAINTENANCE FEE DUE
802915-228025 / 12291-035-228	VIRP312	Yes (claiming priority to an unpublished expired orignal European filing now abandoned)	007882WO02	Patent Cooperation Treaty	Jan Stuyt; De Ruyter	PCT/IB2008/053194 (Pub no. WO2009/022276)	8/8/2008	VERIFICATION OF DESIGN INFORMATION FOR CONTROLLING MANUFACTURE OF A SYSTEM ON A CHIP	Pending		
802915-999035 / 12291-035-999	VIRP313	No	007882US	Utility		12/673445	8/8/2008		Pending		
802915-146035 / 12291-035-146	VIRP313CN	No	007882CN1	China			8/8/2008		Pending		Not due until grant
802915-228036 / 12291-036-228	VIRP314	No	008211WO1	Patent Cooperation Treaty	Klapproth, Peter; Ehmann, Greg; Wingen, Neal.	PCT/IB08/053911 (pub no. 2009/040760)	9/25/2008	CLOCK GENERATOR	Pending		
		Yes	008211USP	U.S. Provisional		60/975,769	9/27/2007		Abandoned		
802915-227036 / 12291-036-227	VIRP314EP	No		EPO		EP08807807.6	9/25/2008		Pending		
802915-999039 / 12291-036-999	VIRP314	No		Utility		12/919,186	9/25/2008		Pending		
802915-228037 / 12291-037-228	VIRP315	No	81047613WO02	Patent Cooperation Treaty	Gregie, Neil; Vos, Antonius Maria Hubertus.	PCT/IB09/050814 (WO 2009/107108 Al)	2/28/2009	CLOCK SWITCHING CIRCUITS AND METHODS	Pending		
		Yes	81047613US01	U.S. Provisional		61/032,304	2/28/2008		Abandoned		
802915-999037 / 12291-037-999	VIRP315	No		Utility		12/919,099	2/28/2009		Pending		
.	VIRP315EP	No		Europe (EPO)		EP 09715351.4	2/28/2009		Pending		
802915-227038 / 12291-038-227		Yes	81050253EP01	Europe (EPO)	Jan Vink	08105281.3	9/9/2008	MEMORY CONTROLLER	Abandoned in favor of PCT filing		
802915-228038 / 12291-038-228	VIRP316	No	81050253WO02	Patent Cooperation Treaty	Jan Vink	PCT/IB2009/053873	9/4/2009		Pending		
		Yes	81057643US01	Provisional	Ehmann, Greg	60/983627	10/30/2007	METHOD AND SYSTEM FOR CLOCK CONTROL FOR POWER-STATE TRANSITIONS	Abandoned in favor of PCT filing		

CAM NUMBER / DOCKET NUMBER	VIRAGE REF.	ORIGINAL FILING?	NXP REF.	PAT TYPE	INVENTORS	APPL. NO.	FILED	TITLE	STATUS	EXPIRATION DATE	MAINTENANCE FEE DUE
802915-228039 / 12291-039-228	VIRP317	No	81057643WO01	Patent Cooperation Treaty		PCT/IB2008/054263 (pub no. 2009/057008)	10/16/2008		Pending		
802915-999039 / 12291-039-999	VIRP317	No		UTIL		12/741,001	10/16/2008		Pending		
802915-002039 / 12291-039-002	VIRP317	No		UK		UK Patent Application No. GB1008149.5					
		Yes	81091292US01	U.S. Provisional	Pontius, Tim	61/032,017	2/27/2008	METHODS AND SYSTEMS RELATED TO A CONFIGURABLE DELAY COUNTER USED WITH VARIABLE FREQUENCY CLOCKS	Abandoned in favor of PCT filing		
802915-228040 / 12291-040-228	VIRP318	No	81091292WO02	Patent Cooperation Treaty		PCT/IB2009/050810 WO/2009/107105	2/27/2009		Pending		
802915-999038 / 12291-038-999	VIRP318	No		Utility		12/919,077	2/27/2009		Pending		
802915-227040 / 12291-040-227	VIRP318EP	No		EPO		EP 09716056.8	2/27/2009		Pending		
		Yes	81337208EP01	Europe (EPO)	Nedalgi, Dharmaraj, M.	08101322.9	2/6/2008	LOW SWING INPUT RECEIVER CIRCUIT	Abandoned in favor of PCT filing		
802915-228041 / 12291-041-228	VIRP319	No	81337208WO02	Patent Cooperation Treaty	.	PCT/IB2009/050401 (pub no. 2009/098626)	2/2/2009		Pending		
802915-999041 / 12291-041-999	VIRP319	No		U.S.		12/866,734	2/2/2009		Pending		
802915-227041 / 12291-041-227	VIRP319EP	No		EPO		EP09708337.2	2/2/2009		Pending		

CAM NUMBER / DOCKET NUMBER	VIRAGE REF.	ORIGINAL FILING?	NXP REF.	PAT TYPE	INVENTORS	APPL. NO.	FILED	TITLE	STATUS	EXPIRATION DATE	MAINTENANCE FEE DUE
802915-228042 / 12291-042-228	VIRP320	Yes (claiming priority to an unpublished expired orignal European filing now abandoned)	81339384WO02	Patent Cooperation Treaty	Burchard, Artur Tadeusz; Kersten, Ger; Molnos, Anca Mariana; Milutinovic, Aleksandar; Goossens, Kees; Gerard Willem; Steffens, Elisabeth; Francisca Maria.	PCT/IB2009/051957	5/12/2009	USING A WORKLOAD PERIOD DETECTOR FOR SYNCHRONIZING WORKLOAD MEASUREMENT PERIOD TO APPLICATION PERIOD	Pending		
802915-228043 / 12291-043-228	VIRP321	Yes (claiming priority to an unpublished expired orignal European filing now abandoned)	81343595WO02	Patent Cooperation Treaty	Tomas Henriksson; Elisabeth Francisca, Maria Steffens.	PCT/IB2009/053260	7/27/2009	LAZY ACCEPT OF TRANSACTION REQUESTS TO IMPROVE ARITRATION DECISIONS	Pending		
802915-228044 / 12291-044-228	VIRP322	Yes (claiming priority to an unpublished expired orignal European filing now abandoned)	81343754WO02	Patent Cooperation Treaty	Tomas Henriksson; Martijn Coenen, Peiter Van Der Wolf; Elisabeth Francisca Maria Steffens.	PCT/IB2009/055014	11/11/2009	INTEGRATED CIRCUIT ARRANGEMENT, MODULE AND CIRCUIT PORTION	Pending		
802915-228045 / 12291-045-228	VIRP323	Yes (claiming priority to an unpublished expired orignal European filing now abandoned)	81359978WO02	Patent Cooperation Treaty	Marc Jeroen; Geuzebroek, Andre Krijn; Nieuwland, Hubertus; Gerardus Hendrikus Vermeulen.	PCT/IB2009/054139	9/22/2009	DATA PROCESSING SYSTEM COMPRISING A MONITOR	Pending		
		Yes	81361131EP01	Europe (EPO)	Tomas Henriksson; Elizabeth	EP08168737	11/10/2008	RESOURCE CONTROLLING	Abandoned in favor of PCT filing		

CAM NUMBER / DOCKET NUMBER	VIRAGE REF.	ORIGINAL FILING?	NXP REF.	PAT TYPE	INVENTORS	APPL. NO.	FILED	TITLE	STATUS	EXPIRATION DATE	MAINTENANCE FEE DUE
802915-228046 / 12291-046-228	VIRP324	No	81361131WO02	Patent Cooperation Treaty		PCT/IB2009/054961	11/9/2009		Pending		
802915-227046 / 12291-046-227	VIRP324EP	No		EPO		9759815.5	11/9/2009				
802915-999036 / 12291-046-999	VIRP324US	No		UTIL		12/919864	8/27/2010				
802915-227047 / 12291-047-227	VIRP325	Yes	81375368EP01	Europe (EPO)	Elisabeth Francisca Maria Steffens; Tomas Henriksson	09154844.6	3/11/2009	SYSTEMS AND METHODS FOR RESOURCE CONTROLLING	Abandoned in favor of PCT filing		3/11/2011
802915-228047 / 12291-047-228	VIRP325	No		Patent Cooperation Treaty		PCT/US2010/026988	3/11/2010		Pending		
802915-012048 / 12291-048-012	VIRP326JP	No	N 016898JP	Japan	Van Der Wolf, Pieter;	2000-548812	4/29/1999	DATA PROCESSING CIRCUIT WITH CACHE MEMORY	Pending		Not due until grant
802915-003048 12291-048-003	VIRP326DE	No	N 016898DE	Germany		99914717.6 (pub no. EP0996891-A1)	4/29/1999	DATA PROCESSING CIRCUIT WITH CACHE MEMORY	Granted patent no. 0996891 B1	4/29/2019	4/29/2010
802915-227048 / 12291-048-227		No	N 016898EP	Europe (EPO)		99914717.6 (pub no. 0996891-A1)	4/29/1999	DATA PROCESSING CIRCUIT WITH CACHE MEMORY	Abandoned		
		Yes	N 016898EPP	Europe (EPO)		98201513.3	5/8/1998	DATA PROCESSING CIRCUIT WITH CACHE MEMORY	Abandoned		
802915-004048 12291-004-012	VIRP326FR	No	N 016898FR	France		99914717.6 (pub no. 0996891-A1)	4/29/1999	DATA PROCESSING CIRCUIT WITH CACHE MEMORY	Granted Patent no. 0996891 B1	4/29/2019	4/29/2010
802915-002048 12291-048-002	VIRP326GB	No	N 016898GB	Great Britain		99914717.6	4/29/1999	DATA PROCESSING CIRCUIT WITH CACHE MEMORY	Granted Patent no. 0996891 B1	4/29/2019	4/29/2010

CAM NUMBER / DOCKET NUMBER	VIRAGE REF.	ORIGINAL FILING?	NXP REF.	PAT TYPE	INVENTORS	APPL. NO.	FILED	TITLE	STATUS	EXPIRATION DATE	MAINTENANCE FEE DUE
		No	N 016898NL	Netherlands		99914717.6	4/29/1999	DATA PROCESSING CIRCUIT WITH CACHE MEMORY	Abandoned		
		No	N 016898TW	Taiwan		87118311 (pub no. 501011, patent no. NI-161750)	11/4/1998	DATA PROCESSING CIRCUIT WITH CACHE MEMORY	Abandoned		
802915-999048 / 12291-048-999	VIRP326	No	N 016898US	U.S. Utility		09/306069	5/6/1999	DATA PROCESSING CIRCUIT WITH CACHE MEMORY AND CACHE MANAGEMENT UNIT FOR ARRANGING SELECTED STORAGE LOCATION IN THE CACHE MEMORY FOR REUSE DEPENDENT ON A POSITION OF PARTICULAR ADDRESS RELATIVE TO CURRENT ADDRESS	Granted	5/6/2019	11.5 Year 5/01/2012
		No	N 016898WO	Patent Cooperation Treaty		PCT/IB1999/000785 (pub no. 1999/059070)	4/29/1999	DATA PROCESSING CIRCUIT WITH CACHE MEMORY	Abandoned		
802915-012049 / 12291-049-012	VIRP326JP	No	US018077JP	Japan	Wingen, Neal T.	03-500753	5/29/2002	A POWER AND FREQUENCY ADJUSTABLE UART DEVICE	Pending		Not due until grant
802915-003049 / 12291-049-003	VIRP327DE	No	US018077DE1	Germany		EP02733103.2	5/29/2002		Granted	5/29/2022	5/29/2010
802915-227049 / 12291-049-227		No	US018077EP	Europe (EPO)		EP02733103.2 (pub no. 1397747-A)	5/29/2002		Abandoned		
802915-004049 / 12291-049-004	VIRP327FR	No	US018077FR1	France		EP02733103.2	5/29/2002		Granted Patent no. 1397747 B1	5/29/2022	5/29/2010
802915-002049 / 12291-049-002	VIRP327GB	No	US018077GB1	Great Britain		EP02733103.2	5/29/2002		Granted Patent no. 1397747 B1	5/29/2022	5/29/2010
802915-187049 / 12291-049-187	VIRP327KR	No	US018077KR	South Korea		10-2003-7001347	5/29/2002		Granted Patent no. 869901	5/29/2022	
	VIRP327	Yes	US018077US	U.S. Utility		09/870918 (pub no. 2002-0184543)	5/31/2001		Granted Patent no. 6,895,518	4/1/2023	7.5 Year 05/17/2012
		No	US018077WO	Patent Cooperation Treaty		PCT/IB2002/001970 (pub no. 2002/097639)	5/29/2002		Abandoned		
802915-012050 / 12291-050-012	VIRP328JP	No	US018110JP	Japan	Ehmann, Gregory	2003-515950	6/28/2002	METHOD AND SYSTEM USING A COMMON RESET AND A SLOWER RESET CLOCK	Pending		Not due until grant

CAM NUMBER / DOCKET NUMBER	VIRAGE REF.	ORIGINAL FILING?	NXP REF.	PAT TYPE	INVENTORS	APPL. NO.	FILED	TITLE	STATUS	EXPIRATION DATE	MAINTENANCE FEE DUE
802915-146050 / 12291-050-146	VIRP328CH	No	US018110CN	China		02802995.X (pub no. 1489723-A)	6/28/2002		Granted Patent no. 02802995.X	6/28/2022	
802915-227050 / 12291-050-227	VIRP328EP	No	US018110EP	Europe (EPO)		02741071.1 (pub no. 1415217-A)	6/28/2002		Pending		6/30/2010
		No	US018110KR	South Korea		10-2004-7000949	6/28/2002		Abandoned		
	VIRP328	Yes	US018110US	U.S. Utility		09/912146 (pub no. 2003-0020524-A1)	7/24/2001		Granted: Patent no. 6,611,158	7/24/2001	11 Year 2013
		No	US018110WO	Patent Cooperation Treaty		PCT/IB2002/002627 (pub no. 2003/010640)	6/28/2002		Abandoned		
802915-146051 / 12291-051-146	VIRP329CH	No	US020148CN1	China	Pontius, Timothy, A.; Jensen, Rune, H.; Rabeler, Thorwald.	3826547.8 (pub no. 1771482)	5/27/2003	ACCESS PROTECTED BUS SYSTEM	Pending		Not due until grant
802915-003051 / 12291-051-003	VIRP329DE	No	US020148DE	Germany		EP03727864.5	5/27/2003		Granted	5/27/2023	5/27/2011
802915-227051 / 12291-051-227		No	US020148EP1	Europe (EPO)		3727864.5 (pub no. 1631910-A)	5/27/2003		Abandoned		
802915-004051 / 12291-051-004	VIRP329FR	No	US020148FR	France		EP03727864.5	5/27/2003		Granted Patent no. 1631910 B1	5/27/2023	5/27/2011
802915-002051 / 12291-051-002	VIRP329GB	No	US020148GB	Great Britain		EP03727864.5	5/27/2003		Granted Patent no. 1631910 B1	5/27/2023	5/27/2011
802915-012051 / 12291-051-012	VIRP329JP	No	US020148JP1	Japan		2005-500172	5/27/2003		Pending		Not due until grant
802915-012052 / 12291-052-012	DIV of VIRP329JP	No		Japan		2010-87292			Pending		
802915-187051 / 12291-051-187	VIRP329KR	No	US020148KR1	South Korea		10-2005-7022562	5/27/2003		Pending		Not due until grant
		Yes	US020148US	U.S. Utility		10/155265; (pub no. 2003-0221030)	5/24/2002		Abandoned (failure to pay issue fee 5/30/2007)		
802915-228051 / 12291-051-228		No	US020148WO	Patent Cooperation Treaty		PCT/IB2003/002359; (pub no. 2004/107181)	5/27/2003		Abandoned		

CAM NUMBER / DOCKET NUMBER	VIRAGE REF.	ORIGINAL FILING?	NXP REF.	PAT TYPE	INVENTORS	APPL. NO.	FILED	TITLE	STATUS	EXPIRATION DATE	MAINTENANCE FEE DUE
	VIRP340	Yes	A 051130US	U.S. Utility	Dennis Koutsoures	09/313244	5/17/1999	SYNCHRONOUS MEMORY SYSTEMS WITH AUTOMATIC BURST MODE SWITCHING	Granted Patent No. 6,457,075	5/17/2019	11.5 Year Due 9/24/2013
	VIRP341	Yes	US 018159US	U.S. Utility	Ehmann, Gregory E.; Gregie, Neil; Bink, Arjan	09/955,704	9/19/2001	DATA COMMUNICATION BUS TRAFFIC GENERATOR ARRANGEMENT	Granted Patent no. 7,020,807 Issued 3/28/06	5/15/2023	7.5 YR 03/28/2013 11.5 YR 03/28/2017
	VIRP342	Yes	US 018134US	U.S. Utility	Ehmann, Gregory E.; Saxena, Swati	09/942,129	8/29/2001	ADAPTIVELY MONITORING BUS SIGNALS	Granted; Patent no. 6,931,524	11/21/2023	7.5 08/16/2012; 11.5 08/16/2016
	VIRP342DE	No	US 018134DE	Germany		EP 02 755 557	8/21/2002		Granted; Patent no.	8/21/2022	8/21/2010
	VIRP342EP	No	US 018134EP	Europe		EP 02 755 557	8/21/2002		Abandoned		
	VIRP342FR	No	US 018134FR	France		EP 02 755 557	8/21/2002		Granted; Patent no.	8/21/2022	8/21/2010
	VIRP342GB	No	US 018134GB	Great Britain		EP 02 755 557	8/21/2002		Granted; Patent no. 1421496	8/21/2022	8/21/2010
802915-012053 / 12991-053-012	VIRP342JP	No	US 018134JP	Japan		2003-523,373	8/21/2002		Granted Patent no. 4180513	8/21/2022	
		No	US 018134WO	PCT		PCT/IB02/031415; Publication WO2003/019379	8/21/2002		Abandoned		

S No.	Virage Reference		EVLC Reference		Application Serial No.	Title	Inventor(s)		Type	Filing Date
1	VIRP-		VL-P001		11/951,338	IMPROVING STATISTICAL YIELD OF A SYSTEM-ON-A-CHIP	Niranjan BEHERA Alexander SHUBAT		Utility Non-Provisional	6-Dec-07
2	VIRP-115PR		VL-P002PR		61/018344	MEMORY CONTROLLERS FOR MEMORY DEVICES	Raghavan MENON Raj MAHAJAN		Provisional	31-Dec-07
3	VIRP-116PR		VL-P003PR		61/018352	DELAY LOCKED LOOP IMPLEMENTATION	Raghavan MENON Raj MAHAJAN		Provisional	31-Dec-07
4	VIRP-109		VL-P004		12/057,355	POWER UP CIRCUIT	Yong ZHANG		Utility Non-Provisional	5-Mar-00
5	VIRP111		VL-P005		12/125,063	POWER SUPPLY REGULATION	Vipin Kumar TIWARI		Utility Non-Provisional	22-May-08
6	VIRP203		VL-P003		12/346,854	A DIGITAL DELAY LOCKED LOOP IMPLEMENTATION FOR PRECISE CONTROL OF TIMING SIGNALS	Raghavan MENON Raj MAHAJAN		Utility Non-Provisional	31-Dec-08
7	VIRP200		VL-P006		12/346,856	SYSTEM AND METHOD FOR CONTROLLING A DYNAMIC RANDOM ACCESS MEMORY	Raghavan MENON Raj MAHAJAN		Utility Non-Provisional	31-Dec-08
8	VIRP201		VL-P007		12/346,859	A DYNAMIC RANDOM ACCESS MEMORY CONTROLLER	Raghavan MENON Raj MAHAJAN		Utility Non-Provisional	31-Dec-08
9	VIRP202		VL-P008		12/346,860	SYSTEM AND METHOD FOR IMPROVING ACCESS EFFICIENCY TO A DYNAMIC RANDOM ACCESS MEMORY	Raghavan MENON Raj MAHAJAN		Utility Non-Provisional	31-Dec-08
10	VIRP119		VL-P009		12/346,862	LOW LEAKAGE ROM ARCHITECTURE	Vineet Kumar SACHAN Deepak SABHARWAL Amit KHANUJA		Utility Non-Provisional	31-Dec-08
11	VIRP205		VL-P010		12/346,866	COMPACT READ ONLY MEMORY CELL	Vineet Kumar SACHAN Deepak SABHARWAL [illegible]		Utility Non-Provisional	31-Dec-08
12	VIRP209		VL-P011		12/711,265	SILICON-ON-INSULATOR BASED LATERALLY DIFFUSED METAL OXIDE SEMICONDUCTOR DEVICE	Andrew E. Horch		Utility Non-Provisional	24-Feb-10
13	VIRP210		VL-P012		12/716,287	A HIGH-VOLTAGE SWITCHING CIRCUIT	Yanyi Liu Wong, Rebecca Shiu Yun Cheng		Utility Non-Provisional	3-Mar-10
14	VIRP208		VL-P013		12/717,966	METHOD OF FABRICATING A GATE OXIDE	Andrew E. Horch		Utility Non-Provisional	5-Mar-10

Client No.	DLG No.	Patent No.	Serial No.	Title	Inventor(s)	Status (or) Patent Issue Date	U.S. Filing Date
VIRP07	1263-0001US	6,363,020	09/455,045	ARCHITECTURE WITH MULTI-INSTANCE REDUNDANCY IM	Alex Shubat and Chang Hee Hong	3/26/2002	12/6/1999
VIRP07	1263-001PCT		PCT/US 00/42421	PCT APPLICATION BASED ON 1263-0001US CASE	Alex Shubat and Chang Hee Hong		11/30/2000
VIRP07CA	1263-0001CA	2,389,986		CANADA - FUSE BOX REDUNDANCY	Alex Shubat and Chang Hee Hong	4/15/2008	
VIRP07CON	1263-001CON	6,556,490	10/099,750	ARCHITECTURE WITH MULTI-INSTANCE REDUNDANCY	Alex Shubat and Chang Hee Hong	4/29/2003	3/15/2002
VIRP07EU	1263-0001EU			REGIONAL ENTRY FOR FUSE BOX REDUNDANCY	Alex Shubat and Chang Hee Hong	Partial Allowance indicated by EPO; Continuing Prosecution	
VIRP11	1263-0002US	6,466,504	09/590,619	COMPILABLE BLOCK CLEAR MECHANISM ON PER I/O BAS	Richard S. Roy	10/15/2002	6/8/2000
VIRP08	1263-0003US	6,356,503	09/510,692	REDUCED LATENCY ROW SELECTION CIRCUIT	Richard S. Roy	3/12/2002	2/23/2000
VIRP10	1263-0004US	6,236,618	09/542,033	CENTRALLY DECODED DIVIDED WORDLINE	Richard S. Roy	5/22/2001	4/3/2000
VIRP12	1263-0005US	6,249,471	09/605,221	FAST FULL SIGNAL DIFFERENTIAL OUTPUT PATH CIRCUIT	Richard S. Roy	6/19/2001	6/28/2000
VIRP13	1263-0006US	6,282,131	09/671,456	SELF-TIMED CLOCK CIRCUITRY IN A MULTI-BANK MEMOR	Richard S. Roy	8/28/2001	9/27/2000
VIRP14	1263-0007US	6,292,427	09/689,352	HIERARCHICAL SENSE AMP AND WRITE DRIVER CIRCUIT	Richard S. Roy	9/18/2001	10/12/2000
VIRP15	1263-0008US	6,466,470	09/706,314	CIRCUITRY FOR RESETTING MEMORY WITHOUT A WRITE	Houn Chang	10/15/2002	11/4/2000
VIRP16	1263-0009US	6,886,078	09/886,577	SIMULTANEOUS ACCESS AND CHACHE LOADING IN A HIE	Richard S. Roy	4/26/2005	6/21/2001
VIRP17	1263-0010US			FUSE BOX ERROR BITMAP	Richard S. Roy		Abandoned per Client
VIRP18	1263-0011US	6,424,556	09/750,949	SYSTEM AND METHOD FOR INCREASING PERFORMANCE	Adam A. Kablanian and Deepak Sabh	7/23/2002	12/28/2000
VIRP18D	1263-011DIV	6,587,364	10/128,441	LOW POWER TECHNIQUE VIA ADDRESS REMAPPING	Adam A. Kablanian and Deepak Sabh	7/1/2003	4/23/2002
VIRP19	1263-0012US	6,385,122	09/773,319	ROW AND COLUMN ACCESSIBLE MEMORY WITH A BUILT-	Houn Chang	5/7/2002	1/31/2001
VIRP23	1263-0013US	7,197,438	09/981,954	TIMING DATA FOR MEMORY COMPILERS	Mehta et al.	3/27/2007	10/18/2001
VIRP24	1263-0014US		60/295,038	HIERARCHICAL RC-NETLIST GENERATOR	Sabharwal et al.		Prov. 6/1/2001
		6,738,953	10/092,056			5/18/2004	Pat. 3/5/2002
VIRP25	1263-0015US	7,093,156	10/144,020	FUSE BOX AND MEMORY GROUPS	Shubat et al.	8/15/2006	5/13/2002
VIPR25CON	1263-0015CON	7,406,620	11/503,641	ETR SCHEME AND INTERFACE	Shubat et al.	7/29/2008	8/14/2006
VIRP26	1263-0016US			LIMITED SWING PRE SENSE-AMP	Jaroslav Raszka		Abandoned per Client
VIRP27	1263-0017US	6,473,356	10/002,568	LOW POWER READ CIRCUITRY	Jaroslav Raszka	10/29/2002	11/1/2001
VIRP28	1263-0018US		60/334,111	X-DEC W/PRECISION BUILT-IN SHUTDOWN	Raszka et al.		Prov. 11/30/2001
		6,597,629	10/223,499			7/22/2003	Pat. 8/19/2002
VIRP38	1263-0019US	6,744,661	10/146,523	HARDENED CELL TO REDUCE SER	Shubat	6/1/2004	5/15/2002
VIRP37	1263-0020US	7,114,118	10/216,598	ETR WITH READ MARGIN TEST I/F	Shubat	9/26/2006	8/9/2002
VIRP37CON	1263-0020CON	7,458,005	11/524,691	ADJUSTABLE READ MARGIN SCHEME	Shubat	11/25/2008	9/21/2006
VIRP39	1263-0021US		60/377,161	MULTI TIME LOOPS FOR ADJUSTABLE READ MARGINS	Sabharwal		Prov. 4/30/2002
		6,711,092	10/279,428			3/23/2004	Pat. 10/24/2002
VIRP65	1263-0022US	7,031,866	10/701,545	METHOD TO TEST REGISTER FILE MEMORY AT SPEED	Behera et al.	4/18/2006	11/5/2003
VIRP65CON	1263-0022CON	7,539,590	11/403,783	SYSTEM AND METHOD FOR TESTING A MEMORY	Behera et al.	5/26/2009	4/13/2006
VIRP66	1263-0023US	7,415,641	10/702,014	METHOD TO REPAIR FAULTY REGISTER FILE MEMORY	Behera et al.	8/19/2008	11/5/2003
VIRP66C1	1263-0023C1		12/188,892	METHOD TO REPAIR FAULTY REGISTER FILE MEMORY	Behera et al.	Pending Non Final OA; Response filed 3/19/2010	8/8/2008
VIRP64	1263-0024US	7,035,129	10/816,763	PARTITIONED SOURCE LINE ARCHITECTURE	Khanuja	4/25/2006	4/2/2004
VIRP64CON	1263-0024CON	7,301,819	11/409,610	ROM WITH PARTITIONED SOURCE LINES	Khanuja	11/27/2007	4/24/2006
VIRP72	1263-0025US	7,061,794	10/813,419	WORDLINE-BASED BITCELL SOURCE BIASING	Shubat et al.	6/13/2006	3/30/2004
VIRP72DIV	1263-0025DIV		11/451,043	SOURCE-BIASED SRAM CELL ARCHITECTURE	Sabharwal et al.	Issue Fee paid 2/16/10; Projected Patent Issue Date: 4/6/2010	6/12/2006
VIRP88	1263-0026US		60/721,822	VIRTUAL GROUND DIFFUSION PROM ARRAY	Khanuja et al.		Prov. 9/29/2005
		7,376,013	11/385,269			5/20/2008	Pat. 3/21/2006
VIRP88CON	1263-0026C1	7,609,550	12/099,640	VIRTUAL GROUND DIFFUSION PROM ARRAY	Khanuja et al.	10/27/2009	4/9/2008
VIRP88DIV	1263-0026D1		12/577,405	COMPACT VIRTUAL GROUND DIFFUSION PROGRAMMABL	Khanuja et al.	Ready for Examination; No OA yet.	10/12/2009
VIRP82	1263-0027PR		60/758,017	PEAK CURRENT MODELING FOR COMPILERS	Tiwari		Prov. 1/11/2006
	1263-0027US		11/593,729			Notice of Allowance mailed 2/16/2010; Issue Fee to be paid.	Pat. 11/7/2006
VIRP94	1263-0028PR		60/789,784	METHOD OF VERIFICATION OF IP INTEGRITY IN SOC	Darbinyan et al.		Prov. 4/6/2006
	1263-0028US	7,673,264	11/732,900			3/2/2010	Pat. 4/5/2007
VIRP97	1263-0029US	7,549,136	11/614,133	ESTIMATION OF INTRINSIC CAPACITANCE OF A MEMORY	Tiwari	6/16/2009	12/22/2006

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VIRP99Z	1263-0030PR		60/816,414	SHARED PROCESSOR ARCHITECTURE	Darbinyan et al.		Prov. 6/23/2006
	1263-0030US		11/766,943			Ready for Examination; No OA yet.	Pat. 6/22/2006
VIRP110	1263-0031US		11/968,021	MEMORY LEAKAGE CONTROL	Tooher et al.	Notice of Allowance mailed 3/9/2010; Issue Fee to be paid.	12/31/2007

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VIRP-0207	461844-0002.0002	6,664,909	09/929,652	Method and Apparatus for Trimming High-Resolution Digital-to-Analog Converter	Diorio, Christopher J Figueroa, Miguel E. Hass, Terry D. Humes, Todd E. Hyde, John D. Lindhorst, Chad A.	16-Dec-2003	US	13-Aug-2001
VIRP-0212	461844-0040.0041	7,508,719	11/601,305	Non-Volatile Memory Cell Circuit With Programming Through Band-To Band Tunneling And Impact Ionization Gate Current	Horch, Andrew E.	24-Mar-2009	US	16-Nov-2006
VIRP-0212CON	461844-0040.0099		12/403,333	Programming Through Band-To Band Tunneling And Impact Ionization Gate Current	Horch, Andrew E.	Pubished SC-Issue Notification	US	12-Mar-2009
VIRP-0213DIV	461844-0002.0045		10/661,037	pFET Synapse Transistor With Structure For Facilitating Charge Injection And/Or Tunneling With Respect To A Floating Gate	Figueroa, Miguel E. Hass, Terry D. Humes, Todd E. Hyde, John D.	Pending SC-Board Decision	US	12-Sep-2003
VIRP-0217	461844-0104.0015		11/387,603	Schottky Junction Diode Devices In CMOS	Ma, Yanjun Oliver, Ronald A. Humes, Todd E. Mavoori, Jaideep	Published Issue Fee Due	US	22-Mar-2006
VIRP-0218	461844-0105.0016		11/387,515	Schottky Junction Diode Devices In CMOS With Multiple Wells	Ma, Yanjun Oliver, Ronald A. Humes, Todd E.	Published SC-OA/Allowance	US	22-Mar-2006
VIRP-0220	461844-0018.0018		11/372,438	Fault Tolerant Non Volatile Memories and Methods	Hyde, John D.	Published SC-Issue Notification	US	9-Mar-2006
VIRP-0221	461844-0019.0019		11/224,743	Pseudo-Nonvolatile Direct-Tunneling Floating-Gate Device	Hyde, John D. Humes, Todd E. Diorio, Christopher J. Mead, Carver A.	Pending SC-OA/Allowance	US	12-Sep-2005
VIRP-0222	461844-0197.0020	7,580,311	11/513,597	Reduced Area High Voltage Switch for NVM	Pesavento, Alberto	25-Aug-2009	US	30-Aug-2006
VIRP-0223	461844-0134.0021		11/490,407	Graded Junction High Voltage Semiconductor Device	Wang, Bin	IDS Due	US	19-Jul-2006
VIRP-0224	461844-0022.0022		11/768,974	One Time Programmable Memory Test Structures and Methods	Humes, Todd E. Horch, Andrew E.	Response to OA Due	US	27-Jun-2007
VIRP-0225	461844-0025.0025		11/981,056	Configurable Single Bit/Dual Bits Memory	Pesavento, Alberto Langlinais, Jaime L.	Pending SC-Issue Notification	US	30-Oct-2007

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VIRP-0226DIV	461844-0025.0031		12/012,910	Radio Frequency (RFID) Tag Including Configurable Single Bit/Dual Bits Memory	Pesavento, Alberto Langlinais, Jaime L.	Pending IDS Due RCE Due	US	5-Feb-2008
VIRP-0227	461844-0026.0026		11/982,277	Adaptive Programming Of Memory Circuit Including Writing Data In Cells Of A Memory Circuit	Humes, Todd E. May, Alex Sutandi, Agustinus	Pending Issue Fee Due	US	31-Oct-2007
VIRP-0228	461844-0028.0028		11/982,276	Methods For Adaptive Programming Of Memory Circuit Including Writing Data in Cells of a Memory Circuit	Humes, Todd E. May, Alex Sutandi, Agustinus	Pending Issue Fee Due	US	31-Oct-2007
VIRP-0229	461844-0029.0029		12/114,574	Non-Volatile Memory Circuit With Tailored Reliability	Ma, Yanjun Mozsgai, Steven I.	Pending SC-OA/Allowance	US	2-May-2008
VIRP-0230	461844-0030.0030		12/143,133	High-Voltage Switch Using Three FETS	Sutandi, Agustinus Wong, Yanyi L.	Pending IDS Due	US	20-Jun-2008
VIRP-0231	461844-0032.0032	7,679,957	11/106,982	Redundant Non-Volatile Memory Cell	Ma, Yanjun Colleran, William T. Gutnik, Vadim	16-Mar-2010	US	15-Apr-2005
VIRP-0232DIV	461844-0032.0033		12/020,522	RFID Tag With Redundant Non-Volatile Memory Cell	Ma, Yanjun Colleran, William T. Gutnik, Vadim	Published Issue Fee Due	US	26-Jan-2008
VIRP-0233	461844-0034.0034		11/842,862	Power-On Reset Apparatus, Systems, And Methods	Khieu, Cong	Pending SC-OA/Allowance	US	21-Aug-2007
VIRP-0234	461844-0035.0035		11/837,810	Electrostatic Discharge Management Apparatus, Systems, And Methods	Khieu, Cong Ma, Yanjun Mavoori, Jaideep	Pending SC-OA/Allowance	US	13-Aug-2007
VIRP-0235DIV	461844-0034.0036		11/965,359	Radio Frequency Identification Device Power-On Reset Management	Khieu, Cong	Pending SC-OA/Allowance	US	27-Dec-2007
VIRP-0236DIV	461844-0035.0037		11/965,307	Radio Frequency Identification Device Electrostatic Discharge Management	Khieu, Cong Ma, Yanjun Mavoori, Jaideep	Pending SC-OA/Allowance	US	27-Dec-2007
VIRP-0237	461844-0038.0038		11/701,710	Non-Volatile Memory Devices Having Floating-Gates Fets With Different Source-Gate And Drain-Gate Border Lengths	Horch, Andrew E.	Published Response to OA Due	US	2-Feb-2007
VIRP-0238DIV	461844-0038.0043		12/006,330	Device Having Floating-Gate Fets With Different Source-Gate And Drain-Gate	Horch, Andrew E.	Published SC-OA/Allowance	US	31-Dec-2007

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VIRP-0239	461844-0039.0039		11/818,757	Only One Time Programmable (OTP) Memory Appear Multiple Times Programmable (MTP)	Pollack, Seth Lindhorst, Chad A.	Pending SC-OA/Allowance	US	15-Jun-2007
VIRP-0240DIV	461844-0039.0044		12/006,321	Memory Management Unit (MMU) To Make	Lindhorst, Chad A.	SC-OA/Allowance	US	31-Dec-2007
VIRP-0241	461844-0040.0040	7,474,568	11/601,474	Non-Volatile Memory With Programming Through Band-To-Band Tunneling And Impact Ionization Gate Current	Horch, Andrew E.	6-Jan-2009	US	16-Nov-2006
VIRP-0242	461844-0042.0042	7,652,921	12/080,127	Multi-Level Non-Volatile Memory Cell With High-VT Enhanced BTBT Device	Horch, Andrew E. Wang, Bin	26-Jan-2010	US	31-Mar-2008
VIRP-0242CON	461844-0042.0100		12/410,417	Non-Volatile Memory Cell With BTBT Programming	Horch, Andrew E.	Published SC-OA/Allowance	US	24-Mar-2009
VIRP-0243	461844-0103.0047	7,049,872	10/681,577	Transistors To Match The Electrical Characteristics Of Interleaved And Pipelined Circuits	Diorio, Christopher J. Humes, Todd E. Thomas, Michael H.	23-May-2006	US	7-Oct-2003
VIRP-0244	461844-0105.0048	6,909,389	10/281,384	Method and Apparatus for Calibration of an Array of Scaled Electronic Circuit Elements	Hyde, John D. Kaplan, David L.	21-Jun-2005	US	24-Oct-2002
VIRP-0245	461844-0049.0049	6,661,278	10/191,779	High Voltage Charge Pump Ciruit	Gilliland, Troy N.	9-Dec-2003	US	8-Jul-2002
VIRP-0246	461844-0050.0050	6,977,527	10/455,261	Method And Apparatus For Suppressing Spurious Values In A Differential Output Current	Hyde, John D.	20-Dec-2005	US	4-Jun-2003
VIRP-0247	461844-0051.0051	6,954,159	10/612,829	Low Distortion Band-Pass Analog To Digital Converter With Feed Forward	Cooper, Scott A. Esterberg, Aanand L.	11-Oct-2005	US	1-Jul-2003
VIRP-0248	461844-0052.0052	6,873,281	10/652,537	Interleaved Digital Correction For MASH Delta-Sigma ADC	Esterberg, Aanand L. Cooper, Scott A.	29-Mar-2005	US	28-Aug-2003
VIRP-0249	461844-0104.0054	6,958,646	10/447,684	Autozeroing Floating-Gate Amplifier	Colleran, William T. Humes, Todd E. Diorio, Christopher J.	25-Oct-2005	US	28-May-2003
VIRP-0250DIV	461844-0104.0055	7,102,438	11/257,897	Autozeroing Floating-Gate Amplifier	Colleran, William T. Humes, Todd E. Diorio, Christopher J.	5-Sep-2006	US	24-Oct-2005
VIRP-0251DIV	461844-0056.0007	7,408,809	11/528,069	Method And Apparatus For Programming Single-Poly pFET-Based Nonvolatile Memory Cells	Diorio, Christopher J. Humes, Todd E.	5-Aug-2008	US	26-Sep-2006
VIRP-0252DIV	461844-0056.0008	7,411,829	11/528,262	Single-Poly pFET-Based Nonvolatile	Humes, Todd E.	12-Aug-2008	US	26-Sep-2006

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VIRP-0253DIV	461844-0056.0009	7,411,828	11/528,150	Method And Apparatus For Programming Single-Poly pFET-Based Nonvolatile Memory Cells	Diorio, Christopher J. Humes, Todd E.	12-Aug-2008	US	26-Sep-2006
VIRP-0255DIV	461844-0056.0023	7,573,749	11/731,228	Counteracting Overtunneling In Nonvolatile Memory Cells	Diorio, Christopher J. Lindhorst, Chad A. Srinivas, Shailendra Pesavento, Alberto Gilliland, Troy N.	11-Aug-2009	US	29-Mar-2007
VIRP-0256CON	461844-0056.0027		11/865,777	pFET Nonvolatile Memory	Pesavento, Alberto Hyde, John D.	Published Final OA Response Due	US	2-Oct-2007
VIRP-0257CON	461844-0056.0046		11/829,370	Hybrid Non-Volatile Memory	Pesavento, Alberto	Published IDS Due	US	27-Jul-2007
VIRP-0258	461844-0056.0056	6,853,583	10/245,183	Method And Apparatus for Preventing Overtunneling in pFET-based Nonvolatile Memory Cells	Diorio, Christopher J. Lindhorst, Chad A. Srinivas, Shailendra Pesavento, Alberto Gilliland, Troy N.	8-Feb-2005	US	16-Sep-2002
VIRP-0259CON	461844-0056.0066	7,149,118	10/936,282	Method And Apparatus For Programming Single-Poly pFET-Based Nonvolatile Memory Cells	Diorio, Christopher J. Humes, Todd E.	12-Dec-2006	US	7-Sep-2004
VIRP-0260CON	461844-0056.0074	7,212,446	10/830,280	Counteracting Overtunneling In Nonvolatile Memory Cells Using Charge Extraction Control	Diorio, Christopher J. Lindhorst, Chad A. Srinivas, Shailendra Pesavento, Alberto Gilliland, Troy N.	1-May-2007	US	21-Apr-2004
VIRP-0261CON	461844-0056.0075	7,283,390	11/237,099	Hybrid Non-Volatile Memory	Pesavento, Alberto	16-Oct-2007	US	28-Sep-2005
VIRP-0262CON	461844-0056.0082	7,289,358	11/335,185	MTP NVM Elements By-Passed for Programming	Pesavento, Alberto Gilliland, Troy N. Bernard, Frédéric J.	30-Oct-2007	US	18-Jan-2006
VIRP-0263	461844-0057.0057	7,187,237	10/268,116	Use of Analog-Valued Floating-Gate Transistors for Parallel and Serial Signal Processing	Humes, Todd E. Oliver, Ronald A. Colleran, William T. Cooper, Scott A.	6-Mar-2007	US	8-Oct-2002

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VIRP-0264DIV	461844-0057.0058	7,061,324	11/055,959	Use Of Analog-Valued Floating-Gate Transistors For Parallel And Serial Signal Processing	Diorio, Christopher J. Humes, Todd E. Oliver, Ronald A. Colleran, William T. Cooper, Scott A.	13-Jun-2006	US	10-Feb-2005
VIRP-0265DIV	461844-0057.0059	7,038,603	11/055,947	Analog To Digital Converter Using Analog-Valued Floating-Gate Transistors	Humes, Todd E. Oliver, Ronald A.	2-May-2006	US	10-Feb-2005
VIRP-0266DIV	461844-0057.0060	7,038,544	11/055,948	Transistors For Parallel And Serial Signal Processing	Humes, Todd E. Oliver, Ronald A.	2-May-2006	US	10-Feb-2005
VIRP-0267DIV	461844-0057.0061	7,389,101	11/055,958	Transistors for Parallel and Serial Signal Processing	Humes, Todd E. Oliver, Ronald A.	17-Jun-2008	US	10-Feb-2005
VIRP-0268CON	461844-0057.0062	7,199,663	11/409,311	Transistors For Parallel And Serial Signal Processing	Humes, Todd E. Oliver, Ronald A.	3-Apr-2007	US	21-Apr-2006
VIRP-0269	461844-0063.0063	7,242,614	10/813,907	Rewriteable Electronic Fuses	Bernard, Frédéric J. Humes, Todd E. Pesavento, Alberto	10-Jul-2007	US	30-Mar-2004
VIRP-0270	461844-0064.0064	7,388,420	10/814,866	Rewriteable Electronic Fuses	Bernard, Frédéric J. Humes, Todd E.	17-Jun-2008	US	30-Mar-2004
VIRP-0271	461844-0065.0065	7,177,182	10/814,868	Rewriteable Electronic Fuses	Bernard, Frédéric J. Humes, Todd E.	13-Feb-2007	US	30-Mar-2004
VIRP-0272	461844-0106.0067	7,145,370	10/814,867	High-Voltage Switches In Single-Well CMOS Processes	Diorio, Christopher J. Gilliland, Troy N.	5-Dec-2006	US	30-Mar-2004
VIRP-0273CON	461844-0068.0068	6,950,342	10/437,262	Differential Floating Gate Nonvolatile Memories	Diorio, Christopher J. Gilliland, Troy N. Pesavento, Alberto	27-Sep-2005	US	12-May-2003
VIRP-0274	461844-0069.0069	6,842,327	10/635,247	High Voltage CMOS-Compatible Capacitors	Diorio, Christopher J. Bernard, Frédéric J.	11-Jan-2005	US	5-Aug-2003
VIRP-0275DIV	461844-0069.0078	7,071,507	10/931,583	High Voltage CMOS-Compatible Capacitors	Diorio, Christopher J. Bernard, Frédéric J.	4-Jul-2006	US	1-Sep-2004
VIRP-0276DIV	461844-0069.0079	7,042,701	10/931,582	High Voltage CMOS-Compatible Capacitors	Diorio, Christopher J. Bernard, Frédéric J.	9-May-2006	US	1-Sep-2004
VIRP-0277DIV	461844-0069.0083	7,262,092	11/326,243	High Voltage CMOS-Compatible Capacitors	Diorio, Christopher J. Bernard, Frédéric J.	28-Aug-2007	US	4-Jan-2006
VIRP-0290CON *	461844-0086.0006		2004-520129	Floating-Gate Semiconductor Structures	Diorio, Christopher J. Humes, Todd E.	Published SC-OA	JP	9-Jul-2003
VIRP-0278CON	461844-0070.0070	7,221,596	10/839,985	pFET Nonvolatile Memory	Bernard, Frédéric J. Hyde, John D.	22-May-2007	US	5-May-2004

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VIRP-0279	461844-0071.0071	7,315,067	10/884,236	Native High-Voltage N-Channel LDMOSFET in Standard Logic CMOS	Wang, Bin	1-Jan-2008	US	2-Jul-2004
VIRP-0280	461844-0072.0072	7,375,398	11/138,888	High Voltage FET Gate Structure	Wang, Bin Wang, Chih-Hsin	20-May-2008	US	26-May-2005
VIRP-0281CON	461844-0111.0011		10/952,708	High-Voltage LDMOSFET And Applications Therefor In Standard CMOS	Wang, Bin Colleran, William T. Wang, Chih-Hsin	Published SC-Board Decision	US	28-Sep-2004
VIRP-0282	461844-0111.0073	7,145,203	10/884,326	Graded-Junction High-Voltage MOSFET in Standard Logic CMOS	Wang, Bin	5-Dec-2006	US	2-Jul-2004
VIRP-0283	461844-0076.0076	7,233,274	11/313,549	Capacitive Level Shifting for Analog Signal Processing	Kuhn, Jay A.	19-Jun-2007	US	20-Dec-2005
VIRP-0284CON	461844-0080.0024		11/748,541	Inverter Non-Volatile Memory Cell And Array System	Wang, Bin Wang, Chih-Hsin Colleran, William T.	Published SC-OA/Allowance	US	15-May-2007
VIRP-0285	461844-0080.0080	7,257,033	11/084,214	Inverter Non-Volatile Memory Cell And Array System	Wang, Bin Wang, Chih-Hsin Colleran, William T.	14-Aug-2007	US	17-Mar-2005
VIRP-0286	461844-0081.0081	7,263,001	11/084,213	Compact Non-Volatile Memory Cell and Array System	Diorio, Christopher J. Humes, Todd E.	28-Aug-2007	US	17-Mar-2005
VIRP-0287 *	461844-0084.0084	5,627,392	08/399,966	Semiconductor Structure for Long Term Learning	Hasler, Paul E. Mead, Carver A.	6-May-1997	US	7-Mar-1995
VIRP-0288 *	461844-0084.0090	5,990,512	08/845,018	Electron Injection and Four-Terminal P-FET Semiconductor Structure for Long-Term	Hasler, Paul E. Mead, Carver A.	23-Nov-1999	US	22-Apr-1997
VIRP-0291DIV *	461844-0086.0012	7,548,460	10/915,107	Floating-Gate Semiconductor Structures	Diorio, Christopher J. Humes, Todd E.	16-Jun-2009	US	9-Aug-2004
VIRP-0293CON *	461844-0086.0053	6,965,142	10/192,773	Floating-Gate Semiconductor Structures	Diorio, Christopher J. Humes, Todd E.	15-Nov-2005	US	9-Jul-2002
VIRP-0294DIV *	461844-0086.0077	7,098,498	10/914,968	Floating-Gate Semiconductor Structures	Diorio, Christopher J. Humes, Todd E.	29-Aug-2006	US	9-Aug-2004
VIRP-0295CON *	461844-0086.0085	5,825,063	08/690,198	Three-Terminal Silicon Synaptic Device	Diorio, Christopher J. Hasler, Paul E. Mead, Carver A. Minch, Bradley A.	20-Oct-1998	US	26-Jul-1996
VIRP-0296 *	461844-0086.0086	5,875,126	08/721,261	Autozeroing Floating-Gate Amplifier	Diorio, Christopher J. Hasler, Paul E. Mead, Carver A. Minch, Bradley A.	23-Feb-1999	US	26-Sep-1996

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VIRP-0297CON *	461844-0086.0087	5,898,613	08/882,717	p-MOS Analog EEPROM Cell	Diorio, Christopher J. Mead, Carver A.	27-Apr-1999	US	25-Jun-1997
VIRP-0298DIV *	461844-0086.0088	5,914,894	09/088,655	Method for Implementing a Learning Function	Hasler, Paul E. Mead, Carver A. Minch, Bradley A.	22-Jun-1999	US	1-Jun-1998
VIRP-0299DIV *	461844-0086.0089	5,986,927	09/189,595	Autozeroing Floating-Gate Amplifier	Hasler, Paul E. Mead, Carver A. Minch, Bradley A.	16-Nov-1999	US	10-Nov-1998
VIRP-0300DIV *	461844-0086.0092	6,144,581	09/201,327	pMOS EEPROM Non-Volatile Data Storage	Diorio, Christopher J. Mead, Carver A.	7-Nov-2000	US	30-Nov-1998
VIRP-0301CON *	461844-0086.0093	6,452,835	09/699,059	pMOS Analog EEPROM Cell	Diorio, Christopher J. Mead, Carver A.	17-Sep-2002	US	27-Oct-2000
VIRP-0302DIV *	461844-0087.0091	6,125,053	09/201,677	Semiconductor Structure for Long-Term Learning	Diorio, Christopher J. Mead, Carver A.	26-Sep-2000	US	30-Nov-1998
VIRP-0303 *	461844-0094.0094	5,258,759	07/962,451	Algorithmic Digital-To-Analog And Analog-To-Digital Conversion	Cauwenberghs, Gert Yariv, Amnon	2-Nov-1993	US	16-Oct-1992
VIRP-0304	461844-0098.0098		12/239,696	pFET Nonvolatile Memory	Pesavento, Alberto	Pending IDS Due	US	26-Sep-2008
VIRP-0305CON *	461844-0094.0095	5,479,170	08/146,660	Method And Apparatus For Long-Term Multi-Valued Storage In Dynamic Analog Memory	Cauwenberghs, Gert Yariv, Amnon	26-Dec-1995	US	2-Nov-1993

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