

PATENT ASSIGNMENT

Electronic Version v1.1
 Stylesheet Version v1.1

| | |
|--|--|
| SUBMISSION TYPE: | NEW ASSIGNMENT |
| NATURE OF CONVEYANCE: | ASSIGNMENT |
| CONVEYING PARTY DATA | |
| Name | Execution Date |
| ANOBIT TECHNOLOGIES LTD. | 06/01/2012 |
| RECEIVING PARTY DATA | |
| Name: | APPLE INC. |
| Street Address: | 1 INFINITE LOOP |
| City: | CUPERTINO |
| State/Country: | CALIFORNIA |
| Postal Code: | 95014 |
| PROPERTY NUMBERS Total: 1 | |
| Property Type | Number |
| Application Number: | 12323544 |
| CORRESPONDENCE DATA | |
| Fax Number: | (512)853-8801 |
| Phone: | 5128538800 |
| Email: | kashby@intprop.com |
| <i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent via US Mail.</i> | |
| Correspondent Name: | MEYERTONS HOOD KIVLIN KOWERT & GOETZEL |
| Address Line 1: | PO BOX 398 |
| Address Line 4: | AUSTIN, TEXAS 78746-0398 |
| ATTORNEY DOCKET NUMBER: | 5888-75804 |
| NAME OF SUBMITTER: | B. Noel Kivlin |
| <p>Total Attachments: 42 source=Assignment_Anobit_to_Apple#page1.tif source=Assignment_Anobit_to_Apple#page2.tif source=Assignment_Anobit_to_Apple#page3.tif source=Assignment_Anobit_to_Apple#page4.tif</p> | |

CH \$40.00 12323544

source=Assignment_Anobit_to_Apple#page5.tif
source=Assignment_Anobit_to_Apple#page6.tif
source=Assignment_Anobit_to_Apple#page7.tif
source=Assignment_Anobit_to_Apple#page8.tif
source=Assignment_Anobit_to_Apple#page9.tif
source=Assignment_Anobit_to_Apple#page10.tif
source=Assignment_Anobit_to_Apple#page11.tif
source=Assignment_Anobit_to_Apple#page12.tif
source=Assignment_Anobit_to_Apple#page13.tif
source=Assignment_Anobit_to_Apple#page14.tif
source=Assignment_Anobit_to_Apple#page15.tif
source=Assignment_Anobit_to_Apple#page16.tif
source=Assignment_Anobit_to_Apple#page17.tif
source=Assignment_Anobit_to_Apple#page18.tif
source=Assignment_Anobit_to_Apple#page19.tif
source=Assignment_Anobit_to_Apple#page20.tif
source=Assignment_Anobit_to_Apple#page21.tif
source=Assignment_Anobit_to_Apple#page22.tif
source=Assignment_Anobit_to_Apple#page23.tif
source=Assignment_Anobit_to_Apple#page24.tif
source=Assignment_Anobit_to_Apple#page25.tif
source=Assignment_Anobit_to_Apple#page26.tif
source=Assignment_Anobit_to_Apple#page27.tif
source=Assignment_Anobit_to_Apple#page28.tif
source=Assignment_Anobit_to_Apple#page29.tif
source=Assignment_Anobit_to_Apple#page30.tif
source=Assignment_Anobit_to_Apple#page31.tif
source=Assignment_Anobit_to_Apple#page32.tif
source=Assignment_Anobit_to_Apple#page33.tif
source=Assignment_Anobit_to_Apple#page34.tif
source=Assignment_Anobit_to_Apple#page35.tif
source=Assignment_Anobit_to_Apple#page36.tif
source=Assignment_Anobit_to_Apple#page37.tif
source=Assignment_Anobit_to_Apple#page38.tif
source=Assignment_Anobit_to_Apple#page39.tif
source=Assignment_Anobit_to_Apple#page40.tif
source=Assignment_Anobit_to_Apple#page41.tif
source=Assignment_Anobit_to_Apple#page42.tif

EXHIBIT A -1
ASSIGNMENT OF PATENT RIGHTS

This patent assignment ("Patent Assignment") is entered into as of the below-date by and between Anobit Technologies Ltd., a company duly incorporated under the law of the State of Israel under Company Number 51-384451-4, with its registered office at 8 Hasadnaot St., Herzliya, Israel ("Assignor"), and Apple Inc., a California corporation with principal place of business at 1 Infinite Loop, Cupertino, CA 95014 ("Assignee").

For good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, Assignor does hereby irrevocably sell, assign, transfer, and convey unto Assignee or its designees all of Assignor's right, title, and interest, including without limitation, the right to sue or assert causes of action for past, present and future infringement, in and to all of the following (collectively, the "Patent Rights"):

- (a) the provisional patent applications, patent applications and patents listed in the attached Exhibit A-2 (the "Patents");
- (b) all provisional patent applications, patent applications, patents or other similar governmental grants or issuances (i) from which any of the Patents directly or indirectly claims priority and/or (ii) for which any of the Patents directly or indirectly forms a basis for priority;
- (c) reissues, re-examinations, extensions, continuations, continuations in part, continuing prosecution applications, requests for continuing examinations, and divisions of any item in the foregoing categories (a) and (b);
- (d) rights to all inventions claimed in any item in the foregoing categories (a) through (c);
- (e) items in any of the foregoing in categories (a) through (d), whether or not expressly listed as Patents below and whether or not claims in any of the foregoing have been rejected, withdrawn, cancelled, or the like;
- (f) rights to all inventions, invention disclosures, and discoveries described in any item in the foregoing categories (a) through (e), and all other rights arising out of such inventions, invention disclosures, and discoveries;
- (g) rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections, or other governmental grants or issuances of any type with respect to any inventions claimed in any item in the foregoing categories (a) through (c), including, without limitation, under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement, or understanding;
- (f) causes of action (whether currently pending, filed, or otherwise) and other enforcement rights under or on account of any of the Patents and/or any item in any of the foregoing categories (a) through (c), including, without limitation, all causes of action and other enforcement rights for (i) damages, (ii) injunctive relief, and (iii) other remedies of any kind for past, current, and future infringement; and
- (i) all rights to collect royalties and other payments under or on account of any of the Patents and/or any item in the foregoing categories (b) through (h).

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models or other governmental grants or

issuances that may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

The terms and conditions of this Assignment of Patent Rights will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

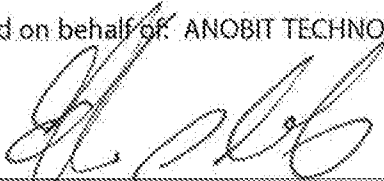
This Assignment of Patent Rights is being entered into in connection with that certain Intellectual Property Purchase Agreement between Assignor and Assignee. If there is any inconsistency between this Assignment of Patent Rights and such Intellectual Property Purchase Agreement, the Intellectual Property Purchase Agreement shall prevail.

[Remainder of Page Intentionally Left Blank]

Signed at Santa Clara County, California USA on L June 2012

ASSIGNOR

For and on behalf of: ANOBIT TECHNOLOGIES LTD.



Name: Elizabeth S. Rafael

Title: Director

Date: L June 2012

ASSIGNEE

For and on behalf of: APPLE INC.



Name: Gene Levoff

Title: Assistant Secretary

Date: L June 2012

EXHIBIT A -2
LIST OF PATENTS ASSIGNED UNDER ASSIGNMENT OF PATENT RIGHTS (EXHIBIT A-1)

EXHIBIT A-2

LIST OF PATENTS ASSIGNED UNDER EXHIBIT A-1 ASSIGNMENT OF PATENT RIGHTS

| Country | Patent Number | Application Number | Publication Number | Title |
|---------|---------------|--------------------|--------------------|---|
| US | | 61471148 | N/A | Recovery from read failures in NAND flash by using volatile memory. |
| US | | 60747106 | N/A | DSP and coding algorithms |
| US | | 60806533 | N/A | High Density Memory Systems and Methods |
| US | | 60821764 | N/A | Algorithms for programming and reading memory devices Additional files: Coding and Decoding Algorithms for Memory Devices Method for Feedback Coded Programming in Memory Devices Non-Linear Equalization in Flash Memories |
| US | | 60822236 | N/A | Algorithms for Increasing Density and Robustness of Memory Devices Additional File: Dynamic data-rate allocation, Precoding for combating impulsive noise |
| US | | 60823650 | N/A | Algorithms for Measuring and Estimating Coupling Ratios in Memory Devices |
| US | | 60825913 | N/A | New Methods for Non-Volatile Memory |
| US | | 60825917 | N/A | Methods for Reducing Coupling Effect in Memory Devices |

| | | | | |
|----|--|----------|-----|---|
| US | | 60827067 | N/A | Methods for Mitigating Disturb Noise in Memory Devices |
| US | | 60862611 | N/A | A Method for High Speed Access to Multi-Level Memory Devices Using Variable Accuracy Programming |
| US | | 60862612 | N/A | Dynamic programming rate allocation for memory devices |
| US | | 60863480 | N/A | A Method to Combat Aging and Crosstalk in Flash Memory Devices |
| US | | 60863491 | N/A | Improved Programming Speed & reliability, by improvement the P&V |
| US | | 60863506 | N/A | Reading & Programming Methods in memory devices |
| US | | 60863810 | N/A | Methods for High Resolution Sampling and Feedback Codes in Memory Devices Feedback Codes (Re-submitted - 16 on 1/11/2006) |
| US | | 60865653 | N/A | High-speed interface |
| US | | 60865665 | N/A | Training sequences |
| US | | 60866071 | N/A | Improved Programming Cycle of Memory Devices |
| US | | 60866860 | N/A | Capacity Management in memory devices |
| US | | 60867204 | N/A | Architecture of high density, high performance memory devices |
| US | | 60867399 | N/A | Architecture of high density, high performance memory devices |

| | | | | |
|----|--|----------|-----|---|
| US | | 60867401 | N/A | Efficient Methods for Mitigating Disturb Noise in Memory Devices |
| US | | 60868342 | N/A | Methods to optimize memory devices structure using a Digital Signal Processor |
| US | | 60868549 | N/A | Methods to compensate on Sense Amplifier mismatch |
| US | | 60868731 | N/A | Method to improve memory devices testing |
| US | | 60870398 | N/A | Application Dependent Memory Device Interface |
| US | | 60870399 | N/A | Methods to improve memory devices latency |
| US | | 60871838 | N/A | Usage of Bad Blocks to Increase Capacity |
| US | | 60882240 | N/A | Memory device in which the size of the input and output pages is different than the actual capacity of a page |
| US | | 60883061 | N/A | An Extension to Memory Device |
| US | | 60883071 | N/A | Method for assessing memory capacity and optimizing memory utilization based on measuring the time periods between programming operations |
| US | | 60885024 | N/A | Method for Mitigating Errors in Memory Devices that Combines DSP and Analog Program and Verify Algorithms |
| US | | 60885987 | N/A | Combined Capacity Management and Coding Schemes for memory devices |

| | | | | |
|----|--|----------|-----|---|
| US | | 60886102 | N/A | Combined Interference Mitigation and Disturb Mitigation with Coding Schemes for Memory Devices |
| US | | 60886429 | N/A | Methods for Error Estimations in Memory Array |
| US | | 60886450 | N/A | Methods for Error Estimations in Memory Array |
| US | | 60888599 | N/A | Adaptive Step Pulse Programming Scheme for Memory Devices |
| US | | 60888828 | N/A | Parameter Optimization in memory devices |
| US | | 60889277 | N/A | Parameter Optimization in memory devices |
| US | | 60889279 | N/A | A detection device with a serial output |
| US | | 60891568 | N/A | Back Pattern Dependency Estimation |
| US | | 60891569 | N/A | Back Pattern Dependency Estimation |
| US | | 60892869 | N/A | Methods to Implement a Combined Interference Mitigation and Disturb Mitigation with Coding Schemes for Memory Devices |
| US | | 60893142 | N/A | Multi Level Read Algorithm |
| US | | 60894290 | N/A | Methods to Calculate the Optimized Thresholds for Reading Memory Devices |
| US | | 60894456 | N/A | Methods to Cancel Crosstalk in Memory Devices |
| US | | 60895746 | N/A | Reduce Power Peaks in Multi-Components Systems |

| | | | | |
|----|--|----------|-----|---|
| US | | 60895748 | N/A | Methods to Optimize ECC and EDC power and typical latency in memory |
| US | | 60896275 | N/A | Methods to Reduce Die Size Area of Memory Devices |
| US | | 60912056 | N/A | Command Set Extension for Memory Devices |
| US | | 60913281 | N/A | Command Set Extension for Memory Devices |
| US | | 60915540 | N/A | Reducing margins in voltage levels of memory devices |
| US | | 60915689 | N/A | Reducing margins in voltage levels of memory devices |
| US | | 60916877 | N/A | Bit Mappings for Multi Level Cells Memory Devices |
| US | | 60916888 | N/A | Reducing margins for the erased level in MLC memory devices |
| US | | 60917649 | N/A | Fragment Coding for Memory devices |
| US | | 60917651 | N/A | Performance Optimization method for systems accessed as slaves |
| US | | 60917652 | N/A | Efficient method for distinguishing between full and partial programmed memory |
| US | | 60917653 | N/A | Methods to Improve Memory Device Functionality |
| US | | 60938192 | N/A | Combating Back Pattern Dependency and Other Distortions in Flash Memory Devices Using Re-read with Modified Read Parameters |

| | | | | |
|----|--|----------|-----|--|
| US | | 60939076 | N/A | Cell Group Parameters Adjustments According Noise Margin |
| US | | 60939077 | N/A | Estimation and Calibration Methods for Memory Devices |
| US | | 60940404 | N/A | Bit Mappings for Multi Level Cells Memory Devices |
| US | | 60941673 | N/A | Memory Devices Using Non-Rectangular Cell Array |
| US | | 60943613 | N/A | Allocating and ordering of pages in MLC memory devices |
| US | | 60943745 | N/A | Detecting Number of Programmed Pages |
| US | | 60943843 | N/A | Power Reduction of Electronic Devices with Memory |
| US | | 60946218 | N/A | Protected Cells in MLC Memory Devices |
| US | | 60947427 | N/A | Improving the program and verify process of memory devices |
| US | | 60947428 | N/A | Improving programming speed of memory devices |
| US | | 60947970 | N/A | Interference mitigation using individual word line erasure operations |
| US | | 60948783 | N/A | Improving P&V Scheme |
| US | | 60948844 | N/A | Methods to calculate the optimal ISPP |
| US | | 60948995 | N/A | Allocation of multi level translation table |
| US | | 60949515 | N/A | Improved coding schemes for memory devices with non-uniform error rate |

| | | | | |
|----|--|----------|-----|--|
| US | | 60949891 | N/A | Methods to Improve DRAM performance |
| US | | 60950884 | N/A | Methods to calculate Soft Metrics from memory device cells |
| US | | 60951215 | N/A | Methods to calculate Soft Metrics from memory device cells |
| US | | 60952276 | N/A | Method for Programming Memory Devices that are Robust to Programming Disturbs |
| US | | 60952572 | N/A | Improved P&V Scheme to Reduce Cross-Talk Variance |
| US | | 60954010 | N/A | Improve Utilization of Redundancy & Spare Bits within Memory Devices |
| US | | 60954012 | N/A | Improve Utilization of Redundancy & Spare Bits within Memory Devices |
| US | | 60954013 | N/A | Memory Controller with Variable Redundancy Requirements |
| US | | 60954163 | N/A | Improve Read Throughput of Memory Device |
| US | | 60954169 | N/A | Methods for Preventing Program Errors in Memory Devices |
| US | | 60954317 | N/A | Method for Improving Programming Speed of Multi-Level Cell Memory Devices without Compromising Reliability |
| US | | 60956931 | N/A | Novel Algorithms for Distortion Estimations in Memory Devices |

| | | | | |
|----|--|----------|-----|--|
| US | | 60968317 | N/A | Method to decrease number of Errors in Flash memory devices in case of Binary Bit Mapping |
| US | | 60968656 | N/A | Methods to Ensure Specific Blocks in Memory Devices are Valid |
| US | | 60970058 | N/A | Method for Improving Programming Speed of Multi-Level Cell Memory Devices without Compromising Reliability |
| US | | 60971593 | N/A | A method to improve mitigation of failed memory programming |
| US | | 60971600 | N/A | An Interface between Memory Extension and Memory Controller |
| US | | 60973452 | N/A | Method for Combating Programming and Reading Memory Devices using Measurements of the Duration of Programming and Erase Operations |
| US | | 60973453 | N/A | Method for Programming Memory Devices |
| US | | 60976435 | N/A | Winding Geometry for Memory Device |
| US | | 60976436 | N/A | Additional Methods to Incorporate Signal Processing Module on Memory Devices |
| US | | 60978146 | N/A | A Method for Reliable Programming of Flash Devices in the Presence of Temperature Variations |
| US | | 60978767 | N/A | A method for generating random numbers using flash memory |

| | | | | |
|----|--|----------|-----|--|
| US | | 60978769 | N/A | A method for counting number of events and maintaining the counter in a memory |
| US | | 60981113 | N/A | A method for reading soft values from a memory device |
| US | | 60981114 | N/A | Estimate and Mitigate Disturbs and Coupling in Erased Level in Memory Devices |
| US | | 60981116 | N/A | Methods for Combating Voltage Shift In Memory Devices |
| US | | 60981117 | N/A | Methods for Combating Erase Failure In Memory Devices |
| US | | 60982480 | N/A | Methods for Combating Voltage Shift In Memory Devices |
| US | | 60983270 | N/A | Securing configuration commands to memory devices |
| US | | 60983272 | N/A | Methods for Combating Voltage Shift In Memory Devices |
| US | | 60983604 | N/A | Reverse Programming Method for Non-Volatile Memories |
| US | | 60983950 | N/A | Combined Coding and Program and Verify method |
| US | | 60985236 | N/A | Programming algorithm in MLC memory devices |
| US | | 60987106 | N/A | Adaptive Allocation of Reference Cells in Memory Devices |
| US | | 60987417 | N/A | Optimized Packing of Variable Capacity Memory Chips in a multi-chip Product |

| | | | | |
|----|--|----------|-----|--|
| US | | 60987632 | N/A | Methods to Reduce Power Peaks of a Memory Storage System |
| US | | 60989129 | N/A | Optimization of sampling in flash memories |
| US | | 60989812 | N/A | Method and Apparatus for Incremental Coding in Memory Devices |
| US | | 60991245 | N/A | Method to reduce number of read operations during erroneous event in Flash devices |
| US | | 60991246 | N/A | A method to adjust reading thresholds |
| US | | 61012424 | N/A | A Programming Scheme for Memory Devices |
| US | | 61012933 | N/A | A Programming Scheme for Memory Devices |
| US | | 61013027 | N/A | Method to efficiently perform random access read in Flash devices |
| US | | 61013032 | N/A | Method to efficiently cancel interference in Flash devices |
| US | | 61014048 | N/A | Programming Method for Multi-Plane Memory Device |
| US | | 61016566 | N/A | Method to efficiently perform random access read in Flash devices |
| US | | 61016568 | N/A | Cyclic Array of Blocks for File System Tables In Memory Devices |
| US | | 61016569 | N/A | Using Mirrored Blocks in Memory Devices |
| US | | 61016570 | N/A | Methods to Improve Read Throughput in the Event of Distortion Cancellation |

| | | | | |
|----|--|----------|-----|---|
| US | | 61016816 | N/A | A Memory Device with Indications to a Memory Controller |
| US | | 61016824 | N/A | Additional Methods to Calculate the Optimized Thresholds for Reading Memory Devices |
| US | | 61017177 | N/A | Additional Methods to Calculate the Optimized Thresholds for Reading Memory Devices |
| US | | 61022340 | N/A | Improving Program Throughput of a Memory Device |
| US | | 61022343 | N/A | MEMORY CELLS WITH NON-UNIFORM PROGRAMMING LEVELS |
| US | | 61022364 | N/A | Enhancement of Error correction code using random bit inversion |
| US | | 61024561 | N/A | Methods to Read Soft Values from Memory Device with minimal Throughput Penalty |
| US | | 61026150 | N/A | Using the parity check equations of an error correction code to estimate and track parameters |
| US | | 61026211 | N/A | Fast Cycling Level Estimation |
| US | | 61028226 | N/A | A Memory Device with Integrated Memory Buffer and Logic |
| US | | 61029428 | N/A | Indication of Cell Status within a Memory Device |
| US | | 61030240 | N/A | Open loop NVRAM programming for increasing write throughput |

| | | | | |
|----|--|----------|-----|--|
| US | | 61030972 | N/A | Method to reduce variance of FLASH cells after retention |
| US | | 61031711 | N/A | Method of Joint decoding in FLASH memories |
| US | | 61031712 | N/A | Open loop NVRAM programming for increasing write throughput |
| US | | 61034511 | N/A | Reading Combined Soft and Hard Information from Memory Devices |
| US | | 61037327 | N/A | Reduced Sense time for Flash Devices |
| US | | 61037328 | N/A | Enhancement of Error correction code using systematic bit inversions |
| US | | 61038758 | N/A | Temperature and Wear Level Estimation and Calibration |
| US | | 61039109 | N/A | Re-using Bad Blocks in Memory Devices |
| US | | 61039813 | N/A | Improving Iterative Decoding Using Added LLR Information |
| US | | 61040800 | N/A | Combined Replaced Cells Information into Distortion Estimation Procedure |
| US | | 61041600 | N/A | Combined Replaced Cells Information into Distortion Estimation Procedure |
| US | | 61043733 | N/A | Testing Procedure for a Memory System with Correction Capabilities |
| US | | 61043734 | N/A | Reducing the peak Power consumption of ECC decoders |
| US | | 61043736 | N/A | Reducing the average Power consumption of ECC decoders |

| | | | | |
|----|--|----------|-----|---|
| US | | 61045627 | N/A | Avoiding BPD errors due to temperature shift |
| US | | 61045628 | N/A | Methods for Combating Voltage Shift In Memory Devices |
| US | | 61046807 | N/A | A system with HDD and SSD |
| US | | 61046809 | N/A | A method to improve HDD Operation |
| US | | 61048191 | N/A | Wear level estimation for Flash devices |
| US | | 61048558 | N/A | Efficient Implementation of Program-After-Erase in Memory Devices |
| US | | 61048669 | N/A | A method for adaptively adjusting PV levels of the memory devices |
| US | | 61052276 | N/A | Method of Hybrid decoding in FLASH memories |
| US | | 61053027 | N/A | Wear level estimation for Flash devices |
| US | | 61053029 | N/A | Efficient Implementation of Program-After-Erase in Memory Devices |
| US | | 61053030 | N/A | A method for adaptively adjusting PV levels of the memory devices |
| US | | 61053031 | N/A | Method of Hybrid decoding in FLASH memories |
| US | | 61054493 | N/A | A New Programming Scheme for Memory Devices |
| US | | 61056488 | N/A | Adaptive Program parameters for Flash devices |
| US | | 61057827 | N/A | Method to calculate interference for memory device cells |

| | | | | |
|----|--|----------|-----|--|
| US | | 61060486 | N/A | Synchronization among storage devices in a RAID SSD system |
| US | | 61061685 | N/A | Optimized Syndrome calculation for BCH decoders |
| US | | 61061689 | N/A | Memory Devices Using Non-Rectangular Cell Array |
| US | | 61074643 | N/A | Memory block sorting based on usage |
| US | | 61074644 | N/A | Battery operated flash module |
| US | | 61076160 | N/A | A New Programming Scheme for Memory Devices |
| US | | 61076161 | N/A | Memory block sorting based on usage |
| US | | 61076163 | N/A | Battery operated flash module |
| US | | 61076192 | N/A | Programming the USB to MSB levels |
| US | | 61076647 | N/A | Fast Recovery from Erase Failures |
| US | | 61076745 | N/A | Modified Erase Verify Procedure |
| US | | 61076748 | N/A | Using Bad Blocks List to Enlarge the Redundant Block List |
| US | | 61077182 | N/A | Use of SLC area to improve read performance while performing XT cancellation |
| US | | 61077183 | N/A | Marking Erased Sectors in the Binary Cache |
| US | | 61078405 | N/A | Improved Read Performance of MLC Blocks using Binary Cache Method and XTALK Cancellation |

| | | | | |
|----|--|----------|-----|--|
| US | | 61078777 | N/A | Multi-Plane Internal Copy Back using Uncoupled Pages |
| US | | 61078778 | N/A | Improved Read Performance of MLC Blocks using Binary Cache Method and XTALK Cancellation |
| US | | 61078780 | N/A | A method for a memory controller to read at thresholds outside memory device boundaries |
| US | | 61078782 | N/A | A method for a MLC memory device controller to restore data from mixed levels |
| US | | 61079140 | N/A | Insertion of Gaps in Binary Cache for non Programmed Pages |
| US | | 61079141 | N/A | Using Snapshots in the Binary Cache for Faster Recovery Time |
| US | | 61080877 | N/A | Modified Erase Verify Procedure |
| US | | 61081047 | N/A | Using Snapshots in the Binary Cache for Faster Recovery Time |
| US | | 61082231 | N/A | Binary Cache Configuration for Enhancing Programming Performance |
| US | | 61082233 | N/A | Multi-Plane Internal Copy Back using Uncoupled Pages |
| US | | 61086164 | N/A | A method for efficient data recovery of multi-bit per cell memory devices during power failure |
| US | | 61086225 | N/A | Program & Read parameters change for Memory devices |

| | | | | |
|----|--|----------|-----|--|
| US | | 61086541 | N/A | A method for efficient data recovery of multi-bit per cell memory devices during power failure |
| US | | 61093334 | N/A | Joint Programming Schemes for Memory Devices |
| US | | 61093366 | N/A | Modified Erase Verify Procedure |
| US | | 61093367 | N/A | Multi-Plane Internal Copy Back using Uncoupled Pages |
| US | | 61093368 | N/A | Using Bad Blocks List to Enlarge the Redundant Block List |
| US | | 61093369 | N/A | Modified Erase Verify Procedure |
| US | | 61093461 | N/A | A method for efficient data recovery of multi-bit per cell memory devices during power failure |
| US | | 61093578 | N/A | Using bad blocks in SSD |
| US | | 61093596 | N/A | Battery operated flash module |
| US | | 61093610 | N/A | SSD Curing |
| US | | 61093613 | N/A | ECC segmentation |
| US | | 61093621 | N/A | Sequential and random partition |
| US | | 61093632 | N/A | Local flash curing |
| US | | 61093722 | N/A | Method for forecasting flash condition |
| US | | 61093723 | N/A | Best available block metric |
| US | | 61093724 | N/A | SSD Flash module |
| US | | 61093727 | N/A | Diagnosis through Life Time and Self Healing Memory Device |

| | | | | |
|----|--|----------|-----|--|
| US | | 61094066 | N/A | Chip level fail recovery on SSD |
| US | | 61094417 | N/A | Global Wear Leveling for Memory Devices |
| US | | 61096805 | N/A | Methods to calculate the optimal ISPP |
| US | | 61096806 | N/A | Peak Sample & Jump method |
| US | | 61096807 | N/A | Method for Saving SSD and Memory Devices Power |
| US | | 61096808 | N/A | Power Efficient Method for Refreshing Memory |
| US | | 61097224 | N/A | Faster Programming method |
| US | | 61098829 | N/A | Improved Copy Back Procedure |
| US | | 61105454 | N/A | Chien Search Using Serial Multipliers |
| US | | 61105580 | N/A | Using Low-Speed Random Access Device To Protect Data Stored in High-Speed Random Access Device |
| US | | 61105580 | N/A | Methods for Error Correction in Storage Systems |
| US | | 61105630 | N/A | Endurance improvement of flash memories in a file system environment |
| US | | 61105814 | N/A | Usage of Binary Cache in a Multi-Die Memory System |
| US | | 61105816 | N/A | A Method to Handle Program Failure Cases |
| US | | 61105818 | N/A | Improving Capacity, endurance and reliability of solid-state disks |

| | | | | |
|----|--|----------|-----|--|
| US | | 61105819 | N/A | Method for combating retention errors during un-plugged storage of memory devices |
| US | | 61109767 | N/A | Methods to Generate Scrambler Seed in memory devices |
| US | | 61112195 | N/A | Efficient raid implementation |
| US | | 61114473 | N/A | Optimized Encoder supporting multiple cyclic codes |
| US | | 61115085 | N/A | A method for equal-division of cells among levels for improving read performance |
| US | | 61115086 | N/A | Storing M bits/cell using an N bits/cell device, where $N < M$ |
| US | | 61118630 | N/A | Modified Erase Verify Procedure |
| US | | 61118632 | N/A | A Method to Handle Program Failure Cases |
| US | | 61119929 | N/A | Co-existence and cooperation between on-memory and external signal processing algorithms to combat memory cell impairments |
| US | | 61119950 | N/A | Page Reordering method to improve read performance while performing XT cancellation or acquisition |
| US | | 61120968 | N/A | Flash Reliable Mode |
| US | | 61120980 | N/A | Refresh mechanism for non-volatile memories using Re-programming of the same page |
| US | | 61120987 | N/A | Method to reduce number of Erasures in NAND device |

| | | | | |
|----|--|----------|-----|--|
| US | | 61141830 | N/A | A Memory Device Interface with Additional Commands |
| US | | 61141842 | N/A | A method for overhauling SSD and non-volatile memory devices |
| US | | 61141855 | N/A | Wider Programming for upper level for Flash devices |
| US | | 61141866 | N/A | Dynamic Over-Provisioning Algorithm that can Improve the Reliability of Memory Devices |
| US | | 61144629 | N/A | Methods for storing M bits/cell using an N bits/cell device, where $N < M$ |
| US | | 61145562 | N/A | Hierarchal Storage Device Management System |
| US | | 61145974 | N/A | Randomizing data in hard drive |
| US | | 61151189 | N/A | Flash solid state disk dynamic power management |
| US | | 61152073 | N/A | Cooperative power management in a multiple flash SSD device |
| US | | 61156520 | N/A | Memory Device with Adjustable & Adaptive Verify Scheme |
| US | | 61157599 | N/A | Enhanced Control over Flash Partial Blocks |
| US | | 61158374 | N/A | Method of Joint decoding in FLASH memories |
| US | | 61162310 | N/A | Method to Improve Program Reliability for Multi Level NAND devices |
| US | | 61163129 | N/A | Reduction of Program Errors using XT Procedure |

| | | | | |
|----|--|----------|-----|--|
| US | | 61163133 | N/A | Memory Controller with External DRAM Capabilities |
| US | | 61163138 | N/A | Flash Read Threshold DataBase operation |
| US | | 61163146 | N/A | Bit Reversal metric for iterative decoders |
| US | | 61168604 | N/A | Improved re-Program operation |
| US | | 61168605 | N/A | Methods for Efficient Copy from Binary Cache to MLC Area in Memory Devices |
| US | | 61171089 | N/A | SSD rapid format |
| US | | 61171092 | N/A | Drive locking |
| US | | 61172833 | N/A | Improved Soft Sample Operation in Non-Volatile Memory |
| US | | 61175030 | N/A | A Method for Optimal Thresholds Estimation |
| US | | 61176949 | N/A | Utilizing SLC Cache scheme in a Memory Device |
| US | | 61180156 | N/A | Reduce System Overhead during Read Operation from Memory Device |
| US | | 61181678 | N/A | Higher Program Voltage for special SLC Word Lines |
| US | | 61182763 | N/A | Varying verify bias during PV process |
| US | | 61187676 | N/A | Improving Memory Device Operation by Varying Vpass |
| US | | 61218080 | N/A | Improving Memory Device Operation by Varying Vpass |
| US | | 61221582 | N/A | Chien Search Using Multiple basis representation |

| | | | | |
|----|--|----------|-----|--|
| US | | 61224897 | N/A | Dynamic allocation of SLC/MLC according to estimated heat distribution |
| US | | 61225929 | N/A | Programming the USB to MSB levels |
| US | | 61229780 | N/A | Allocating blocks for testing and monitoring |
| US | | 61229788 | N/A | Design of Rate Compatible codes |
| US | | 61229793 | N/A | Efficient Interference coefficient measurement |
| US | | 61230127 | N/A | Handling Program Failure Cases |
| US | | 61234688 | N/A | Systems and method for curing element in memory element array |
| US | | 61234695 | N/A | Using a memory device with Fast and Enhanced read modes |
| US | | 61234699 | N/A | Efficient Decoding of Error Correction Codes (ECC) |
| US | | 61240280 | N/A | NAND block Unified conditioning |
| US | | 61243726 | N/A | Memory Device Curing |
| US | | 61244493 | N/A | SSD Flash module |
| US | | 61244500 | N/A | Diagnosis through Life Time and Self Healing Memory Device |
| US | | 61244506 | N/A | Joint Programming Schemes for Memory Devices |
| US | | 61246999 | N/A | Improve Program Throughput by reordering pages |
| US | | 61248915 | N/A | Chien Search Latency reduction |

| | | | | |
|----|--|----------|-----|--|
| US | | 61251787 | N/A | Methods for estimating block's condition during operation time |
| US | | 61251807 | N/A | Encoding the modulo 2 sum of different pages in a flash device in order to decrease the probability of page failures |
| US | | 61251829 | N/A | Hard LDPC Bit Flipping Decoding Using 2 Bits For Every Information Node |
| US | | 61251836 | N/A | Efficient End To End Data Protection Method in Flash Storage Systems |
| US | | 61256200 | N/A | Reduce Read thresholds sets |
| US | | 61262568 | N/A | A Method for Measuring Read Disturb |
| US | | 61263836 | N/A | Method of maintaining quality of service for Random Access Memories Perfect Bank DRAM |
| US | | 61263859 | N/A | Interleaved ECC method for Random Access Memories |
| US | | 61264673 | N/A | Efficient readout schemes for analog memory cell devices |
| US | | 61264809 | N/A | LLR Unit Architecture |
| US | | 61265763 | N/A | Wordline Issue |
| US | | 61286814 | N/A | SSD – Read and Write performance balancing |
| US | | 61290547 | N/A | Method of data compression for flash based storage devices |
| US | | 61290552 | N/A | Offline methods of data compression for flash based storage devices |

| | | | | |
|----|--|----------|-----|--|
| US | | 61290559 | N/A | Accelerated data programming method for flash devices |
| US | | 61292229 | N/A | Recipe Command & Status |
| US | | 61293676 | N/A | Hibernation Storage Area Usage for Over Provisioning during Activity Time |
| US | | 61293808 | N/A | Recovery from memory device failure using redundancy |
| US | | 61293814 | N/A | Method for error correction using remote data storage |
| US | | 61294498 | N/A | Varying verify bias during PV process |
| US | | 61301302 | N/A | Termination criteria for iterative decoders |
| US | | 61303415 | N/A | LDPC code design for optimized performance |
| US | | 61324429 | N/A | Reuse of host hibernation storage space by memory controller |
| US | | 61326269 | N/A | Special read commands for Efficient interference cancellation and soft ECC decoding for memory devices |
| US | | 61326858 | N/A | special areas - v1 |
| US | | 61330961 | N/A | Improved Soft Sample Operation in Non-Volatile Memory |
| US | | 61330970 | N/A | Special read commands for Efficient interference cancellation and soft ECC decoding for memory devices |

| | | | | |
|----|--|----------|-----|---|
| US | | 61330989 | N/A | Efficient copy and program commands with an option to stop/ resume or to break long operations to short steps |
| US | | 61334606 | N/A | Adaptive over- provisioning in memory systems |
| US | | 61356521 | N/A | sending address after data while programming NAND FLASH. |
| US | | 61357114 | N/A | Current Peaks Smoothing |
| US | | 61358970 | N/A | Constant Bit Rate Streaming Command for Storage Systems |
| US | | 61361458 | N/A | Determining read threshold sets and optimizing their usage |
| US | | 61361946 | N/A | Pipeline Management SSD |
| US | | 61363248 | N/A | Shaping Methods for Combating Voltage Range Degradation Due to Shift Effects In Memory Arrays |
| US | | 61363655 | N/A | Handling power failures and program failures in memory devices |
| US | | 61364198 | N/A | NAND Soft Read Cache |
| US | | 61364406 | N/A | Redundant data storage in multi die memory system |
| US | | 61367894 | N/A | Read and Write Cache in hybrid drives |
| US | | 61369667 | N/A | Program non integer bits per cell across wordlines |
| US | | 61369719 | N/A | Avoid selecting last punched block |

| | | | | |
|----|--|----------|-----|--|
| US | | 61369764 | N/A | Codes for multi-die redundancy |
| US | | 61370817 | N/A | High Endurance Cache in Flash Memory Devices |
| US | | 61372913 | N/A | Combating the cell to cell interference to erased cells |
| US | | 61372921 | N/A | Combating the cell to cell interference to erased cells |
| US | | 61373883 | N/A | Redundant data storage in multi die memory system |
| US | | 61374377 | N/A | Soft ECC Direction |
| US | | 61380233 | N/A | A method for fast programming of NAND memory devices in a manner that reduces voltage shifts of erased cells |
| US | | 61386570 | N/A | Optimization of Hybrid Disk performance |
| US | | 61386633 | N/A | NAND block Unified conditioning |
| US | | 61390193 | N/A | Special read commands for Efficient interference cancellation and soft ECC decoding for memory devices |
| US | | 61406610 | N/A | NAND Soft Read Cache |
| US | | 61408659 | N/A | Battery-less SSD that is Robust to Power Failures and Holds Variables in RAM |
| US | | 61417218 | N/A | Differential Level Programming |
| US | | 61417315 | N/A | Shaping Methods for Combating Voltage Range Degradation Due to Shift Effects In Memory Arrays |

| | | | | |
|----|--|----------|-----|---|
| US | | 61417429 | N/A | NV memory system optimizations |
| US | | 61417433 | N/A | NV memory system optimizations |
| US | | 61419922 | N/A | Bootable PCIe-connected memory or storage computer device |
| US | | 61426542 | N/A | Combinations of NVRAM and DRAM systems |
| US | | 61431442 | N/A | protecting boot data against reflow and read disturb |
| US | | 61431444 | N/A | Unified Flash and RAM |
| US | | 61432219 | N/A | Data-Out Prediction and Pre Fetching in Bridged High Rate Systems |
| US | | 61435307 | N/A | NVRAM partition |
| US | | 61436606 | N/A | Use of Spare blocks for SLC cache |
| US | | 61436619 | N/A | Verifying Program Operation |
| US | | 61440867 | N/A | Recovery from Bit flip in memory system |
| US | | 61440868 | N/A | Structured data mapping |
| US | | 61442252 | N/A | Memory Protection Against WL Failure |
| US | | 61447111 | N/A | Incremental redundancy codes |
| US | | 61447113 | N/A | Adaptive memory partition between units |
| US | | 61448201 | N/A | Storage device with sideband interface for boot |
| US | | 61454584 | N/A | Management Parity LBA separately partition |

| | | | | |
|----|--|----------|-----|---|
| US | | 61454599 | N/A | A storage system that exports multiple disk interface |
| US | | 61466941 | N/A | MCP eMMC |
| US | | 61469854 | N/A | Interference mitigation using individual word line erasure operations |
| US | | 61471257 | N/A | Serial PPN |
| US | | 61472203 | N/A | Memory system running scripts |
| US | | 61472629 | N/A | Low Power SERDES interface |
| US | | 61475241 | N/A | data storage in analog memory cells using a non-integer number of bits per cell |
| US | | 61476287 | N/A | SAS Target Performance optimizations |
| US | | 61482213 | N/A | Provisional: LDPC Decoders interaction |
| US | | 61482216 | N/A | Provisional: LDPC Double rate soft decoder |
| US | | 61486284 | N/A | NAND LSB pages utilization |
| US | | 61486330 | N/A | Sparse Programming Method |
| US | | 61486341 | N/A | Advanced Programming Methods |
| US | | 61494916 | N/A | Dual FTL |
| US | | 61497074 | N/A | Cache block garbage collection |
| US | | 61528771 | N/A | SAS Target Performance optimizations |
| US | | 61529267 | N/A | Codes for multi-die redundancy |
| US | | 61529938 | N/A | Provisional-Page mode FTL tables in SLC |

| | | | | |
|----|--|------------|-----------------|---|
| US | | 61534389 | N/A | IPR Proposals |
| US | | 61536597 | N/A | Using dynamic mapping for die balancing in solid state drives |
| US | | 61536598 | N/A | Selective secure erase in solid state drives |
| US | | 61537144 | N/A | Optimized decoding of linear codes |
| US | | 61543813 | N/A | Single Event Upset Protection in Cache Memories |
| US | | 61557428 | N/A | Efficient Programming schemes to protect data from power failure during programming |
| US | | 12/880,101 | Non-Publication | REUSE OF HOST HIBERNATION STORAGE SPACE BY MEMORY CONTROLLER |
| US | | 12/963,649 | Non-Publication | Memory Management Schemes for Non-Volatile Memory Devices |
| US | | 12/987,174 | Non-Publication | Redundant data storage in multi-die memory systems |
| US | | 12/987,175 | Non-Publication | Redundant data storage in multi-die memory systems |
| US | | 13/021,754 | Non-Publication | Reducing Peak Current in Memory Systems |
| US | | 13/047,822 | Non-Publication | Data Storage Commands with Data Preceding Address |
| US | | 13/170,202 | Non-Publication | ESTIMATION OF MEMORY CELL READ THRESHOLDS BY SAMPLING INSIDE PROGRAMMING LEVEL DISTRIBUTION INTERVALS |

| | | | | |
|----|-----------|------------|-----------------|--|
| US | | 13/171,467 | Non-Publication | Efficient Selection of Memory Blocks for Compaction |
| US | | 13/192,495 | Non-Publication | Data storage at a non-integer number of bits per cell |
| US | | 13/192,504 | Non-Publication | Interference mitigation in analog memory cells using individual word line erasure operations |
| US | | 13/284,913 | 20120044762 | REJUVENATION OF ANALOG MEMORY CELLS |
| US | 7,924,648 | 11/945,575 | 20080126686 | MEMORY POWER AND PERFORMANCE MANAGEMENT |
| US | 7,706,182 | 11/949,135 | 20080130341 | ADAPTIVE PROGRAMMING OF ANALOG MEMORY CELLS |
| US | 7,900,102 | 11/957,970 | 20080148115 | HIGH-SPEED PROGRAMMING OF MEMORY DEVICES |
| US | 7,593,263 | 11/958,011 | 20080158958 | MEMORY DEVICE WITH REDUCED READING LATENCY |
| US | 8,005,086 | 11/995,801 | 20080198650 | Distortion estimation and cancellation in memory devices |
| US | 7,821,826 | 11/995,805 | 20100110787 | MEMORY CELL READOUT USING SUCCESSIVE APPROXIMATION |
| US | 7,697,326 | 11/995,806 | 20090103358 | REDUCING PROGRAMMING ERROR IN MEMORY DEVICES |
| US | 7,466,575 | 11/995,811 | 20080198652 | MEMORY DEVICE PROGRAMMING USING COMBINED SHAPING AND LINEAR SPREADING |
| US | 8,151,163 | 11/995,812 | 20100115376 | AUTOMATIC DEFECT MANAGEMENT IN MEMORY DEVICES |

| | | | | |
|----|-----------|------------|-----------------|--|
| US | 8,060,806 | 11/995,813 | US20100131826 | ESTIMATION OF NON-LINEAR DISTORTION IN MEMORY DEVICES |
| US | 7,975,192 | 11/995,814 | US20100165730 | READING MEMORY CELLS USING MULTIPLE THRESHOLDS |
| US | 8,156,403 | 11/996,054 | 20090024905 | COMBINED DISTORTION ESTIMATION AND ERROR CORRECTION CODING FOR MEMORY DEVICES |
| US | 7,751,240 | 12/019,011 | 20080181001 | MEMORY DEVICE WITH NEGATIVE READ THRESHOLDS |
| US | 8,151,166 | 12/037,487 | 20080219050 | REDUCTION OF BACK PATTERN DEPENDENCY EFFECTS IN MEMORY DEVICES |
| US | 8,001,320 | 12/045,520 | 20080263262 | COMMAND INTERFACE FOR MEMORY DEVICES |
| US | | 12/063,544 | 20100157641 | MEMORY DEVICE WITH ADAPTIVE CAPACITY |
| US | | 12/119,069 | 20080282106 | DATA STORAGE WITH INCREMENTAL REDUNDANCY |
| US | 7,925,936 | 12/171,797 | Non-Publication | MEMORY DEVICE WITH NON-UNIFORM PROGRAMMING LEVELS |
| US | 8,068,360 | 12/178,318 | 20090106485 | READING ANALOG MEMORY CELLS USING BUILT-IN MULTI-THRESHOLD COMMANDS |
| US | | 12/186,867 | 20090043951 | PROGRAMMING SCHEMES FOR MULTI-LEVEL ANALOG MEMORY CELLS |
| US | 7,773,413 | 12/245,749 | 20090091979 | RELIABLE DATA STORAGE IN ANALOG MEMORY CELLS IN THE PRESENCE OF TEMPERATURE VARIATIONS |

| | | | | |
|----|-----------|------------|-----------------|--|
| US | 8,000,141 | 12/251,471 | Non-Publication | COMPENSATION FOR VOLTAGE DRIFTS IN ANALOG MEMORY CELLS |
| US | | 12/323,544 | 20090144600 | EFFICIENT RE-READ OPERATIONS IN ANALOG MEMORY CELL ARRAYS |
| US | | 12/332,368 | 20090158126 | EFFICIENT INTERFERENCE CANCELLATION IN ANALOG MEMORY CELL ARRAYS |
| US | | 12/332,370 | 20090157964 | EFFICIENT DATA STORAGE IN MULTI-PLANE MEMORY DEVICES |
| US | 8,085,586 | 12/344,233 | 20090168524 | WEAR LEVEL ESTIMATION IN ANALOG MEMORY CELLS |
| US | | 12/355,817 | 20090187803 | DECODING OF ERROR CORRECTION CODE USING PARTIAL BIT INVERSION |
| US | 8,156,398 | 12/364,531 | 20090199074 | PARAMETER ESTIMATION BASED ON ERROR CORRECTION CODE PARITY CHECK EQUATIONS |
| US | 7,924,587 | 12/388,528 | 20090213653 | programming of analog memory cells using a single programming pulse per state transition |
| US | 7,864,573 | 12/390,522 | 20090213654 | Programming analog memory cells for reduced variance after retention |
| US | | 12/397,368 | 20090228761 | EFFICIENT READOUT FROM ANALOG MEMORY CELLS USING DATA COMPRESSION |
| US | 8,059,457 | 12/405,275 | 20090240872 | MEMORY DEVICE WITH MULTIPLE-ACCURACY READ COMMANDS |
| US | | 12/419,304 | Non-Publication | HIGH-PERFORMANCE ECC DECODER |

| | | | | |
|----|-----------|------------|-----------------|---|
| US | 7,924,613 | 12/497,707 | Non-Publication | DATA STORAGE IN ANALOG MEMORY CELLS WITH PROTECTION AGAINST PROGRAMMING INTERRUPTION |
| US | | 12/522,175 | 20100091535 | ADAPTIVE ESTIMATION OF MEMORY CELL READ THRESHOLDS |
| US | | 12/534,893 | Non-Publication | IMPROVED DATA STORAGE IN ANALOG MEMORY CELLS USING MODIFIED PASS VOLTAGES |
| US | 7,995,388 | 12/534,898 | Non-Publication | DATA STORAGE USING MODIFIED VOLTAGES |
| US | 8,169,825 | 12/551,567 | Non-Publication | RELIABLE DATA STORAGE IN ANALOG MEMORY CELLS SUBJECTED TO LONG RETENTION PERIODS |
| US | | 12/551,583 | Non-Publication | SEGMENTED DATA STORAGE |
| US | 8,000,135 | 12/558,528 | Non-Publication | ESTIMATION OF MEMORY CELL READ THRESHOLDS BY SAMPLING INSIDE PROGRAMMING LEVEL DISTRIBUTION INTERVALS |
| US | | 12/579,430 | Non-Publication | EFFICIENT PROGRAMMING OF ANALOG MEMORY CELL DEVICES |
| US | | 12/579,432 | Non-Publication | EFFICIENT DATA STORAGE IN STORAGE DEVICE ARRAYS |
| US | | 12/597,494 | 20100131827A1 | MEMORY DEVICE WITH INTERNAL SIGNAL PROCESSING UNIT |
| US | | 12/607,078 | Non-Publication | DATA SCRAMBLING IN MEMORY DEVICES |
| US | | 12/607,085 | Non-Publication | DATA SCRAMBLING SCHEMES FOR MEMORY DEVICES |

| | | | | |
|----|-----------|------------|-----------------|---|
| US | | 12/616,151 | Non-Publication | CONFIGURABLE ENCODER FOR CYCLIC ERROR CORRECTION CODES |
| US | | 12/618,732 | 20100124088-A1 | STORAGE AT M BITS/CELL DENSITY IN N BITS/CELL ANALOG MEMORY CELL DEVICES, M>N |
| US | | 12/649,358 | Non-Publication | EFFICIENT READOUT SCHEMES FOR ANALOG MEMORY CELL DEVICES |
| US | 8,174,857 | 12/649,360 | Non-Publication | EFFICIENT READOUT SCHEMES FOR ANALOG MEMORY CELL DEVICES USING MULTIPLE READ THRESHOLD SETS |
| US | | 12/649,382 | 20100165689 | REJUVENATION OF ANALOG MEMORY CELLS |
| US | | 12/677,114 | 20100199150 | DATA STORAGE IN ANALOG MEMORY CELL ARRAYS HAVING ERASE FAILURES |
| US | | 12/680,901 | 20100220510 | OPTIMIZED SELECTION OF MEMORY UNITS IN MULTI-UNIT MEMORY DEVICES |
| US | | 12/688,883 | Non-Publication | HIERARCHICAL DATA STORAGE SYSTEM |
| US | | 12/714,501 | 20100220509 | SELECTIVE ACTIVATION OF PROGRAMMING SCHEMES IN ANALOG MEMORY CELL ARRAYS |
| US | 8,174,905 | 12/721,585 | 20100157675 | PROGRAMMING ORDERS FOR REDUCING DISTORTION IN ARRAYS OF MULTI-LEVEL ANALOG MEMORY CELLS |
| US | | 12/728,287 | 20100250836 | USE OF HOST SYSTEM RESOURCES BY MEMORY CONTROLLER |
| US | | 12/728,289 | Non-Publication | Dual ECC decoder |

| | | | | |
|----|-----------|------------|-----------------|--|
| US | | 12/728,296 | Non-Publication | DATABASE OF MEMORY READ THRESHOLDS |
| US | | 12/758,003 | Non-Publication | Selective re-programming of analog memory cells |
| US | 7,881,107 | 12/758,044 | 20100195390 | MEMORY DEVICE WITH NEGATIVE READ THRESHOLDS |
| US | | 12/797,615 | 20100332955A1 | Chien search using multiple basis representation |
| US | | 12/822,207 | Non-Publication | ADAPTIVE OVER-PROVISIONING IN MEMORY SYSTEMS |
| US | | 12/843,029 | Non-Publication | Efficient LDPC codes |
| US | | 12/876,170 | Non-Publication | EFFICIENT STORAGE OF ERROR CORRECTION INFORMATION IN DRAM |
| US | | 12/890,724 | Non-Publication | ERROR CORRECTION CODING OVER MULTIPLE MEMORY PAGES |
| US | | 12/913,815 | Non-Publication | Termination Criteria for Iterative Decoders |
| US | | 13/069,406 | Non-Publication | Cache memory for hybrid disk drives |
| US | | 13/088,361 | Non-Publication | Read commands for reading interfering memory cells |
| US | 8,145,984 | 13/114,049 | US20110225472A1 | READING MEMORY CELLS USING MULTIPLE THRESHOLDS |
| US | | 13/171,761 | Non-Publication | Interference-aware assignment of programming levels in analog memory cells |
| US | | 13/192,501 | Non-Publication | Data storage at a non-integer number of bits per cell |
| US | | 13/195,852 | Non-Publication | Read threshold setting based on soft readout statistics |

| | | | | |
|----|--|------------|-----------------|--|
| US | | 13/214,257 | Non-Publication | MEMORY DEVICE WITH MULTIPLE-ACCURACY READ COMMANDS |
| US | | 13/231,963 | Non-Publication | Memory Management For Unifying Memory Cell Conditions |
| US | | 13/239,408 | 20120026788 | Distortion estimation and cancellation in memory devices |
| US | | 13/239,411 | 20120026789 | Distortion estimation and cancellation in memory devices |
| US | | 13/284,909 | Non-Publication | MEMORY DEVICE WITH MULTIPLE-ACCURACY READ COMMANDS |
| US | | 13/338,335 | Non-Publication | Sparse programming of Analog Memory Celles |
| US | | 13/355,536 | Non-Publication | Block Management Schemes in Hybrid SLC/MLC Memory |
| US | | 13/356,694 | Non-Publication | Advanced Programming Verification Schemes for Analog Memory Cells |
| US | | 13/371,443 | Non-Publication | Protection Against Word Line Failure in Memory Devices |
| US | | 13/405,308 | N/A | Error Correction Codes for Incremental Redundancy |
| US | | 13/405,309 | N/A | AUTOMATIC DEFECT MANAGEMENT IN MEMORY DEVICES |
| US | | 13/412,731 | N/A | Programming orders for reducing distortion based on neighboring rows |
| US | | 13/412,780 | N/A | Reducing distortion using joint storage |

| | | | | |
|-----|--|-------------------|----------------|---|
| US | | 13/419,452 | N/A | Independent Management of Data and Parity Logical Block Addresses |
| US | | 13/419,453 | N/A | Storage System Exporting Internal Storage Rules |
| US | | 13/426,799 | N/A | Selective Date Storage in LSB and MSB Pages |
| US | | 13/429,385 | N/A | Redundant Storage in Non-Volatile Memory by Storing Redundancy Information in Volatile Memory |
| US | | 13/439,860 | N/A | Efficient connection management in a SAS target |
| US | | 13/439,863 | N/A | High-performance SAS target |
| US | | 13/471,483 | N/A | ENHANCED PROGRAMMING AND ERASURE SCHEMES FOR ANALOG MEMORY CELLS |
| US | | 13/471,484 | N/A | PROGRAMMING AND ERASURE SCHEMES FOR ANALOG MEMORY CELLS |
| PCT | | PCT/IB2012/052375 | N/A | Sparse programming of Analog Memory Cells |
| PCT | | PCT/IB2012/052376 | N/A | Selective Date Storage in LSB and MSB Pages |
| PCT | | PCT/IL2007/000575 | WO 2007/132452 | REDUCING PROGRAMMING ERROR IN MEMORY DEVICES |
| PCT | | PCT/IL2007/000576 | WO 2007/132453 | Distortion estimation and cancellation in memory devices |
| PCT | | PCT/IL2007/000579 | WO 2007/132456 | MEMORY DEVICE WITH ADAPTIVE CAPACITY |
| PCT | | PCT/IL2007/000580 | WO 2007/132457 | COMBINED DISTORTION ESTIMATION AND ERROR CORRECTION CODING FOR MEMORY DEVICES |

| | | | | |
|-----|--|----------------------------------|----------------|---|
| PCT | | PCT/IL2007/000581 | WO 2007/132458 | MEMORY DEVICE PROGRAMMING USING COMBINED SHAPING AND LINEAR SPREADING |
| PCT | | PCT/IL2007/001059 | WO 2008/026203 | ESTIMATION OF NON-LINEAR DISTORTION IN MEMORY DEVICES |
| PCT | | PCT/IL2007/001315 | WO 2008/053472 | READING MEMORY CELLS USING MULTIPLE THRESHOLDS |
| PCT | | PCT/IL2007/001316 | WO 2008/053473 | MEMORY CELL READOUT USING SUCCESSIVE APPROXIMATION |
| PCT | | PCT/IL2007/001488 | WO 2008/068747 | AUTOMATIC DEFECT MANAGEMENT IN MEMORY DEVICES |
| PCT | | PCT/IL2008/000176 (Cancelled) | N/A | MEMORY DEVICE WITH NON-UNIFORM PROGRAMMING LEVELS |
| PCT | | PCT/IL2008/000329 | WO 2008/111058 | ADAPTIVE ESTIMATION OF MEMORY CELL READ THRESHOLDS |
| PCT | | PCT/IL2008/000519 | WO 2008/139441 | MEMORY DEVICE WITH INTERNAL SIGNAL PROCESSING UNIT |
| PCT | | PCT/IL2008/001188 | WO/2009/037691 | PROGRAMMING ORDERS FOR REDUCING DISTORTION IN ARRAYS OF MULTI-LEVEL ANALOG MEMORY CELLS |
| PCT | | PCT/IL2008/001356 | WO/2009/050703 | DATA STORAGE IN ANALOG MEMORY CELL ARRAYS HAVING ERASE FAILURES |
| PCT | | PCT/IL2008/001446 | WO/2009/063450 | OPTIMIZED SELECTION OF MEMORY UNITS IN MULTI-UNIT MEMORY DEVICES |

| | | | | |
|----|--|-------------------|--------------|---|
| KR | | 10-2008-7028793 | N/A | COMBINED DISTORTION ESTIMATION AND ERROR CORRECTION CODING FOR MEMORY DEVICES |
| KR | | 10-2008-7028919 | N/A | MEMORY DEVICE WITH ADAPTIVE CAPACITY |
| KR | | 10-2008-7029297 | N/A | Distortion estimation and cancellation in memory devices |
| KR | | 10-2010-7006449 | N/A | OPTIMIZED SELECTION OF MEMORY UNITS IN MULTI-UNIT MEMORY DEVICES |
| JP | | 2009-508668 | N/A | MEMORY DEVICE WITH ADAPTIVE CAPACITY |
| JP | | 20090318085550-m1 | N/A | COMBINED DISTORTION ESTIMATION AND ERROR CORRECTION CODING FOR MEMORY DEVICES |
| CN | | 200780026181.3 | CN101512661A | COMBINED DISTORTION ESTIMATION AND ERROR CORRECTION CODING FOR MEMORY DEVICES |
| CN | | 200880005741.1 | CN101715595A | ADAPTIVE ESTIMATION OF MEMORY CELL READ THRESHOLDS |
| CN | | 2011102948683 | CN102394101A | MEMORY DEVICE WITH ADAPTIVE CAPACITY |
| CN | | 200780026094.8 . | CN101501779A | MEMORY DEVICE WITH ADAPTIVE CAPACITY |
| CN | | 200780026121.1. | CN101496110A | Distortion estimation and cancellation in memory devices |
| CN | | 200780040493X | CN101601094A | READING MEMORY CELLS USING MULTIPLE THRESHOLDS |