PATENT ASSIGNMENT

Electronic Version v1.1

Stylesheet Version v1.1

SUBMISSION TYPE	DN TYPE: NEW ASSIGNMENT						
NATURE OF CONVI	EYANCE:	Partial Release of Security Interest					
CONVEYING PARTY DATA							
	Name Execution Date						
Credit Suisse Mana	gement LLC		08/31/2011				
Name:	Retro Reflective Optics, LLC						
Name:	Retro Reflective Optics, LLC						
Street Address:	20 Depot Street						
Internal Address:	Suite 2A						
City:	Peterborough						
State/Country:	NEW HAMPSHIRE						
Postal Code:	03458						
PROPERTY NUMBERS Total: 25							

Property Type	Number
Patent Number:	5510644
Patent Number:	5808349
Patent Number:	6175247
Patent Number:	6301179
Patent Number:	6765245
Patent Number:	6689628
Patent Number:	6930319
Patent Number:	7842972
Patent Number:	7772038
Application Number:	11919299
Patent Number:	6617938
Patent Number:	6906326
Patent Number:	7196349
Patent Number:	5858817
	PATENT

OP \$1000.00 5510644

07856410	
08142545	
08202576	
60081673	
60137224	
60367429	
60632710	
60722309	
60722308	
60181559	
	08142545 08202576 60081673 60137224 60367429 60632710 60722309

Fax Number:(503)224-2084Email:docket@stofoco.comCorrespondence will be sent to the e-mail address first; if that is unsuccessful, it will be sentvia US Mail.Correspondent Name:Stolowitz Ford Cowger LLPAddress Line 1:621 SW Morrison StAddress Line 2:Suite 600Address Line 4:Portland, OREGON 97205

ATTORNEY DOCKET NUMBER:	5566 (SEC AGMT PAR REL)				
NAME OF SUBMITTER:	Jeffrey J. Richmond				
Total Attachments: 8 source=5566 Partial Release of Security Int source=5566 Partial Release of Security Int	p1-8_083112#page2.tif p1-8_083112#page3.tif p1-8_083112#page4.tif p1-8_083112#page5.tif p1-8_083112#page6.tif p1-8_083112#page7.tif				

PARTIAL RELEASE OF SECURITY INTEREST

This partial release of security interest is made and executed by Credit Suisse Management LLC, located at 11 Madison Avenue, New York, New York 10010 ("**CS**") in favor of Retro Reflective Optics, LLC, located at 20 Depot Street, Suite 2A, Peterborough, NH 03458 ("**RRO**").

A. CS loaned money to RRO, and RRO granted CS a security interest, pursuant to:

(a) a Security Agreement dated January 22, 2010 ("Security Agreement"), in all personal property of debtor, wherever located, now owned or hereafter acquired, and all proceeds and products of the foregoing; and

(b) a Patent Security Agreement dated January 22, 2010 ("**Patent Security Agreement**"), in all of RRO's Patents and Patent Rights (as defined in the Patent Security Agreement), all general intangibles and all intellectual or other intangible property of RRO of any kind or nature associated with or arising out of any of the aforementioned properties and assets and not otherwise described above, and all proceeds of any and all of the foregoing;

such security interest to secure indebtedness and obligations of RRO to CS.

B. CS recorded or filed its security interest as follows:

(a) Copies of the Patent Security Agreement were recorded in the United States Patent and Trademark Office as follows:

<u>Debtor</u>	Secured Party	Execution Date	Reel/Frame	Recordation Date
Retro Reflective Optics, LLC	Credit Suisse Management LLC	01/22/2010	023905/0580	02/08/2010
Retro Reflective Optics, LLC	Credit Suisse Management LLC	01/22/2010	024016/0434	03/02/2010

(b) A UCC financing statement (the "**Financing Statement**"), prepared in accordance with the Security Agreement was filed in the State of Delaware as follows:

Debtor	Secured Party	Initial Filing #	<u>SRV</u>	Recordation Date
Retro Reflective Optics, LLC	Proskauer Rose LLP (As Representative for Credit Suisse Management LLC)	2010 0239396	100065473	01/22/2010

NOW, THEREFORE, for valuable consideration received, by its execution of this Partial Release of Security Interest, CS hereby irrevocably and unconditionally releases all right, title and interest in all of the following (and only the following):

(a) the patents and patent applications described in **Exhibit A** (the "Patents");"

(b) all patents and patent applications (i) to which any of the Patents directly or indirectly claims priority, (ii) for which any of the Patents directly or indirectly forms a basis for priority, and/or (iii) that incorporate by reference, or are incorporated by reference into, the Patents and that were co-owned patents/applications at the time of such incorporation by reference;

(c) all reissues, reexaminations, extensions, continuations, continuations in part, continuing prosecution applications, requests for continuing examinations, divisions, registrations of any item in any of the foregoing categories (a) and (b);

(d) all foreign patents, foreign patent applications, and foreign counterparts claiming priority to or from any item in any of the foregoing categories (a) through (c), including, without limitation, certificates of invention, utility models, industrial design protection, design patent protection, and other governmental grants or issuances;

(e) all items in any of the foregoing in categories (b) through (d), whether or not expressly listed as Patents below and whether or not claims in any of the foregoing have been rejected, withdrawn, cancelled, or the like;

(f) inventions, invention disclosures, and discoveries described in any of the Patents and/or any item in the foregoing categories (b) through (e) that (i) are included in any claim in the Patents and/or any item in the foregoing categories (b) through (e) and/or (ii) are subject matter capable of being reduced to a patent claim in a reissue or reexamination proceeding brought on any of the Patents and/or any item in the foregoing categories (b) through (e);

(g) all rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections, or other governmental grants or issuances of any type based on any item in any of the foregoing categories (a) through (f), including, without limitation, under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement, or understanding;

(h) all causes of action (whether known or unknown or whether currently pending, filed, or otherwise) and other enforcement rights under, or on account of, any of the Patents and/or any item in any of the foregoing categories (b) through (g), including, without limitation, all causes of action and other enforcement rights for

- (1) damages,
- (2) injunctive relief, and
- (3) any other remedies of any kind

for past, current, and future infringement; and

(i) all rights to collect royalties and other payments under or on account of any of the Patents and/or any item in any of the foregoing categories (b) through (h).

If necessary or desired, CS hereby authorizes RRO's authorized representative to file UCC Financing Statement Amendment(s) with the applicable filing office(s) in order to memorialize the release of any such security interest by CS.

This Release is governed by the law of the State of Delaware, excluding its choice of law principles to the contrary. This Release shall be binding upon RRO and its successors and assigns and inures, to the benefit of, with respect to the Patents (including any purchaser). CS acknowledges that it is aware that it may hereafter discover facts different from or in addition to what it now knows, believes or suspects to be true with respect to the matters herein released, that such facts may give rise to claims, causes of action, damages, consequences or results that are unforeseen or unsuspected, and that CS is nonetheless giving up its rights, and the releases in this Release Agreement will be and remain in effect in all respects as complete, general releases, notwithstanding any such different or additional facts.

This is a partial release only and does not release any property from said security interests, or other encumbrances or liens other than that specifically described above. Nothing in this Partial Release of Security Interest shall in any way impair, alter or diminish the effect, security interest, lien or encumbrance of the Security Agreement and Patent Security Agreement on the remaining part of the collateral not specifically released therefrom or any of the rights and remedies contained therein.

IN WITNESS WHEREOF, the und	ersigned has o	executed this Par	tial Release of	Security
Interest on this 3 1 day of Angua	, 2011.			2
	······································			

Credit Suisse Management LLC

By:	Howard X	<u> </u>
Name <u>:</u>	HOWARD SHAMS	
Its:	AUTHORIZED SIGNATORY	

Patent or Application No.	Country	Filing Date	<u>Title of Patent and First</u> Named Inventor
5,510,644	US	09/23/1994	CDTE x-ray detector for use at
3,310,011	05	09/23/1994	room temperature
			Karl A. Harris
5,808,349	US	12/05/1995	Magnetized photoconductive semiconductor switch
			Konstantinos Papadopoulos
6,175,247	US	04/09/1999	Context switchable field
			programmable gate array with
			public-private addressable
			sharing of intermediate data
	***		Jose R. Vazquez
6,301,179	US	05/12/2000	Self-equalized low power
			precharge sense amp for high
			speed SRAMS
			David C. Lawson
6,765,245	US	12/19/2002	Gate array core cell for VLSI
			ASIC devices
			Jai P. Bansal
6,689,628	US	08/15/2002	Method for dense pixel
			fabrication
			Lawrence F. Depaulis
6,930,319	US	12/12/2003	Method for dense pixel
			fabrication and product thereof
			Lawrence F. Depaulis
7,842,972	US	12/01/2005	Low-temperature-grown
			(LTG) insulated-gate PHEMT
			device and method
			Dong Xu
7,772,038	US	06/23/2006	CMOS process for fabrication
			of ultra small or non standard
			size or shape semiconductor
			die
			Daniel N. Carothers
11/919,299	US	10/02/2006	Process to fabricate integrated
			MWIR emitter

038-13653/AGR/3093920.3

Patent or Application No.	Country	Filing Date	<u>Title of Patent and First</u> <u>Named Inventor</u>
			Daniel N. Carothers
6,617,938	US	04/01/2002	Return to zero and sampling pulse generating circuits and method for direct digital up conversion
			James J. Komiak
DE60316422	DE	03/24/2003	Return to zero and sampling pulse generating circuits and method for direct digital up conversion
			James J. Komiak
FR1495540	FR	03/24/2003	Return to zero and sampling pulse generating circuits and method for direct digital up conversion
		0.0.10.1.10.0.00	James J. Komiak
GB1495540	GB	03/24/2003	Return to zero and sampling pulse generating circuits and method for direct digital up conversion
			James J. Komiak
6,906,326	US	07/25/2003	Quantum dot infrared photodetector focal plane array
			Frederick E. Koch
7,196,349	US	02/17/2005	Resonant cavity enhanced multi-quantum well light modulator and detector
5,858,817	US	10/10/1996	F. Elliott Koch Process to personalize master slice wafers and fabricate high density VLSI components with a single masking step
			Jai P. Bansal
6,169,702	US	05/26/1999	Memory device having a chip select speedup feature and associated methods
			David Lawson

038-13653/AGR/3093920.3

			<u>Title of Patent and First</u>
Patent or Application No.	<u>Country</u>	Filing Date	Named Inventor
07/856,410	US	03/23/1992	CDTE x-ray detector for use at
			room temperature
			Karl A. Harris
08/142,545	US	10/22/1993	CDTE x-ray detector for use at
			room temperature
			Karl A. Harris
08/202,576	US	02/28/1994	Magnetized photoconductive
			semiconductor switch
			Konstantinos Papadopoulos
60/081,673	US	04/14/1998	Public/private addressable
			sharing scheme for
			intermediate data management
			for a context switchable field
			programmable gate array
			Jose R. Vazquez
60/137,224	US	06/01/1999	Self-equalized low power
			precharge sense amp for high
			speed memory
			David C. Lawson
60/367,429	US	03/25/2002	Gate array core cell for VLSI
			ASIC devices
			Jai P. Bansal
60/632,710	US	12/01/2004	Low-growth-temperature
			insulated-gate device
			Kirby B. Nichols
PCT/US2005/043357	WO	12/01/2005	Low-temperature-grown
			(LTG) insulated-gate PHEMT
			device and method
			Robert Actis
60/722,309	US	09/30/2005	CMOS process for fabrication
			of ultra small or non standard
			size or shape semiconductor
			die
			Daniel N. Carothers
PCT/US2006/024630	WO	06/23/2006	CMOS process for fabrication
			of ultra small or non standard

Patent or Application No.	<u>Country</u>	Filing Date	<u>Title of Patent and First</u> Named Inventor
			size or shape semiconductor die
			Daniel N. Carothers
60/722,308	US	09/30/2005	Process to fabricate integrated MWIR emitter
			Daniel N. Carothers
PCT/US2006/038308	WO	10/02/2006	Process to fabricate integrated MWIR emitter
			Daniel N. Carothers
EP1495540	EP	03/24/2003	Return to zero and sampling pulse generating circuits and method for direct digital up conversion
			James J. Komiak
PCT/US2003/009073	WO	03/24/2003	Return to zero and sampling pulse generating circuits and method for direct digital up conversion
			James J. Komiak
PCT/US2004/022862	WO	07/15/2004	Quantum dot infrared photodetector focal plane array
			Alavi Kambiz
PCT/US2006/005209	WO	02/15/2006	Resonant cavity enhanced multi-quantum well light modulator and detector
			Alavi Kambiz
60/181,559	US	02/10/2000	Self-equalized low power precharge sense amp for high speed memory
	L		David C. Lawson

038-13653/AGR/3093920.3

RECORDED: 07/11/2012