PATENT ASSIGNMENT

Electronic Version v1.1 Stylesheet Version v1.1

SUBMISSION TYPE:

NEW ASSIGNMENT

NATURE OF CONVEYANCE:

Termination and Release of Security Interest in Patents

CONVEYING PARTY DATA

Name	Execution Date
Silicon Valley Bank	10/12/2012

RECEIVING PARTY DATA

Name:	Mercury Computer Systems, Inc.	
Street Address:	201 Rivemeck Road	
City:	Chelmsford	
State/Country:	MASSACHUSETTS	
Postal Code:	01824	

PROPERTY NUMBERS Total: 42

Property Type	Number
Patent Number:	7623732
Patent Number:	7453922
Patent Number:	7376175
Patent Number:	7327780
Patent Number:	7302462
Patent Number:	7302237
Patent Number:	7257816
Patent Number:	7248623
Patent Number:	7218668
Patent Number:	7210062
Patent Number:	7203221
Patent Number:	7177344
Patent Number:	7164706
Patent Number:	7139306
Patent Number:	7110440
	PATENT

REEL: 029119 FRAME: 0355

PATENT "

Patent Number:	7110437
Patent Number:	7110431
Patent Number:	7106742
Patent Number:	7099374
Patent Number:	7031258
Patent Number:	7007058
Patent Number:	6879486
Patent Number:	6781831
Patent Number:	6759588
Patent Number:	6754684
Patent Number:	6697255
Patent Number:	6690575
Patent Number:	6683787
Patent Number:	6678773
Patent Number:	6661657
Patent Number:	6625632
Patent Number:	6609140
Patent Number:	6243762
Patent Number:	6227897
Patent Number:	5950203
Patent Number:	5721828
Patent Number:	5602729
Patent Number:	5598568
Application Number:	12060732
Application Number:	11746463
Application Number:	11951920
Application Number:	11129123

CORRESPONDENCE DATA

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PATENT
REEL: 029119 FRAME: 0356

	Linda A. Salera
Total Attachments: 4 source=Mercury_Keybank Patent Release# source=Mercury_Keybank Patent Release# source=Mercury_Keybank Patent Release# source=Mercury_Keybank Patent Release#	page2.tif page3.tif

PATENT REEL: 029119 FRAME: 0357

TERMINATION AND RELEASE OF SECURITY INTEREST IN PATENTS

This TERMINATION AND RELEASE OF SECURITY INTEREST IN PATENTS, dated as of October 12, 2012 ("Release"), is made by Mercury Computer Systems, Inc., a Massachusetts corporation ("Grantor").

WHEREAS, Grantor and Silicon Valley Bank ("Bank") are parties to that certain Loan and Security Agreement dated as of February 12, 2010 (as may be amended, restated, supplemented, modified, extended, renewed or replaced from time to time, the "Loan Agreement");

WHEREAS, pursuant to the Loan Agreement, Grantor executed and delivered to Bank, the Intellectual Property Security Agreement dated as of February 12, 2010 and recorded at the United States Patent and Trademark Office ("<u>USPTO</u>") on February 20, 2010 at Reel 023963 Frame 0227 (the "Agreement");

WHEREAS, in connection with the Loan Agreement, Grantor granted to Bank a continuing security interest in, amongst other things, any and all right, title and interest of Grantor in, to, and under all the patents, patent applications and like protections, including without limitation, improvements, divisions, continuations, renewals, reissues, extensions and continuations-in-part of the same, and licenses and proceeds of the foregoing, including without limitation the items set forth on Schedule A hereto;

WHEREAS, Grantor has paid in full all Obligations (under and as defined in the Loan Agreement) in accordance with the terms of that certain Pay-off Letter, dated October 12, 2012 (the "Pay-off Letter"), by and between Grantor and Bank; and

WHEREAS, pursuant to the Pay-off Letter, Bank has authorized Grantor, or any other party on behalf of the Grantor, to prepare and file this Release to evidence the discharge and release of Bank's security interests in Grantor's assets as contemplated in the Pay-off Letter.

NOW THEREFORE, Grantor hereby acknowledges that, pursuant to the Pay-off Letter, the Bank has (a) terminated, cancelled, discharged, and released the mortgage, pledge, and hypothecation and lien on and security interest in and to the right, title, and interest in, to, and under all the patents, patent applications and like protections, including without limitation, improvements, divisions, continuations, renewals, reissues, extensions and continuations-in-part of the same, and licenses and proceeds of the foregoing, including without limitation the items listed on <u>Schedule A</u> attached hereto; and (b) authorized the recordation of this Release with the USPTO.

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IN WITNESS WHEREOF, the Grantor has caused this Termination and Release of Security Interest in Patents to be duly executed as of the date first set forth above.

Grantor:

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Name Kaula M. Riccon

Title: Chief Financial Officer

(Signature Pago to Patent Release)

Schedule A

Patents

No.	Issued	Filing Date	Jurisdiction	Title
	Patent No.			
	m <00 moo		7.161	Method and apparatus for digital image filtering with
1,	7,623,732		US	discrete filter kernels using graphics hardware
				Wireless communication systems and methods for
_	7 462 022		5 1 C)	contiguously addressable memory enabled multiple
2.	7,453,922		US	processor based multiple user detection Wireless communications systems and methods for cache
3.	7,376,175		US	enabled multiple processor based multiple user detection
3,	7,370,173		0	Wireless communications systems and methods for
4.	7,327,780		US	multiple operating system multiple user detection
	1,521,100			Framework and methods for dynamic execution of digital
5,	7,302,462		US	data processor resources
	1,202,102			Wideband signal generators, measurement devices,
				methods of signal generation, and methods of signal
6.	7,302,237		US	analysis
	7,000			Digital data processing apparatus and methods with
				dynamically configurable application execution on
7,	7,257,816		US	accelerated resources
				Wireless communications systems and methods for short-
8.	7,248,623		US	code multiple user detection
***************************************			······································	Wireless communications systems and methods for virtual
				user based multiple user detection utilizing vector
9.	7,218,668		US	processor generated mapped cross-correlation matrices
			***************************************	Wireless communications systems and methods for
				nonvolatile storage of operating parameters for multiple
10.	7,210,062		US	processor based multiple user detection
				Load balancing computational methods in a short-code
11.	7,203,221		US	spread-spectrum communications system
				Wireless communication systems and methods for long-
				code communications for regenerative multiple user
12.	7,177,344		US	detection involving implicit waveform subtraction
				Computational methods for use in a short-code spread-
13,	7,164,706		US	spectrum communications system
				Wireless communication systems and methods for long-
				code communications for regenerative multiple user
14	7 120 200		TIO	detection involving pre-maximal combination matched
14.	7,139,306		US	filter outputs
1.0	7110440		170	Wireless communications systems and methods for
15,	7,110,440		US	multiple processor based multiple user detection
				Wireless communications systems and methods for direct memory access and buffering, of digital signals for
16.	7,110,437		US	multiple user detection
10,			UD.	Hardware and software for performing computations in a
17.	7,110,431		US .	short-code spread-spectrum communications system
) 4 L L Mg-E-2 L		O.U.	Method and system for link fabric error detection and
18.	7,106,742		US	message flow control
. 2, 43 1,	1,200,170			Wireless communication systems and methods for long-
				code communications for regenerative multiple user
19,	7,099,374		US .	detection involving matched-filter outputs
20.	7,031,258		US	Digital data system with link level message flow control

A/75218972,4

PATENT REEL: 029119 FRAME: 0360

No.	Issued Patent No.	Filing Date	Jurisdiction	Title
				Methods and apparatus for binary division using look-up
21.	7,007,058		US	table
22.	6,879,486		US	Central inlet circuit board assembly
23.	6,781,831		US	Card-cage with integrated control and shaping of flow resistance curve for multiple plenum chambers
24.	6,759,588		US	Circuit board assembly, with a combination thermal, shock, vibration, and/or electromagnetic compatibility cover
25.	6,754,684		US	Method and apparatus for median filter on SIMD architecture digital data processor
26、	6,697,255		US	Circuit board assembly with integrated shaping and control of flow resistance curve
27.	6,690,575		US.	Digital data processor chassis with flow balanced air intake into multiple circuit board assemblies
28.	6,683,787		US	Circuit board assembly with integrated air plenum chamber using self-aligning heat sinks
29.	6,678,773		US	Bus protocol independent method and structure for managing transaction priority, ordering and deadlocks in a multi-processing system
30.	6,661,657		US	Circuit board assembly for use in a central inlet chassis configuration
31,	6,625,632		US	Method and apparatus for square root generation using bit manipulation and instruction interleaving
32.	6,609,140		US	Methods and apparatus for fast fourier transforms
				Methods and apparatus for data access and program
33.	6,243,762		US	generation on a multiprocessing, computer
34.	6,227,897		US	System for high-bandwidth electrical coupling,
35,	5,950,203		US	Method and apparatus for high-speed access to and sharing of storage devices on a networked digital data processing system
36.	5,721,828		US	Multicomputer memory access architecture
37,	5,602,729		US	Method and apparatus for monitoring and controlling multiprocessor digital data processing systems
38.	5,598,568		US	Multicomputer memory access architecture

Patent Applications

No.	Patent Application No.	Title
	***************************************	Real-Time. Three-Dimensional Synthetic Vision Display of Sensor-Validated
1,:	12060732	Terrain Data
2,	11746463	Rugged Chip Packaging
		Methods, Apparatus and Systems for Enhanced Synthetic Vision and Multi-Sensor
3.	11951920	Data Fusion to Improve Operational Capabilities of Unmanned Aerial Vehicles
4,	11129123	Daughter Card Approach to Employing Multiple Graphics Cards within a System

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RECORDED: 10/12/2012