PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
NXP B.V.	07/19/2012

RECEIVING PARTY DATA

Name:	Integrated Device Technology, Inc.
Street Address:	6024 Silver Creek Valley Road
City:	San Jose
State/Country:	CALIFORNIA
Postal Code:	95138

PROPERTY NUMBERS Total: 9

Property Type	Number
Application Number:	12933410
Application Number:	13121951
Application Number:	13123615
Application Number:	13124780
Application Number:	13085748
Application Number:	13116967
Application Number:	10261843
Application Number:	10576555
Application Number:	11587105

OP $360.00 12933410

CORRESPONDENCE DATA

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ATTORNEY DOCKET NUMBER:	70107.332
NAME OF SUBMITTER:	Gary J. Edwards

Total Attachments: 6
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Deed of Transfer of Patents

THE UNDERSIGNED:

(1) **NXP B.V.**, a limited liability company incorporated in the Netherlands, with corporate seat in Eindhoven, the Netherlands, and address at High Tech Campus 60, 5656AG Eindhoven, the Netherlands ("**NXP**"),

and

(2) **Integrated Device Technology, Inc.**, a company incorporated under the laws of Delaware, with its registered office in 6024 Silver Creek Valley Road, San Jose, California, 95138, United States of America ("**Assignee**").

hereinafter also referred to individual as a "**Party**" and collectively as the "**Parties**",

WHEREAS:

(A) NXP and the Assignee have entered into that certain Business Purchase Agreement dated as of [_____] 2012 (the "**Agreement**"); and

(B) Pursuant to the Agreement, and on certain terms and conditions as specified in an intellectual property transfer and license agreement entered into by the Parties (the "**IPTLA**"), NXP has, on behalf of itself and its Affiliates, agreed to assign to Assignee the Patents listed in Schedule A (the "**Transferred Patents**"); and

(C) By this Deed of Transfer (the "**Deed**"), Assignee wishes to acquire and NXP hereby wishes to assign all right, title and interest in and to the Transferred Patents.

HAVE AGREED AS FOLLOWS:

1. Definitions

When used in this Deed, the following capitalised terms shall have the meaning set forth below:

"**Affiliates**" means, in respect of the Assignee, any and all Persons with respect to which, now or hereafter, Assignee; or in respect of NXP, any and

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all Persons with respect to which, now or hereafter, NXP Semiconductors N.V., directly or indirectly, holds more than fifty percent (50%) of the nominal value of, or more than fifty percent (50%) of the voting power at general meetings, or has the power to appoint and to dismiss a majority of the directors or otherwise to direct the activities of such Person, or any other Person qualifying as a 'subsidiary' as referred to in Section 2:24a of the Netherlands Civil Code, excluding in the case of Affiliates of NXP or NXP Semiconductors N.V. Trident Microsystems, Inc. and its downstream affiliates.

"**Patents**" means United States and foreign patents and patent applications, registered design and registered design applications, any patents that issue as a result of those patent applications, and any renewals, reissues, re-examinations, extensions, continuations, continuations-in-part, subsequent divisions and substitutions relating to any of the patents and patent applications, as well as any inventions described in invention disclosures and any patents that issue as a result of patent applications filed for those invention disclosures.

Any capitalised term used in this Deed but not defined shall have the same meaning as ascribed thereto in the IPTLA.

2. Transfer of ownership of Transferred Patents

By this Deed, NXP hereby sells, assigns, transfers, conveys and delivers to Assignee all of NXP's right, title and interest in and to the Transferred Patents. NXP authorizes and requests the patent register (including any applicable foreign or international office or register) to record Assignee as owner of the Transferred Patents, as assignee of all of NXP's right, title and interest in, to and under the same, for the sole use and enjoyment of Assignee, its successors, assigns or other legal representatives.

3. Variation to Deed

No variation, extension, cancellation or translation of any expressed terms of this Deed (including in Schedule A) shall be binding upon NXP or Assignee unless made in writing and signed by a duly authorised representative of NXP and Assignee.

4. Additional assignment documents; further assurance

Assignee will be responsible for effectuating the recordation of the assignment and transfer of the Transferred Patents listed in Schedule A. NXP and Assignee shall, at each other's request, and without further consideration, execute and do (or procure to be executed and done by any of their respective

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Affiliates) all such deeds, documents, acts and things as the requesting party may from time to time reasonably require in order to effectuate or to formalise the transfer of the Transferred Patents to Assignee on a jurisdiction by jurisdiction basis and to cause the Transferred Patents to be recorded at the relevant patent registers around the world in the name of Assignee or any other Affiliate designated by Assignee.

5. Observance legal requirements

Assignee and NXP undertake to observe and act in accordance with all applicable legal conditions and terms required in order to effectuate the recordation of the assignment and transfer of the Transferred Patents in the relevant registers.

6. Costs for recordation

The costs for the recordation of the assignment and transfer of the Transferred Patents in the relevant registers will be borne by Assignee.

7. Applicable law and jurisdiction

This Deed shall be governed by and in accordance with the laws of the Netherlands. Any action or proceeding in respect of any claim arising out of or related to this Deed shall be solely conducted by NXP and the Assignee in accordance with the dispute settlement procedure provided in the BPA.

8. No rescission and no nullification

Each Party waives its right to rescind (ontbinden) this Deed on the basis of section 6:265 of the Netherlands Civil Code. Furthermore, a mistaken Party shall bear the risk of any mistake (dwaling) in entering into this Deed.

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IN EVIDENCE WHEREOF, the Parties have caused this Deed to be signed by their duly authorised representatives effective as of [•] .

NXP B.V.

(signature)
Name: Marc Schouten
Title: Head IP Creation & Strategy

Integrated Device Technology, Inc.

(signature)
Name: Vince Tortolano
Title: VP, General Counsel

Schedule A

NXP Reference	Title	AppNr	PubNr	PatNr	Region
81341002WO02	Flash ADC based on random offset spread	IB2009/051132	WO2009115990		WO
81341002EP04	Flash ADC based on random offset spread	09723168.2	EP2263318		EP
81341002US05	Flash ADC based on random offset spread	12/933410	US20110012771		US
81346706WO	Switched-capacitor pipeline stage with inter-symbol interference suppression	IB2009/052492	WO2010004455		WO
81346706US03	Switched-capacitor pipeline stage with inter-symbol interference suppression	12/999567	US20110095930		US
81346845WO	Background gain calibration of pipelined analog-to-digital converters using a 3-state transfer function	IB2009/054340	WO2010041187		WO
81346845EP03	Background gain calibration of pipelined analog-to-digital converters using a 3-state transfer function	09787360.8	EP2335355		EP
81346845US04	Background gain calibration of pipelined analog-to-digital converters using a 3-state transfer function	13/121951	US20110285564		US
81354017WO	Reference and range-scaling switched-capacitor pipeline stage	IB2009/054345	WO2010043999		WO
81354017EP03	Reference and range-scaling switched-capacitor pipeline stage	09740963.5	EP2338229		EP
81354017US04	Reference and range-scaling switched-capacitor pipeline stage	13/123615	US20110193736		US
81356715WO02	Element calibration of stage DAC in pipelined analog to digital converters	IB2009/054583	WO2010046831		WO
81356715US03	Element calibration of stage DAC in pipelined analog to digital converters	13/124780	US20110199244		US
81356715EP04	Element calibration of stage DAC in pipelined analog to digital converters	09743923.6	EP2351225		EP
81395130EP01	Analog demultiplexer for time-interleaved ADC with chopping and reset functionality	10160085.6	EP2378668		EP
81395130US03	Analog demultiplexer for time-interleaved ADC with chopping and reset functionality	13/085748	US20110254717		US
81396994EP01	Multiphase LO generation for the DAC mixer, the harmonic-reject mixers, and for the multiphase fractional divider with multistage re-clocking	10250980.9	EP2391000		EP

81396994US03	Multiphase LO generation for the DAC mixer, the harmonic-reject mixers, and for the multiphase fractional divider with multistage re-clocking	13/116967	US20110291732		US
NL010679US	HIGH SPEED HIGH RESOLUTION ADC ARCHITECTURE	10/261843	US20030076253	US6731231	US
NL031246EP2	DUAL RESIDUE PIPE-LINE ADC	04770279.0	EP1678831	EP1678831	EP
NL031246US1	DUAL RESIDUE PIPE-LINE ADC	10/576555	US20070132629	US7330145	US
NL031246GB04	DUAL RESIDUE PIPE-LINE ADC	04770279.0		GB1678831	GB
NL040410EP2	CANCELLATION OF RANDOM ERRORS OF UNIT ELEMENTS IN A DAC	05718692.6	EP1741190	EP1741190	EP
NL040410US1	CANCELLATION OF RANDOM ERRORS OF UNIT ELEMENTS IN A DAC	11/587105	US20070222653	US7394414	US
NL040410GB	CANCELLATION OF RANDOM ERRORS OF UNIT ELEMENTS IN A DAC	05718692.6		GB1741190	GB