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To the Director of the U.S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

1. Name of conveying party(ies):
Micron Technology, Inc.

Additional name(s) of conveying party(ies) attached? [ ] Yes [X] No

2. Name and address of receiving party(ies)
Name: Round Rock Research, LLC
Internal Address:
Street Address:
P. O. Box 1042
City: Mount Kisco
State: New York
Country: United States of America Zip: 10549
Additional name(s) & address(es) attached? [ ] Yes [X] No

3. Nature of conveyance/Execution Date(s):
Execution Date(s): March 16, 2012
[X] Assignment [ ] Merger [ ] Change of Name
[ ] Security Agreement [ ] Joint Research Agreement
[ ] Government Interest Assignment
[ ] Executive Order 9424, Confirmatory License
[ ] Other

4. Application or patent number(s):
[ ] This document is being filed together with a new application.
A. Patent Application No.(s)
13/657,392
B. Patent No.(s)
Additional numbers attached? [ ] Yes [X] No

5. Name and address to whom correspondence concerning document should be mailed:
Name: Richard J. Botos
LERNER, DAVID, LITTENBERG, KRUMHOLZ & MENTLIK, LLP
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6. Total number of applications and patents involved: 1

7. Total fee (37 CFR 1.21(h) & 3.41) $ 40.00

[X] Authorized to be charged to deposit account
[ ] Enclosed
[ ] None required (government interest not affecting title)

8. Payment Information
Deposit Account Number 12-1095
Authorized User Name Richard J. Botos

9. Signature:
Richard J. Botos
Signature
January 17, 2013
Date
Richard J. Botos - 32,016
Name of Person Signing
Total number of pages including cover sheet, attachments, and documents: 9

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CH $40.00 121095 13657392

CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS

This Confirmatory Assignment of Patent Rights (the "Agreement") is entered into this **16th day of March, 2012** (the "Closing Date"), by and between Micron Technology, Inc., a Delaware corporation ("Assignor"), and Round Rock Research, LLC, a Delaware limited liability company ("Assignee").

WHEREAS, Assignor and Assignee are parties to the Patent Sale and Transfer Agreement dated December 30th, 2009 (the "Patent Sale and Transfer Agreement") and to the letter agreement dated January 31, 2012 (the "Letter Agreement") amending the Patent Sale and Transfer Agreement; capitalized terms used but not otherwise defined in this Agreement shall have the respective meaning assigned thereto in the Patent Sale and Transfer Agreement as amended by the Letter Agreement;

WHEREAS, Assignor has agreed to sell, convey, transfer, assign and deliver to Assignee all of Assignor's (and its Subsidiaries') right, title and interest in and to the patents, including corresponding Patent Families, listed on the Assigned Patent List attached hereto (collectively, the "Assigned Patents");

WHEREAS, Assignee is now desirous of acquiring the entire and exclusive right, title and interest in and to the Assigned Patents in the United States and throughout the world; and

WHEREAS, Assignor is now willing to assign to Assignee all rights, title and interest in and to the Assigned Patents in the United States and throughout the world;

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged by Assignor, Assignor hereby assigns, transfers and conveys to Assignee, its successors, legal representatives and assigns, and Assignee hereby accepts, all of Assignor's right, title and interest in the United States and throughout the world in and to the Assigned Patents and any and all Letters Patent that are or may be granted thereon, and any legal equivalent thereof that may be granted in any country or countries foreign to the United States, in each case including without limitation any extensions, substitutes, continuations, divisions, reissues, reexaminations, and renewals thereof, or other equivalents thereof, and further, all rights and privileges pertaining to the Assigned Patents and any and all Letters Patent that are or may be granted thereon, and any legal equivalent thereof that may be granted in any country or countries foreign to the United States, in each case including, without limitation, the right and power, if any, to petition, sue or otherwise seek and recover damages, profits and any other remedy (monetary, injunctive, declaratory or other) in the United States and anywhere throughout the world for any past, present and future infringement thereof, conversion or misappropriation of, or other injury, offense, violation, breach of duty or wrong relating to, any of the Assigned Patents, or any license, agreement, contract or other matter relating thereto.

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks of the United States of America and the appropriate officers of all other jurisdictions in which the Assigned Patents are or may be registered or in which applications included among the Assigned Patents are pending, to record the title of Assignee, its successors, legal representatives and

assigns, as owner of all right, title and interest in and to the Assigned Patents, and to issue to Assignee, its successors, legal representatives and assigns, all Letters Patent and any legal equivalent thereof that may be granted in any country or countries foreign to the United States and recordations of patent rights resulting from any application included among the Assigned Patents, in accordance with the terms of this instrument.

Except to the extent that federal law preempts state law with respect to the matters covered hereby, this Agreement shall be governed by and construed in accordance with the laws of the State of Delaware, without giving effect to any of the principles of conflicts of laws thereof that would result in the application of the laws of another jurisdiction to this Agreement.

This Agreement shall be binding on, and shall inure to the benefit of, the parties hereto and their respective successors and assigns, and may be executed in two or more counterparts, each of which shall be deemed to be an original, but all of which shall constitute one and the same agreement. Each of the parties hereto agrees to accept and be bound by facsimile signatures hereto.

Each party represents that it has taken all necessary action to authorize the execution and delivery of this Agreement.

[The remainder of this page has been intentionally left blank.]

IN WITNESS WHEREOF, the parties hereto have caused this Agreement to be executed by their respective duly authorized officers, as of the date first written above.

ASSIGNOR:

MICRON TECHNOLOGY, INC.
8000 S. Federal Way
Boise, ID 83716

By: _____ O.K. DK
Name: Roderic W. Lewis
Title: Vice President of Legal Affairs, General Counsel and Corporate Secretary

ASSIGNEE:

ROUND ROCK RESEARCH, LLC
P. O. Box 1042
Mount Kisco, NY 10549

By: _____
Name: John Desmarais
Title: President

On this **16th day of March, 2012**, before me appeared Roderic W. Lewis, the person who signed this instrument, who acknowledged that he signed it as a free act on his own behalf or on behalf of the Assignor with authority to do so.

State of IDAHO)
) ss.
County of Ada)

ALICIA A. BROWN NOTARY PUBLIC STATE OF IDAHO

_____
Comm expires 6/9/12

[Note that federal patent assignments must also include a cover sheet. See 37 C.F.R. 3.28]

ASSIGNED PATENT LIST

Docket Number	Patent	Ctry	Title	Priority Date	Filing Date	Issue Date	Publication Number	Serial Number
1993-0292.00/US	5813590	US	EXTENDED TRAVEL WIRE BONDING MACHINE	16-Dec-95	16-Dec-95	29-Sep-98		08/574,156
1993-0292.01/US	6015079	US	A POSITIONING DEVICE FOR CONTROLLING THE POSITION OF A WORKPIECE IN A HORIZONTAL PLANE	16-Dec-95	04-Aug-97	18-Jan-00		08/905,183
1993-0292.03/US	6196445	US	A METHOD FOR POSITIONING A BOND HEAD IN A WIRE BONDING MACHINE	16-Dec-95	08-Dec-98	06-Mar-01		09/208,279
1993-0292.05/US	6223967	US	A POSITIONING DEVICE FOR CONTROLLING THE POSITION OF A WORKPIECE IN A HORIZONTAL PLANE	16-Dec-95	01-Feb-99	01-May-01		09/241,467
1993-0292.06/US	6253991	US	EXTENDED TRAVEL WIRE BONDING MACHINE	16-Dec-95	23-Oct-00	03-Jul-01		09/695,376
1993-0292.07/US	6276594	US	A METHOD FOR POSTIONING THE BOND HEAD IN A WIRE BONDING MACHINE	16-Dec-95	23-Oct-00	21-Aug-01		09/695,110
1993-0292.08/US	6253990	US	A METHOD FOR POSITIONING THE BOND HEAD IN A WIRE BONDING MACHINE	16-Dec-95	23-Oct-00	03-Jul-01		09/695,111
1993-0292.09/US	6321970	US	A METHOD FOR POSTIONING THE BOND HEAD IN A WIRE BONDING MACHINE	16-Dec-95	23-Oct-00	27-Nov-01		09/695,368
1995-0226.00/US	6021459	US	MEMORY SYSTEM HAVING FLEXIBLE BUS STRUCTURE AND METHOD	23-Apr-97	23-Apr-97	01-Feb-00		08/847,641
1995-0226.01/US	6212123	US	MEMORY SYSTEM HAVING FLEXIBLE BUS STRUCTURE AND METHOD	23-Apr-97	13-Jul-99	03-Apr-01		09/351,879
1995-0226.02/US	6567335	US	MEMORY SYSTEM HAVING FLEXIBLE BUS STRUCTURE AND METHOD	23-Apr-97	13-Nov-00	20-May-03		09/711,416
1995-0226.03/US	6320815	US	MEMORY SYSTEM HAVING FLEXIBLE BUS STRUCTURE AND METHOD	23-Apr-97	13-Nov-00	20-Nov-01		09/711,623
1995-0226.04/US	6516936	US	MEMORY SYSTEM HAVING FLEXIBLE BUS STRUCTURE AND METHOD	23-Apr-97	13-Nov-00	04-Feb-03		09/711,417
1995-0226.05/US	6353571	US	MEMORY SYSTEM HAVING FLEXIBLE BUS STRUCTURE AND METHOD	23-Apr-97	13-Nov-00	05-Mar-02		09/711,812
1995-0226.06/US	6396729	US	MEMORY SYSTEM HAVING FLEXIBLE BUS STRUCTURE AND METHOD	23-Apr-97	13-Nov-00	28-May-02		09/711,413
1995-0762.00/US	5615159	US	MEMORY SYSTEM WITH NON-VOLATILE DATA STORAGE UNIT AND METHOD OF INITIALIZING SAME	28-Nov-95	28-Nov-95	25-Mar-97		08/563,505
1995-0762.01/US	5677885	US	MEMORY SYSTEM WITH NON-VOLATILE DATA STORAGE UNIT AND METHOD OF INITIALIZING SAME	28-Nov-95	15-Nov-96	14-Oct-97		08/751,072
1996-0620.00/US	5976964	US	METHOD OF IMPROVING INTERCONNECT OF SEMICONDUCTOR DEVICES BY UTILIZING A FLATTENED BALL BOND	22-Apr-97	22-Apr-97	02-Nov-99		08/840,604
1996-0620.01/US	6034440	US	METHOD OF IMPROVING INTERCONNECT OF SEMICONDUCTOR DEVICES BY UTILIZING A FLATTENED BALL BOND	22-Apr-97	19-Jan-99	07-Mar-00		09/234,140

Docket Number	Patent	Ctry	Title	Priority Date	Filing Date	Issue Date	Publication Number	Serial Number
1996-0820.02/US	6165887	US	METHOD OF IMPROVING INTERCONNECT OF SEMICONDUCTOR DEVICES BY UTILIZING A FLATTENED BALL BOND	22-Apr-97	07-Sep-99	26-Dec-00		09/391,638
1996-0820.03/US	6420256	US	METHOD OF IMPROVING INTERCONNECT OF SEMICONDUCTOR DEVICES BY USING A FLATTENED BALL BOND	22-Apr-97	06-Oct-00	16-Jul-02		09/684,448
1996-0820.04/US	6624059	US	METHOD OF IMPROVING INTERCONNECT OF SEMICONDUCTOR DEVICES BY UTILIZING A FLATTENED BALL BOND	22-Apr-97	15-Jul-02	23-Sep-03		10/197,271
1997-1363.00/US	6107109	US	SEMICONDUCTOR INTERCONNECT HAVING LASER MACHINED CONTACTS	18-Dec-97	18-Dec-97	22-Aug-00		08/993,965
1997-1363.01/US	6294837	US	SEMICONDUCTOR INTERCONNECT HAVING LASER MACHINED CONTACTS	18-Dec-97	30-Aug-99	25-Sep-01		09/385,606
1997-1363.02/US	6833613	US	SEMICONDUCTOR INTERCONNECT HAVING LASER MACHINED CONTACTS	18-Dec-97	25-Sep-01	21-Dec-04		09/961,646
1997-1363.03/US	6620731	US	METHOD FOR FABRICATING SEMICONDUCTOR COMPONENTS AND INTERCONNECTS WITH CONTACTS ON OPPOSING SIDES	18-Dec-97	04-Jan-02	16-Sep-03		10/036,355
1997-1363.04/US	6903443	US	METHOD FOR FABRICATING SEMICONDUCTOR COMPONENTS AND INTERCONNECTS WITH CONTACTS ON OPPOSING SIDES	18-Dec-97	11-Dec-02	07-Jun-05	US2003-0080408	10/316,349
1997-1363.05/US	6998344	US	METHOD FOR FABRICATING SEMICONDUCTOR COMPONENTS BY FORMING CONDUCTIVE MEMBERS USING SOLDER	18-Dec-97	31-Mar-04	14-Feb-06	US2004-0178491	10/815,083
1997-1363.06/US	6952054	US	SEMICONDUCTOR PACKAGE HEAVING INTERCONNECT WITH CONDUCTIVE MEMBERS	18-Dec-97	08-Apr-04	04-Oct-05	US2004-0188824	10/820,674
1999-0231.00/US	6418070	US	MEMORY DEVICE TESTER AND METHOD FOR TESTING REDUCED POWER STATES	02-Sep-99	02-Sep-99	09-Jul-02		09/388,566
1999-0231.01/US	6674677	US	MEMORY DEVICE TESTER AND METHOD FOR TESTING REDUCED POWER STATES	02-Sep-99	12-Jun-02	06-Jan-04	US2002-0149981	10/166,887
1999-0231.02/US	6775192	US	MEMORY DEVICE TESTER AND METHOD FOR TESTING REDUCED POWER STATES	02-Sep-99	12-Jun-02	10-Aug-04	US2002-0190706	10/167,817
1999-0231.03/US	6914843	US	MEMORY DEVICE TESTER AND METHOD FOR TESTING REDUCED POWER STATES	02-Sep-99	12-Jun-02	05-Jul-05	US2002-0149982	10/170,561
1999-0231.04/US	7161866	US	MEMORY DEVICE TESTER AND METHOD FOR TESTING REDUCED POWER STATES	02-Sep-99	01-Jul-05	09-Jan-07	US2005-0243638	11/173,307
2004-0017.00/CN		CN	IMPROVED POWER-PROFILE VIA MEMORY COMMAND DELAY BALANCING IN A DAISY-CHAINED MEMORY TOPOLOGY	19-Aug-04	09-Aug-05			200580028359.9
2004-0017.00/DE	1779251	DE	IMPROVED POWER-PROFILE VIA MEMORY COMMAND DELAY BALANCING IN A DAISY-CHAINED MEMORY TOPOLOGY	19-Aug-04	09-Aug-05	01-Jul-09		05784488.8
2004-0017.00/EP	EP1 779 251B1	EP	IMPROVED POWER-PROFILE VIA MEMORY COMMAND DELAY BALANCING IN A DAISY-CHAINED MEMORY TOPOLOGY	19-Aug-04	09-Aug-05	01-Jul-09		05784488.8

Docket Number	Patent	Ctry	Title	Priority Date	Filing Date	Issue Date	Publication Number	Serial Number
2004-0017.00/FR	1779251	FR	IMPROVED POWER-PROFILE VIA MEMORY COMMAND DELAY BALANCING IN A DAISY-CHAINED MEMORY TOPOLOGY	19-Aug-04	09-Aug-05	01-Jul-09		05784488.8
2004-0017.00/GB	1779251	GB	IMPROVED POWER-PROFILE VIA MEMORY COMMAND DELAY BALANCING IN A DAISY-CHAINED MEMORY TOPOLOGY	19-Aug-04	09-Aug-05	01-Jul-09		05784488.8
2004-0017.00/JP	4742347	JP	MEMORY COMMAND DELAY BALANCING IN A DAISY-CHAINED MEMORY TOPOLOGY	19-Aug-04	09-Aug-05	20-May-11		2007-527876
2004-0017.00/KR	0883007	KR	IMPROVED POWER-PROFILE VIA MEMORY COMMAND DELAY BALANCING IN A DAISY-CHAINED MEMORY TOPOLOGY	19-Aug-04	01-Feb-07	03-Feb-09		2007-7002577
2004-0017.00/TW	I317068	TW	IMPROVED POWER-PROFILE VIA MEMORY COMMAND DELAY BALANCING IN A DAISY-CHAINED MEMORY TOPOLOGY	19-Aug-04	12-Aug-05	11-Nov-09	200619950	94127497
2004-0017.00/US	7669027	US	MEMORY COMMAND DELAY BALANCING IN A DAISY-CHAINED MEMORY TOPOLOGY	19-Aug-04	19-Aug-04	23-Feb-10	US2006-0041730	10/922,299
2004-0017.01/US	7908451	US	MEMORY COMMAND DELAY BALANCING IN A DAISY-CHAINED MEMORY TOPOLOGY	19-Aug-04	19-Jan-10	15-Mar-11		12/689,495
2004-0017.02/US		US	MEMORY COMMAND DELAY BALANCING IN A DAISY-CHAINED MEMORY TOPOLOGY	19-Aug-04	23-Feb-11			13/033,364
2004-0653.00/US	7164611	US	DATA RETENTION KILL FUNCTION	26-Oct-04	26-Oct-04	16-Jan-07	US2006-0087882	10/973,208
2004-0653.01/US	7477554	US	DATA RETENTION KILL FUNCTION	26-Oct-04	20-Jul-06	13-Jan-09	US-2006-0294291-A1	11/490,215
2004-0653.02/US	7751263	US	DATA RETENTION KILL FUNCTION	26-Oct-04	12-Jan-09	06-Jul-10	2009-153181	12/352,485
2004-0653.03/US	8023344	US	DATA RETENTION KILL FUNCTION	26-Oct-04	30-Jun-10	20-Sep-11	2010-0265781	12/827,686
2004-0653.04/US		US	DATA RETENTION KILL FUNCTION	26-Oct-04	19-Sep-11			13/236,394
2005-0534.00/US	7966450	US	NON-VOLATILE HARD DRIVE CACHE SYSTEM AND METHOD	01-Sep-05	01-Sep-05	21-Jun-11		11/219,324
2005-0534.01/US		US	NON-VOLATILE HARD DRIVE CACHE SYSTEM AND METHOD	01-Sep-05	16-May-11			13/108,805
2005-0710.00/CN		CN	MEMORY SYSTEM AND METHOD HAVING VOLATILE AND NON-VOLATILE MEMORY DEVICES AT SAME HIERARCHICAL LEVEL	19-Jan-07	07-Dec-07		CN 101573760A	200780049323.8
2005-0710.00/DE		DE	MEMORY SYSTEM AND METHOD HAVING VOLATILE AND NON-VOLATILE MEMORY DEVICES AT SAME HIERARCHICAL LEVEL	22-Jan-07	07-Dec-07			078653615
2005-0710.00/EP		EP	MEMORY SYSTEM AND METHOD HAVING VOLATILE AND NON-VOLATILE MEMORY DEVICES AT SAME HIERARCHICAL LEVEL	22-Jan-07	07-Dec-07			07865361.5
2005-0710.00/FR		FR	MEMORY SYSTEM AND METHOD HAVING VOLATILE AND NON-VOLATILE MEMORY DEVICES AT SAME HIERARCHICAL LEVEL	22-Jan-07	07-Dec-07			078653615
2005-0710.00/GB		GB	MEMORY SYSTEM AND METHOD HAVING VOLATILE AND NON-VOLATILE MEMORY DEVICES AT SAME HIERARCHICAL LEVEL	22-Jan-07	07-Dec-07			078653615

Docket Number	Patent	Ctry	Title	Priority Date	Filing Date	Issue Date	Publication Number	Serial Number
2005-0710.00/KR	10-1080498	KR	MEMORY SYSTEM AND METHOD HAVING VOLATILE AND NON-VOLATILE MEMORY DEVICES AT SAME HIERARCHICAL LEVEL	19-Jan-07	07-Dec-07	31-Oct-11		10-2009-7015356
2005-0710.00/NL		NL	MEMORY SYSTEM AND METHOD HAVING VOLATILE AND NON-VOLATILE MEMORY DEVICES AT SAME HIERARCHICAL LEVEL	22-Jan-07	07-Dec-07			078653615
2005-0710.00/US	7564722	US	MEMORY SYSTEM AND METHOD HAVING VOLATILE AND NON-VOLATILE MEMORY DEVICES AT SAME HIERARCHICAL LEVEL		22-Jan-07	21-Jul-09		11/656,578
2005-0710.01/US	7778092	US	MEMORY SYSTEM AND METHOD HAVING VOLATILE AND NON-VOLATILE MEMORY DEVICES AT SAME HIERARCHICAL LEVEL	19-Jan-07	02-Jul-09	17-Aug-10		12/497,400
2005-0710.02/US	7916553	US	MEMORY SYSTEM AND METHOD HAVING VOLATILE AND NON-VOLATILE MEMORY DEVICES AT SAME HIERARCHICAL LEVEL	19-Jan-07	02-Jul-10	29-Mar-11		12/830,113
2005-0710.03/US		US	MEMORY SYSTEM AND METHOD HAVING VOLATILE AND NON-VOLATILE MEMORY DEVICES AT SAME HIERARCHICAL LEVEL	19-Jan-07	18-Mar-11			13/051,329
2005-1078.00/CN		CN	MEMORY DEVICE ARCHITECTURES AND OPERATION	30-Jan-07	29-Jan-08		CN 101595528 A	0880003512.6
2005-1078.00/KR	10-1084820	KR	MEMORY DEVICE ARCHITECTURES AND OPERATION	30-Jan-07	29-Jan-08	11-Nov-11		10-09-7018004
2005-1078.00/TW		TW	MEMORY DEVICE ARCHITECTURES AND OPERATION	30-Jan-07	30-Jan-08		200847169	097103531
2005-1078.00/US	7791952	US	MEMORY DEVICE ARCHITECTURES AND OPERATION		30-Jan-07	07-Sep-10		11/699,964
2005-1078.01/US	7990775	US	METHODS OF OPERATING MEMORY DEVICES INCLUDING DIFFERENT SETS OF LOGICAL ERASE BLOCKS	30-Jan-07	03-Sep-10	02-Aug-11	US2010-0329038	12/875,763
2005-1078.02/US		US	MEMORY DEVICES AND THEIR OPERATION WITH DIFFERENT SETS OF LOGICAL ERASE BLOCKS	30-Jan-07	01-Aug-11		US-2011-0286272-A1	13/195,308
2005-1088.00/CN		CN	METHOD AND APPARATUS FOR IMPROVING STORAGE PERFORMANCE USING A BACKGROUND ERASE	25-May-06	23-May-07		CN 101479808A	200780023659.4
2005-1088.00/DE	2022059	DE	METHOD AND APPARATUS FOR IMPROVING STORAGE PERFORMANCE USING A BACKGROUND ERASE	25-May-06	23-May-07	27-Oct-10	2022059	07795303.2
2005-1088.00/EP	2022059	EP	METHOD AND APPARATUS FOR IMPROVING STORAGE PERFORMANCE USING A BACKGROUND ERASE	25-May-06	23-May-07	27-Oct-10	2022059	07795303.2
2005-1088.00/FR	2022059	FR	METHOD AND APPARATUS FOR IMPROVING STORAGE PERFORMANCE USING A BACKGROUND ERASE	25-May-06	23-May-07	27-Oct-10	2022059	07795303.2
2005-1088.00/GB	2022059	GB	METHOD AND APPARATUS FOR IMPROVING STORAGE PERFORMANCE USING A BACKGROUND ERASE	25-May-06	23-May-07	27-Oct-10	2022059	07795303.2
2005-1088.00/KR	10-1060799	KR	METHOD AND APPARATUS FOR IMPROVING STORAGE PERFORMANCE USING A BACKGROUND ERASE	25-May-06	23-May-07	24-Aug-11		10-2008-7031195

Docket Number	Patent	Ctry	Title	Priority Date	Filing Date	Issue Date	Publication Number	Serial Number
2005-1088.00/US	7564721	US	METHOD AND APPARATUS FOR IMPROVING STORAGE PERFORMANCE USING A BACKGROUND ERASE		25-May-06	21-Jul-09	US2007-0274134	11/442,514
2005-1088.01/US	7742344	US	METHOD AND APPARATUS FOR IMPROVING STORAGE PERFORMANCE USING A BACKGROUND ERASE	25-May-06	25-Jun-09	22-Jun-10	US2009-0257284	12/491,846
2005-1089.00/US	7466600	US	SYSTEM AND METHOD FOR INITIATING A BAD BLOCK DISABLE PROCESS IN A NON-VOLATLE MEMORY		03-Aug-06	16-Dec-08		11/499,231
2005-1089.01/US	7692984	US	SYSTEM AND METHOD FOR INITIATING A BAD BLOCK DISABLE PROCESS IN A NON-VOLATLE MEMORY	03-Aug-06	06-Dec-08	06-Apr-10		12/330,359
2006-0941.00/US	7925844	US	MEMORY REGISTER DEFINITON SYSTEMS AND METHODS		29-Nov-07	12-Apr-11	US-2009-0141564-A1	11/947,596
2006-0941.01/US		US	MEMORY REGISTER ENCODING SYSTEMS AND METHODS	29-Nov-07	29-Mar-11		US-2011-0179221-A1	13/074,917
2007-0249.00/CN		CN	HYBRID MEMORY MANAGEMENT	28-May-08	28-May-09		CN 102047230 A	200980119526.9
2007-0249.00/EP		EP	HYBRID MEMORY MANAGEMENT	28-May-08	28-May-09		EP 2291746	09767334.7
2007-0249.00/JP		JP	HYBRID MEMORY MANAGEMENT	28-May-08	28-May-09			2011-511797
2007-0249.00/KR		KR	HYBRID MEMORY MANAGEMENT	28-May-08	28-May-09			10-2010-7029386
2007-0249.00/US	8060719	US	HYBRID MEMORY MANAGEMENT		28-May-08	15-Nov-11	US-2009-0300269-A1	12/127,945
2007-0249.01/US		US	HYBRID MEMORY MANAGEMENT	28-May-08	14-Nov-11			13/295,616