Form **PTO-1595** (Rev. 03-11)
OMB No. 0651-0027 (exp. 03/31/2015)

U.S. DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

RECORDATION FORM COVER SHEET
PATENTS ONLY

To the Director of the U.S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

1. Name of conveying party(ies):

Vertical Circuits (Assignment For The Benefit of Creditors), LLC

Additional name(s) of conveying party(ies) attached? [ ] Yes [X] No

2. Name and address of receiving party(ies)

Name: Invensas Corporation

Internal Address:

Street Address:

2702 Orchard Parkway

City: San Jose

State: California

Country: United States of America Zip: 95134

Additional name(s) & address(es) attached? [ ] Yes [X] No

3. Nature of conveyance/Execution Date(s):

Execution Date(s): November 9, 2012

[X] Assignment [ ] Merger [ ] Change of Name
[ ] Security Agreement [ ] Joint Research Agreement
[ ] Government Interest Assignment
[ ] Executive Order 9424, Confirmatory License
[ ] Other

4. Application or patent number(s):

[ ] This document is being filed together with a new application.

A. Patent Application No.(s)

11/744,142
12/046,651
12/124,077
12/913,604
13/041,192
61/556,075
61/556,141

B. Patent No.(s)

5,657,206	5,891,761	6,124,633	6,486,528
5,661,087	5,936,302	6,134,118	7,215,018
5,675,180	5,994,170	6,188,126	7,245,021
5,698,895	6,080,596	6,255,726	7,535,109
5,837,566	6,098,278	6,271,598	7,705,432
			7,923,349

Additional numbers attached? [ ] Yes [X] No

5. Name and address to whom correspondence concerning document should be mailed:

Name: Daryl K. Neff
LERNER, DAVID, LITTENBERG, KRUMHOLZ & MENTLIK, LLP

Internal Address: Atty. Dkt.: **TIPI 6.2-036**

Street Address: 600 South Avenue West

City: Westfield

State: NJ Zip: 07090

Phone Number: 908-654-5000

Fax Number: 908-654-7866

Email Address: ataylor@ldlkm.com

6. Total number of applications and patents involved: 28

7. Total fee (37 CFR 1.21(h) & 3.41) $ 1,120.00

[X] Authorized to be charged to deposit account
[ ] Enclosed
[ ] None required (government interest not affecting title)

8. Payment Information

Deposit Account Number 12-1095

Authorized User Name Daryl K. Neff

9. Signature:

Signature — January 30, 2013 Date

Daryl K. Neff - 38,253
Name of Person Signing

Total number of pages including cover sheet, attachments, and documents: 10

3026192_1.docx

CH $1120.00 121095 11744142

CONFIRMATORY DEED OF ASSIGNMENT

THIS DEED OF ASSIGNMENT ("Assignment"), EFFECTIVE AS OF OCTOBER 26, 2012, IS MADE BY AND BETWEEN

VERTICAL CIRCUITS (ASSIGNMENT FOR THE BENEFIT OF CREDITORS), LLC (hereinafter "**ASSIGNOR**"), a California limited liability company, with its principal place of business located at 1100 La Avenida Street, Building A, Mountain View, California 94043, United States of America; and

INVENSAS CORPORATION (hereinafter "**INVENSAS**"), a Delaware corporation with its principal place of business at 2702 Orchard Parkway, San Jose, California 95134, United States of America.

WHEREAS:

A **ASSIGNOR** is the sole owner in respect of the issued, expired and abandoned patents and patent applications listed in the attached Exhibit (hereinafter "the **PATENTS**"); and

B **INVENSAS** is desirous of acquiring all of the right, title and interest in and to the **PATENTS** and any foreign counterpart patents and applications thereof.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, **ASSIGNOR** has sold, assigned and transferred, and does hereby sell, assign and transfer to **INVENSAS** all of **ASSIGNOR's** right, title and interest in (i) the **PATENTS**; (ii) all reissues, extensions, revivals, renewals, reexaminations and foreign counterpart patents and applications thereof, and (iii) the right to sue for and recover damages for any past, present or future infringement of the **Patents** or such foreign counterpart patents and applications, the same to be held and enjoyed by **INVENSAS** for its own use and enjoyment, and for the use and enjoyment of its successors, assigns and other legal representatives, to the end of the term or terms thereof granted or revived, reissued or reexamined as fully and entirely as the same would have been held and enjoyed by **ASSIGNOR**, if this assignment and sale had not been made.

IN WITNESS WHEREOF, **ASSIGNOR** has caused these presents to be signed by its duly appointed officer having full authority in the circumstances; and **INVENSAS** has caused these presents to be signed by its duly appointed officer having full authority in the circumstances.

And if the issue date and/or patent number of any of the **PATENTS** is unknown to **ASSIGNOR** and **INVENSAS** at the time this Assignment is executed, **ASSIGNOR** does hereby authorize its attorneys to insert on this Assignment the issue date and patent number of the said **PATENT** when known.

ASSIGNOR hereby declares that **INVENSAS** may take the steps for recordation of this assignment in the sole name of **INVENSAS**.

SIGNED for and on behalf of

VERTICAL CIRCUITS (ASSIGNMENT FOR THE BENEFIT OF CREDITORS), LLC

By _____ on November 9 2012
(Signature) (Date)

Michael A. Maidy, Manager
(Print Name and Title)

State of California) SS:

County of Santa Clara

On this 9th day of November, 2012 before me, Hangama Aziz, personally appeared Michael A. Maidy, who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the instrument and acknowledged to me that he executed the same in his authorized capacity and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

_____
(Notary Public)

HANGAMA AZIZ
Commission # 1981067
Notary Public - California
Santa Clara County
My Comm. Expires Jun 7, 2016

SIGNED for and on behalf of

INVENSAS CORPORATION

by _____ on Nov-13- 2012
(Signature) (Date)

Simon McElrea, President

State of California) SS:

County of Santa Clara)

On this 13th day of November, 2012 before me, Santa Clara Notary Public, personally appeared Simon McElrea, who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

_____
(Notary Public)

SALINA DIAZ
Commission # 1889526
Notary Public - California
Santa Clara County
My Comm. Expires May 16, 2014

EXHIBIT A
IDENTIFIED PATENTS AND PATENT APPLICATIONS

Date Format (MM/DD/YYYY)

1. United States Listed Issued Patents and Pending Patent Applications

US Issued Patents

Patent Number	Filing Date	Application Number	Issue Date	Publication Number	Title
5657206	01/19/1995	08/374,421	08/12/1997	-	Conductive Epoxy Flip-Chip Package and Method
5661087	06/07/1995	08/476,623	08/26/1997	-	Vertical Interconnect Process for Silicon Segments
5675180	06/23/1994	08/265,081	10/07/1997	-	Vertical Interconnect Process for Silicon Segments
5698895	01/20/1995	08/376,149	12/16/1997	-	Silicon segment programming method and apparatus
5837566	04/24/1997	08/847,309	11/17/1998	-	Vertical Interconnect Process for Silicon Segments
5891761	08/22/1997	08/918,502	04/06/1999	-	Vertical interconnect process for silicon segments with thermally Conductive Epoxy Preform
5936302	04/25/1997	08/845,655	08/10/1999	-	Speaker Diaphragm
5994170	04/25/1997	08/845,654	11/30/1999	-	Silicon Segment Programming Method
6080596	08/22/1997	08/920,273	06/27/2000	-	Method for Forming Vertical Interconnect Process for Silicon Segments with Dielectric Isolation
6098278	08/22/1997	08/917,447	08/08/2000	-	Method for Forming Conductive Epoxy Flip-Chip on Chip
6124633	08/22/1997	08/918,501	09/26/2000	-	Vertical interconnect process for silicon segments with thermally Conductive Epoxy Preform
6134118	04/03/1997	08/834,798	10/17/2000	-	Conductive Epoxy Flip-Chip Package and Method
6188126	04/24/1997	08/842,448	02/13/2001	-	Vertical Interconnect Process for Silicon Segments
6255726	08/21/1997	08/915,620	07/03/2001	-	Vertical Interconnect Process for Silicon Segments with Dielectric Isolation
6271598	08/22/1997	08/918,500	08/07/2001	-	Conductive Epoxy Flip-Chip on Chip
6486528	08/23/1999	09/378,879	11/26/2002	-	Silicon Segment Programming Apparatus and Three Terminal Fuse Configuration
7215018	03/25/2005	11/090,969	05/08/2007	2005-0230802	Stacked Die BGA or LGA Component Assembly
7245021	03/31/2005	11/097,829	07/17/2007	2005-0230802	Micropede Stacked Die Component Assembly

Patent Number	Filing Date	Application Number	Issue Date	Publication Number	Title
7535109	05/03/2007	11/744,153	05/19/2009	2007-0252262	Die Assembly Having Electrical Interconnect
7705432	12/17/2004	11/016,558	4/27/2010	2005-0224952	Three Dimensional Six Surface Conformal Die Coating
7843046	08/27/2008	12/199,667	11/30/2010	2009-0206458	Flat leadless packages and stacked leadless package assemblies
7863159	11/25/2008	12/323,288	01/04/2011	2009-0315174	Semiconductor die separation method
7923349	06/19/2008	12/142,589	04/12/2011	2008-0315434	Wafer level surface passivation of stackable integrated circuit chips
8159053	09/28/2010	12/892,739	04/17/2012	2011-0012246	Flat leadless packages and stacked leadless package assemblies
8178978	03/12/2009	12/403,175	5/15/2012	2009-0230528	Support mounted electrically interconnected die assembly

US Pending Applications

Application Number	Filing Date	Publication Number	Title
11/744,142	05/03/2007	2007-0284716	Assembly Having Stacked Die Mounted On Substrate
12/046,651	03/12/2008	2008-0224279	Vertical electrical interconnect formed on support prior to die mount
12/124,077	05/20/2008	2008-0303131	Electrically Interconnected Stacked Die Assemblies
12/199,080	08/27/2008	2009-0065916	Semiconductor Die Mount by Conformal Die Coating
12/821,454	06/23/2010	2010-0327461	Electrical interconnect for die stacked in zig-zag configuration
12/913,529	10/27/2010	2011-0266684	Selective Die Electrical Insulation By Additive Process
12/913,604	10/27/2010	2011-0037159	Electrically Interconnected Stacked Die Assemblies
12/939,524	11/04/2010	2011-0272825	Stacked Die Assembly Having Reduced Stress Electrical Interconnects
12/982,376	12/30/2010	2011-0101505	Semiconductor Die Separation Method
13/041,192	03/04/2011	2011-0147943	Wafer level surface passivation of stackable integrated circuit chips
13/109,996	05/17/2011	2012-0119385	Electrical Connector Between Die Pad and Z-Interconnect for Stacked Die Assemblies
13/243,877	09/23/2011	2012-0248607	Semiconductor Die Having Fine Pitch Electrical Interconnects
61/556,075	11/04/2011	-	EMI Shield
61/556,141	11/04/2011	-	Bonding Wedge
13/456,126	04/25/2012	-	Support mounted electrically interconnected die assembly

2. Foreign Listed Issued Patents and Pending Patent Applications

Foreign Issued Patents

Patent Number	Country	Filing Date	Application Number	Issue Date	Publication Number	Title
766909	EP	06/08/1995	95923676.1	12/19/2001	766909	Vertical Interconnect Process for Silicon Segments
1158570	EP	06/08/1995	01115235.2	05/03/2006	1158570	Vertical Interconnect Process for Silicon Segments
377657	KR	06/08/1995	10-1996-0707364	03/13/2003	-	Vertical Interconnect Process for Silicon Segments
536823	KR	08/14/1998	10-2000-7001499	12/08/2005	-	Vertical interconnect process for silicon segments with thermally Conductive Epoxy Preform
593567	KR	08/14/1998	10-2000-7001498	6/20/2006	-	Vertical Interconnect Process for Silicon Segments with Dielectric Isolation

Foreign Pending Applications

Country	Filing Date	Application Number	Publication Number	Title
CN	03/12/2009	200980112952.X	101999167 A	Support mounted electrically interconnected die assembly
CN	08/28/2009	200980133534.9	102132411 A	Image Sensor
CN	12/09/2009	200980149285.2	102246298	Stacked die assembly having reduced stress electrical interconnects
CN	06/23/2010	201080035256.6	102473697 A	Electrical interconnect for die stacked in zig-zag configuration
JP	02/18/2009	2010-547716	2011-512691	Flat leadless packages and stacked leadless package assemblies
JP	03/12/2009	2010-550853	2011-514012	Support mounted electrically interconnected die assembly
JP	12/09/2009	2011-540873	2012-511835	Semiconductor die interconnect formed by aerosol application of electrically conductive material
JP	06/23/2010	2012-517680	-	Electrical interconnect for die stacked in zig-zag configuration
KR	04/12/2005	10-2006-7023770	-	Micropede Stacked Die Component Assembly
KR	04/12/2005	10-2006-7023775	2007-0022264	Stacked Die BGA or LGA Component Assembly
KR	06/04/2008	10-2010-7007558	10-2010-069669	Electrically Interconnect Formed by Pulsed Dispense
KR	06/04/2008	10-2010-7000565	10-2010-020518	Electrically interconnected stacked die assemblies
KR	10/15/2008	10-2010-7010817	10-2010-087329	Chip Scale Stacked Die Package
KR	02/18/2009	10-2010-7019120	10-2010-115784	Flat leadless packages and stacked leadless package assemblies
KR	03/12/2009	10-2010-7019834	10-2010-123858	Support mounted electrically interconnected die assembly
KR	06/15/2009	10-2010-7028918	10-2011038636	Semiconductor Die Separation Method

Country	Filing Date	Application Number	Publication Number	Title
KR	08/28/2009	10-2011-7002579	10-2011051191	Image Sensor
KR	12/09/2009	10-20117015983	10-2011-103413	Semiconductor die interconnect formed by aerosol application of electrically conductive material
KR	06/23/2010	10-2012-7002117	10-2012-055541	The electrical interconnect for die stacked in zig-zag configuration.
TW	04/11/2005	94111358	200605298	Stacked Die BGA or LGA Component Assembly
TW	04/11/2005	94111359	200605299	Micropede Stacked Die Component Assembly
TW	06/06/2008	97121194	200921887	Electrical interconnect formed by pulsed dispense
TW	06/06/2008	97121195	200913208	Electrically interconnected stacked die assemblies
TW	06/19/2008	97122985	200915453	Wafer level surface passivation of stackable integrated circuit chips
TW	06/20/2008	97123103	200917391	Three-dimensional circuitry formed on integrated circuit device using two-dimensional fabr cation
TW	09/09/2008	97134551	200931605	Semiconductor die mount by conformal die coating
TW	10/16/2008	97139739	200941662	Chip Scale Stacked Die Package
TW	02/19/2009	98105276	200952144	Flat leadless packages and stacked leadless package assemblies
TW	03/12/2009	98108067	201005916	Support mounted electrically interconnected die assembly
TW	06/15/2009	98119939	201013768	Semiconductor die separation method
TW	12/09/2009	98142058	201030935	Semiconductor die interconnect formed by aerosol application of electrically conductive material
TW	05/11/2010	99114942	201115662	Flip-chip underfill
TW	06/23/2010	99120462	201119007	Electrical interconnect for die stacked in zig-zag configuration
TW	10/27/2010	99136720	201125036	Selective die electrical insulation by additive process
TW	11/02/2010	99137634	201138062	Stacked die assembly having reduced stress electrical interconnects
TW	05/19/2011	100117575	201220411	Electrical connector between die pad and z-interconnect for stacked die assemblies
TW	09/30/2011	100135584	201232732	Semiconductor Die Having Fine Pitch Electrical Interconnects
WO	05/18/2011	PCT/US2011/036941	WO 2011/146579	Electrical Connector Between Die Pad and Z-Interconnect for Stacked Die Assemblies
WO	09/26/2011	PCT/US2011/053294	WO 2012/050812	Semiconductor Die Having Fine Pitch Electrical Interconnects

J. Foreign Listed Abandoned/Expired/Unknown Status Patents and Applications

Foreign Abandoned and Expired Patents and Applications

Patent Number	Country	Filing Date	Application Number	Issue Date	Publication Number	Title
-	DE	8/20/1992	3872828	-	DE3872828	Halbleterkristallplaettchen-Stapel
695 24 756.5	DE	06/08/1995	95923676.1	12/19/2001	766909	Method for Forming Vertical Interconnect Process for Silicon Segments with Dielectric Isolation
695 34 976.7	DE	06/08/1995	01115235.2	5/3/2006	1158570	Conductive epoxy flip-chip on chip
0314437	EP	10/25/1988	88310029.9	07/15/1992	-	Semiconductor Wafer Array
-	EP	08/14/1998	98943211.7	-	1029346	Vertical interconnect process for silicon segments with thermally conductive epoxy preform
-	EP	08/14/1998	98944438.5	-	1029360	Vertical interconnect process for silicon segments with dielectric isolation
-	EP	04/12/2005	05735136.3	-	1743369	Micropede Stacked Die Component Assembly
-	EP	04/12/2005	05736129.7	-	1743370	Three Dimensional Six Surface Conformal Die Coating
-	EP	04/12/2005	05736405.1	-	1763894	Stacked Die BGA or LGA Component Assembly
-	FR	06/08/1995	95923676.1	12/19/2001	766909	Vertical Interconnect Process for Silicon Segments
-	FR	06/08/1995	01115235.2	5/3/2006	1158570	Vertical Interconnect Process for Silicon Segments
-	GB	06/08/1995	95923676.1	12/19/2001	766909	Vertical Interconnect Process for Silicon Segments
-	GB	06/08/1995	01115235.2	5/3/2006	1158570	Vertical Interconnect Process for Silicon Segments
2117118	JP	10/27/1988	63-271951	-	02-001152	Semiconductor Wafer Array and its Manufacture
3895768	JP	06/08/1995	08-503164	03/22/2007	10-508154	The perpendicular/vertical interconnection method for a silicon/silicone segment
-	JP	07/29/1998	2000-505650	-	2001-512292A	Conductive epoxy flip-chip on chip
-	JP	08/14/1998	2000-508139	-	2001-514449	Vertical interconnect process for silicon segments with thermally Conductive Epoxy Preform
-	JP	08/14/1998	2000-510170	-	2001-516148	Vertical Interconnect Process for Silicon Segments with Dielectric Isolation
-	JP	08/11/2006	2006-220350	-	2007-019527	Method of Vertical Interconnection for Silicon Segments
-	JP	06/15/2009	2011-514731	-	2011-525055	Semiconductor Die Separation Method
-	JP	08/28/2009	2011-525248	-	2012-501555	Image Sensor
-	KR	07/29/1998	10-2000-7000963	-	10-2001-0022384	Conductive Epoxy Flip-Chip on Chip

Patent Number	Country	Filing Date	Application Number	Issue Date	Publication Number	Title
-	KR	04/12/2005	10-2006-7023768	-	-	Three Dimensional Six Surface Conformal Die Coating
766909	NL	06/08/1995	95923676.1	12/19/2001	766909	Vertical Interconnect Process for Silicon Segments
1158570	NL	06/08/1995	01115235.2	05/03/2006	1158570	Vertical Interconnect Process for Silicon Segments
271487	TW	08/12/1994	83107388	03/01/1996	-	-
-	TW	04/11/2005	94111357	-	200603257	Three Dimensional Six Surface Conformal Die Coating
-	TW	03/13/2008	97108898	-	200903752	Vertical electrical interconnect formed on support prior to die mount
-	TW	08/28/2009	98129108	-	201015707	Image Sensor
-	WO	06/08/1995	PCT/1995/06884	-	WO 1996/000494	Vertical Interconnect Process for Silicon Segments
-	WO	12/28/1995	PCT/US1995/16704	-	WO 96/22620	Conductive Epoxy Flip-Chip
-	WO	12/28/1995	PCT/US1995/17020	-	WO 96/22622	Silicon segment programming method and apparatus
-	WO	07/29/1998	PCT/US1998/15659	-	WO 99/007015	Conductive Epoxy Flip-Chip on Chip
-	WO	08/14/1998	PCT/US1998/16901	-	WO 1999/10925	Vertical interconnect process for silicon segments with thermally Conductive Epoxy Preform
-	WO	08/14/1998	PCT/US1998/16900	-	WO/1999/009599	Vertical Interconnect Process for Silicon Segments with Dielectric Isolation
-	WO	07/20/2001	PCT/US01/23018	-	WO/2002/001981	Vertically Integrated Chip on Chip Circuit Stack
-	WO	04/12/2005	PCT/US2005/12373	-	WO 2005/101494	Three Dimensional Six Surface Conformal Die Coating
-	WO	04/12/2005	PCT/US2005/12412	-	WO 2005/101492	Stacked Die BGA or LGA Component Assembly
-	WO	04/12/2005	PCT/US2005/12394	-	WO 2005/101491	Micropede Stacked Die Component Assembly
-	WO	03/12/2008	PCT/US2008/56633	-	WO 2008/115744	Vertical electrical interconnect formed on support prior to die mount
-	WO	06/04/2008	PCT/US2008/65788	-	WO 2009/32371	Electrical Interconnect Formed by Pulsed Dispense
-	WO	06/04/2008	PCT/US2008/65793	-	WO 2008/154255	Electrically Interconnected Stacked Die Assemblies
-	WO	06/11/2008	PCT/US2008/66561	-	WO 2008/154580	Method for Optimized Integrated Circuit Chip Interconnection
-	WO	06/11/2008	PCT/US2008/66568	-	WO/2008/154582	Semiconductor Die Coating and Interconnection Fixture and Method
-	WO	06/19/2008	PCT/US2008/067541	-	WO 2008/157722	Wafer level surface passivation of stackable integrated circuit chips

Patent Number	Country	Filing Date	Application Number	Issue Date	Publication Number	Title
-	WO	06/20/2008	PCT/US2008/67722	-	WO 2008/157779	Three-dimensional circuitry formed on integrated circuit device using two-dimensional fabrication
-	WO	08/26/2008	PCT/US2008/073365	-	WO 2009/026171	Stacked Die Vertical Interconnect Formed by Transfer of Interconnect Material
-	WO	08/27/2008	PCT/US2008/74450	-	WO 2009/35849	Semiconductor Die Mount by Conformal Die Coating
-	WO	10/15/2008	PCT/US2008/79948	-	WO 09/52150	Chip Scale Stacked Die Package
-	WO	02/18/2009	PCT/US2009/34368	-	WO 2009/105449	Flat leadless packages and stacked leadless package assemblies
-	WO	03/12/2009	PCT/US2009/36921	-	WO 2009/114670	Support mounted electrically interconnected die assembly
-	WO	06/15/2009	PCT/US2009/47389	-	WO 2009/155247	Semiconductor Die Separation Method
-	WO	08/28/2009	PCT/US2009/55421	-	WO 2010/025401	Image Sensor
-	WO	12/09/2009	PCT/US2009/67386	-	WO 2010/068699	Semiconductor Die Interconnect Formed by Aerosol Application of Electrically Conductive Material
-	WO	05/10/2010	PCT/US2010/34198	-	WO 2010/132338	Flip-chip underfill
-	WO	06/23/2010	PCT/US2010/39639	-	WO 2010/151578	Electrical interconnect for die stacked in zig-zag configuration
-	WO	10/27/2010	PCT/US2010/54325	-	WO 2011/056668	Selective Die Electrical Insulation By Additive Process
-	WO	11/04/2010	PCT/US2010/55472	-	WO 2011/056987	Stacked Die Assembly Having Reduced Stress Electrical Interconnects

2944588_1.DOC