PATENT ASSIGNMENT

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
MetaRAM, Inc.	09/11/2009

RECEIVING PARTY DATA

Name:	Google Inc.
Street Address:	1600 Amphitheatre Parkway
City:	Mountain View
State/Country:	CALIFORNIA
Postal Code:	94043

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	13620199

CH $40.00 13620199

CORRESPONDENCE DATA

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ATTORNEY DOCKET NUMBER:	16113-1941002
NAME OF SUBMITTER:	Lori L. Stewart/
Signature:	/Lori L. Stewart/
Date:	05/20/2013

Total Attachments: 6

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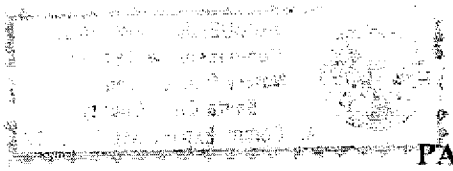

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

PATENT ASSIGNMENT

WHEREAS, MetaRAM, Inc., hereinafter referred to as "Assignor," a Delaware corporation with a place of business at 101 Metro Drive, Suite 350, San Jose CA 95110 is the sole owner of the entire right, title and interest in and to the patents and patent applications listed in Exhibit A to this Assignment (collectively, "Listed Patents and Applications"); and

WHEREAS, Google Inc., hereinafter referred to as "Assignee," a Delaware corporation with a place of business at 1600 Amphitheatre Parkway, Mountain View, CA 94043, is desirous of obtaining the entire right, title and interest in and to the Listed Patents and Applications;

NOW, THEREFORE, in consideration of good and valuable consideration, the receipt of which is hereby acknowledged, Assignor has sold, assigned, transferred and set over, and by these presents does hereby sell, assign, transfer and set over, unto said Assignee, its successors, legal representatives and assigns, its entire right, title and interest in, to and under the said the Listed Patents and Applications, including all pending applications, as well as all divisions, renewals and continuations thereof, and all Letters Patent of the United States which may be granted thereon and all reissues and extensions thereof, and all applications for Letters Patent which may hereafter be filed for inventions embodied by said pending applications in any country or countries foreign to the United States, and all Letters Patent which may be granted for said inventions embodied by said pending applications in any country or countries foreign to the United States and all extensions, renewals and reissues thereof and all rights of priority in any such country or countries based upon the filing of said pending applications in the United States which are created by any law, treaty or international convention; and I hereby authorize and request the Commissioner of Patents of the United States, and any Official of any country or countries foreign to the United States, whose duty it is to issue patents on any such applications as aforesaid, to issue all Letters Patent for said inventions to Google Inc., its successors, legal representatives and assigns, in accordance with the terms of this instrument.

IN WITNESS WHEREOF, MetaRAM, Inc., has caused this instrument to be signed by a duly authorized corporate officer and its corporate seal to be affixed, as of this 11TH day of SEPTEMBER, 2009.

MetaRAM, Inc.

By: _____

Name: SURESH RAJAN

Title: PRESIDENT & CEO

JACQUELINE LAWRENCE
Commission # 1812785
Notary Public - California
Santa Clara County
My Comm. Expires Sep 11, 2012

STATE OF California)
) ss
COUNTY OF Santa Clara)

On this 11th day of September, 2009 before me personally appeared Suresh Rajan ~~personally known to me (or~~ proved on the basis of satisfactory evidence) to be the person whose name is subscribed to this Assignment, who, being duly sworn, did say that he is the President and CEO of MetaRAM, Inc., and that he duly executed the foregoing instrument for and on behalf of MetaRAM, Inc., being duly authorized to do so and that said individual acknowledged said instrument to be the free act and deed of said corporation.

Notary Public

My commission expires: Sep. 11, 2012

ACCEPTED BY:

Date: SEPTEMBER 11, 2009

GOOGLE INC.

By:

Name: DONALD HARRISON

Title: DEPUTY GENERAL COUNSEL

STATE OF California)
) SS
COUNTY OF Santa clara)

On SEPTEMBER 11TH, 2009, before me, Mariano Curat, notary Public, personally appeared Donald E. Harrison who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to this Assignment and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on this Assignment the person(s), or the entity upon behalf of which the person(s) acted, executed this Assignment.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

Notary Public

MARIANO CURAT
Commission # 1851849
Notary Public - California
San Francisco County
My Comm. Expires Jun 28, 2013

Exhibit A

MRAM ID	ID	Title	Jurisdiction
0001	60/693631	An Integrated Memory Core And Memory Interface Circuit	US
0001	PCT/US2007002324	An Integrated Memory Core And Memory Interface Circuit	WO
0001	7515453	An Integrated Memory Core And Memory Interface Circuit	US
0002	60/713815	Methods And Apparatus of Stacking DRAMs	US
0003	60/772414	Multi-Rank Memory Buffer and Memory Stack	US
0005	60/814234	Memory Systems and Memory Modules	US
0006	11/515167	Stackable Low-Profile Lead Frame Package	US
0007	11/588739	Active Raw Card For Dual In-Line Memory Module	US
0009	US20070014168	Method and Circuit For Configuring Memory Core Integrated Circuit Dies With Memory Interface Integrated Circuit Dies	US
0010	US20080027702	System And Method For Simulating A Different Number Of Memory Circuits	US
0011	US20080025137	System And Method For Simulating An Aspect Of A Memory Circuit	US
0012	US20080025108	System And Method For Delaying A Signal Communicated From A System To At Least One Of A Plurality Of Memory Circuits	US
0013	US20080025136	System And Method For Storing At Least A Portion Of Information Received In Association With A First Operation For Use In Performing A Second Operation	US
0014	US20080031072	Power Saving System And Method For Use With A Plurality Of Memory Circuits	US
0015	US20080025122	Memory Refresh System And Method	US
0016	US20080028135	Multiple-Component Memory Interface System And Method	US
0017	7379316	Methods And Apparatus Of Stacking DRAMs	US
0018	US20080028136	Method And Apparatus For Refresh Management Of Memory Modules	US
0019	US20080031030	System And Method For Power Management In Memory Systems	US
0020	US20070058471	Methods And Apparatus of Stacking DRAMs	US
0021	PCT/US2007028109	Methods And Apparatus of Stacking DRAMs	WO
0025	US20080027697	Memory Circuit Simulation System And Method	US

		With Power Saving Capabilities	
0026	US20080123459	Combined Signal Delay And Power Saving System And Method For Use With A Plurality Of Memory Circuits	US
0027	US20080027703	Memory Circuit Simulation System And Method With Refresh Capabilities	US
0028	60/823229	Autonomous Refresh and Data Protection in Memory Circuits	US
0030	PCT/US2008063251	Memory Circuit System and Method	WO
0034	60/826356	System, Method And Computer Program Product For Multi-Rank Asymmetric Memory Modules	US
0035	US20080037353	Interface Circuit System And Method For Performing Power Management Operations During A Command-Related Latency	US
0037	7386656	Interface Circuit System And Method For Performing Power Saving Operations In Conjunction With Only A Portion Of A Memory Circuit	US
0038	7392338	Interface Circuit System And Method For Autonomously Performing Power Saving Operations In Conjunction With A Plurality Of Memory Circuits	US
0039	US20080082763	Apparatus And Method For Power Management Of Memory Circuits By A System Or Component Thereof	US
0040	60/849631	System And Method For Increasing Capacity And Performance Of Flash Storage	US
0041	US20080086588	System And Method For Increasing Capacity, Performance, And Flexibility Of Flash Storage	US
0042	60/865624	Memory Subsystem And Method	US
0043	60/865623	Multi-Rank Partial Width Memory Modules	US
0044	60/865627	System And Method For Memory Control	US
0046	US20080115006	System And Method For Adjusting The Timing Of Signals Associated With A Memory System	US
0047	US20080056014	Memory Device With Emulated Characteristics	US
0048	US20070195613	Memory Module With Memory Stack And Interface With Enhanced Capabilities	US
0049	US20080126690	Memory Module With Memory Stack	US
0051	US20070204075	System And Method For Reducing Command Scheduling Constraints Of Memory Circuits	US
0052	PCT/US2007095080	Memory Circuit System And Method	WO
0053	US20070192563	System And Method For Translating An Address	US

		Associated With A Command Communicated Between A System And Memory Circuits	
0054	US20080010435	Memory Systems And Memory Modules	US
0055	US20080028137	Method And Apparatus For Refresh Management Of Memory Modules	US
0056	11/855805	System, Method, And Apparatus For Allowing Electrical Communication Between Integrated Circuit Package Contacts And Circuit Board Contacts	US
0060	12/144396	Memory Subsystem And Method	US
0062	US20080062773	System and Method for Simulating An Aspect Of A Memory Circuit	US
0063	61/030534	Emulation Of Abstracted DIMMs Using Abstracted DRAMs	US
0071	11/855826	System And Method For Providing Additional Space Between An Integrated Circuit And A Circuit Board For Positioning A Component Therebetween	US
0073	11/939432	System For Multi-Rank Partial Width Memory Modules	US
0074	11/858518	System And Method For Multi-Rank Asymmetric Memory Modules	US
0075	11/941589	Optimal Channel Design For Memory Devices For Providing A High-Speed Memory Interface	US
0076	US20080120443	System And Method For Reducing Command Scheduling Constraints Of Memory Circuits	US
0077	US20080109595	System And Method For Reducing Command Scheduling Constraints Of Memory Circuits	US
0078	US20080109206	Memory Device With Emulated Characteristics	US
0079	US20080126692	Memory Device With Emulated Characteristics	US
0080	US20080126687	Memory Device With Emulated Characteristics	US
0081	US20080126688	Memory Device With Emulated Characteristics	US
0082	US20080126689	Memory Device With Emulated Characteristics	US
0083	US20080103753	Memory Device With Emulated Characteristics	US
0084	US20080104314	Emulation Of Memory	US
0085	US20080133825	System And Method For Simulating An Aspect Of A Memory Circuit	US
0086	US20090024789	Memory Circuit System And Method	US
0087	US20090024790	Memory Circuit System and Method	US
0088	US20080109597	Method And Apparatus For Refresh Management Of Memory Modules	US
0089	US20080109598	Method And Apparatus For Refresh Management Of Memory Modules	US

0090	61/014740	Embossed Heat Spreader	US
0092	DE112006001810	An Integrated Memory Core And Memory Interface Circuit	DE
0093	2441726	An Integrated Memory Core And Memory Interface Circuit	GB
0094	US2008544437	An Integrated Memory Core And Memory Interface Circuit	JP
0095	10-2008-7001812	An Integrated Memory Core And Memory Interface Circuit	KR
0098	US20080239857	Interface Circuit System And Method For Performing Power Management Operations In Conjunction With Only A Portion Of A Memory Circuit	US
0099	US20080239858	Interface Circuit System And Method For Autonomously Performing Power Management Operations In Conjunction With A Plurality Of Memory Circuits	US
0100	PCT/US2008/001507	Memory Circuit System and Method	WO
0107	12/057306	Standard Hybrid Memory Module	US
0108	12/378328	Emulation Of Abstracted DIMMs Using Abstracted DRAM	US
0110	US20080170425	Methods And Apparatus of Stacking DRAMs	US
0111	DE112006002300	Methods And Apparatus of Stacking DRAMs	DE
0112	GB2444663A	Methods And Apparatus of Stacking DRAMs	GB
0113	JP2009507324	Methods And Apparatus of Stacking DRAMs	JP
0114	10-2008-7005172	Methods And Apparatus of Stacking DRAMs	KR
0115	12/203100	Embossed Heat Spreader	US
0117	61/083497	Memory Subsystem With Ganged Ranks	US
0120	2008-554369	Memory Circuit System And Method	JP
0121	10-2008-7019582	Memory Circuit System And Method	KR
0122	2005303	Memory Circuit System And Method	EU
0124	61/083878	Memory Subsystem With Ganged Ranks	US
0126	12/508496	Configurable Memory System	US
0127	EU2054803	Memory Circuit System And Method	EU
0130	61/185585	Programming Of DIMM Termination Resistance Values	US
0133	12/507682	System And Method For Simulating An Aspect Of A Memory Circuit	US
0134	12/510134	Method And Circuit For Configuring Memory Core Integrated Circuit Dies With Memory Interface Integrated Circuit Dies	US