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U.S. DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

# RECORDATION FORM COVER SHEET
# PATENTS ONLY

To the Director of the U.S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

**1. Name of conveying party(ies):**
Atwater Ventures Limited

Additional name(s) of conveying party(ies) attached? [ ] Yes [X] No

**2. Name and address of receiving party(ies)**

Name: Invensas Corporation
Internal Address:
Street Address:
2702 Orchard Parkway
City: San Jose
State: California
Country: United States of America Zip: 95134
Additional name(s) & address(es) attached? [ ] Yes [X] No

**3. Nature of conveyance/Execution Date(s):**

Execution Date(s): April 18, 2013

[X] Assignment [ ] Merger [ ] Change of Name
[ ] Security Agreement [ ] Joint Research Agreement
[ ] Government Interest Assignment
[ ] Executive Order 9424, Confirmatory License
[ ] Other

**4. Application or patent number(s):**

[ ] This document is being filed together with a new application.

A. Patent Application No.(s)
12/991,143

B. Patent No.(s)
7,576,413 8,017,452
7,825,026 8,110,911
7,838,983 8,399,980

Additional numbers attached? [ ] Yes [X] No

**5. Name and address to whom correspondence concerning document should be mailed:**

Name: Daryl K. Neff
LERNER, DAVID, LITTENBERG, KRUMHOLZ & MENTLIK, LLP
Internal Address: Atty. Dkt.: TIPI 5.2-038
Street Address: 600 South Avenue West
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Fax Number: 908-654-7866
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**6. Total number of applications and patents involved:** 7

**7. Total fee** (37 CFR 1.21(h) & 3.41) $ 280.00

[X] Authorized to be charged to deposit account
[ ] Enclosed
[ ] None required (government interest not affecting title)

**8. Payment Information**

Deposit Account Number 12-1095
Authorized User Name Daryl K. Neff

**9. Signature:**

Signature — Date: May 22, 2013

Daryl K. Neff - 38,253
Name of Person Signing

Total number of pages including cover sheet, attachments, and documents: 9

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CH $280.00 121095 1299114

**DEED OF ASSIGNMENT**

THIS DEED OF ASSIGNMENT ("**Assignment**"), EFFECTIVE AS OF APRIL 19 2013, IS MADE BY AND BETWEEN

Atwater Ventures Limited (hereinafter "**ASSIGNOR**"), a Bahamian company, with its principal place of business located at New Providence Financial Center, Suite 1000, East Bay Street, Nassau, Bahamas; and

Invensas Corporation (hereinafter "**ASSIGNEE**"), a Delaware corporation, with its principal place of business located at 2702 Orchard Parkway, San Jose, California 95134, United States of America.

WHEREAS:

A **ASSIGNOR** is the sole owner in respect of the patents and patent applications listed in the attached Appendix (hereinafter "the **PATENTS**"); and

B **ASSIGNEE** is desirous of acquiring all of the worldwide right, title and interest in and to the **PATENTS** and the inventions disclosed therein.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, **ASSIGNOR** has sold, assigned and transferred, and does hereby sell, assign and transfer to **ASSIGNEE** all of the worldwide right, title and interest in (i) the **PATENTS** and the inventions and improvements disclosed therein; (ii) all reissues, divisionals, continuations, continuations-in-part, extensions, renewals, reexaminations and foreign counterparts thereof, and other patents, patent applications, certificates of invention other governmental grants resulting from the **PATENTS**; (iii) all patents and applications which claim priority to or have common disclosure or common priority with any such patents or patent applications (for the avoidance of doubt, patents which include partial commonalities such as figures or patents whose features of the inventions are different from those of the **PATENTS** may be excluded), and (iv) any **PATENT** that as of the Effective Date is subject to a Disclaimer Issue with respect to any other such patent or patent application; and (v) all rights corresponding to any of the foregoing throughout the world (including the right to claim the priority date of any of the **PATENTS** and the right to sue for and recover damages for any past, present or future infringement of the Patents), the same to be held and enjoyed by **ASSIGNEE** for its own use and enjoyment, and for the use and enjoyment of its successors, assigns and other legal representatives, to the end of the term or terms of said **PATENTS** granted or reissued or reexamined as fully and entirely as the same would have been held and enjoyed by **ASSIGNOR**, if this assignment and sale had not been made.

IN WITNESS WHEREOF, **ASSIGNOR** has caused these presents to be signed by its duly appointed trustee having full authority to convey its property; and **ASSIGNEE** has caused these presents to be signed by its duly appointed trustee.

And if the issue date and/or patent number of any of the **PATENTS** is unknown to **ASSIGNOR** and **ASSIGNEE** at the time this Assignment is executed, **ASSIGNOR** does hereby authorize its attorneys to insert on this Assignment the issue date and patent number of said any patent when known.

**ASSIGNOR** hereby declares that **ASSIGNEE** may take the steps for recordal of this assignment in the sole name of **ASSIGNEE**.

**ASSIGNOR** hereby undertakes that it shall, without further consideration, but at the expense of **ASSIGNEE**, execute all documents and do all such acts and things as **ASSIGNEE** may in its absolute discretion consider necessary or desirable to enable Letters Patent or any other form of protection to be issued in respect of any of said **PATENTS** and the inventions disclosed therein in any part of the world. **ASSIGNOR** also agrees, without further consideration, but at the expense of **ASSIGNEE**, to enable or to assist **ASSIGNEE** to defend oppositions thereto, to maintain the **PATENTS** and to prosecute for the infringement thereof.

SIGNED for and on behalf of

**ATWATER VENTURES LIMITED**

By _____ on April 18, 2013
(Signature) (Date)

Nathaniel Bosfield, Director
(Print Name and Title)

Commonwealth of The Bahamas:

New Providence

On this 18th day of April, 2013 before me, Frederica G. McCartney, personally appeared Nathaniel Bosfield, who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

Before me,
_____
(Notary Public)

SIGNED for and on behalf of

**INVENSAS CORPORATION**

by _____ on May 9th, 2013
(Signature) (Date)

Simon McElrea, President
(Print Name and Title)

State of California ) SS:

County of )

On this 9th day of May, 2013 before me, Lisa A. Gianotti, personally appeared Simon McElrea, who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

_____
(Notary Public)

LISA A. GIANOTTI
Commission # 1982878
Notary Public - California
Santa Clara County
My Comm. Expires Oct 1, 2016

**APPENDIX**
**LISTED PATENTS AND PATENT APPLICATIONS**

Date Format (MM/DD/YYYY)

1. United States Listed Issued Patents and Pending Patent Applications

US Issued Patents

| Patent Number | Filing Date | Application Number | Issue Date | Publication Number | Title |
|---|---|---|---|---|---|
| 7576413 | 03/29/2007 | 11/576,323 | 08/18/2009 | US 2008-0061402 | Packaged Stacked Semiconductor Device and Method for Manufacturing the Same |
| 7825026 | 11/15/2006 | 11/569,144 | 11/02/2010 | US 2007-0187812 | Method for Processing Copper Surface, Method for Forming Copper Pattern Wiring and Semiconductor Device Manufacturing Using Such Method |
| 7838983 | 10/19/2007 | 11/911,990 | 11/23/2010 | US 2009-0140364 | Packaged Semiconductor Device and Method of Manufacturing the Packaged Semiconductor Device |
| 8017452 | 10/28/2008 | 12/259,329 | 09/13/2011 | US 2009-0050994 | Method of Manufacturing Semiconductor Device with Electrode for External Connection and Semiconductor Device Obtained by Means of Said Method |
| 8110911 | 07/22/2010 | 12/864,125 | 02/07/2012 | US 2010-0295178 | Semiconductor Chip Package with Post Electrodes |
| 8399980 | 09/29/2010 | 12/935,341 | 03/19/2013 | US 2011-0012269 | Electronic Component Used for Wiring and Method for Manufacturing the Same |

US Pending Applications

| Application Number | Filing Date | Publication Number | Title |
|---|---|---|---|
| 12/991,143 | 11/05/2010 | US 2011-0057325 | Chip-Size Double Side Connection Package and Method for Manufacturing the Same |

2. Foreign Listed Issued Patents and Pending Patent Applications

Foreign Issued Patents

| Patent Number | Country | Filing Date | Application Number | Issue Date | Publication Number | Title |
|---|---|---|---|---|---|---|
| ZL2009801 16752.1 | CN | 05/07/2009 | 2009801167 52.1 | 10/10/2012 | 102017133 | Chip-Size Double Side Connection Package and Method for Manufacturing the Same |
| 4635202 | JP | 07/20/2005 | 2005-209450 | 12/03/2010 | 2007-027526 | The Manufacturing Method of a Double-Sided Electrode Package |
| 4783906 | JP | 11/29/2005 | 2006-547931 | 07/22/2011 | - | The Packaged Laminated Semiconductor Device and Its Manufacturing Method |
| 4765055 | JP | 06/07/2004 | 2004-167891 | 06/24/2011 | 2005-347654 | Forming Method of Copper Surface Protection Film and Processing Method of Copper Surface Where Protection Film is Formed |
| 4635209 | JP | 04/04/2006 | 2007-514522 | 12/03/2010 | - | The Manufacturing Method of a Semiconductor Package |
| 4274290 | JP | 11/15/2007 | 2008-529403 | 03/13/2009 | - | The Manufacturing Method of the Semiconductor Device of a Double-Sided Electrode Structure |
| 3870273 | JP | 08/12/2005 | 2005-233994 | 10/27/2006 | 2006-210872 | Process for Forming copper Pattern Interconnect Line, Semiconductor Device Fabricated Using That Method, and Nano Copper Metal Particle |
| 10-1189100 | KR | 04/04/2006 | 10-2007-7024617 | 10/02/2012 | 10-2008-0003832 | Semiconductor Package and Method for Manufacturing Same |
| 10-1150322 | KR | 01/16/2009 | 10-2010-7014511 | 05/21/2012 | 10-2010-0089894 | Semiconductor Chip Package and Manufacturing Method Thereof |

| Patent Number | Country | Filing Date | Application Number | Issue Date | Publication Number | Title |
|---|---|---|---|---|---|---|
| 10-1169580 | KR | 03/27/2009 | 10-2010-7017429 | 07/24/2012 | 10-2010-0108587 | Electronic Component Used for Wiring and Method for Manufacturing the Same |
| 10-1195786 | KR | 05/07/2009 | 10-2010-7024709 | 10/24/2012 | 10-2010-0129784 | Chip-Size Double Side Connection Package and Method for Manufacturing the Same |
| I305034 | TW | 04/24/2006 | 095114554 | 01/01/2009 | 2007-03589 | Packaged semiconductor device and method of manufacturing the packaged semiconductor device |

Foreign Pending Applications

| Country | Filing Date | Application Number | Publication Number | Title |
|---|---|---|---|---|
| CN | 03/27/2009 | 200980111830.9 | 101983429 | Electronic Component Used for Wiring and Method for Manufacturing the Same |
| EP | 01/16/2009 | 09707063.5 | 2239773 | Semiconductor Chip Package and Manufacturing Method Thereof |
| EP | 03/27/2009 | 09728901.1 | 2261974 | Electronic Component Used for Wiring and Method for Manufacturing the Same |
| JP | 01/31/2008 | 2008-020775 | 2009-182208 | Semiconductor Chip Package, and Method of Manufacturing the Same |
| JP | 03/31/2008 | 2008-090189 | 2009-246104 | Electronic Method for Wiring and its Manufacturing Method |
| JP | 11/14/2008 | 2008-292360 | 2010-118614 | Semiconductor Device Packaging Structure and Its Manufacturing Method |
| JP | 05/07/2009 | 2010-511020 | - | Chip-Size Double Side Connection Package and Method for Manufacturing the Same |
| TW | 03/27/2009 | 098110152 | 201013889 | Electronic Component Used for Wiring and Method for Manufacturing the Same |

3. US and Foreign Listed Abandoned/Expired Patents and Applications

| Patent Number | Country | Filing Date | Application Number | Issue Date | Publication Number | Title |
|---|---|---|---|---|---|---|
| - | JP | 12/28/2004 | 2004-378965 | - | - | Process for Forming Copper Pattern Interconnect Line, Semiconductor Device Fabricated Using That Method, and Nano Copper Metal Particle |
| - | JP | 11/28/2006 | 2006-320058 | - | - | Method for Manufacturing Semiconductor Device Having Dual-Face Electrode Structure and Semiconductor Device Manufactured by the Method |
| - | JP | 05/09/2008 | 2008-123445 | - | - | Chip-Size Double Side Connection Package and Method for Manufacturing the Same |
| - | JP | 04/26/2005 | 2005-127266 | - | - | Semiconductor Package and Method for Manufacturing Same |
| - | JP | 11/30/2004 | 2004-345274 | - | - | Packaged Stacked Semiconductor Device and Method for Manufacturing Same |
| - | WO | 06/03/2005 | PCT/JP2005/010223 | - | WO 2005/122230 | Method for Processing Copper Surface, Method for Forming Copper Pattern Wiring and Semiconductor Device Manufactured Using Such Method |
| - | WO | 11/29/2005 | PCT/JP2005/021852 | - | WO 2006/059589 | Packaged Stacked Semiconductor Device and Method for Manufacturing Same |
| - | WO | 04/04/2006 | PCT/JP2006/307087 | - | WO 2006/117961 | Semiconductor Package and Method for Manufacturing Same |
| - | WO | 11/15/2007 | PCT/JP2007/072157 | - | WO 2008/065896 | Method for Manufacturing Semiconductor Device Having Dual-Face Electrode Structure and Semiconductor Device Manufactured by the Method |

| Patent Number | Country | Filing Date | Application Number | Issue Date | Publication Number | Title |
|---|---|---|---|---|---|---|
| - | WO | 01/06/2009 | PCT/JP2009/050530 | - | WO 2009/096240 | Semiconductor Chip Package and Manufacturing Method Thereof |
| - | WO | 03/27/2009 | PCT/JP2009/056273 | - | WO 2009/123048 | Electronic Component Used for Wiring and Method for Manufacturing the Same |
| - | WO | 05/07/2009 | PCT/JP2009/001998 | - | WO 2009/136495 | Chip-Size Double Side Connection Package and Method for Manufacturing the Same |