PATENT ASSIGNMENT

Electronic Version v1.1
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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Acacia Research Group LLC	02/10/2012

RECEIVING PARTY DATA

Name:	Chip Packaging Solutions LLC
Street Address:	6136 Frisco Square Blvd.
Internal Address:	Suite 385
City:	Frisco
State/Country:	TEXAS
Postal Code:	75034

PROPERTY NUMBERS Total: 16

Property Type	Number
Patent Number:	6369451
Patent Number:	6677668
Patent Number:	6002178
Patent Number:	6249052
Patent Number:	6093969
Patent Number:	6301121
Patent Number:	5838072
Patent Number:	6392304
Patent Number:	6785617
Patent Number:	6588123
Patent Number:	6083792
Patent Number:	6165843
Patent Number:	6265754
Patent Number:	6184092

CH $640.00 6369451

Patent Number:	6204677
Patent Number:	5691240

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent via US Mail when the fax attempt is unsuccessful.

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NAME OF SUBMITTER:	Kristy Kappelman
Signature:	/kristy kappelman/
Date:	06/18/2013

Total Attachments: 4
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ASSIGNMENT

WHEREAS, ACACIA RESEARCH GROUP LLC, a Texas limited liability company, having a place of business at 6136 Frisco Square Blvd. Suite 385, Frisco, TX 75034 (hereafter, together with any successors, legal representatives or assigns thereof, called "Assignor") is the owner of the entire right, title, and interest and assignee of **the U.S. Patents listed in the Exhibit attached hereto**;

AND WHEREAS, CHIP PACKAGING SOLUTIONS LLC, a Texas limited liability company having a place of business at 6136 Frisco Square Blvd. Suite 385, Frisco, TX 75034 (hereafter, together with any successors, legal representatives or assigns thereof, called "ASSIGNEE") wants to acquire the entire right, title and interest in and to said **U.S. Patents listed in the Exhibit attached hereto,** and all the inventions therein, and Assignor is willing to enter into such assignment.

NOW, THEREFORE, effective on February 10, 2012 and in consideration of the sum of One Dollar ($1.00) in hand paid and other good and valuable consideration the receipt of which from ASSIGNEE is hereby acknowledged, Assignor has sold, assigned, transferred and set over, and does hereby sell, assign, transfer and set over to ASSIGNEE the entire right, title and interest in and to the **U.S. Patents listed in the Exhibit attached hereto,** and all patents, patent applications, foreign patents, foreign patent applications, continuations, continuations-in-part, divisionals, extensions, renewals, reissues and re-examinations related to all inventions thereof, including without limitation, all rights to claim priority on the basis thereof, all rights to sue for past, present and future infringement, including the right to collect and receive any damages, royalties, or settlements for such infringements, all rights to sue for injunctive or other equitable relief, and any and all causes of action relating to any of the inventions or discoveries thereof;

Assignor hereby covenants that it has full right to convey the entire interest herein assigned, and that it has not executed, and will not execute, any agreement in conflict with this Assignment;

Assignor hereby further covenants and agrees that it will communicate to ASSIGNEE any and all facts known to it respecting said patents, and testify in any legal proceeding, sign all lawful papers, execute and deliver all papers and take any actions that may be necessary or desirable to perfect the title to any aforementioned patents and inventions, execute all divisional, continuation, reexamination, reissue and substitute applications, and make all rightful oaths and generally do everything possible to aid ASSIGNEE to obtain and enforce proper patent protection for said inventions in all countries.

FOR USPTO RECORDING

IN TESTIMONY WHEREOF, I hereunto set my hand this 10th day of February, 2012.

ACACIA RESEARCH GROUP LLC
(Assignor)

By _____

Name: Dooyong Lee

Title: Chief Executive Officer

EXHIBIT

U.S. PATENTS & APPLICATIONS

US Patent No.	US Appl. No.	Filing Date	Issue Date	Title
6,369,451	09/229,139	1/12/1999	4/9/2002	Solder balls and columns with stratified underfills on substrate for flip chip joining
6,677,668	09/727,913	11/28/2000	1/13/2004	Configuration for testing a substrate mounted with a most performance-demanding integrated circuit
	*60/071,177	01-13-1998		SOLDER BALLS AND COLUMNS WITH STRATIFIED UNDERFILLS ON SUBSTRATE FOR FLIP CHIP JOINING
6,002,178	08/968,981	11/12/1997	12/14/1999	Multiple chip module configuration to simplify testing process and reuse of known-good chip-size package (CSP)
6,249,052	09/314,493	5/18/1999	6/19/2001	Substrate on chip (SOC) multiple-chip module (MCM) with chip-size-package (CSP) ready configuration
	*60/087,604	06-01-1998		SUBSTRATE ON CHIP (SOC) MULTIPLE-CHIP MODULE (MCM) WITH CHIP-SIZE-PACKAGE (CSP) READY CONFIGURATION
	90/009,741			SUBSTRATE ON CHIP (SOC) MULTIPLE-CHIP MODULE (MCM) WITH CHIP-SIZE-PACKAGE (CSP) READY CONFIGURATION
	90/009,784	07-20-2010		SUBSTRATE ON CHIP (SOC) MULTIPLE-CHIP MODULE (MCM) WITH CHIP-SIZE-PACKAGE (CSP) READY CONFIGURATION
6,093,969	09/313,562	5/13/1999	7/25/2000	Face-to-face (FTF) stacked assembly of substrate-on-bare-chip (SOBC) modules
6,301,121	09/287,218	4/5/1999	10/9/2001	Direct-chip-attach (DCA) multiple chip module (MCM) with repair-chip ready site to simplify assembling and testing process
5,838,072	08/805,391	2/24/1997	11/17/1998	Intrachip power distribution package and method for semiconductors having a supply node electrically interconnected with one or more
6,392,304	09/190,660	11/12/1998	5/21/2002	Multi-chip memory apparatus and associated method
	*09/894,739	06-28-2001		Multi-chip memory apparatus and associated method
6,785,617	09/905,416	7/13/2001	8/31/2004	Method and apparatus for wafer analysis
6,588,123	10/004,680	12/5/2001	7/8/2003	Apparatus and method for preventing a wafer mapping system of an SMIF system from being polluted by corrosive gases remaining on wafers
*5,691,223	08/772,210	12/20/1996	11/25/1997	Method of fabricating a capacitor over a bit line DRAM process
6,083,792	08/774,753	12/30/1996	7/4/2000	Manufacturing process of a split gate flash

				memory unit
6,165,843	09/048,832	3/20/1998	12/26/2000	Covered slit isolation between integrated circuit devices
6,265,754	09/687,022	10/13/2000	7/24/2001	Covered slit isolation between integrated circuit devices
6,184,092	09/444,988	11/23/1999	2/6/2001	Self-aligned contact for trench DMOS transistors
6,204,677	09/159,079	9/22/1998	3/20/2001	Contact pressure jig for signal analysis
5,691,240	08/754,602	11/20/1996	11/25/1997	Method for forming blanket planarization of the multilevel interconnection

* Denotes expired or abandoned patent or patent application