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RECORDATION FORM COVER SHEET
PATENTS ONLY

To the Director of the U.S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

1. Name of conveying party(ies):
Micron Technology, Inc.

Additional name(s) of conveying party(ies) attached? [ ] Yes [X] No

2. Name and address of receiving party(ies)
Name: Round Rock Research, LLC
Internal Address:
Street Address:
Suite 2100
101 Hudson Street
City: Jersey City
State: New Jersey
Country: United States of America Zip: 07302
Additional name(s) & address(es) attached? [ ] Yes [X] No

3. Nature of conveyance/Execution Date(s):
Execution Date(s): December 23, 2009
[X] Assignment [ ] Merger [ ] Change of Name
[ ] Security Agreement [ ] Joint Research Agreement
[ ] Government Interest Assignment
[ ] Executive Order 9424, Confirmatory License
[ ] Other

4. Application or patent number(s):
[ ] This document is being filed together with a new application.
A. Patent Application No.(s)
12/925,280
B. Patent No.(s)
Additional numbers attached? [ ] Yes [X] No

5. Name and address to whom correspondence concerning document should be mailed:
Name: Richard J. Botos
LERNER DAVID, LITTENBERG, KRUMHOLZ & MENTLIK, LLP
Internal Address: Atty. Dkt.:
Street Address: 600 South Avenue West
City: Westfield
State: NJ Zip: 07090
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Fax Number: 908-654-7866
Email Address: mcormier@ldlkm.com

6. Total number of applications and patents involved: 1

7. Total fee (37 CFR 1.21(h) & 3.41) $ 40.00
[X] Authorized to be charged to deposit account
[ ] Enclosed
[ ] None required (government interest not affecting title)

8. Payment Information
Deposit Account Number 12-1095
Authorized User Name Richard J. Botos

9. Signature:
Signature — July 10, 2013 Date
Richard J. Botos - 32,016
Name of Person Signing
Total number of pages including cover sheet, attachments, and documents: 5

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CH $40.00 121095 12925280

EXHIBIT A

CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS

This Confirmatory Assignment of Patent Rights (the "Agreement") is entered into this 30th day of December, 2009 (the "Closing Date"), by and between Micron Technology, Inc., a Delaware corporation ("Assignor"), and Round Rock Research, LLC, a Delaware limited liability company ("Assignee").

WHEREAS, Assignor and Assignee are party to that certain Patent Sale and Transfer Agreement dated on or about the date hereof (as in effect from time to time, the "Patent Sale and Transfer Agreement"); capitalized terms used but not otherwise defined in this Agreement shall have the respective meaning assigned thereto in the Patent Sale and Transfer Agreement;

WHEREAS, pursuant to the Patent Sale and Transfer Agreement, Assignor has agreed to sell, convey, transfer, assign and deliver to Assignee all of Assignor's (and its Subsidiaries') right, title and interest, including Patent Rights, in and to the Patents listed on Schedule A hereto (collectively, the "Assigned Patents");

WHEREAS, Assignee is now desirous of acquiring the entire and exclusive right, title and interest in and to the Assigned Patents in the United States and throughout the world; and

WHEREAS, Assignor is now willing to assign to Assignee all rights, title and interest in and to the Assigned Patents in the United States and throughout the world; and

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged by Assignor, Assignor hereby assigns, transfers and conveys to Assignee, its successors, legal representatives and assigns, and Assignee hereby accepts, all of Assignor's right, title and interest in the United States and throughout the world in and to the Assigned Patents and any and all Letters Patent that are or may be granted thereon, and any legal equivalent thereof that may be granted in any country or countries foreign to the United States, in each case including without limitation any extensions, substitutes, continuations, continuations-in-part, divisions, reissues, reexaminations, and renewals thereof, or other equivalents thereof, and further, all rights and privileges pertaining to the Assigned Patents and any and all Letters Patent that are or may be granted thereon, and any legal equivalent thereof that may be granted in any country or countries foreign to the United States, including, without limitation, the right, if any, to petition, sue or otherwise seek and recover damages, profits and any other remedy (monetary, injunctive, declaratory or other) in the United States and anywhere throughout the world for any past, present and future infringement thereof, conversion or misappropriation of, or other injury, offense, violation, breach of duty or wrong relating to, any of the Assigned Patents, or any license, agreement, contract or other matter relating thereto.

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks of the United States of America and the appropriate officers of all other jurisdictions in which the Assigned Patents are or may be registered or in which applications included among the Assigned Patents are pending, to record the title of Assignee, its successors, legal representatives and assigns, as owner of all right, title and interest in and to the Assigned Patents, and to issue to Assignee, its successors, legal representatives and assigns, all Letters Patent and any legal

equivalent thereof that may be granted in any country or countries foreign to the United States and recordations of patent rights resulting from any application included among the Assigned Patents, in accordance with the terms of this instrument.

Except to the extent that federal law preempts state law with respect to the matters covered hereby, this Agreement shall be governed by and construed in accordance with the laws of the State of Delaware, without giving effect to any of the principles of conflicts of laws thereof that would result in the application of the laws of another jurisdiction to this Agreement.

This Agreement shall be binding on, and shall inure to the benefit of, the parties hereto and their respective successors and assigns, and may be executed in two or more counterparts, each of which shall be deemed to be an original, but all of which shall constitute one and the same agreement. Each of the parties hereto agrees to accept and be bound by facsimile signatures hereto.

Each party represents that it has taken all necessary action to authorize the execution and delivery of this Agreement.

[The remainder of this page has been intentionally left blank.]

IN WITNESS WHEREOF, the parties hereto have caused this Agreement to be executed by their respective duly authorized officers, as of the date first written above.

ASSIGNOR:

MICRON TECHNOLOGY, INC.

By: _____
Name: Steve R. Appleton
Title: Chairman and CEO

ASSIGNEE:

ROUND ROCK RESEARCH, LLC

By: _____
Name: John Desmarais
Title: Manager

On this 23rd day of December 2009, before me appeared Steven R. Appleton, the person who signed this instrument, who acknowledged that he/she signed it as a free act on his/her own behalf or on behalf of the Assignor with authority to do so.

State of IDAHO)
) ss.
County of Ada)

JAN REUNER NOTARY PUBLIC STATE OF IDAHO

[Note that federal patent assignments must also include a cover sheet. See 37 C.F.R. 3.28]

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Schedule A Patents

2002-1110.01/US	US	24-May-04	METHOD AND APPARATUS FOR ESTABLISHING AND MAINTAINING DESIRED READ LATENCY IN HIGH SPEED DRAM	Issued	16-Aug-05	6930955	10/851,081
2002-1133.00/US	US	13-Nov-03	STRUCTURE AND METHOD OF FABRICATING A TRANSISTOR HAVING A TRENCH GATE	Issued	27-Sep-05	6949795	10/712,212
2002-1133.01/US	US	20-Jan-05	STRUCTURE AND METHOD OF FABRICATING A TRANSISTOR HAVING A TRENCH GATE	Issued	19-Feb-08	7332419	11/038,985
2002-1133.02/US	US	20-Sep-05	STRUCTURE AND METHOD OF FABRICATING A TRANSISTOR HAVING A TRENCH GATE	Issued	09-Oct-07	7279710	11/231,090
2002-1133.03/US	US	19-Feb-08	STRUCTURE AND METHOD OF FABRICATING A TRANSISTOR HAVING A TRENCH GATE	Pending			12/033,730
2002-1239.00/US	US	07-Apr-03	CHIP SCALE IMAGE SENSOR SEMICONDUCTOR PACKAGE	Issued	12-Jul-05	6917090	10/408,183
2002-1239.01/US	US	17-May-04	METHOD FOR FABRICATING IMAGE SENSOR SEMICONDUCTOR PACKAGE	Issued	29-Nov-05	6969632	10/847,413
2002-1239.02/US	US	26-Jul-04	IMAGING SYSTEM	Issued	08-May-07	7215015	10/899,258
2002-1261.00/US	US	02-Apr-03	PASSIVATION CMP	Issued	09-Oct-07	7279353	10/404,145
2002-1261.01/US	US	29-Jun-04	PASSIVATION PLANARIZATION	Issued	05-Sep-06	7101727	10/878,350
2002-1261.02/US	US	14-Mar-07	PASSIVATION PLANARIZATION	Pending			11/717,739
2002-1327.00/US	US	01-Apr-04	MEMORY MODULES HAVING ACCURATE OPERATING CURRENT VALUES STORED THEREON AND METHODS FOR FABRICATING AND IMPLEMENTING SUCH DEVICES	Issued	22-Jul-08	7404071	10/816,239
2002-1327.01/US	US	28-Jul-06	MEMORY MODULES HAVING ACCURATE OPERATING PARAMETERS STORED THEREON AND METHODS FOR FABRICATING AND IMPLEMENTING SUCH DEVICES	Issued	20-Jan-09	7480792	11/495,964
2002-1328.00/US	US	01-Apr-04	TECHNIQUES FOR STORING ACCURATE OPERATING CURRENT VALUES	Issued	25-Apr-06	7035159	10/816,424
2002-1328.01/US	US	24-Jan-06	TECHNIQUES FOR STORING ACCURATE OPERATING CURRENT VALUES	Issued	31-Jul-07	7251181	11/338,200
2002-1328.02/US	US	24-Jan-06	TECHNIQUES FOR STORING ACCURATE OPERATING CURRENT VALUES	Issued	03-Mar-09	7499362	11/338,279
2002-1328.03/US	US	24-Jan-06	TECHNIQUES FOR STORING ACCURATE OPERATING CURRENT VALUES	Issued	19-Feb-08	7333384	11/338,155
2002-1328.04/US	US	05-Feb-09	TECHNIQUES FOR STORING ACCURATE OPERATING CURRENT VALUES	Pending			12/366,550
2002-1371.00/US	US	24-Jun-03	MEMORY DEVICE HAVING DATA PATHS WITH MULTIPLE SPEEDS	Issued	01-Nov-05	6961269	10/608,743
2002-1371.01/US	US	28-Dec-04	MEMORY DEVICE HAVING DATA PATHS WITH MULTIPLE SPEEDS	Issued	09-Sep-08	7423918	11/024,200
2002-1371.02/US	US	29-Aug-08	MEMORY DEVICE HAVING DATA PATHS WITH MULTIPLE SPEEDS	Pending			12/201,405
2002-1401.00/US	US	19-Aug-03	HYBRID OPEN AND FOLDED DIGIT LINE ARCHITECTURE	Issued	13-Dec-05	6975552	10/644,610
2002-1495.00/CN	CN	07-May-04	NAND FLASH MEMORY WITH IMPROVED READ AND VERIFICATION THRESHOLD UNIFORMITY	Pending			0480016318.3
2002-1495.00/EP	EP	07-May-04	NAND FLASH MEMORY WITH IMPROVED READ AND VERIFICATION THRESHOLD UNIFORMITY	Pending			04 751 586.7
2002-1495.00/JP	JP	07-May-04	MEMORY WITH UNIFORMED READ AND VERIFICATION THRESHOLD	Issued	14-Nov-08	4215803	2006-532842
2002-1495.00/KR	KR	07-May-04	MEMORY WITH UNIFORM READ AND VERIFICATION THRESHOLD	Issued	13-Apr-07	709642	10-2005-7021098
2002-1495.00/SG	SG	07-May-04	NAND FLASH MEMORY WITH IMPROVED READ AND VERIFICATION THRESHOLD UNIFORMITY	Issued	29-Sep-06	117061	200507193-1
2002-1495.00/US	US	08-May-03	NAND FLASH MEMORY WITH IMPROVED READ AND VERIFICATION THRESHOLD UNIFORMITY	Issued	13-Dec-05	6975542	10/431,862
2002-1495.01/US	US	05-May-05	NAND FLASH MEMORY WITH READ AND VERIFICATION FOR THRESHOLD UNIFORMITY	Issued	18-Jul-06	7079419	11/122,708