

PATENT ASSIGNMENT

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
Name	Execution Date
RPX Corporation	07/03/2013
RECEIVING PARTY DATA	
Name:	HTC Corporation
Street Address:	No. 23, Xinghua Rd.
City:	Taoyuan City, Taoyuan County
State/Country:	TAIWAN
Postal Code:	330
PROPERTY NUMBERS Total: 31	
Property Type	Number
Patent Number:	5540601
Patent Number:	5625800
Patent Number:	5715106
Patent Number:	5787099
Patent Number:	5793236
Patent Number:	5802392
Patent Number:	5802584
Patent Number:	5812755
Patent Number:	5821798
Patent Number:	5828870
Patent Number:	5831472
Patent Number:	5853297
Patent Number:	5889972
Patent Number:	5913924
Patent Number:	5919253

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Patent Number:	5920490
Patent Number:	5923867
Patent Number:	5937182
Patent Number:	5939933
Patent Number:	5940862
Patent Number:	5948076
Patent Number:	6000018
Patent Number:	6041431
Patent Number:	6044207
Patent Number:	6092233
Patent Number:	6101585
Patent Number:	6105094
Patent Number:	6055587
Patent Number:	6154802
Patent Number:	6002737
Patent Number:	6085278

CORRESPONDENCE DATA

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ATTORNEY DOCKET NUMBER:	250840-9010
NAME OF SUBMITTER:	Daniel R. McClure
Signature:	/Daniel R. McClure/
Date:	07/18/2013

Total Attachments: 3

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EXHIBIT B

Patent Assignment

This patent assignment ("Assignment") is entered into as of July 3, 2013 by and between RPX Corporation, a Delaware corporation, with principal place of business at One Market Plaza, Steuart Tower, Suite 800, San Francisco, CA 94105 ("Assignor"), and HTC Corporation, a corporation organized under the laws of Taiwan, having a principal place of business at No. 23, Xinghua Rd., Taoyuan City, Taoyuan County 330, Taiwan, R.O.C. ("Assignee").

For good and valuable consideration, the receipt of which is hereby acknowledged, Assignor hereby irrevocably assigns to Assignee, Assignor's entire right, title, and interest throughout the world in and to:

- (a) the issued patents identified on Schedule 1 hereto (the "Assigned Patents");
- (b) all reexaminations, reissues, extensions and renewals of any of the Assigned Patents;
- (c) all causes of action (whether known or unknown or whether currently pending, filed or otherwise) and other enforcement rights under or on account of, the Assigned Patents and any of the foregoing subcategory (b), including, without limitation, all causes of action and other enforcement rights for damages, injunctive relief, and any other remedies of any kind for past, current and future infringement; and
- (d) all rights to collect royalties or other payments under or on account of the Assigned Patents and any of the foregoing subcategories (b) and (c).

The terms and conditions of this Assignment will inure to the benefit of Assignor, its successors, assigns, and other legal representatives and will be binding upon Assignee, its successors, assigns, and other legal representatives.

Assignor:

Notary Seal: (see attached)

RPX Corporation

By: Paul M. Sariceni

Name: Paul M. Sariceni

Title: SVP & Chief IP Officer

Date: July 3, 2013

PATENT

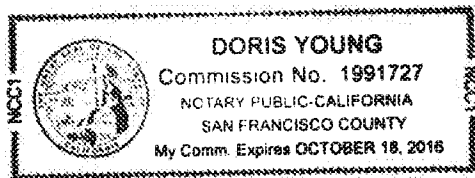
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State of California)
) ss.
County of San Francisco)

On July 3, 2013 before me, Doris Young, Notary Public, personally appeared Paul M. Saraceni, who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.



By: [Signature]
Name: Doris Young
Notary Public

My commission expires: October 18, 2016

SCHEDULE 1
PATENTS

Patent Family	Patent No.	Title
1	5540601	Adapter for computer interface
2	5625800	SCB array external to a host adapter integrated circuit
3	5715106	Disk system with headerless track format, embedded servo fields and constant density recording
4	5787099	System and method for encoding and decoding data using numerical computations in galois fields
5	5793236	Dual edge D flip flop
6	5802392	System for transferring 32-bit double word IDE data sequentially without an intervening instruction by automatically incrementing I/O port address and translating incremented address
7	5802584	Hardware alignment in a headerless disk drive architecture
8	5812755	Logical and physical zones for management of defects in a headerless disk drive architecture
9	5821798	Method for determining whether bi-directional or unidirectional data line circuits are used
10	5828870	Method and apparatus for controlling clock skew in an integrated circuit
11	5831472	Integrated circuit design for single ended receiver margin tracking
12	5853297	System and method for co-planar and nearly co-planar printed circuit board extension docking system
13	5889972	Bus to bus bridge deadlock prevention system
14	5913924	Use of a stored signal to switch between memory banks
15	5919253	Hot-switchable SCSI controller having output drivers with quick turn-on
16	5920490	Integrated circuit test stimulus verification and vector extraction system
17	5923867	Object oriented simulation modeling
18	5937182	Design verification system using expect buffers
19	5939933	Intentionally mismatched mirror process inverse current source
20	5940862	Data sector mark generation for a headerless disk drive architecture
21	5948076	Method and system for changing peripheral component interconnect configuration registers
22	6000018	System for aligning control words for identifying boundaries of headerless data sectors using automatic incrementing and discarding of data frame numbers
23	6041431	Method and apparatus for performing error correction code operations
24	6044207	Enhanced dual port I/O bus bridge
25	6092233	Pipelined Berlekamp-Massey error locator polynomial generating apparatus and method
26	6101585	Mechanism for incremental backup of on-line files
27	6105094	Method and apparatus for allocating exclusive shared resource requests in a computer system
28	6055587	Integrated circuit SCSI I/O cell having signal assertion edge triggered timed glitch filter that defines a strobe masking period to protect the contents of data latches
29	6154802	Redundant bus bridge systems and methods using separately-powered bus bridges
30	6002737	Timer using a single counter to track multiple time-outs
31	6085278	Communications interface adapter for a computer system including posting of system

PATENT

RECORDED: 07/18/2013

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