PATENT ASSIGNMENT

Electronic Version v1.1
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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Seneca Merger Sub, Inc.	01/12/2012

RECEIVING PARTY DATA

Name:	FormFactor, Inc.
Street Address:	7005 Southfront Road
City:	Livermore
State/Country:	CALIFORNIA
Postal Code:	94551

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	12334368

CH $40.00 12334368

CORRESPONDENCE DATA

Fax Number: 4087208383
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.
Phone: 408-720-8300
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Correspondent Name: James C. Scheller
Address Line 1: 1279 Oakmead Parkway
Address Line 4: Sunnyvale, CALIFORNIA 94085

ATTORNEY DOCKET NUMBER:	23227.P053
NAME OF SUBMITTER:	James C. Scheller, Reg. No. 31,195
Signature:	/James C. Scheller/
Date:	07/26/2013

Total Attachments: 10
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ASSIGNMENT

In consideration of good and valuable consideration, the receipt of which is hereby acknowledged, Seneca Merger Sub, Inc., a Delaware corporation (hereinafter referred to as "Assignor"), by its undersigned duly authorized officer, hereby sells, assigns, and transfers to FormFactor, Inc., a corporation of Delaware, having a place of business at 7005 Southfront Road, Livermore, California, 94551, (hereinafter referred to as "Assignee"), and its successors, assigns, and legal representatives, the entire world-wide right, title, and interest in and to Assignor's world-wide patent rights in and to the issued patents and patent applications listed on Schedule A, and including any and all improvements that are disclosed in the patents and applications for patents, and in and to said patents and applications and all divisional, continuing, substitute, renewal, reissue, and all other patents and patent applications that have been or shall be filed in the United States and all other countries of the world on any of said improvements; and in and to all original and reissued patents that have been or shall be issued in the United States and all other countries of the world on said improvements; and in and to all rights of priority resulting from the filing of said United States applications and patents and in and to all causes of action for past and present infringement of any of such patents and patent applications.

For: Seneca Merger Sub, Inc.

Date: January 12, 2012

By: **Name:** Stuart L. Merkadeau

Title: Vice President

For: FormFactor, Inc.

Date: January 12, 2012

By: **Name:** Stuart L. Merkadeau

Title: Senior Vice President, General Counsel and Secretary

Assignment Document Return Address:
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
1279 Oakmead Parkway
Sunnyvale, CA 94085
(408) 720-8300

ASSIGNMENT OF LETTERS PATENT AND APPLICATIONS FOR LETTERS PATENT

THIS ASSIGNMENT OF LETTERS PATENT AND APPLICATIONS FOR LETTERS PATENT (this "**Assignment**") is entered into as of October 9, 2009 by and among Electroglas, Inc., a Delaware corporation ("**Electroglas**"), Electroglas International, Inc., a Delaware corporation ("**International**", and together with Electroglas, "**Assignors**") and Seneca Merger Sub, Inc. a Delaware corporation (the "**Assignee**").

W I T N E S S E T H:

WHEREAS, Assignors and Assignee entered into that certain Asset Purchase Agreement dated as of October 9, 2009 (the "**Purchase Agreement**" capitalized terms used but not otherwise defined herein have the meanings given them in the Purchase Agreement);

WHEREAS, pursuant to the Purchase Agreement, Assignors have agreed to assign certain rights and agreements to Assignee, and Assignee has agreed to assume certain obligations of Assignors, as set forth herein and therein;

WHEREAS, Assignors are the owners of all right, title and interest in, to and under the issued patents and patent applications listed on Schedule A (collectively, the "**Patents**");

WHEREAS, Assignee is desirous of acquiring Assignors's entire worldwide right, title and interest in, to and under the Patents; and

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, the Assignee and Assignors, intending to be legally bound, agree as follows:

1. Assignors do hereby sell, assign and transfer unto Assignee their entire right, title and interest in and to the Patents and all letters patents in all countries of the world based thereon or corresponding thereto, and all divisional, continuing, continuation-in-part, and reissue applications therefor, and the patents which may be thereupon issued, including any and all rights to file applications and receive patents in all countries of the world, the same to be held and enjoyed by Assignee to the full end of the term for which said letters patent may be granted, as fully and entirely as the same would have been held and enjoyed by Assignors had this assignment and sale not been made; and Assignors hereby agree to sign all necessary papers and do all lawful acts reasonably requisite in connection with the prosecution, assignment, enforcement and disclaimer of each and every patent application based upon the Patents, without further

compensation, but at the expense of Assignee or its successors and assigns, and Assignors assign to Assignee all rights to sue for infringement, including past infringement if any, of any Patent or patent based upon or corresponding to the Patents.

2. Assignors do hereby authorize and request the officials of all countries in which the Patents are now or in the future will be issued to issue to Assignee all of Assignors's entire right, title and interest in and to the same for the sole use and enjoyment of Assignee, its successors and assigns.

3. Assignor grants the attorney of record the power to insert on this Assignment any further identification that may be necessary or desirable in order to comply with the rules of the United States Patent and Trademark Office, or rules of other entities including but not limited to United States or foreign governments or patent offices, for recordation of this document.

4. Assignors represent that each Assignor has the rights, titles, and interests to convey as set forth herein, and covenants with Assignee that the Assignors have not made and will not hereafter make any assignment, grant, mortgage, license, or other agreement affecting the right, title, and interest herein conveyed.

5. Capitalized terms used without definitions in this Assignment shall have the same meanings ascribed to such capitalized terms in the Purchase Agreement. This Assignment shall be construed and interpreted in accordance with the Purchase Agreement. Nothing in this Assignment shall, or shall be deemed to, modify or otherwise affect any provisions of the Purchase Agreement or affect or modify any of the rights or obligations of the parties under the Purchase Agreement. In the event of any conflict between the provisions hereof and the provisions of the Purchase Agreement, the provisions of the Purchase Agreement shall govern and control.

6. This Assignment may not be supplemented, altered or modified in any manner except by a writing signed by all parties hereto. The failure of any party to enforce any terms or provisions of this Assignment shall not waive any of its rights under such terms or provisions. This Assignment shall bind and inure to the benefit of the respective parties and their assigns, transferees and successors.

7. This Assignment may be executed in one or more counterparts, and by the different parties hereto in separate counterparts, each of which when executed will be deemed to be an original but all of which taken together will constitute one and the same agreement.

[Signatures appear on next page.]

IN WITNESS WHEREOF, the parties hereto have executed this Assignment of Letters Patent and Applications for Letters Patent as of the date first set forth above.

ASSIGNORS:

ELECTROGLAS, INC.

By: _____
Name: Tom Bruton
Title: CFO

ELECTROGLAS INTERNATIONAL, INC.

By: _____
Name:

ASSIGNEE:

Seneca Merger Sub, Inc.

By: _____
Name:
Title:

IN WITNESS WHEREOF, the parties hereto have executed this Assignment of Letters Patent and Applications for Letters Patent as of the date first set forth above.

ASSIGNORS:

ELECTROGLAS, INC.

By: _____
Name:
Title:

ELECTROGLAS INTERNATIONAL, INC.

By: _____
Name:

ASSIGNEE:

Seneca Merger Sub, Inc.

By: _____
Name: Jean VERMET
Title:

SCHEDULE A

US Patent Number	Title
7453260	Testing circuits on substrate
7368929	Methods and apparatuses for improved positioning in a probing system
7362116	Method for probing impact sensitive and thin layered substrate
7352198	Methods and apparatuses for improved stabilization in a probing system
7345466	Method and apparatus for cleaning a probe card
7259548	Testing circuits on substrate
7180284	Testing circuits on substrates
7098649	Testing circuits on substrates
7002337	Testing circuits on substrates
6861859	Testing circuits on substrates
6781394	Testing circuits on substrate
6771060	Testing circuits on substrates
6756801	Apparatus for electrical testing of a substrate having a plurality of terminals
6711304	Method and apparatus for measuring angular rotation of an object
6668076	Apparatus and method for projecting an alignment image
6549649	Apparatus and method for projecting an alignment image
6547409	Method and apparatus for illuminating projecting features on the surface of a semiconductor wafer
6417683	Apparatus for electrical testing of a substrate having a plurality of terminals
6389702	Method and apparatus for motion control
6320372	Apparatus and method for testing a substrate having a plurality of terminals
6310985	Measuring angular rotation of an object
6127790	Method and apparatus for passively trimming sawyer motors to correct for yaw errors
6114780	Electromagnetic actuating mechanism
6096567	Method and apparatus for direct probe sensing
5982132	Rotary wafer positioning system and method
5703969	System and method for recognizing visual indicia
5656942	Prober and tester with contact interface for integrated circuits-containing wafer held docked in a vertical plane
5553168	System and method for recognizing visual indicia
5515452	Optical character recognition illumination method and system

5450203	Method and apparatus for determining an objects position, topography and for imaging
5344238	Ball bearing assembly
5019771	Contact sensing for integr+ated circuit testing
4123706	Probe construction
4066943	High speed precision chuck assembly
4056777	Microcircuit test device with multi-axes probe control
4034293	Micro-circuit test probe
4001685	Micro-circuit test probe
3940676	Damping control for positioning apparatus
3939414	Micro-circuit test apparatus
3936743	High speed precision chuck assembly
5019771	Contact sensing for integrated circuit testing
5010295	Ball screw supported Z stage
4935676	Method of moving head to correct for hysteresis
4607525	Height measuring system
4455512	System for linear motor control
4335338	Linear motor
4324047	Universal high speed holder
4030527	Automatic cable forming system
4009428	Control system for magnetic positioning device
3814895	Laser scriber control system
3689892	Electronic control apparatus having learn and automatic operate modes
3628120	Closed loop stepping motor control system with seek reference capability
3569720	Photoelectric limit sensing assembly and system
3499714	Mask alignment apparatus
3499640	Chuck assembly for automatic wafer die sort machine
3437929	Automatically indexed probe assembly for testing semiconductor wafer and the like
3409727	Diffusion furnace
3385921	Diffusion furnace with high speed recovery
3311694	Diffusion furnace and method utilizing high speed recovery
3370120	Diffusion furnace and method utilizing high speed recovery
3299196	Diffusion furnace
3291969	Temperature control system for a diffusion furnace
3192358	Multiple point bonding apparatus
3134559	Tensioning device
3116889	Threading device with magazine and method
3050617	Thermocompression lead bonding apparatus

US Patent	Title

Application Number	
US20070164770	Method and apparatuses for dynamic probe adjustment
US200220158643	Method of apparatus for generating values for selected pixels used in evaluating semiconductor wafer bumps
US20080150565	Method and apparatuses for improved positioning in a probing system
US20080150559	Method for probing impact sensitive and thin layered substrate
US20080100321	Method and apparatuses for improved stabilization in a probing system

Unpublished US Patent Application Number	Title	Date Filed
12/334,378	Chained Motion	May 2009
12/334,368	Adaptive control	May 2009
12/152,599	Prealigner Search	May 2008

Foreign Patent Number	Title
DE69831917	Improved method and apparatus for wafer probe sensing
EP0919817	Improved method and apparatus for wafer probe sensing
KR598787	Improved method and apparatus for wafer probe sensing
KR729008	Apparatus for electrical testing of a substrate having a pluarality of terminals
SG86056	Apparatus for electrical testing of a substrate having a pluarality of terminals
TW163700	Apparatus for electrical testing of a substrate having a pluarality of terminals
KR295376	Apparatus for electrical testing of a substrate having a pluarality of terminals
CN100385247	Testing circuits on substrates
MY130993A	Testing circuits on substrates
SG104057	Testing circuits on substrates
TW232307	Testing circuits on substrates
TW274890	Testing circuits on substrates
CN100354640	Testing circuits on substrates
MY129912A	Testing circuits on substrates
PH1-2004-500563	Testing circuits on substrates
SG103706	Testing circuits on substrates

TW223075	Testing circuits on substrates
CN101305288	Methods and apparatuses for dynamic probe adjustment
JP2009524050	Methods and apparatuses for dynamic probe adjustment
KR1020080093410	Methods and apparatuses for dynamic probe adjustment
WO2007084204	Methods and apparatuses for dynamic probe adjustment
Taiwan 95141942	**Methods and apparatuses for dynamic probe adjustment**
CN101297206	Methods and apparatuses for improved positioning in a probing system
JP2009524238	Methods and apparatuses for improved positioning in a probing system
KR1020080093408	Methods and apparatuses for improved positioning in a probing system
WO2007084206	Methods and apparatuses for improved positioning in a probing system
Taiwan 95141943	**Methods and apparatuses for improved positioning in a probing system**
CN101297205	Methods and apparatuses for improved stabilization in a probing system
JP2009524237	Methods and apparatuses for improved stabilization in a probing system
KR1020080093409	Methods and apparatuses for improved stabilization in a probing system
WO2007084205	Methods and apparatuses for improved stabilization in a probing system
Taiwan 95141940	**Methods and apparatuses for improved stabilization in a probing system**
CN101238380	Method and apparatus for cleaning a probe card
JP2009503904	Method and apparatus for cleaning a probe card
KR1020080042105	Method and apparatus for cleaning a probe card
WO2007016599	Method and apparatus for cleaning a probe card
Singapore 200805742-4	**Method and apparatus for cleaning a probe card**
EP1446672	Testing circuits on substrates
JP2005507082	Testing circuits on substrates
WO03036308	Testing circuits on substrates
EP1438597	Testing circuits on substrate
JP2005507081	Testing circuits on substrate
WO03036307	Testing circuits on substrate
TW274890	Testing circuits on substrates
WO03036306	Testing circuits on substrates
Korea 2004-7005909	**Testing circuits on substrates**
Malaysia PI20064244	**Testing circuits on substrates**
AU 6071900	Apparatus For Electrical Testing Of A Substrate

EP1210612	Apparatus for electrical testing of a substrate having a pluarality of terminals
JP2003526088	Apparatus for electrical testing of a substrate having a pluarality of terminals
TW504578	Apparatus for electrical testing of a substrate having a pluarality of terminals
WO0104652	Apparatus for electrical testing of a substrate having a pluarality of terminals
JP11317429	Method and apparatus for direct probe sensing
JP11191584	Rotary wafer positioning system and method
EP0842438	Prober and tester with contact interface for integrated circuits-containing wafer held docked in a vertical plane
JP11509981	Prober and tester with contact interface for integrated circuits-containing wafer held docked in a vertical plane
WO9704324	Prober and tester with contact interface for integrated circuits-containing wafer held docked in a vertical plane
CA1229427	Height measuring system
JP1807312	Height measuring system
CA1194921	System for linear motor control
EP0093912	System for linear motor control
JP58207896	System for linear motor control
CA972851	Control system for magnetic positioning device
DE2123872	Control system for magnetic positioning device
FR209138	Control system for magnetic positioning device
GB1353171	Control system for magnetic positioning device
GB1353172	Control system for magnetic positioning device
JP55018926	Control system for magnetic positioning device
GB954569	Thermocompression lead bonding apparatus
CA674563	Thermocompression lead bonding apparatus
DE2009532	English Title Not Available
FR2037747	English Title Not Available
NL7003244	English Title Not Available
FR1304863	English Title Not Available
KR1020040062573	Apparatus and method for handling and testing of wafers
KR1020020036834	Apparatus for electrical testing of a substrate having a plurality of terminals
KR1020020008108	IC test software system for mapping logical functional test data of logic integrated circuits to physical representation
KR100295376	English Title Not Available