PATENT ASSIGNMENT

Electronic Version v1.1
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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	Release of Lien on Patent

CONVEYING PARTY DATA

Name	Execution Date
BARCLAYS BANK PLC	08/05/2013

RECEIVING PARTY DATA

Name:	SPANSION LLC
Street Address:	915 DEGUIGNE DRIVE
City:	SUNNYVALE
State/Country:	CALIFORNIA
Postal Code:	94088

Name:	SPANSION INC.
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Postal Code:	94088

Name:	SPANSION TECHNOLOGY INC.
Street Address:	915 DEGUIGNE DRIVE
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Postal Code:	94088

Name:	SPANSION TECHNOLOGY LLC
Street Address:	915 DEGUIGNE DRIVE
City:	SUNNYVALE
State/Country:	CALIFORNIA
Postal Code:	94088

PROPERTY NUMBERS Total: 52

Property Type	Number

OP $2080.00 5815438

Patent Number:	5815438
Patent Number:	5995417
Patent Number:	6181605
Patent Number:	6240020
Patent Number:	6269025
Patent Number:	6295228
Patent Number:	6307783
Patent Number:	6504757
Patent Number:	7154769
Patent Number:	6707713
Patent Number:	6728913
Patent Number:	6996004
Patent Number:	7266664
Patent Number:	7286398
Patent Number:	7342830
Patent Number:	7362620
Patent Number:	7564720
Patent Number:	7626253
Patent Number:	7859096
Patent Number:	8329562
Patent Number:	8330263
Application Number:	13711443
Patent Number:	7675776
Patent Number:	7706186
Patent Number:	7743203
Patent Number:	7761740
Patent Number:	7602639
Patent Number:	7869281
Patent Number:	7945792
Patent Number:	7949851
Patent Number:	7953919
Patent Number:	8239875
Patent Number:	7968990
Patent Number:	7979667
Patent Number:	7995386

	8010776
Patent Number:	8041895
Patent Number:	8085588
Patent Number:	8117521
Patent Number:	6175522
Patent Number:	6175523
Patent Number:	6397313
Patent Number:	6219276
Patent Number:	6424569
Patent Number:	6452869
Patent Number:	7042766
Patent Number:	7184338
Patent Number:	7630245
Patent Number:	7643371
Patent Number:	7739559
Patent Number:	7895406
Patent Number:	7894267

CORRESPONDENCE DATA

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NAME OF SUBMITTER:	Sonya Jackman
Signature:	/Sonya Jackman/
Date:	08/05/2013

Total Attachments: 12
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TERMINATION AND RELEASE OF

SECURITY INTEREST IN PATENT COLLATERAL

THIS TERMINATION AND RELEASE OF SECURITY INTEREST IN PATENT COLLATERAL (this "Termination"), dated as of August 5, 2013, is executed by BARCLAYS BANK PLC, as collateral agent (in such capacity, "Collateral Agent") in favor of SPANSION LLC, a Delaware limited liability company, SPANSION INC., a Delaware corporation, SPANSION TECHNOLOGY INC., a Delaware corporation, and SPANSION TECHNOLOGY LLC, a Delaware limited liability company (collectively, jointly and severally "Grantors"). All capitalized terms used in this Termination and not otherwise defined herein, shall have the respective meanings given to such terms in the Patent Security Agreement (defined below).

RECITALS

A. Pursuant to that certain Patent Security Agreement, dated as of May 10, 2010 (the "Patent Security Agreement"), executed by Grantors in favor of the Collateral Agent and the that certain Amended and Restated Pledge and Security Agreement, dated as of December 13, 2012, executed by the Grantors in favor of the Collateral Agent, Grantors granted to Collateral Agent a security interest in the Patent Collateral (defined below).

B. The Patent Security Agreement was recorded with the Patent Division of the United States Patent and Trademark Office on June 4, 2010, at Reel/Frame 024522/0338 to evidence the security interest granted under the Patent Security Agreement.

C. Collateral Agent agrees to terminate and release its security interest in the Patent Collateral specified below and to file this Termination with respect to such release of its security interest as herein provided.

AGREEMENT

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, Collateral Agent expressly terminates and releases all of Collateral Agent's right, title and interest in, to and under the following (the "Patent Collateral"):

(a) all Patents set forth on Schedule 1 hereto;

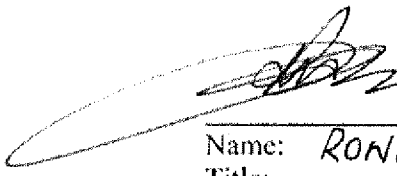
(b) all Patent Licenses in connection with the Patents described in clause (a) above; and

(c) all income, royalties, proceeds and liabilities due or payable, except to the extent received by Collateral Agent prior to the date of this Termination, or asserted under and with respect to any of the foregoing, including, without limitation, all rights to sue and recover at law or in equity for any past, present and future infringement, misappropriation, dilution, violation or other impairment thereof.

[Signature Page Follows]

IN WITNESS WHEREOF, Collateral Agent has executed and delivered this Termination as of the day and year first above written.

BARCLAYS BANK PLC,
as Collateral Agent



Name: RONNIE GLENN
Title: VICE PRESIDENT

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SCHEDULE 1
TO
TERMINATION AND RELEASE OF
SECURITY INTEREST IN PATENT COLLATERAL

FAMILY	COUNTRY	PATENT NUMBER	APPLICATION NUMBER	FILING DATE	PATENT TITLE
1	US	5815438	08/810,170	2/28/1997	OPTIMIZED BIASING SCHEME FOR NAND READ AND HOT-CARRIER WRITE OPERATIONS
2	DE	69904856.7	99950160.4	10/5/1999	A SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON-VOLATILE MEMORY ARRAY
2	EP	1125302		10/5/1999	A SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON-VOLATILE MEMORY ARRAY
2	FR	1125302	99950160.4	10/5/1999	A SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON-VOLATILE MEMORY ARRAY
2	GB	1125302	99950160.4	10/5/1999	A SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON-VOLATILE MEMORY ARRAY
2	JP		2002-528841	4/19/2001	SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON-VOLATILE MEMORY ARRAY
2	KR	564378	7004996/2001	10/5/1999	SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON-VOLATILE MEMORY ARRAY
2	TW	142628	88118017	10/19/1999	SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON-VOLATILE MEMORY ARRAY

FAMILY	COUNTRY	PATENT NUMBER	APPLICATION NUMBER	FILING DATE	PATENT TITLE
2	US	5995417	09/175,646	10/20/1998	SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON - VOLATILE MEMORY ARRAY
2	PCT	WO0024002		10/5/1999	SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON - VOLATILE MEMORY ARRAY
3	US	6181605	09/414,750	10/6/1999	GLOBAL ERASE/PROGRAM VERIFICATION APPARATUS AND METHOD
4	US	6240020	09/427,406	10/25/1999	METHOD OF BITLINE SHIELDING IN CONJUNCTION WITH A PRECHARGING SCHEME FOR NAND-BASED FLASH MEMORY DEVICES
5	US	6269025	09/500,699	2/9/2000	MEMORY SYSTEM HAVING A PROGRAM AND ERASE VOLTAGE MODIFIER
6	US	6295228	09/514,933	2/28/2000	SYSTEM FOR PROGRAMMING MEMORY CELLS
7	US	6307783	09/794,485	2/26/2001	DESCENDING STAIRCASE READ TECHNIQUE FOR A MULTILEVEL CELL NAND FLASH MEMORY DEVICE
8	US	6504757	09/922,415	8/3/2001	DOUBLE BOOSTING SCHEME FOR NAND TO IMPROVE PROGRAM INHIBIT CHARACTERISTICS
9	US	7154769	11/052,689	2/7/2005	MEMORY DEVICE INCLUDING BARRIER LAYER FOR IMPROVED SWITCHING SPEED AND DATA RETENTION

FAMILY	COUNTRY	PATENT NUMBER	APPLICATION NUMBER	FILING DATE	PATENT TITLE
9	PCT	WO02006086248		2/6/2006	MEMORY DEVICE INCLUDING BARRIER LAYER FOR IMPROVED SWITCHING SPEED AND DATA RETENTION
10	TW	I222071	90103881	2/21/2001	INTERLACED MULTI-LEVEL MEMORY
10	US	6707713	09/516,478	3/1/2000	INTERLACED MULTI-LEVEL MEMORY
10	PCT	WO0167462		2/6/2001	INTERLACED MULTI-LEVEL MEMORY
11	US	6728913	09/513698	2/25/2000	DATA RECYCLING IN MEMORY
12	US	6996004	10/700,414	11/4/2003	MINIMIZATION OF FG-FG COUPLING IN FLASH MEMORY
13	EP	1239488		2/26/2002	MEMORY DEVICE FOR CONTROLLING NONVOLATILE AND VOLATILE MEMORIES
13	JP	4017177	2002-4150		MEMORY DEVICE
13	US	7266664	10/077,778	2/20/2002	MEMORY DEVICE FOR CONTROLLING NONVOLATILE AND VOLATILE MEMORIES
14	JP	4672673	2006-546540	11/30/2004	SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING SAID SEMICONDUCTOR DEVICE
14	US	7286398	11/290,002	11/30/2005	SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING SAID SEMICONDUCTOR DEVICE
14	PCT	2006059374		11/30/2004	SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING SAID SEMICONDUCTOR DEVICE
15	US	7342830	11/332,263	1/17/2006	PROGRAM AND PROGRAM VERIFY

FAMILY	COUNTRY	PATENT NUMBER	APPLICATION NUMBER	FILING DATE	PATENT TITLE
					OPERATIONS FOR FLASH MEMORY
16	JP	4896011	2007-512381	3/31/2005	SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME
16	US	7362620	11/394,491	3/31/2006	SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME
16	PCT	2006106577		3/31/2005	SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME
17	TW	I342024	96124086	7/3/2007	NONVOLATILE STORAGE AND ERASE CONTROL
17	US	7564720	11/879,989	7/18/2007	NONVOLATILE STORAGE AND ERASE CONTROL
17	PCT	2008010258		7/18/2006	NONVOLATILE STORAGE AND ERASE CONTROL METHOD
18	JP	4871280	2007-533065	8/30/2005	SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING SAME
18	US	7626253	11/514,390	8/30/2006	COMPUTING DEVICE INCLUDING A STACKED SEMICONDUCTOR DEVICE
18	US	7859096	12/624,117	11/23/2009	SEMICONDUCTOR DEVICE
18	US	8329562	12/965,706	12/11/2012	METHODS OF MAKING A SEMICONDUCTOR DEVICE
18	US	8330263	12/965,672	12/10/2010	SEMICONDUCTOR DEVICE
18	US		13/711,443	12/11/2012	SEMICONDUCTOR DEVICE AND FABRICATION

FAMILY	COUNTRY	PATENT NUMBER	APPLICATION NUMBER	FILING DATE	PATENT TITLE
					METHOD THEREFORE
18	PCT	2007026392		8/30/2005	SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFORE
19	US	7675776	11/963,286	12/21/2007	BIT MAP CONTROL OF ERASE BLOCK DEFECT LIST IN A MEMORY
20	JP		2008117505	3/6/2007	SEMICONDUCTOR DEVICE AND ITS CONTROL METHOD
20	TW		200901197	10/31/2007	SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREOF
20	US	7706186	11/982,864	11/5/2007	CONTROLLING A SEMICONDUCTOR DEVICE
20	PCT	2008057498		11/5/2007	CONTROLLING A SEMICONDUCTOR DEVICE
21	US	7743203	11/747,608	5/11/2007	MANAGING FLASH MEMORY BASED UPON USAGE HISTORY
22	US	7761740	11/955,9334	12/13/2007	POWER SAFE TRANSLATION TABLE OPERATION IN FLASH MEMORY
23	US	7602639	11/957,309	12/14/2007	READING ELECTRONIC MEMORY UTILIZING RELATIONSHIPS BETWEEN CELL STATE DISTRIBUTIONS
23	US	7869281	12/550,642	8/31/2009	READING ELECTRONIC MEMORY UTILIZING RELATIONSHIPS BETWEEN CELL STATE DISTRIBUTIONS
24	TW	200926201	97139850	10/17/2008	TAMPER REACTIVE MEMORY DEVICE TO SECURE DATA FROM

FAMILY	COUNTRY	PATENT NUMBER	APPLICATION NUMBER	FILING DATE	PATENT TITLE
					TAMPER ATTACKS
24	US	7945792	11/873,980	10/14/2007	TAMPER REACTIVE MEMORY DEVICE TO SECURE DATA FROM TAMPER ATTACKS
24	PCT	2009052385		10/17/2008	TAMPER REACTIVE MEMORY DEVICE TO SECURE DATA FROM TAMPER ATTACKS
25	US	7949851	11/966,919	12/28/2007	TRANSLATION MANAGEMENT OF LOGICAL BLOCK ADDRESSES AND PHYSICAL BLOCK ADDRESSES
26	US	7953919	11/963,306	12/21/2007	PHYSICAL BLOCK ADDRESSING OF ELECTRONIC MEMORY DEVICES
26	US	8239875	11/962,918	12/21/2007	COMMAND QUEUING FOR NEXT OPERATIONS OF MEMORY DEVICES
27	JP	5192825	2007-554752	1/17/2006	SEMICONDUCTOR DEVICE, METHOD OF FABRICATING SEMICONDUCTOR DEVICE, AND METHOD OF FABRICATING STACKED SEMICONDUCTOR DEVICE
27	US	7968990	11/654,704	1/17/2007	SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME
27	PCT	2007083351		1/17/2006	SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME
28	US	7979667	11/953,501	12/10/2007	MEMORY ARRAY SEARCH ENGINE
29	US	7995386	12/275,663	11/21/2008	APPLYING NEGATIVE GATE VOLTAGE TO

FAMILY	COUNTRY	PATENT NUMBER	APPLICATION NUMBER	FILING DATE	PATENT TITLE
					WORDLINES ADJACENT TO WORDLINE ASSOCIATED WITH READ OR VERIFY TO REDUCE ADJACENT WORDLINE DISTURB
30	US	8010776	11/957,793	12/17/2007	ADAPTIVE SYSTEM BOOT ACCELERATOR FOR COMPUTING SYSTEMS
31	US	8041895	12/020,698	1/28/2008	TRANSLATION TABLE COHERENCY MECAHANISM USING CACHE WAY AND SET INDEX WRITE BUFFERS
32	US	8085588	12/433,084	4/30/2009	SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREOF
33	US	8117521	12/198,381	8/26/2008	IMPLEMENTATION OF RECYCLING UNUSED ECC PARITY BITS DURING FLASH MEMORY PROGRAMMING
34	US	6175522	09/408,846	9/30/1999	READ OPERATION SCHEME FOR A HIGH-DENSITY, LOW VOLTAGE, AND SUPERIOR RELIABILITY NAND FLASH MEMORY DEVICE
35	AT		248400	9/15/2003	REDUNDANT DUAL BANK ARCHITECTURE FOR A SIMULTANEOUS OPERATION FLASH MEMORY
35	CN		1379878	11/13/2002	REDUNDANT DUAL BANK ARCHITECTURE FOR SIMULTANEOUS OPERATION FLASH MEMORY

FAMILY	COUNTRY	PATENT NUMBER	APPLICATION NUMBER	FILING DATE	PATENT TITLE
35	EP	1224549		10/9/2000	REDUNDANT DUAL BANK ARCHITECTURE FOR A SIMULTANEOUS OPERATION FLASH MEMORY
35	JP		2003512690	10/9/2000	REDUNDANT DUAL BANK ARCHITECTURE FOR A SIMULTANEOUS OPERATION FLASH MEMORY
35	TW	484055	TW097139850	4/21/2002	REDUNDANT DUAL BANK ARCHITECTURE FOR A SIMULTANEOUS OPERATION FLASH MEMORY
35	US	6175523	09/433,187	10/25/1999	PRECHARGING MECHANISM AND METHOD FOR NAND-BASED FLASH MEMORY DEVICES
35	PCT	WO0129668		4/26/2001	REDUNDANT DUAL BANK ARCHITECTURE FOR A SIMULTANEOUS OPERATION FLASH MEMORY
36	US	6397313	09/632,390	8/4/2000	REDUNDANT DUAL BANK ARCHITECTURE FOR A SIMULTANEOUS OPERATION FLASH MEMORY
37	US	6219276	09/513,643	2/25/2000	MULTILEVEL CELL PROGRAMMING
37	US	6424569	09/513,027	2/25/2000	USER SELECTABLE CELL PROGRAMMING
37	PCT	WO0163615		2/6/2001	USER SELECTABLE CELL PROGRAMMING
38	US	6452869	09/794,478	2/26/2001	ADDRESS BROADCASTING TO A PAGED MEMORY DEVICE TO ELIMINATE ACCESS LATENCY PENALTY

FAMILY	COUNTRY	PATENT NUMBER	APPLICATION NUMBER	FILING DATE	PATENT TITLE
39	US	7042766	10/896,651	7/22/2004	METHOD OF PROGRAMMING A FLASH MEMORY DEVICE USING MULTILEVEL CHARGE STORAGE
40	EP	1785998		8/30/2004	SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE TESTING METHOD, AND PROGRAMMING METHOD
40	US	7184338	11/215,253	8/30/2005	SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE TESTING METHOD, AND PROGRAMMING METHOD
40	PCT	2006025083		8/30/2004	SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE TESTING METHOD, AND PROGRAMMING METHOD
41	US	7630245	11/543,399	10/4/2006	SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREFOR
41	PCT	WO2007043133		10/4/2005	SEMICONDUCTOR DEVICE AND METHOD FOR CONTROLLING SAME
42	JP		2008-165917	12/28/2006	SEMICONDUCTOR DEVICE AND ITS CONTROL METHOD
42	TW	I359425	96149656	12/24/2007	SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME
42	US	7643371	11/986,385	11/20/2007	ADDRESS/DATA MULTIPLEXED DEVICE
42	PCT	2008082606		12/28/2007	SEMICONDUCTOR

FAMILY	COUNTRY	PATENT NUMBER	APPLICATION NUMBER	FILING DATE	PATENT TITLE
					DEVICE AND METHOD OF CONTROLLING THE SAME
43	JP	5014125	2007-518819	5/30/2005	SEMICONDUCTOR DEVICE AND PROGRAM DATA REDUNDANCY METHOD THEREFOR
43	US	7739559	11/444,251	5/30/2006	SEMICONDUCTOR DEVICE AND PROGRAM DATA REDUNDANCY METHOD THEREFOR
43	PCT	2006129345		5/30/2005	SEMICONDUCTOR DEVICE AND PROGRAM DATA REDUNDANCY METHOD THEREFOR
44	JP		2008-152549	12/18/2006	MEMORY DEVICE, AND PASSWORD STORAGE METHOD FOR MEMORY DEVICE
44	TW	366832	96145085	11/28/2007	MEMORY DEVICE AND PASSWORD STORING MTHOD THEREOF
44	US	7895406	11/986,332	11/20/2007	MEMORY DEVICE AND PASSWORD STORING METHOD THEREOF
44	PCT	2008076999		12/17/2007	MEMORY DEVICE AND PASSWORD STORING METHOD THEREOF
45	US	7894267	11/929,741	10/30/2007	DETERMINISTIC PROGRAMMING ALGORITHM THAT PROVIDES TIGHTER CELL DISTRIBUTIONS WITH A REDUCED NUMBER OF PROGRAMMING PULSES