PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY AGREEMENT

CONVEYING PARTY DATA

Name	Execution Date
SRC Computers, LLC	09/23/2013

RECEIVING PARTY DATA

Name:	Freeman Capital Partners LP
Street Address:	100 Cresent Court, Ste. 1450
City:	Dallas
State/Country:	TEXAS
Postal Code:	75201

PROPERTY NUMBERS Total: 38

Property Type	Number
Patent Number:	6076152
Patent Number:	6247110
Patent Number:	6961841
Patent Number:	7237091
Patent Number:	6026459
Patent Number:	6295598
Patent Number:	6594736
Patent Number:	6339819
Patent Number:	6836823
Patent Number:	6434687
Patent Number:	7155602
Patent Number:	7167976
Patent Number:	7373440
Patent Number:	7197575
Patent Number:	7565461

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Patent Number:	7421524
Patent Number:	7124211
Patent Number:	7406573
Patent Number:	7225324
Patent Number:	7620800
Patent Number:	7003593
Patent Number:	6996656
Patent Number:	6941539
Patent Number:	6983456
Patent Number:	7703085
Patent Number:	7299458
Patent Number:	6964029
Patent Number:	7155708
Patent Number:	7134120
Patent Number:	7424552
Patent Number:	7680968
Patent Number:	7149867
Patent Number:	7890686
Application Number:	11456466
Application Number:	13286996
Application Number:	13287322
Application Number:	13365090
Application Number:	13903720

CORRESPONDENCE DATA

Fax Number: 2142008253

Correspondence will be sent via US Mail when the fax attempt is unsuccessful.

Phone: 214-651-5170

Email: jennifer.pierce@haynesboone.com

Correspondent Name: Haynes and Boone, LLP

Address Line 1: 2323 Victory Avenue, Suite 700

Address Line 4: Dallas, TEXAS 75219

ATTORNEY DOCKET NUMBER:	50233.2
NAME OF SUBMITTER:	Jennifer Pierce
Signature:	/Jennifer Pierce/
Date:	

	09/23/2013

Total Attachments: 24
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INTELLECTUAL PROPERTY SECURITY AGREEMENT

THIS INTELLECTUAL PROPERTY SECURITY AGREEMENT (this "***Agreement***") is entered into as of September 23, 2013, among SRC COMPUTERS, LLC, a Delaware limited liability company ("***Grantor***") and FREEMAN CAPITAL PARTNERS LP ("***Secured Party***").

RECITALS

WHEREAS, pursuant to that certain Credit Agreement dated as of even date herewith (the "***Credit Agreement***"), between Grantor and Secured Party, the Secured Party has agreed to extend a term loan to Grantor;

WHEREAS, in order to induce Secured Party to extend the loan, Grantor has agreed to execute and deliver to Secured Party this Agreement and to grant Secured Party a security interest in all of the copyrights, trademarks, patents, and trade secrets of Grantor, as described below, to secure the prompt payment, performance and discharge in full of all of Grantor's obligations under the Credit Agreement and the other Loan Documents (as defined in the Credit Agreement).

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt payment, performance and discharge of its obligations under the Credit Agreement and the other Loan Documents, Grantor hereby agrees as follows:

1. Grant of Security

To secure its obligations under the Credit Agreement and other related documents and subject to the terms set forth therein, Grantor grants to Secured Party a security interest in all of Grantor's rights, priorities and privileges in the following (all of which shall collectively be called the "***Intellectual Property Collateral***"):

(i) all United States and foreign copyrights (including Community designs), including copyrights in software and databases, and all Mask Works (as defined under 17 U.S.C. 901 of the U.S. Copyright Act), whether registered or unregistered, and, with respect to any and all of the foregoing: (a) all registrations and applications therefor, including the registrations and applications referred to on ***Exhibit A***; (b) all extensions and renewals thereof; (c) all rights corresponding thereto throughout the world; (d) all rights to sue for past, present and future infringements thereof; and (e) all products and proceeds of the foregoing, including any income, royalties, and awards and any claim by Debtor against third parties for past, present, or future infringement of any Copyright or any Copyright licensed under any Copyright License (collectively, the "***Copyrights***");

(ii) any and all agreements providing for the granting of any right in or to Copyrights (whether Debtor is licensee or licensor thereunder), including each agreement referred to on ***Exhibit A*** (collectively, the "***Copyright Licenses***");

(iii) all United States and foreign patents and certificates of invention, or similar industrial property rights, and applications for any of the foregoing, including: (a) each patent and patent application referred to on ***Exhibit B***; (b) all reissues, divisions, continuations, continuations-in-part, extensions, renewals, and reexaminations thereof; (c) all rights corresponding thereto throughout the world; (d) all inventions and improvements described therein; (e) all rights to sue for past, present and future infringements thereof; (f) all licenses, claims, damages, and proceeds of suit arising therefrom; and (g) all products and proceeds of the foregoing, including any income, royalties, and

awards and any claim by Debtor against third parties for past, present, or future infringement of any Patent or any Patent licensed under any Patent License (collectively, the "***Patents***");

(iv) all agreements providing for the granting of any right in or to Patents (whether Debtor is licensee or licensor thereunder), including each agreement referred to on ***Exhibit B*** (collectively, the "***Patent Licenses***");

(v) all United States and foreign trademarks, trade names, corporate names, company names, business names, fictitious business names, Internet domain names, service marks, certification marks, collective marks, logos, other source or business identifiers, designs and general intangibles of a like nature, all registrations and applications for any of the foregoing, including: (a) the registrations and applications referred to on ***Exhibit C***; (b) all extensions or renewals of any of the foregoing; (c) all of the goodwill of the business connected with the use of and symbolized by the foregoing; (d) the right to sue for past, present and future infringement or dilution of any of the foregoing or for any injury to goodwill; and (e) all products and proceeds of the foregoing, including any income, royalties, and awards and any claim by Debtor against third parties for past, present, or future infringement of any Trademark or any Trademark licensed under any Trademark License (collectively, the "***Trademarks***");

(vi) any and all agreements providing for the granting of any right in or to Trademarks (whether Debtor is licensee or licensor thereunder), including each agreement referred to on ***Exhibit C*** (collectively, the "***Trademark Licenses***");

(vii) all trade secrets and all other confidential or proprietary information and know-how, whether or not such Trade Secret has been reduced to a writing or other tangible form, including all Documents and things embodying, incorporating, or referring in any way to such Trade Secret, including: (a) the right to sue for past, present and future misappropriation or other violation of any Trade Secret; and (b) all products and proceeds of the foregoing, including any income, royalties, and awards and any claim by Debtor against third parties for past, present, or future infringement of any Trade Secrets or any Trade Secrets licensed under any Trade Secret License (collectively, the "***Trade Secrets***");

(viii) any and all agreements providing for the granting of any right in or to Trade Secrets (whether Debtor is licensee or licensor thereunder), including each agreement referred to on ***Exhibit D*** (collectively, the "***Trade Secret Licenses***");

(ix) all rights to obtain any reissues, renewals or extensions of the foregoing; and

(x) all causes of action for infringement of the foregoing.

2. Security Agreement

This security interest is granted in conjunction with the security interest granted to Secured Party pursuant to that certain Security Agreement, dated as of even date herewith, by Grantor for the benefit of Secured Party (the "***Security Agreement***"). Grantor hereby acknowledges and affirms that the rights and remedies of Secured Party with respect to the security interest in the Intellectual Property Collateral made and granted hereby are more fully set forth in the Security Agreement, the terms and provisions of which are incorporated by reference herein as if fully set forth herein.

3. Recordation

Grantor authorizes the Commissioner for Patents, the Commissioner for Trademarks and the Register of Copyrights and any other government officials to record and register this Agreement upon request by the Secured Party.

4. Successors and Assigns

This Agreement will be binding on and shall inure to the benefit of the parties hereto and their respective successors and assigns.

5. Governing Law

This Agreement and any claim, controversy, dispute or cause of action (whether in contract or tort or otherwise) based upon, arising out of or relating to this Agreement and the transactions contemplated hereby shall be governed by, and construed in accordance with, the laws of the United States and the State of Texas.

6. Miscellaneous

This Agreement may be executed in any number of counterparts and by different parties on separate counterparts, each of which, when executed and delivered, is an original, and all taken together, constitute one Intellectual Property Security Agreement. Delivery of an executed counterpart of a signature page to this Agreement by facsimile or in electronic (i.e., "pdf" or "tif" format) shall be effective as delivery of a manually executed counterpart of this Agreement.

[Signature Page Follows.]

1IN WITNESS WHEREOF, the parties have caused this Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

SRC COMPUTERS, LLC

Address of Grantor:

4240 N. Nevada Avenue
Colorado Springs, CO 80907

By: Teresa M Kreps
Name: TERESA M KREPS
Title: CHIEF FINANCIAL OFFICER

Attn:
CHIEF FINANCIAL OFFICER

[Signature Page of Secured Party Follows]

SECURED PARTY:

Address:

100 Crescent Court, Ste. 1450
Dallas, Texas 75201

FREEMAN CAPITAL PARTNERS LP

Attn:

By: _____
Name:
Title:

EXHIBIT A

Copyrights

None.

EXHIBIT B

Patents

Country	Patent No.	Issue Date	Inventor(s)	Title
USA	6,076,152	12/17/1997	Jon M. HUPPENTHAL, Paul A. LESKAR	MULTIPROCESSOR COMPUTER ARCHITECTURE INCORPORATING A PLURALITY OF MEMORY ALGORITHM PROCESSORS IN THE MEMORY SUBSYSTEM
CAN	2,313,462	12/3/1998	Jon M. HUPPENTHAL, Paul A. LESKAR	MULTIPROCESSOR COMPUTER ARCHITECTURE INCORPORATING A PLURALITY OF MEMORY ALGORITHM PROCESSORS IN THE MEMORY SUBSYSTEM
CAN DIV	2,515,283	12/3/1998	Jon M. HUPPENTHAL, Paul A. LESKAR	MULTIPROCESSOR COMPUTER ARCHITECTURE INCORPORATING A PLURALITY OF MEMORY ALGORITHM PROCESSORS IN THE MEMORY SUBSYSTEM
CON	6,247,110	1/12/2000	Jon M. HUPPENTHAL, Paul A. LESKAR	MULTIPROCESSOR COMPUTER ARCHITECTURE INCORPORATING A PLURALITY OF MEMORY ALGORITHM PROCESSORS IN THE MEMORY SUBSYSTEM

CON2	6,961,841	1/8/2003	Jon M. HUPPENTHAL, Paul A. LESKAR	MULTIPROCESSOR COMPUTER ARCHITECTURE INCORPORATING A PLURALITY OF MEMORY ALGORITHM PROCESSORS IN THE MEMORY SUBSYSTEM
CON3	7,237,091	10/20/2004	Jon M. HUPPENTHAL, Paul A. LESKAR	MULTIPROCESSOR COMPUTER ARCHITECTURE INCORPORATING A PLURALITY OF MEMORY ALGORITHM PROCESSORS IN THE MEMORY SUBSYSTEM
JPN	4921638	12/3/1998	Jon M. HUPPENTHAL, Paul A. LESKAR	MULTIPROCESSOR COMPUTER ARCHITECTURE INCORPORATING A PLURALITY OF MEMORY ALGORITHM PROCESSORS IN THE MEMORY SUBSYSTEM
USA	6,026,459	2/3/1998	Jon M. HUPPENTHAL	SYSTEM AND METHOD FOR DYNAMIC PRIORITY CONFLICT RESOLUTION IN A MULTI-PROCESSOR COMPUTER SYSTEM HAVING SHARED MEMORY RESOURCES
CAN	2,317,543	1/29/1999	Jon M. HUPPENTHAL	SYSTEM AND METHOD FOR DYNAMIC PRIORITY CONFLICT RESOLUTION IN A MULTI-PROCESSOR COMPUTER SYSTEM HAVING SHARED MEMORY RESOURCES

USA	6,295,598	6/30/1998	Jonathan L. BERTONI, Lee A. BURTON	SPLIT DIRECTORY-BASED CACHE COHERENCY TECHNIQUE FOR A MULTI-PROCESSOR COMPUTER SYSTEM
USA	6,594,736	8/15/2000	David PARKS	SYSTEM AND METHOD FOR SEMAPHORE AND ATOMIC OPERATION MANAGEMENT IN A MULTIPROCESSOR
USA	6,339,819	5/3/2000	Jon M. HUPPENTHAL, Paul A. LESKAR	MULTIPROCESSOR WITH EACH PROCESSOR ELEMENT ACCESSING OPERANDS IN LOADED INPUT BUFFER AND FORWARDING RESULTS OF FIFO OUTPUT BUFFER
AUS	2001245761	3/16/2001	Jon M. HUPPENTHAL, Paul A. LESKAR	ENHANCED MEMORY ALGORITHMIC PROCESSOR ARCHITECTURE FOR MULTIPROCESSOR COMPUTER SYSTEMS
USA	6,836,823	11/5/2001	Lee A. BURTON	BANDWIDTH ENHANCEMENT FOR UNCACHED DEVICES

USA	6,434,687	6/22/2001	John M. HUPPENTHAL	SYSTEM AND METHOD FOR ACCELERATING WEB SITE ACCESS AND PROCESSING UTILIZING A COMPUTER SYSTEM INCORPORATING RECONFIGURABLE PROCESSORS OPERATING UNDER A SINGLE OPERATIONAL SYSTEM IMAGE
AUS	2002303661	5/6/2002	John M. HUPPENTHAL	SYSTEM AND METHOD FOR WEB SERVER WITH A RECONFIGURABLE PROCESSOR OPERATING UNDER SINGLE OPERATION SYSTEM IMAGE
CAN	2,448,223	5/6/2002	John M. HUPPENTHAL	SYSTEM AND METHOD FOR WEB SERVER WITH A RECONFIGURABLE PROCESSOR OPERATING UNDER SINGLE OPERATION SYSTEM IMAGE
JPN	4713080	5/6/2002	John M. HUPPENTHAL	SYSTEM AND METHOD FOR WEB SERVER WITH A RECONFIGURABLE PROCESSOR OPERATING UNDER SINGLE OPERATION SYSTEM IMAGE
JPN DIV	4990244	8/21/2008	John M. HUPPENTHAL	SYSTEM AND METHOD FOR WEB SERVER WITH A RECONFIGURABLE PROCESSOR OPERATING UNDER SINGLE OPERATION SYSTEM IMAGE

USA	7,155,602	12/5/2001	Daniel POZNANOVIC	INTERFACE FOR INTEGRATING RECONFIGURABLE PROCESSORS INTO A GENERAL PURPOSE COMPUTING SYSTEM
CON	7,167,976	5/31/2005	Daniel POZNANOVIC	INTERFACE FOR INTEGRATING RECONFIGURABLE PROCESSORS INTO A GENERAL PURPOSE COMPUTING SYSTEM
USA	7,373,440	8/17/2001	Jon M. HUPPENTHAL, Lee A. BURTON, Thomas R. SEEMAN	SWITCH/NETWORK ADAPTER PORT FOR CLUSTERED COMPUTERS EMPLOYING A CHAIN OF MULTI-ADAPTIVE PROCESSORS IN A DUAL IN-LINE MEMORY MODULE FORMAT
CIP	7,197,575	1/10/2003	Jon M. HUPPENTHAL, Lee A. BURTON, Thomas R. SEEMAN	SWITCH/NETWORK ADAPTER PORT COUPLING A RECONFIGURABLE PROCESSING ELEMENT TO ONE OR MORE MICROPROCESSORS FOR USE WITH INTERLEAVED MEMORY CONTROLLERS
CIP JPM	4703189	12/12/2003	Jon M. HUPPENTHAL, Lee A. BURTON, Thomas R. SEEMAN	SWITCH/NETWORK ADAPTER PORT COUPLING A RECONFIGURABLE PROCESSING ELEMENT TO ONE OR MORE MICROPROCESSORS FOR USE WITH INTERLEAVED MEMORY CONTROLLERS

CIP2	7,565,461	8/15/2005	Jon M. HUPPENTHAL, Lee A. BURTON, Thomas R. SEEMAN	SWITCH/NETWORK ADAPTER PORT COUPLING A RECONFIGURABLE PROCESSING ELEMENT TO ONE OR MORE MICROPROCESSORS FOR USE WITH INTERLEAVED MEMORY CONTROLLERS
DIV	7,421,524	11/23/2004	Jon M. HUPPENTHAL, Lee A. BURTON, Thomas R. SEEMAN	SWITCH/NETWORK ADAPTER PORT FOR CLUSTERED COMPUTERS EMPLOYING A CHAIN OF MULTI-ADAPTIVE PROCESSORS IN A DUAL IN-LINE MEMORY MODULE FORMAT
GB	1442378	5/6/2002	Jon M. HUPPENTHAL, Lee A. BURTON, Thomas R. SEEMAN	SWITCH/NETWORK ADAPTER PORT FOR CLUSTERED COMPUTERS EMPLOYING A CHAIN OF MULTI-ADAPTIVE PROCESSORS IN A DUAL IN-LINE MEMORY MODULE FORMAT
JPN	4128956	5/6/2002	Jon M. HUPPENTHAL, Lee A. BURTON, Thomas R. SEEMAN	SWITCH/NETWORK ADAPTER PORT FOR CLUSTERED COMPUTERS EMPLOYING A CHAIN OF MULTI-ADAPTIVE PROCESSORS IN A DUAL IN-LINE MEMORY MODULE FORMAT

USA	7,124,211	10/23/2002	Chris DICKSON, Daniel POZNANOVIC, David CALIGA, James E. O'CONNOR	SYSTEM AND METHOD FOR EXPLICIT COMMUNICATIO OF MESSAGES BETWEEN PROCESSES RUNNING ON DIFFERENT NODES IN A CLUSTERED MULTIPROCESSOR SYSTEM
JPN	4416658	9/16/2003	Chris DICKSON, Daniel POZNANOVIC, David CALIGA, James E. O'CONNOR	SYSTEM AND METHOD FOR EXPLICIT COMMUNICATIO OF MESSAGES BETWEEN PROCESSES RUNNING ON DIFFERENT NODES IN A CLUSTERED MULTIPROCESSOR SYSTEM
DIV/CIP	7,406,573	9/8/2005	Denis O. KELLAM, Jon M. HUPPENTHAL	RECONFIGURABLE PROCESSOR ELEMENT UTILIZING BOTH COURSE AND FINE GRAINED RECONFIGURABLE ELEMENTS
USA	7,225,324	10/31/2002	David CALIGA, Jon M. HUPPENTHAL	MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS
CON	7,620,800	4/9/2007	David CALIGA, Jon M. HUPPENTHAL	MULTI-ADAPTIVE PROCESSING SYSTEMS AND TECHNIQUES FOR ENHANCING PARALLELISM AND PERFORMANCE OF COMPUTATIONAL FUNCTIONS

JPN	4430844	9/16/2003	David CALIGA, Jon M. HUPPENTHAL	ENHANCED PARALLEL PERFORMANCE MULTI-ADAPTIVE COMPUTATIONAL SYSTEM
USA	7,003,593	10/29/2002	John M. HUPPENTHAL, Lee A. BURTON, Thomas R. SEEMAN	COMPUTER SYSTEM ARCHITECTURE AND MEMORY CONTROLLER FOR CLOSE-COUPLING WITHIN A HYBRID PROCESSING SYSTEM UTILIZING AN ADAPTIVE PROCESSOR INTERFACE PORT
USA	6,996,656	10/31/2002	Lee A. BURTON	SYSTEM AND METHOD FOR PROVIDING AN ARBITRATED MEMORY BUS IN A HYBRID COMPUTING SYSTEM
USA	6,941,539	10/31/2002	Jeffrey HAMMES	EFFICIENCY OF RECONFIGURABLE HARDWARE
JPN	4330535	9/22/2003	Jeffrey HAMMES	TECHNIQUE FOR IMPROVING THE EFFICIENCY OF RECONFIGURABLE HARDWARE
USA	6,983,456	10/31/2002	Daniel POZNANOVIC, David BARKER, Jeffrey HAMMES, Jeffrey Paul BROOKS, Jon STEIDEL, Lisa KRAUSE	PROCESS FOR CONVERTING PROGRAMS IN HIGH-LEVEL PROGRAMMING LANGUAGES TO A UNIFIED EXECUTABLE FOR HYBRID COMPUTING PLATFORMS

CON	7,703,085	10/4/2005	Daniel POZNANOVIC, David BARKER, Jeffrey HAMMES, Jeffrey Paul BROOKS, Jon STEIDEL, Lisa KRAUSE	PROCESS FOR CONVERTING PROGRAMS IN HIGH-LEVEL PROGRAMMING LANGUAGES TO A UNIFIED EXECUTABLE FOR HYBRID COMPUTING PLATFORMS
JP DIV	5036801	12/28/2009	Daniel POZNANOVIC, David BARKER, Jeffrey HAMMES, Jeffrey Paul BROOKS, Jon STEIDEL, Lisa KRAUSE	PROCESS FOR CONVERTING PROGRAMS IN HIGH-LEVEL PROGRAMMING LANGUAGES TO A UNIFIED EXECUTABLE FOR HYBRID COMPUTING PLATFORMS
JPN	4482454	9/30/2003	Daniel POZNANOVIC, David BARKER, Jeffrey HAMMES, Jeffrey Paul BROOKS, Jon STEIDEL, Lisa KRAUSE	PROCESS FOR CONVERTING PROGRAMS IN HIGH-LEVEL PROGRAMMING LANGUAGES TO A UNIFIED EXECUTABLE FOR HYBRID COMPUTING PLATFORMS
USA	7,299,458	10/31/2002	Jeffrey HAMMES	SYSTEM AND METHOD FOR CONVERTING CONTROL FLOW GRAPH REPRESENTATIONS TO CONTROL-DATAFLOW GRAPH REPRESENTATIONS
USA	6,964,029	10/31/2002	Daniel POZNANOVIC, Jeffrey HAMMES, Jon STEIDEL, Lisa KRAUSE	SYSTEM AND METHOD FOR PARTITIONING CONTROL-DATAFLOW GRAPH REPRESENTATIONS

USA	7,155,708	10/31/2002	Daniel POZNANOVIC, Jeffrey HAMMES, Lonnie GLIEM	DEBUGGING AND PERFORMANCE PROFILING USING CONTROL-DATAFLOW GRAPH REPRESENTATIONS WITH RECONFIGURABLE HARDWARE EMULATION
JPN	4403080	10/6/2003	Daniel POZNANOVIC, Jeffrey HAMMES, Lonnie GLIEM	DEBUGGING USING CONTROL-DATAFLOW GRAPH WITH RECONFIGURABLE HARDWARE EMULATION
USA	7,134,120	1/14/2003	Jeffrey HAMMES	MAP COMPILER PIPELINED LOOP STRUCUTRE
JPN	4330582	10/17/2003	Jeffrey HAMMES	MAP COMPILER PIPELINED LOOP STRUCUTRE
USA	7,424,552	7/11/2003	Lee A. BURTON	SWITCH/NETWORK ADAPTER PORT INCORPORATING SHARED MEMORY RESOURCES SELECTIVELY ACCESSIBLE BY A DIRECT EXECUTION LOGIC ELEMENT AND ONE OR MORE DENSE LOGIC DEVICES
CIP/DIV	7,680,968	8/6/2007	Lee A. BURTON	SWITC/NETWORK ADAPTER PORT INCORPORATING SHARED MEMORY RESOURCES SELECTIVELY ACCESSIBLE BY A DIRECT EXECUTION LOGIC ELEMENT AND ONE OR MORE DENSE LOGIC DEVICES IN A FULLY BUFFERED DUAL IN-LINE MEMORY MODULE FORMAT (FB-DIMM)

DE	EP1652058	6/29/2004	Lee A. BURTON	SWITCH NETWORK ADAPTER PORT INCORPORATING SELECTIVELY ACCESSIBLE SHARED MEMORY RESOURCES
FR	EP1652058	6/29/2004	Lee A. BURTON	SWITCH NETWORK ADAPTER PORT INCORPORATING SELECTIVELY ACCESSIBLE SHARED MEMORY RESOURCES
GB	EP1652058	6/29/2004	Lee A. BURTON	SWITCH NETWORK ADAPTER PORT INCORPORATING SELECTIVELY ACCESSIBLE SHARED MEMORY RESOURCES
USA	7,149,867	6/16/2004	Daniel POZNANOVIC, David CALIGA, Jeffrey HAMMES	SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE
USA	7,890,686	10/17/2005	Bryan CONNER	DYNAMIC PRIORITY CONFLICT RESOLTUION IN A MULTI-PROCESSOR COMPUTER SYSTEM HAVING SHARED RESOURCES
Pending Patent Applications				
Country	**Serial No.**	**Filing Date**	**Inventor(s)**	**Title**
EPO	98963778.0	12/3/1998	Jon M. HUPPENTHAL, Paul A. LESKAR	MULTIPROCESSOR COMPUTER ARCHITECTURE INCORPORATING A PLURALITY OF MEMORY ALGORITHM PROCESSORS IN THE MEMORY SUBSYSTEM

JP DIV	2009-270774	11/27/2009	Jon M. HUPPENTHAL, Paul A. LESKAR	MULTIPROCESSOR COMPUTER ARCHITECTURE INCORPORATING A PLURALITY OF MEMORY ALGORITHM PROCESSORS IN THE MEMORY SUBSYSTEM
EPO	02731698.3	5/6/2002	Jon M. HUPPENTHAL	SYSTEM AND METHOD FOR WEB SERVER WITH A RECONFIGURABLE PROCESSOR OPERATING UNDER SINGLE OPERATION SYSTEM IMAGE
EP DIV	EP10183862.1	9/16/2003	David CALIGA, Jon M. HUPPENTHAL	ENHANCED PARALLEL PERFORMANCE MULTI-ADAPTIVE COMPUTATIONAL SYSTEM
EPO	03749789.8	9/22/2003	Jeffrey HAMMES	TECHNIQUE FOR IMPROVING THE EFFICIENCY OF RECONFIGURABLE HARDWARE
EPO	03759616.0	9/30/2003	Daniel POZNANOVIC, David BARKER, Jeffrey HAMMES, Jeffrey Paul BROOKS, Jon STEIDEL, Lisa KRAUSE	PROCESS FOR CONVERTING PROGRAMS IN HIGH-LEVEL PROGRAMMING LANGUAGES TO A UNIFIED EXECUTABLE FOR HYBRID COMPUTING PLATFORMS
EPO	03773109.8	10/1/2003	Jeffrey HAMMES	SYSTEM AND METHOD FOR CONVERTING FLOW GRAPH REPRESENTATIONS TO CONTROL-DATAFLOW GRAPH REPRESENTATIONS

EPO	03759724.2	10/2/2003	Daniel POZNANOVIC, Jeffrey HAMMES, Jon STEIDEL, Lisa KRAUSE	SYSTEM AND METHOD FOR PARTITIONING CONTROL-DATAFLOW GRAPH REPRESENTATIONS
EPO	03776468.5	10/17/2003	Jeffrey HAMMES	MAP COMPILER PIPELINED LOOP STRUCTURE
EPO	04776806.4	6/17/2004	Daniel POZNANOVIC, David CALIGA, Jeffrey HAMMES	SYSTEM AND METHOD OF ENHANCING EFFICIENCY AND UTILIZATION OF MEMORY BANDWIDTH IN RECONFIGURABLE HARDWARE
USA	11/456,466	7/10/2006	Jeffrey HAMMES	ELIMINATION OF STREAM CONSUMER LOOP OVERSHOOT EFFECTS
USA	13/286,996	11/1/2011	Jon M. HUPPENTHAL, Lee A. BURTON, Thomas R. SEEMAN	HETEROGENEOUS COMPUTING SYSTEM COMPRISING A SWITCH/NETWORK ADAPTER PORT INTERFACE UTILIZING LOAD-REDUCED DUAL IN-LINE MEMORY MODULES (LR-DIMMS) INCORPORATING ISOLATION MEMORY BUFFERS

EP	EP11187824.5	11/4/2011	Jon M. HUPPENTHAL, Lee A. BURTON, Thomas R. SEEMAN	HETEROGENEOUS COMPUTING SYSTEM COMPRISING A SWITCH/NETWORK ADAPTER PORT INTERFACE UTILIZING LOAD-REDUCED DUAL IN-LINE MEMORY MODULES (LR-DIMMS) INCORPORATING ISOLATION MEMORY BUFFERS
JP	2011-243285	11/7/2011	Jon M. HUPPENTHAL, Lee A. BURTON, Thomas R. SEEMAN	HETEROGENEOUS COMPUTING SYSTEM COMPRISING A SWITCH/NETWORK ADAPTER PORT INTERFACE UTILIZING LOAD-REDUCED DUAL IN-LINE MEMORY MODULES (LR-DIMMS) INCORPORATING ISOLATION MEMORY BUFFERS
USA	13/287,322	11/2/2011	David CALIGA, David POINTER	SYSTEM AND METHOD FOR COMPUTATIONAL UNIFICATION OF HETEROGENEOUS IMPLICIT AND EXPLICIT PROCESSING ELEMENTS
EP	11188402.9	11/9/2011	David CALIGA, David POINTER	SYSTEM AND METHOD FOR COMPUTATIONAL UNIFICATION OF HETEROGENEOUS IMPLICIT AND EXPLICIT PROCESSING ELEMENTS

JP	2011-243501	11/7/2011	David CALIGA, David POINTER	SYSTEM AND METHOD FOR COMPUTATIONAL UNIFICATION OF HETEROGENEOUS IMPLICIT AND EXPLICIT PROCESSING ELEMENTS
USA	13/365,090	2/2/2012	James GUZY, Jeffrey HAMMES, John M. HUPPENTHAL, Thomas R. SEEMAN	MOBILE ELECTRONIC DEVICES UTILIZING RECONFIGURABLE PROCESSING TECHNIQUES TO ENABLE HIGHER SPEED APPLICATIONS WITH LOWERED POWER CONSUMPTION
EP	12197336.6	12/14/2012	James GUZY, Jeffrey HAMMES, John M. HUPPENTHAL, Thomas R. SEEMAN	MOBILE ELECTRONIC DEVICES UTILIZING RECONFIGURABLE PROCESSING TECHNIQUES TO ENABLE HIGHER SPEED APPLICATIONS WITH LOWERED POWER CONSUMPTION
JP	2012-273882	12/17/2012	James GUZY, Jeffrey HAMMES, John M. HUPPENTHAL, Thomas R. SEEMAN	MOBILE ELECTRONIC DEVICES UTILIZING RECONFIGURABLE PROCESSING TECHNIQUES TO ENABLE HIGHER SPEED APPLICATIONS WITH LOWERED POWER CONSUMPTION

USA	13/903,720	5/28/2013	David CALIGA, John M. HUPPENTHAL, Lee A. BURTON, Tim TEWALT	MULTI-PROCESSOR COMPUTER ARCHITECTURE INCORPORATING DISTRIBUTED MULTI-PORTED COMMON MEMORY MODULES
Patent Applications in Preparation				
Country	**Docket No.**	**Expected Filing Date**	**Inventor(s)**	**Title**
NONE				

EXHIBIT C

Trademarks

Trademark Name	Registration Number	Registration Date
SRC®	3,164,434	10/31/2006
Hi-Bar®	2,980,597	08/02/2005
MAP®	2,772,045	10/07/2003

EXHIBIT D

Trade Secrets Licenses