PATENT ASSIGNMENT COVER SHEET

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
RMI CORPORATION	12/29/2009

RECEIVING PARTY DATA

Name:	NETLOGIC MICROSYSTEMS, INC.
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City:	MOUNTAIN VIEW
State/Country:	CALIFORNIA
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PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	13253044

OP $40.00 13253044

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ATTORNEY DOCKET NUMBER:	4875.167000B
NAME OF SUBMITTER:	PRANAY K. PATTANI
Signature:	/Pranay K. Pattani, Reg. No. 66,587/
Date:	10/10/2013

Total Attachments: 19
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PATENT ASSIGNMENT

This Patent Assignment (the "Assignment") is made and entered into by and between **RMI CORPORATION**, a corporation organized and existing under and by virtue of the laws of the state of Delaware and having its principal place of business at 18920 Forge Drive, Cupertino, California 95014 (hereinafter referred to as "ASSIGNOR"), and **NETLOGIC MICROSYSTEMS, Inc.**, a corporation organized and existing under and by virtue of the laws of the state of Delaware and having its principal place of business at 1875 Charleston Road, Mountain View, CA 94043-1215 (hereinafter referred to as "ASSIGNEE").

NOW, THEREFORE, for good and valuable consideration, the receipt of which is hereby acknowledged, the parties hereto agree as follows:

1) The ASSIGNOR hereby sells, assigns, transfers and sets over unto the said ASSIGNEE (i) all right, title and interest in and to the patents and applications listed on EXHIBIT A ("Assigned Patents"), and all right, title and interest in and to all patents, applications, and inventions not yet filed as an application owned by ASSIGNOR, or for which ASSIGNOR has rights or interests to assign ("Assigned Patents") with the right to file, and all right title and interest in, divisionals, continuations, continuations-in-part, substitute, continued prosecution, request for continued examination, renewals, reexaminations and reissues of the Assigned Patents, including but not limited to the right to file, prosecute and issue patent applications and patents claiming priority to the Assigned Patents; (ii) all patents and applications to which any of the Assigned Patents claim priority; and (iii) all past, present and future claims against any person with respect to the Assigned Patents, and all rights to

recover past, present and future damages and remedies for the infringement or misappropriation of the Assigned Patents ("Assigned Claims"), with all of the foregoing hereinafter collectively referred to as "Assigned Patent rights".

2) The foregoing assignment of rights, title, and interest is not only in the United States and its territorial possessions, but in all countries foreign thereto to be obtained for the Assigned Patents, and to any continuation, division, renewal, substitute or reissue thereof or any legal equivalent thereof in the United States or a foreign country for the full term or terms for which the same may be granted, including all priority rights under any international conventions or treaties; and ASSIGNOR hereby authorizes and requests the United States Commissioner of Patents and Trademarks, and any officials of foreign countries whose duty it is to issue patents or any legal equivalent thereof, to issue the Assigned Patents to ASSIGNEE, its successors and assigns, in accordance with this Assignment.

3) The ASSIGNOR hereby covenants that no assignment, sale, agreement or encumbrance has been or will be made or entered into which would conflict with the Agreement; the ASSIGNOR further covenants that ASSIGNEE will, upon its request, be provided promptly with all pertinent facts and documents relating to said patents as may be known and accessible to ASSIGNOR and will testify as to the same in any interference or litigation related thereto and will promptly execute and deliver to ASSIGNEE or its legal representative any and all papers, instruments or affidavits required to apply for, obtain, maintain, issue and enforce said application, said patents and said equivalents in the United States or in any foreign country, which may be necessary or desirable to carry out the purposes thereof.

4) This Assignment shall be governed by the laws of the State of California.

"ASSIGNOR"	"ASSIGNEE"
RMI CORPORATION	NETLOGIC MICROSYSTEMS, Inc.
By: Roland Cortes	By: Roland Cortes
Signature: RBC	Signature: RBC
Title: Corporate Secretary	Title: Vice President, General Counsel
Date: 12-29-2009	Date: 12-29-2009

EXHIBIT A
Assigned Patents

Issued U.S. Patents

Patent Number	Title	Jurisdiction	Date Issued
7,617,241	Method and apparatus for enhanced hashing	US	11/10/2009
7,627,721	Advanced processor with cache coherency	US	12/01/2009
7,627,717	ADVANCED PROCESSOR MESSAGING APPARATUS INCLUDING FAST MESSAGING RING COMPONENTS CONFIGURED TO ACCOMODATE POINT-TO-POINT TRANSFER OF NON-MEMORY RELATED MESSAGES	US	12/01/2009
7613201	Stacked Network Switch Using Resilient Packet Ring Communication Protocol	US	11/03/2009
7586911	Method and Apparatus For Packet Transmit Queue Control	US	9/08/2009
7562196	Method and Apparatus for Determining Precedence in a Classification Engine	US	7/14/2009
7538696	System and Method for Huffman Decoding Within A Compression Engine	US	5/26/2009
7538695	System and Method for Deflate Processing Within a Compression Engine	US	5/26/2009
7536631	Advanced Communication Apparatus and Method for Verified Communication	US	5/19/2009
7516119	METHOD AND APPARATUS FOR ACTION GROUP GENERATION AND ARBITRATION IN A CLASSIFICATION ENGINE	US	4/7/2009
7509476	Advanced Processor Translation Lookaside Buffer Management in a	US	3/24/2009

Patent Number	Title	Jurisdiction	Issue Date
	Multithreaded System		
7509462	Advanced Processor With Use Of Bridges On A Data Movement Ring For Optimal Redirection Of Memory And I/O traffic	US	3/24/2009
7487379	High Performance Integrated Circuit With Low Skew Clocking Networks and Improved Low Power Operating Mode Having Reduced Recovery Time	US	2/3/2009
7487369	Low-Power Cache System and Method	US	2/3/2009
7471682	Method and Apparatus For Providing Internal Table Extensibility Based On Product Configuration	US	12/30/2008
7467243	Advanced Processor With Scheme For Optimal Packet Flow In A Multi-Processor System On A Chip	US	12/16/2008
7461213	Advanced Processor System Using Request, Data, Snoop, and Response Rings	US	12/2/2008
7461215	Advanced Processor With Implementation Of Memory Ordering On A Ring Based Data Movement Network	US	12/2/2008
7447204	Method and Device for the Classification and Redirection of Data Packets in a Heterogeneous Network	US	11/4/2008
7426216	Advanced Telecommunications Router And Crossbar Switch Controller	US	9/16/2008
7426608	Method and Apparatus for Constructing a Search Key	US	9/16/2008
7420969	Network Switch With A Parallel Shared Memory	US	9/2/2008
7346757	Advanced Processor Translation Lookaside Buffer Management In A	US	3/18/2008

Patent Number	Title	Jurisdiction	Date Issued
	Multithreaded System		
7334086	Advanced Processor With System On A Chip Interconnect Technology	US	2/19/2008
7333512	Dynamic Mixing TDM Data with Data Packets	US	2/19/2008
7327758	Method Of Generating, Transmitting, Receiving And Recovering Synchronous Frames With Non-Standard Speeds	US	2/5/2008
7260095	Technique For Deallocation Of Memory In A Multicasting Environment	US	8/21/2007
7234019	METHOD AND APPARATUS FOR IMPLEMENTING A SEARCH ENGINE USING AN SRAM	US	6/19/2007
7213111	METHOD AND APPARATUS FOR DETERMINING PRECEDENCE IN A CLASSIFICATION ENGINE	US	5/1/2007
7206323	INTERFACING 622.08 MHz LINE INTERFACE TO A 77.76 MHz SONET FRAMER	US	4/17/2007
7188232	PIPELINED PROCESSING WITH COMMIT SPECULATION STAGING BUFFER AND LOAD/STORE CENTRIC EXCEPTION HANDLING	US	3/6/2007
7174441	METHOD AND APPARATUS FOR PROVIDING INTERNAL TABLE EXTENSIBILITY WITH EXTERNAL INTERFACE	US	2/6/2007
7173927	HYBRID NETWORK TO CARRY SYNCHRONOUS AND ASYNCHRONOUS TRAFFIC OVER SYMMETRIC AND ASYMMETRIC LINKS	US	2/6/2007
7164860	Advanced Multi-Protocol Optical Transport Network	US	1/16/2007

Patent Number	Title	Application	Date Issued
7165102	Adaptive Link Quality Management For Wireless Medium	US	1/16/2007
7099584	Advanced Error Correcting Optical Transport Network	US	8/29/2006
7072345	PROGRAMMABLE INTEGRATED CIRCUIT FOR USE IN A NETWORK SWITCH	US	7/4/2006
7062767	METHOD FOR COORDINATING INFORMATION FLOW BETWEEN COMPONENTS	US	6/13/2006
7046681	NETWORK SWITCH FOR ROUTING NETWORK TRAFFIC	US	5/16/2006
7028069	DYNAMIC CIRCUIT USING EXCLUSIVE STATES	US	4/11/2006
7002916	ASYNCHRONOUS TRANSFER MODE TRAFFIC SHAPERS	US	2/21/2006
7002978	SCHEDULING TECHNIQUES FOR DATA CELLS IN A DATA SWITCH	US	2/21/2006
6963895	FLOATING POINT PIPELINE METHOD AND CIRCUIT FOR FAST INVERSE SQUARE ROOT CALCULATIONS	US	11/8/2005
6775788	Method for providing a synchronous communication and transaction between functions on an integrated circuit therefore the functions operate independently at their own optimized speeds	US	8/10/2004
6735689	METHOD AND SYSTEM FOR REDUCING TAKEN BRANCH PENALTY	US	5/11/2004
6708282	METHOD AND SYSTEM FOR INITIATING COMPUTATION UPON UNORDERED RECEIPT OF DATA	US	3/16/2004
6694408	SCALABLE REPLACEMENT METHOD AND SYSTEM IN A	US	2/17/2004

Patent Number	Title	Jurisdiction	Date Issued
	CACHE MEMORY		
6686774	SYSTEM AND METHOD FOR A HIGH SPEED, BI-DIRECTIONAL, ZERO TURNAROUND TIME, PSEUDO DIFFERENTIAL BUS CAPABLE OF SUPPORTING ARBITRARY NUMBER OF DRIVERS AND RECEIVERS	US	2/3/2004
6594753	METHOD AND APPARATUS FOR DUAL ISSUE OF PROGRAM INSTRUCTIONS TO SYMMETRIC MULTIFUNCTIONAL EXECUTION UNITS	US	7/15/2003
6530011	METHOD AND APPARATUS FOR VECTOR REGISTER WITH SCALAR VALUES	US	3/4/2003
6480872	FLOATING-POINT AND INTEGER MULTIPLY-ADD AND MULTIPLY-ACCUMULATE	US	11/12/2002
6400599	Cache Memory Cell With A Pre-Programmed State	US	6/4/2002
6388471	SINGLE PHASE EDGE TRIGGER REGISTER	US	5/14/2002
6349098	METHOD AND APPARATUS FOR FORMING A VIRTUAL CIRCUIT	US	2/19/2002
6311292	Circuit, Architecture And Method For Analyzing The Operation Of A Digital Processing System	US	10/30/2001
6292061	LOW-VOLTAGE CMOS PHASE-LOCKED LOOP (PLL) FOR HIGH-PERFORMANCE MICROPROCESSOR CLOCK GENERATION	US	9/18/2001
6255879	DIGITAL PROGRAMMABLE DELAY ELEMENT	US	7/3/2001
6252818	Apparatus And Method For Operating A Dual Port Memory Cell	US	6/26/2001

Patent Number	Title	Jurisdiction	Issue Date
6252819	REDUCED LINE SELECT DECODER FOR A MEMORY ARRAY	US	6/26/2001
6229812	SCHEDULING TECHNIQUES FOR DATA CELLS IN A DATA SWITCH	US	5/8/2001
6198723	ASYNCHRONOUS TRANSFER MODE TRAFFIC SHAPERS	US	3/6/2001
6092129	METHOD AND APPARATUS FOR COMMUNICATING SIGNALS BETWEEN CIRCUITS OPERATING AT DIFFERENT FREQUENCIES	US	7/18/2000
6088784	PROCESSOR WITH MULTIPLE EXECUTION UNITS AND LOCAL AND GLOBAL REGISTER BYPASSES	US	7/11/2000
6085271	SYSTEM BUS ARBITRATOR FOR FACILITATING MULTIPLE TRANSACTIONS IN A COMPUTER SYSTEM	US	7/4/2000
6070229	Cache Memory Cell With A Preprogrammed State	US	5/30/2000
6069893	Asynchronous Transfer Mode Switching Architectures Having Connection Buffers	US	5/30/2000
6055606	WRITEBACK CACHE CELL WITH A DUAL PORTED DIRTY BIT CELL AND METHOD FOR OPERATING SUCH A CACHE CELL	US	4/25/2000
6035388	METHOD AND APPARATUS FOR DUAL ISSUE OF PROGRAM INSTRUCTIONS TO SYMMETRIC MULTIFUNCTIONAL EXECUTION UNITS	US	3/7/2000

Issued Non-U.S. Patents

Patent Number	Title	Jurisdiction	Date Issued
233630	Advanced Processor	IN	3/31/2009
ZL200480006509.1	Method and Device for the Classification and Redirection of Data Packets in a Heterogeneous Network	CN	5/20/2009
ZL200480024380.7	Advanced Processor	CN	6/10/2009
I225346	Crossbar Switch controller and method of Optimizing the Same	TW	1/6/2009

Filed U.S. Patent Applications

Application Serial Number	Title	Jurisdiction	Filing Date
12/627,915	ADVANCED PROCESSOR WITH CACHE COHERENCY	US	11/30/2009
12/633,702	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR RE-DIRECTING A MESSAGE FROM A FIRST QUEUE TO A SECOND QUEUE IN RESPONSE TO A REQUEST BY THE RECEIVER AGENT ASSOCIATED WITH THE SECOND QUEUE	US	12/08/09
12/582622	Advanced Processor With Fast Messaging Network Technology	US	10/20/2009
12/571230	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR CONDITIONALLY SENDING A REQUEST FOR DATA TO A HOME NODE	US	9/30/2009
12/571233	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR CONDITIONALLY SENDING A REQUEST FOR DATA TO A NODE BASED ON A DETERMINATION	US	9/30/2009
12/567608	METHOD AND APPARATUS FOR ENHANCED HASHING	US	9/25/2009
12/567595	Stacked Network Switch Using Resilient	US	9/25/2009

Application/Control Number	Title	Jurisdiction	Filing Date
	Packet Ring Communication Protocol		
12/363101	Method and Device for Accessing Variable Length Code Information	US	1/30/2009
12/363076	Method and Device for Decoding Video Information	US	1/30/2009
12/332061	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR SENDING A SNOOP REQUEST TO ONLY NODES IN A MULTIPROCESSOR SYSTEM THAT AT LEAST POTENTIALLY INCLUDE A COPY OF REQUESTED DATA	US	12/10/2008
12/325050	NETWORK-ON-CHIP SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR TRANSMITTING MESSAGES UTILIZING A CENTRALIZED ON-CHIP SHARED MEMORY SWITCH	US	11/28/2008
12/262211	Device For Decoding A Video Stream And Method Thereof	US	10/31/2008
12/261808	Advanced Processor With Credit Based Scheme For Optimal Packet Flow In A Multi-Processor System On A Chip	US	10/30/2008
12/242161	Method and Device for Accessing Variable Length Code Information	US	9/30/2008
12/242838	High Performance Low Voltage Level Shifter Systems and Methods	US	9/30/2008
12/202285	Method And Device Of Processing Video	US	8/31/2008
12/202293	Method and Device for Reordering Video Information	US	8/31/2008
12/201689	System and Method for Reducing Latency Associated with Timestamps in a Multi-core, Multi-threaded Processor	US	8/29/2008
12/198776	OUTPUT QUEUED SWITCH WITH A PARALLEL SHARED MEMORY, AND METHOD OF OPERATING SAME	US	8/26/2008
12/170269	Advanced Telecommunications Router And Crossbar Switch Controller	US	7/9/2008

Application/Control Number	Title	Jurisdiction	Filing Date
12/169465	System And Method For Performing Left/Right Shift, Rotate, Extract And Insert Functions Utilizing the Same Hardware Shifter or Rotator	US	7/8/2008
12/120082	System And Method For Offloading Packet Protocol Encapsulation From Software	US	5/13/2008
12/102473	SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR CREATING DEPENDENCIES AMONGST INSTRUCTIONS USING TAGS	US	4/14/2008
12/055061	System, Method, And Computer Program Product For Receiving Timer Objects From Local Lists In A Global List For Being Used To Execute Events Associated Therewith	US	3/25/2008
12/046675	Segmented Write Bitline System And Method	US	3/12/2008
12/031524	System, Method, and Computer Program Product for Saving and Restoring A Compression/Decompression State	US	2/14/2008
12/028586	System and Method for Parsing and Allocating a Plurality of Packets to Processor Core Threads	US	2/8/2008
12/019576	Delegating Network Processor Operations to Star Topology Serial Bus Interfaces	US	1/24/2008
12/018144	ADVANCED PROCESSOR TRANSLATION LOOKASIDE BUFFER MANAGEMENT IN A MULTITHREADED SYSTEM	US	1/22/2008
12/014685	Dynamic Mixing of TDM Data with Data Packets	US	1/15/2008
11/967690	System, Method and Device to Encode and Decode Video Data Having Multiple Video Data Formats	US	12/31/2007
11/967697	System, Method and Device for Processing Macroblock Video Data	US	12/31/2007

Application/Control Number	Title	Jurisdiction	Filing Date
11/961910	Advanced Processor Translation Lookaside Buffer Management In A Multithreaded System	US	12/20/2007
11/852916	System And Method For Performing A Register Renaming Operation Utilizing Hardware Which Is Capable Of Operating In At Least Two Modes Utilizing Registers Of Multiple Widths	US	9/10/2007
11/849166	System and method for Huffman Decoding within a compression engine	US	8/31/2007
11/847170	Age Matrix For Queue Dispatch Order	US	8/29/2007
11/831887	Delegating Network Processor Operations to Star Topology Serial Bus Interfaces	US	7/31/2007
11/830727	Age Matrix For Queue Dispatch Order	US	7/30/2007
11/820350	Age Matrix For Queue Dispatch Order	US	6/19/2007
11/801937	Method and Apparatus for Implementing a Search Engine Using an SRAM	US	5/10/2007
11/799293	Universal Branch Identifier for Invalidation of Speculative Instructions	US	4/30/2007
11/652827	Systems And Methods For Utilizing An Extended Translation Look-Aside Buffer Having A Hybrid Memory Structure	US	1/11/2007
11/336188	System And Method For Performing Concatenation Of Diversely Routed Channels	US	1/20/2006
11/236324	Scaleable channel scheduler system and method	US	9/26/2005
11/093184	Mechanism for Managing Access to Resources in a Heterogeneous Data Redirection Device	US	3/28/2005
10/968460	Prefix Matching Structure and Method For Fast Packet Switching	US	10/18/2004
10/930938	Multi-Core Multi-Threaded Processing Systems With Instruction Reordering In An In-Order Pipeline	US	8/31/2004

Application Serial Number	Title	Jurisdiction	Filing Date
10/930939	Advanced processor with mechanism for maximizing resource usage in an in-order pipeline with multiple threads	US	8/31/2004
10/930455	Advanced Processor With Mechanism for Fast Packet Queuing Operations	US	8/31/2004
10/931003	Advanced Processor With Interrupt Delivery Mechanism For Multi-Threaded Multi-CPU System on a Chip	US	8/31/2004
10/930937	Advanced Processor With Interfacing Messaging Network To A CPU	US	8/31/2004
10/931014	Advanced Processor With Mechanism for Packet Distribution at High Line Rate	US	8/31/2004
10/930456	Advanced Processor With Mechanism For Enforcing Ordering Between Information Sent On Two Independent Networks	US	8/31/2004
10/930175	Advanced Processor With A Thread Aware Return Address Stack Optimally Used Across Active Threads	US	8/31/2004
10/898007	Advanced Processor Scheduling In A Multithreaded System	US	7/23/2004
10/826215	Stacked Network Switch Using Resilient Packet Ring Communication Protocol	US	4/16/2004
10/740910	Extended Reach Media Access Architecture	US	12/19/2003
10/703842	METHOD AND APPARATUS FOR ENHANCED HASHING	US	11/7/2003
10/687784	Encoding-Based Multicast Packet Duplication Control Suitable For VLAN Systems	US	10/17/2003
10/687786	Method and Apparatus For Packet Transmit Queue Control	US	10/17/2003
10/682579	Advanced telecommunications processor	US	10/08/2003
10/452563	Multi-Protocol Communication Circuit	US	5/30/2003
10/023972	Integration of network, data link, and physical layer to adapt network traffic	US	12/17/2001
10/023633	Network node with multi-medium interfaces	US	12/17/2001

Application/Serial Number	Title	Registration	Filing Date
60/416838	Advanced telecommunications processor	US	10/8/2002
60/490236	Advanced telecommunications processor	US	7/25/2003
60/630527	High performance integrated circuit with low skew clocking networks and improved low power operating mode having reduced recovery time	US	11/22/2004
60/342636	Advanced optical transport network and components therefor	US	12/21/2001
60/434328	Technique for deallocation of memory in a multicasting environment	US	12/17/2002
60/443159	Classification of packets in a heterogeneous data redirection device	US	1/27/2003
60/645841	System and method for providing flexible data packet processing and SONET/SDH processing	US	1/21/2005
11/831884	Technique For Deallocation of Memory In A Multicasting Environment	US	7/31/2007
60/333945	Advanced telecommunications router and crossbar switch controller	US	11/20/2001
60/435120	Advanced communication apparatus and method for verified communication	US	12/19/2002
60/463992	Stacked network switch using resilient packed ring communication protocol	US	4/18/2003
60/512121	Prefix matching structure and method for fast packet switching	US	10/17/2003
60/426691	Multi-protocol serializer-deserializer (SerDes)	US	11/15/2002
60/434956	Extended reach media access architecture	US	12/20/2002
09/496862	Clock distribution system and design method	US	2/20/2000
09/562060	System for Efficient Instruction and Program Counter Storage in a Unified Fetch Buffer	US	5/1/2000
09/564714	Method and Apparatus for Register Bypass	US	5/3/2000

Application Serial Number	Title	Jurisdiction	Filing Date
	Using a Source Identification and a Result Buffer		
09/562059	Method and system of a tag row decoder with multiple cycle access	US	5/1/2000
09/562054	Robust Clock Synchronization for the I/O Interface of Half Point Divide Mode CPU Operation and Bypass PLL Testing	US	5/1/2000
09/911553	Method and System for Speculative Memory Operations	US	7/23/2001
09/938450	System and Method for Group Permission in a Virtual Memory	US	8/23/2001
09/970250	Dynamic Circuit Using Exclusive States	US	10/3/2001
09/562063	Dynamic Circuit Using Exclusive States	US	5/1/2000
09/970112	Dynamic Circuit Using Exclusive States	US	10/3/2001
60/029652	ASYNCHRONOUS TRANSFER MODE SWITCHING ARCHITECTURES HAVING CONNECTION BUFFERS	US	10/28/1996
60/273964	Interfacing 622.08 MHz LVDS line interface to a 77.76 MHz SONET framer	US	3/6/2001
60/256540	Packet-based dual-ring broadband wireless network	US	12/18/2000
60/276610	Architecture optimized to support fixed-rate synchronous native TDM data (SONET) and burstry asynchronous data transmission over metropolitan area networking using any physical medium including but not limited to optical or wireless medium	US	3/16/2001
11/710249	Methods and systems for optimizing placement on a clock signal distribution network	US	2/23/2007
61/085385	High Performance Low Voltage Level Shifter Systems and Methods	US	7/31/2008
61/077107	System and Method for Performing Left/Right Shift, Rotate, Extract and Insert Functions Utilizing the Same Hardware Shifter or Rotator	US	6/30/2008

Application/Serial Number	Title	Jurisdiction	Filing Date
12/242131	Method and Device for Decoding Video Information	US	9/30/2008
61/101465	Method and Device for Accessing Variable Length Code Information	US	9/30/2008

Filed Non-U.S. Patent Applications

Application/Serial Number	Title	Jurisdiction	Filing Date
National Stage of PCT/US2008/009040	DELEGATING NETWORK PROCESSOR OPERATIONS TO STAR TOPOLOGY SERIAL BUS INTERFACES	CN	7/25/2008
08794748.7	DELEGATING NETWORK PROCESSOR OPERATIONS TO STAR TOPOLOGY SERIAL BUS INTERFACES	EP	7/25/2008
PCT/US2009/065802	NETWORK-ON-CHIP SYSTEM, METHOD, AND COMPUTER PROGRAM PRODUCT FOR TRANSMITTING MESSAGES UTILIZING A CENTRALIZED ON-CHIP SHARED MEMORY SWITCH	WO	11/24/2009
PCT/US09/58919	Device For Decoding A Video Stream And Method Thereof	WO	9/30/2009
PCT/US09/54160	Method And Device of Processing Video	WO	8/18/2009
PCT/US09/04657	System and Method for Reducing Latency Associated with Timestamps in a Multi-Core, Multi-Threaded Processor	WO	8/13/2009
PCT/US2009/001685	System And Method For Offloading Packet Protocol Encapsulation From Software	WO	3/16/2009
PCT/US2009/001383	RECEIVING TIMER OBJECTS FROM LOCAL LISTS IN A GLOBAL LIST TO EXECUTE EVENTS	WO	3/3/2009
PCT/US2009/000635	System and Method for Parsing and Allocating a Plurality of Packets to Processor Core Threads	WO	1/30/2009
PCT/US2008/087084	System, Method and Device for Processing Macroblock Video Data	WO	12/17/2008

Application/Serial Number	Title	Jurisdiction	Filing Date
2009-264696	Advanced Processor	JP	7/23/2004
2008-215090	Advanced Processor	JP	7/23/2004
PCT/US2008/009040	Delegating Network Processor Operations to Star Topology Serial Bus Interfaces	WO	7/25/2008
PCT/US2008/008107	System and Method for Compression Processing Within a Compression Engine	WO	6/26/2008
PCT/US2008/007723	Age Matrix For Queue Dispatch Order	WO	6/19/2008
097115993	Universal Branch Identifier for Invalidation of Speculative Instructions	TW	4/30/2008
PCT/US2008/005509	Universal Branch Identifier for Invalidation of Speculative Instructions	WO	4/29/2008
06748548.2	Mechanism for Managing Access to Resources in a Heterogeneous Data Redirection Device	EU	3/21/2006
06719108.0	System And Method For Performing Concatenation Of Diversely Routed Channels	EU	1/20/2006
2007-552302	System And Method For Performing Concatenation Of Diversely Routed Channels	JP	1/20/2006
200680005461.1	System And Method For Performing Concatenation Of Diversely Routed Channels	CN	1/20/2006
06114311.7	Advanced Processor	HK	12/29/2006
06104923.8	Method and Device for the Classification and Redirection of Data Packets in a Heterogeneous Network	HK	1/27/2004
2006-7001707	Advanced Processor	KR	1/25/2006
2006-521286	Advanced Processor	JP	7/23/2004
95102426	System And Method For Performing Concatenation Of Diversely Routed Channels	TW	1/23/2006
93122312	Advanced Processor	TW	7/26/2004
04705699.9	Method and Device for the Classification and Redirection of Data Packets in a	EU	1/27/2004

Application Serial Number	Title	Jurisdiction	Filing Date
	Heterogenous Network		
PCT/US04/23871	ADVANCED PROCESSOR	WO	7/23/2004
PCT/US04/02399	METHOD AND DEVICE FOR THE CLASSIFICATION AND REDIRECTION OF DATA PACKETS IN A HETEROGENEOUS NETWORK	WO	1/27/2004
PCT/US06/037252	SCALEABLE CHANNEL SCHEDULER SYSTEM AND METHOD	WO	9/25/2006
PCT/US06/010401	MECHANISM FOR MANAGING ACCESS TO RESOURCES IN A HETEROGENEOUS DATA REDIRECTION DEVICE	WO	3/21/2006
PCT/US06/002144	SYSTEM AND METHOD FOR PERFORMING CONCATENATION OF DIVERSELY ROUTED CHANNELS	WO	1/20/2006
PCT/US01/44499	NETWORK SWITCH WITH A PARALLEL SHARED MEMORY AND METHOD OF OPERATION	WO	11/28/2001
PCT/US02/037571	ADVANCED TELECOMMUNICATIONS ROUTER AND CROSSBAR SWITCH CONTROLLER	WO	11/21/2002
PCT/US99/08033	ASYNCHRONOUS TRANSFER MODE TRAFFIC SHAPERS	WO	4/13/1999
PCT/US01/49065	NETWORK NODE WITH MULTI-MEDIUM INTERFACES	WO	12/17/2001