PATENT ASSIGNMENT COVER SHEET

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
HVVI SEMICONDUCTOR, INC.	06/28/2012

RECEIVING PARTY DATA

Name:	ESTIVATION PROPERTIES LLC
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Internal Address:	SUITE 101
City:	DOVER
State/Country:	DELAWARE
Postal Code:	19904

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	13690184

OP $40.00 13690184

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ATTORNEY DOCKET NUMBER:	098888-7921
NAME OF SUBMITTER:	PAUL S. HUNTER
Signature:	/Paul S. Hunter/
Date:	10/21/2013

Total Attachments: 9
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Revised Exhibit B

ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, HVVi Semiconductor, Inc., a Delaware corporation, with an address at 4949 West Ray Road, Suite 4376, Chandler, AZ 85226 (***"Assignor"***), does hereby sell, assign, transfer, and convey unto Estivation Properties LLC, a Delaware limited liability company, having an address at 160 Greentree Drive, Suite 101; Dover, DE 19904 (***"Assignee"***), or its designees, all right, title, and interest that exist today and may exist in the future in and to any and all of the following (collectively, the ***"Patent Rights"***):

(a) the patent applications and patents listed in the table below (the "***Patents***");

Patent or Application No.	**Country**	**Filing Date**	**Title of Patent and First Named Inventor**
7656003	US	08/25/2006	Electrical Stress Protection Apparatus and Method of Manufacture Robert Bruce Davies
TW096130560	TW	08/17/2007	Electrical Stress Protection Apparatus and Method of Manufacture Robert Bruce Davies
7888746	US	12/15/2006	Semiconductor Structure and Method of Manufacture Michael Albert Tischler
TW096147283	TW	12/11/2007	Semiconductor Structure and Method of Manufacture Michael Albert Tischler
7812454	US	09/11/2008	Semiconductor Structure and Method of Manufacture Bishnu Prasanna Gogoi
TW097137968	TW	10/02/2008	Semiconductor Structure and Method of Manufacture Bishnu Prasanna Gogoi
8049261	US	10/02/2008	Semiconductor Structure and Method of Manufacture Bishnu Prasanna Gogoi
TW097133646	TW	09/02/2008	Semiconductor Structure and

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
			Method of Manufacture Bishnu Prasanna Gogoi
7985977	US	12/09/2008	Sacrificial Pillar Dielectric Platform Bishnu Prasanna Gogoi
8063467	US	12/09/2008	Semiconductor Structure and Method of Manufacture Michael Albert Tischler
7998829	US	12/09/2008	Semiconductor Structure and Method of Manufacture Michael Albert Tischler
8049297	US	12/09/2008	Semiconductor Structure and Method of Manufacture Michael Albert Tischler
8133794	US	12/09/2008	Semiconductor Structure and Method of Manufacture Michael Albert Tischler
7335534	US	01/06/2006	Semiconductor component and method of manufacture Jeanne S. Pavio
7999250	US	02/27/2009	Silicon-Germanium-Carbon Semiconductor Structure Bishnu Prasanna Gogoi
CN200980107766.7	CN	02/27/2009	Silicon-Germanium-Carbon Semiconductor Structure Bishnu Prasanna Gogoi
TW098106994	TW	03/04/2009	Silicon-Germanium-Carbon Semiconductor Structure Bishnu Prasanna Gogoi
11/387209	US	03/23/2006	Power semiconductor device and method therefor

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
			Robert Bruce Davies
11/387210	US	03/23/2006	Power semiconductor device and method therefor Robert Bruce Davies
7898057	US	03/23/2006	Radio frequency power semiconductor device package comprising dielectric platform and shielding plate Robert Bruce Davies
7847369	US	10/16/2009	Radio frequency power semiconductor device comprising matrix of cavities as dielectric isolation structure Robert Bruce Davies
CNZL200580000549.X	CN	01/06/2005	Power semiconductor device and method therefor Robert Bruce Davies
JP2006-104154	JP	04/05/2006	Power semiconductor device and method therefor Robert Bruce Davies
JP4473834	JP	04/05/2006	Power semiconductor device and method therefor Robert Bruce Davies
JP2006-104156	JP	04/05/2006	Power semiconductor device and method therefor Robert Bruce Davies
JP2006-526445	JP	01/06/2005	Power semiconductor device and method therefor Robert Bruce Davies
KR10-0786488	KR	12/23/2005	Power Semiconductor Device Robert Bruce Davies
7777295	US	12/08/2008	Semiconductor structure and method of manufacture

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
			Bishnu Prasanna Gogoi
8048760	US	07/09/2010	Semiconductor Structure and Method of Manufacture Bishnu Prasanna Gogoi
CN200880125637.6	CN	12/11/2008	Semiconductor Structure and Method of Manufacture Bishnu Prasanna Gogoi
TW097148263	TW	12/11/2008	Semiconductor Structure and Method of Manufacture Bishnu Prasanna Gogoi
7598588	US	10/26/2007	Semiconductor structure and method of manufacture Robert Bruce Davies
EP08842013.8	EP	07/25/2008	Semiconductor structure and method of manufacture Robert Bruce Davies
TW097129925	TW	08/06/2008	Semiconductor structure and method of manufacture Robert Bruce Davies
8067834	US	08/21/2007	Semiconductor Component Daniel D. Moline
EP08796612.3	EP	07/25/2008	Semiconductor Component and Method of Manufacture Daniel D. Moline
TW097129919	TW	08/06/2008	Semiconductor Component and Method of Manufacture Daniel D. Moline
12/364209	US	02/02/2009	Semiconductor Device Having a Diamond Substrate Heat Spreader Jeffrey Dale Crowder

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
TW099103042	TW	02/02/2010	Semiconductor Device Having a Diamond Substrate Heat Spreader Jeffrey Dale Crowder
7811896	US	12/08/2008	Semiconductor structure and method of manufacture Bishnu Prasanna Gogoi
7919801	US	10/21/2008	RF power transistor structure and a method of forming the same Bishnu Prasanna Gogoi
TW097141070	TW	10/24/2008	Semiconductor Structure and Method of manufacture Bishnu P. Gogoi
8133783	US	10/21/2008	Semiconductor device having different structures formed simultaneously Bishnu P. Gogoi
8125044	US	10/21/2008	Semiconductor structure having a unidirectional and a bidirectional device and method of manufacture Bishnu P. Gogoi
CN200880113235.4	CN	10/23/2008	Semiconductor Structure and Method of manufacture Bishnu P. Gogoi
CN200880113357.3	CN	10/23/2008	Semiconductor Structure and Method of manufacture Bishnu P. Gogoi
TW097141036	TW	10/24/2008	Semiconductor Structure and Method of manufacture Bishnu P. Gogoi
TW097141065	TW	10/24/2008	Semiconductor Structure and

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
			Method of manufacture Bishnu P. Gogoi
7605451	US	06/27/2006	RF power transistor having an encapsulated chip package Dan Moline
12/506721	US	07/21/2009	Flange Package For A Semiconductor Device Alex Elliott
8022485	US	10/09/2008	Transistor Structure Having Reduced Input Capacitance Robert Bruce Davies
8076724	US	10/09/2008	Transistor Structure Having an Active Region and a Dielectric Platform Region Robert Bruce Davies
7847350	US	10/09/2008	Transistor Structure Having a Trench Drain Robert Bruce Davies
12/917163	US	11/01/2010	Transistor Structure Having a Trench Drain Robert Bruce Davies
8008720	US	10/09/2008	Transistor Structure Having a Conductive Layer Formed Contiguous in a Single Deposition Robert Bruce Davies
8008719	US	10/09/2008	Transistor Structure Having Dual Shield Layers Robert Bruce Davies
CN200880113402.5	CN	10/23/2008	Semiconductor Structure and Method of manufacture Bishnu P. Gogoi

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
12/691917	US	01/22/2010	Semiconductor Structure Formed without Requiring Thermal Oxidation Bishnu Prasanna Gogoi

(b) all patents and patent applications (i) to which any of the Patents directly or indirectly claims priority, (ii) for which any of the Patents directly or indirectly forms a basis for priority, and/or (iii) that were co-owned applications that incorporate by reference, or are incorporated by reference into, the Patents;

(c) all reissues, reexaminations, extensions, continuations, continuations in part, continuing prosecution applications, requests for continuing examinations, divisions, registrations of any item in any of the foregoing categories (a) and (b);

(d) all foreign patents, patent applications, and counterparts relating to any item in any of the foregoing categories (a) through (c), including, without limitation, certificates of invention, utility models, industrial design protection, design patent protection, and other governmental grants or issuances;

(e) all items in any of the foregoing in categories (b) through (d), whether or not expressly listed as Patents below and whether or not claims in any of the foregoing have been rejected, withdrawn, cancelled, or the like;

(f) inventions, invention disclosures, and discoveries described in any of the Patents and/or any item in the foregoing categories (b) through (e) that (i) are included in any claim in the Patents and/or any item in the foregoing categories (b) through (e), (ii) are subject matter capable of being reduced to a patent claim in a reissue or reexamination proceeding brought on any of the Patents and/or any item in the foregoing categories (b) through (e), and/or (iii) could have been included as a claim in any of the Patents and/or any item in the foregoing categories (b) through (e);

(g) all rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections, or other governmental grants or issuances of any type related to any item in any of the foregoing categories (a) through (f), including, without limitation, under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement, or understanding;

(h) all causes of action (whether known or unknown or whether currently pending, filed, or otherwise) and other enforcement rights under, or on account of, any of the Patents and/or any item in any of the foregoing categories (b) through (g), including, without limitation, all causes of action and other enforcement rights for

(1) damages,
(2) injunctive relief, and
(3) any other remedies of any kind

for past, current, and future infringement; and

(i) all rights to collect royalties and other payments under or on account of any of the Patents and/or any item in any of the foregoing categories (b) through (h).

Assignor represents, warrants and covenants that:

(1) Assignor has the full power and authority, and has obtained all third party consents, approvals and/or other authorizations required to enter into this Agreement and to carry out its obligations hereunder, including the assignment of the Patent Rights to Assignee; and

(2) Assignor owns, and by this document assigns to Assignee, all right, title, and interest to the Patent Rights, including, without limitation, all right, title, and interest to sue for infringement of the Patent Rights. Assignor has obtained and properly recorded previously executed assignments for the Patent Rights as necessary to fully perfect its rights and title therein in accordance with governing law and regulations in each respective jurisdiction. The Patent Rights are free and clear of all liens, claims, mortgages, security interests or other encumbrances, and restrictions. There are no actions, suits, investigations, claims or proceedings threatened, pending or in progress relating in any way to the Patent Rights.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

Assignor will, at the reasonable request of Assignee and without demanding any further consideration therefore, do all things reasonably necessary, proper, or advisable, including without limitation, the execution, acknowledgment, and recordation of specific assignments, oaths, declarations, and other documents on a country-by-country basis, to assist Assignee in obtaining, perfecting, sustaining, and/or enforcing the Patent Rights.

The terms and conditions of this Assignment of Patent Rights will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed at Hilo on June 28, 2012.

ASSIGNOR:

HVVi Semiconductor, Inc.

By: _____
Name: DAVID H. LUTZ
Title: CEO HVVi
(Signature MUST be attested)

ATTESTATION OF SIGNATURE PURSUANT TO 28 U.S.C. § 1746

The undersigned witnessed the signature of DAVID H LUTZ to the above Assignment of Patent Rights on behalf of HVVi Semiconductor, Inc. and makes the following statements:

1. I am over the age of 18 and competent to testify as to the facts in this Attestation block if called upon to do so.

2. DAVID H LUTZ is personally known to me (or proved to me on the basis of satisfactory evidence) and appeared before me on JUNE 28, 2012 to execute the above Assignment of Patent Rights on behalf of HVVi Semiconductor, Inc.

3. DAVID H LUTZ subscribed to the above Assignment of Patent Rights on behalf of HVVi Semiconductor, Inc.

I declare under penalty of perjury under the laws of the United States of America that the statements made in the three (3) numbered paragraphs immediately above are true and correct.

EXECUTED on June 28, 2012 (date)

_____
Print Name: MARY LUTZ