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PATENT ASSIGNMENT COVER SHEET

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SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	ASSIGNMENT	

CONVEYING PARTY DATA

Name	Execution Date
INTELLECTUAL VENTURES FUND 100 LLC	12/30/2013

RECEIVING PARTY DATA

Name:	SECURE AXCESS LLC		
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PROPERTY NUMBERS Total: 22

Property Type	Number
Patent Number:	5687121
Patent Number:	5777923
Patent Number:	5822252
Patent Number:	5768193
Patent Number:	5748538
Patent Number:	5774396
Patent Number:	5848000
Patent Number:	6381670
Patent Number:	5920503
Patent Number:	5777924
Patent Number:	5917757
Patent Number:	5856942
Patent Number:	5856945
Patent Number:	5914896
	PATENT

REEL: 032342 FRAME: 0065

Patent Number:	6023188
Patent Number:	RE37419
Patent Number:	6356615
Patent Number:	6076115
Patent Number:	6085248
Patent Number:	6108713
Patent Number:	6172990
Patent Number:	6393489

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Date:	03/04/2014	

Total Attachments: 4

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PATENT REEL: 032342 FRAME: 0066

Exhibit A-2 ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, Intellectual Ventures Fund 100 LLC, a Delaware limited liability company, having an address at 2711 Centerville Road, Suite 400, Wilmington, DE 19808 ("Assignor"), does hereby sell, assign, transfer, and convey unto Secure Axcess LLC, a Texas limited liability company with an office at 555 Republic Drive, Suite 200, Plano, TX 75074 ("Assignee"), all of Assignor's right, title, and interest in and to the following (collectively, the "Assigned Patent Rights"):

(a) the patents and patent applications listed in the table below (the "Patents");

Patent No.		<u>Issue Date</u>	
(Application No.)	Country	(Filing Date)	Title of Patent Inventor(s)
5687121	US	5/14/1996	Flash EEPROM worldline decoder
			Peter W. Lee; Hsing-Ya Tsao; Fu-Chang Hsu
5777923	US	6/17/1996	Flash memory read/write controller
			Peter W. Lee; Hsing-Ya Tsao; Fu-Chang Hsu
5822252	US	7/5/1996	Flash memory wordline decoder with overerase repair
			Peter W. Lee; Hsing-Ya Tsao; Fu-Chang Hsu
5768193	US	11/7/1996	Bit-refreshable method and circuit for
			refreshing a nonvolatile flash memory
			Peter W. Lee; Hsing-Ya Tsao; Fu-Chang Hsu
5748538	US	11/14/1996	OR-plane memory cell array for flash memory with bit-based write capability, and methods for programming and erasing the memory cell array
		1	Peter W. Lee; Hsing-Ya Tsao; Fu-Chang Hsu
5774396	US	12/9/1996	Flash memory with row redundancy
			Peter W. Lee; Hsing-Ya Tsao; Fu-Chang Hsu
5848000	US	3/18/1997	Flash memory address decoder with novel latch structure
6381670	US	3/25/1997	Peter W. Lee; Hsing-Ya Tsao; Fu-Chang Hsu
0301070	ပစ	312311991	Flash memory array having maximum and minimum threshold voltage detection for eliminating over-erasu
		<u></u>	

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PATENT REEL: 032342 FRAME: 0067

Patent No. (Application No.)	Country	<u>Issue Date</u> (Filing Date)	Title of Patent Inventor(s)
			Peter Wung Lee; Hsing-Ya Tsao; Fu-Chang Hsu; Wen-Tan Fan
5920503	US	5/2/1997	Flash memory with novel bitline decoder and sourceline latch
5777924	US	6/5/1997	Peter W. Lee; Fu-Chang Hsu; Hsing-Ya Tsao Flash memory array and decoding architecture
5917757	US	6/25/1997	Peter W. Lee; Fu-Chang Hsu; Hsing-Ya Tsao Flash memory with high speed erasing structure using thin oxide semiconductor devices
5856942	US	6/30/1997	Peter W. Lee; Fu-Chang Hsu; Hsing-Ya Tsao Flash memory array and decoding architecture
30305-12	05	0/30/1997	
5856945	US	8/5/1997	Peter W. Lee; Fu-Chang Hsu; Hsing-Ya Tsao Method for preventing sub-threshold leakage in flash memory cells to achieve accurate reading, verifying, and fast over-erased vt correction
T04.1004			Peter W. Lee; Fu-Chang Hsu; Hsing-Ya Tsao
5914896	US	8/22/1997	Flash memory with high speed erasing structure using thin oxide and thick oxide semiconductor devices
(002100	TIG	1/1 7/1 000	Peter W. Lee; Fu-Chang Hsu; Hsing-Ya Tsao
6023188	US	1/15/1999	Positive/negative high voltage charge pump system
DE107410	TTG		Peter W. Lee; Hsing-Ya Tsao; Fu-Chang Hsu
RE37419	US	10/29/1999	Flash memory array and decoding architecture
6356615	US	10/13/1999	Fu-Chang Hsu; Hsing-Ya Tsao; Peter W. Lee Programmable event counter system
			Brett Coon; David Keppel; Charles R Price
CNZL00814184.3	CN	9/6/2000	Programmable event computer system
GB1234277	GB	9/6/2000	Brett Coon; David Keppel; Charles R Price Programmable event counter system
		2/0/2000	
KR10-0596761	KR	9/6/2000	Brett Coon; David Keppel; Charles R Price Programmable event counter system

PATENT REEL: 032342 FRAME: 0068

Patent No.	C	Issue Date	THU OD (IT)
(Application No.)	Country	(Filing Date)	Title of Patent Inventor(s)
6076115	US	4/24/1997	Brett Coon; David Keppel; Charles R Price Media access control receiver and network
0070113	05	7/27/179/	management system
			management by bronn
	ļ		Alak K. Deb; Praveen D. Kumar; Namakkal S.
			Sambamurthy; Linh Tien Truong; Devendra K.
(005040	TTC	4/0 4/4 007	Tripathi
6085248	US	4/24/1997	Media access control transmitter and parallel
			network management system
		1	Alak K. Deb; Praveen D. Kumar; Namakkal S.
			Sambamurthy; Linh Tien Truong; Devendra K.
			Tripathi
6108713	US	4/24/1997	Media access control architectures and network
			management systems
			Alak K. Deb; Praveen D. Kumar; Namakkal S.
			Sambamurthy; Linh Tien Truong; Devendra K.
			Tripathi
6172990	US	11/12/1997	Media access control micro-risc stream
			processor and method for implementing the
			same
			Alak K. Deb; Namakkal S. Sambamurthy;
			William H. Bares
6393489	US	6/13/2000	Media access control architectures and network
			management systems
		•	Alala W. Dala Danasa D. Wassa and J. J. G.
			Alak K. Deb; Praveen D. Kumar; Namakkal S. Sambamurthy; Linh Tien Truong; Devendra K.
			Tripathi

- (b) any reissues, reexaminations, extensions, continuations, continuing prosecution application, requests for continuing examinations, divisions, and registrations of any of the Patents;
- (c) rights to apply in any or all countries of the world for future patents, certificates of invention, utility models, industrial design protections, design patent protections, or other future governmental grants or issuances of any type related to the Patents; and
- (d) causes of action and enforcement rights of any kind under, or on account of, any of the Patents and/or any of the items described in either of the foregoing categories (b) or (c), including, without limitation, all causes of action, enforcement rights and all other rights to seek and obtain any other remedies of any kind for past, current and future infringement; and

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all future patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Assigned Patent Rights in the name of Assignee, as the assignee to the entire interest therein. This Assignment of Patent Rights will inure for the benefit of any permitted successors or assigns of Assignee.

Assignor will, at the reasonable request of Assignee, take all reasonable steps necessary and proper, to confirm the assignment to Assignee of the Assigned Patent Rights pursuant to this Assignment of Patent Rights, including without limitation, the execution, acknowledgment, and recordation of specific assignments, oaths, declarations, and other documents on a country-by-country basis, to assist Assignee in obtaining and perfecting the Assigned Patent Rights

IN WITNESS WHEREOF this Assignment of Patent Rights is executed on <u>Jorenhor</u>, <u>30</u>, <u>2013</u>.

ASSIGNOR:

Intellectual Ventures Fund 100%LC

Name: Title:

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RECORDED: 03/04/2014