PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
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EPAS ID: PAT2745939

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY AGREEMENT

CONVEYING PARTY DATA

Name	Execution Date
LUXTERA, INC.	06/29/2012

RECEIVING PARTY DATA

Name:	Silicon Valley Bank
Street Address:	3003 Tasman Drive
City:	Santa Clara
State/Country:	CALIFORNIA
Postal Code:	95054

PROPERTY NUMBERS Total: 13

Property Type	Number
Patent Number:	8289067
Patent Number:	8358940
Patent Number:	8577191
Patent Number:	8592745
Patent Number:	8625935
Patent Number:	8649639
Patent Number:	8626002
Patent Number:	8604866
Patent Number:	8440989
Patent Number:	8433162
Application Number:	13156990
Application Number:	13568406
Application Number:	13568616

CORRESPONDENCE DATA

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ATTORNEY DOCKET NUMBER:	354271-100
NAME OF SUBMITTER:	TROY ZANDER
Signature:	/s/ Troy Zander
Date:	02/27/2014

Total Attachments: 9
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SECOND AMENDED AND RESTATED INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Second Amended and Restated Intellectual Property Security Agreement is entered into as of June 29, 2012 by and between SILICON VALLEY BANK ("SVB," and in its capacity as a collateral agent under the Second Amended and Restated Loan and Security Agreement between SVB, Horizon Technology Finance Corporation and Grantor (as defined below) "Collateral Agent"), and LUXTERA, INC., a Delaware corporation ("Grantor") and amends and restates in its entirety that certain Amended and Restated Intellectual Property Security Agreement by and between Bank and Grantor dated as of March 17, 2010, (the "Original Agreement").

RECITALS

A. Lenders have agreed to make certain advances of money and to extend certain financial accommodation to Grantor (the "Loans") in the amounts and manner set forth in that certain Second Amended and Restated Loan and Security Agreement by and among Collateral Agent, the Lenders a party thereto and Grantor dated as of the Effective Date (as the same may be amended, modified or supplemented from time to time, the "Loan Agreement"; capitalized terms used herein are used as defined in the Loan Agreement). The Lenders are willing to make the Loans to Grantor, but only upon the condition, among others, that Grantor shall grant to Collateral Agent, for the ratable benefit of the Lenders, and to each Lender, a security interest in certain Copyrights, Trademarks, Patents, and Mask Works to secure the obligations of Grantor under the Loan Agreement.

B. Pursuant to the terms of the Loan Agreement, Grantor has granted to Collateral Agent, for the ratable benefit of the Lenders, and each Lender, a security interest in all of Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of its obligations under the Loan Agreement, Grantor hereby represents, warrants, covenants and agrees as follows:

AGREEMENT

To secure its obligations under the Loan Agreement, Grantor grants and pledges to Collateral Agent, for the ratable benefit of the Lenders, and each Lender, a security interest in all of Grantor's right, title and interest in, to and under its intellectual property (including without limitation those Copyrights, Patents and Trademarks listed on Schedules A, B and C hereto), and including without limitation all proceeds thereof (such as, by way of example but not by way of limitation, license royalties and proceeds of infringement suits), the right to sue for past, present and future infringements, all rights corresponding thereto throughout the world and all re-issues, divisions continuations, renewals, extensions and continuations-in-part thereof.

This security interest is granted in conjunction with the security interest granted to Collateral Agent, for the ratable benefit of the Lenders, and each Lender under the Loan Agreement. The rights and remedies of Collateral Agent with respect to the security interest granted hereby are in addition to those set forth in the Loan Agreement and the other Loan Documents, and those which are now or hereafter available to Collateral Agent as a matter of law or equity. Each right, power and remedy of Collateral Agent provided for herein or in the Loan Agreement or any of the Loan Documents, or now or hereafter existing at law or in equity shall be cumulative and concurrent and shall be in addition to every right, power or remedy provided for herein and the exercise by Collateral Agent of any one or more of the rights, powers or remedies provided for in this Intellectual Property Security Agreement, the Loan Agreement or any of the other Loan Documents, or now or hereafter existing at law or in equity, shall not preclude the simultaneous or later exercise by any person, including Collateral Agent, of any or all other rights, powers or remedies.

Except as otherwise set forth herein, this Agreement is intended to and does completely amend and restate, without novation, the Original Agreement. All security interests granted under the Original Agreement are hereby confirmed and ratified and shall continue to secure all Obligations under this Agreement and the other Loan Documents.

IN WITNESS WHEREOF, the parties have caused this Second Amended and Restated Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

LUXTERA, INC.

By: _____

Title: CFO

Address of Grantor:

2320 Camino Vida Roble
Carlsbad, CA 92011

Attn: CFO

COLLATERAL AGENT:

SILICON VALLEY BANK

Address of SVB:

3003 Tasman Drive
Santa Clara, CA 95054-1191

By: _____

Title: _____

Attn: _____

IN WITNESS WHEREOF, the parties have caused this Second Amended and Restated Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

LUXTERA, INC.

Address of Grantor:

2320 Camino Vida Roble
Carlsbad, CA 92011

Attn: _____

By: _____

Title: _____

COLLATERAL AGENT:

SILICON VALLEY BANK

Address of SVB:

3003 Tasman Drive
Santa Clara, CA 95054-1191

Attn: _____

By: _____

Title: RELATIONSHIP MANAGER

EXHIBIT A

Copyrights

Description	Registration Number	Registration Date
None.		

EXHIBIT B

Patents

	Description	Patent/ App No.	Date Filed
1.	Photonic Input/Output Port (Galian Patent)	6788847	28-Mar-02
2.	Structure and Method for Coupling Light Between Dissimilar Waveguides	7082235	10-Sep-02
3.	Strip Loaded Waveguide with Low Index Transition Layer	6834152	9-Sep-02
4.	Strip Loaded Waveguide Integrated with Electronics Components	6917727	9-Sep-02
5.	Tunable Resonant Cavity Based on the Field Effect in Semiconductors	6839488	10-Sep-02
6.	Modulator Based Tunable Resonant Cavity	6895148	10-Sep-02
7.	Tuning the Index of a Waveguide Structure	7120338	10-Sep-02
8.	Electronically Biased Strip Loaded Waveguide	6990257	9-Sep-02
9.	Method of Incorporating Germanium within a CMOS Process	6887773	10-Jun-03
10.	Integrated Dual Waveguides	7027673	19-Jun-03
11.	Waveguide Photodetector with Integrated Electronics Divisional of #22	7453132	19-Jun-03
12.	CMOS Process Silicon Waveguides	7010208	24-Jun-03
13.	Active Waveguides for Optoelectronic Devices	6999670	2-Feb-06
14.	Optical Waveguide Grating Coupler	7245803	11-Feb-04
15.	Optical Waveguide Grating Coupler with Scattering Elements of Varying Configurations	7260289	11-Feb-04
16.	Optical Waveguide Grating Coupler Incorporating Reflective Optical Elements and Anti-Reflection Elements	7184625	10-Feb-04
17.	Fiber to Chip Coupler	7162124	11-Mar-04
18.	Electronically Controllable Arrayed Waveguide Grating	7139455	17-Mar-04
19.	Polarization Splitting Grating Coupler	7006732	12-Dec-03
20.	Wafer-Level Testing of Optical and Optoelectronic Chips	7184626	7-Apr-04
21.	PN Diode Optical Modulators Fabricated in Rib Waveguides	7116853	11-Aug-04
22.	PN Diode Optical Modulators Fabricated in Strip-Loaded Waveguides	7136544	11-Aug-04
23.	Photonic Interconnect System for Integrated Circuits	7251386	14-Jan-04
24.	Photonic Input/Output Port (Continuation of #12)	7269326	7-Apr-04
25.	Doping Profiles in PN Diode Optical Modulators	7085443	11-Aug-04
26.	Distributed Amplifier Optical Modulators	7039258	13-Aug-04
27.	Silicon on Insulator Resonator Sensors and Modulators and Method of Operating the Same	7095010	4-Dec-03
28.	Use of Grating Couplers as Demux in Multi-Mode Fiber	7194166	26-Aug-05
29.	Optical Probes With Spacing Sensors For Wafer Level Testing Of Optical And Optoelectronic Chips	7183759	17-Dec-04
30.	Littrow Gratings As Alignment Structures For Wafer Level Testing Of Optical And Optoelectronic Chips	7024066	17-Dec-04
31.	Optical Alignment Loops For Wafer Level Testing Of Optical And Optoelectronic Chips	7224174	17-Dec-04
32.	Strip Loaded Waveguide with Low Index Transition Layer (Continuation of #14)	7127147	11-Nov-04
33.	Tunable Resonant Cavity Based on the Field Effect in Semiconductors (Divisional of #16)	7164821	5-Nov-04
34.	Germanium Integrated CMOS Wafer and Method for Manufacturing the Same	7262117	22-Feb-05
35.	Photonic Input/Output Port (Continuation of #42)	7031562	1-Feb-05
36.	Optoelectronic Alignment Structure for the Wafer Level Testing of Optical and Optoelectronic Chips	7298939	16-Mar-05
37.	PLC for Connecting Optical Fibers to Optical or Optoeletronic Devices	7366380	18-Apr-05

	Description	Patent/ App No.	Date Filed
38.	CMOS Process Polysilicon Strip Loaded Waveguides with a Three Layer Core	7116881	7-Jul-05
39.	CMOS Process Polysilicon Strip Loaded Waveguides with a Two Layer Core	7136563	7-Jul-05
40.	Polysilicon and Silicon Dioxide Light Scatterers for Silicon Waveguides	7095936	14-Jul-05
41.	Polysilicon Light Scatterers for Silicon Waveguides	7046894	14-Jul-05
42.	Polysilicon and Silicon Dioxide Light Scatterers for Silicon Waveguides on Five Layer Substrates	6993236	7-Jul-05
43.	Polysilicon Light Scatterers for Silicon Waveguides on Five Layer Substrates	7058273	14-Jul-05
44.	Light Scattering Structures Formed in Silicon Waveguides	7251403	7-Jul-05
45.	Light Scattering Structures Formed in Upper Layers of Strip Loaded Waveguides	7054533	15-Jul-05
46.	Light Scattering Structures Formed in Upper Layer of Strip Loaded Waveguides	7082245	15-Jul-05
47.	Light Scattering Structures Formed in Lower Layers of Strip Loaded Waveguides	7079742	15-Jul-05
48.	Light Scattering Strucutres Formed in Lower Layer of Strip Loaded Waveguides	7082246	15-Jul-05
49.	Light Scattering Structures Formed in Silicon Strip Loaded Waveguides	7054534	15-Jul-05
50.	CMOS Process Active Waveguides	7072556	29-Aug-05
51.	CMOS Process Active Waveguides on Five Layer Substrates	7218826	29-Aug-05
52.	CMOS Process Waveguide Coupler	7082247	29-Aug-05
53.	Electronically Biased Strip Loaded Waveguide (Continuation of #19)	7167606	28-Mar-05
54.	Modulator Based on Tunable Resonant Cavity	7203403	7-Apr-05
55.	Germanium Silicon Heterostructure Photodetectors	7397101	7-Jul-05
56.	Germanium Integration	7340709	7-Jul-05
57.	Flip-Chip Devices Formed on Photonic Integrated Circuit Chips (CIP of #52/P004-#23)	11/195,357	2-Aug-05
58.	Enhancing the Sensitivity of Resonant Optical Modulating and Switching Devices (Allowed-5/26/09)	11/584,754	20-Oct-06
59.	Polarization Splitting Grating Coupler (divisional of #35)	7068887	26-Oct-05
60.	Active Waveguides for Optoelectronic Devices (divisional of #26)	7046895	8-Nov-05
61.	Active Waveguides for Optoelectronic Devices (divisional of #26)	7046896	8-Nov-05
62.	Integrated Photonic-Electronic Circuits and Systems (divisional of #40)	7259031	8-Nov-05
63.	Wafer-Level Testing of Optical and Optoelectronic Chips (divisional of #36)	7262852	14-Nov-05
64.	Optical Waveguide Grating Coupler Incorporating Reflective Optical Elements and Anti-Reflection Elements (divisional of #29)	7184627	16-Nov-05
65.	Optical Waveguide Grating Coupler with Varying Scatter Cross Sections (continuation of 28)	7260293	6-Dec-05
66.	Systems and Methods for Testing Germanium Devices	7358527	3-Feb-06
67.	Distributed Amplifier Optical Modulators (cont of 54)	7450787	27-Feb-06
68.	Integrated Dual Waveguides (continuation of #21)	7231105	17-Mar-06
69.	Polarization Splitting Grating Couplers (continuation of #113)	7298945	17-Mar-06
70.	Doping Profiles in PN Diode Optical Modulators (continuation of #53)	7251408	5-Apr-06
71.	Design of CMOS Integrated Germanium Photodiodes	7613369	13-Apr-07
72.	Distributed Amplifier Optical Modulators Continuation in Part of #54	7515775	29-Sep-06
73.	Integrated Transceiver with Lightpipe Coupler (div/ cont of #123) (allowed on 3/1/10)	11/611,084	14-Dec-06
74.	Waveguide Photodetector with Integrated Electronics Divisional of #22	7616904	23-Feb-07

	Description	Patent/ App No.	Date Filed
75.	Optoelectronic Alignment Structure for the Wafer Level Testing of Optical and Optoelectronic Chips (Div of #79)	7412138	28-Feb-07
76.	Cont of #70 Optical Alignment Loops For Wafer Level Testing Of Optical And Optoelectronic Chips	7378861	26-Feb-07
77.	Cont of # 117 Wafer-Level Testing of Optical and Optoelectronic Chips (divisional of #36)	7586608	28-Mar-07
78.	Si Surface Cleaning for Semiconductor Circuits	11/871,987	13-Oct-07
79.	Method and Circuit for encoding Multi-Level Pulse Amplitude Modulated Signals Using Integrated Optoelectronic Devices	12/555,291	8-Sep-09
80.	Method and System for Split Voltage Domain Transmitter Circuits	12/208,650	11-Sep-08
81.	Method and System for a Narrowband, Non-linear Optoelectronic Receiver	12/245,867	6-Oct-08
82.	Cont of # 150 -divisional of #117 Wafer-Level Testing of Optical and Optoelectronic Chips (divisional of #36)	12/041,845	12-Feb-08
83.	Low Loss Optical Interconnect	12/362,154	29-Jan-09
84.	Method And System For Optoelectronic(s) Transceiver(s) Integrated on a CMOS Chip- Combined with #154	12/241,961	30-Sep-08
85.	Method and System for a Slope-Insensitive Mach-Zehnder Modulator	61/269,476	
86.	Method and System for an Avalanche Optical Modulator	61/269,478	
87.	Method and System for Split Voltage Domain Receiver Circuits	12/208,668	11-Sep-08
88.	Method and Systen fir a Light Source Assembly Supporting Direct Coupling To An Integrated Circuit	61/079,358	9-Jul-09
89.	Optical non-contact wafer level test apparatus for CMOS photonics chips	61/275,756	
90.	METHOD AND SYSTEM FOR MONOLITHIC INTEGRATION OF PHOTONICS AND ELECTRONICS IN CMOS PROCESSES	12/554,449	4-Sep-09
91.	Methods of coupling optical signals into silicon optoelectronic chips	61/198,660	6-Nov-09
92.	Integrated control system for laser and Mach-Zehnder interferometer	61/198,079	3-Nov-09
93.	Distributed Amplifier Optical Modulators (Divisional of #134 - Continuation in Part of #54 for claims 31-41)	12/352,415	12-Jan-09
94.	Single Laser Bidirectional Link	61/207,958	18-Feb-10
95.	Integrated Transceiver with Lighpipe Coupler (divisional #138)	12/483,699	12-Jun-09
96.	Optoelectronic Receivers for Uncoded Data	61/270,665	10-Jul-09
97.	Method and circuit for encoding multi-level pulse amplitude modulated signals using integrated optoelectronic devices (Same as #153- convert 153 for earlier priority date per IP Mtg 8/12/09)	61/270,304	10-Jul-09
98.	Process to fabricate a near infrared waveguide heterojunction phototransistor integrated in a CMOS SOI wafer	61/274,580	19-Aug-09
99.	Near Infrared waveguide heterojunction phototransistor integrated in a CMOS SOI wafer	61/274,588	19-Aug-09
100.	High sensitivity optical receiver using a near infrared waveguide heterojunction phototransistor integrated in a CMOS SOI wafer	61/274,605	19-Aug-09
101.	Method for Circuit Bandwidth Enhancement Using Hybrid Inductors	61/276,580	
102.	Intrusion Detection and Protection Method for Optical Interconnect	61/280,375	2-Nov-09
103.	Method and circuits for implementing high-speed elevtrical interfaces between semi conductor dies in optical communication systems		
104.	Waveguide Mode Filter		
105.	Method and system for coupling optical signals into silicon optoelectronic chips	12/614,024	6-Nov-09
106.	Method and system for a feedback transimpedance amplifier with sub-40khz low-frequency cutoff	13/175,545	1-Jul-11

	Description	Patent/ App No.	Date Filed
107.	Method and system for a light source assembly supporting direct coupling to an integrated circuit	8,168,939	1-May-12
108.	Integrated transceiver with lightpipe coupler	8,165,431	24-Apr-12
109.	Integrated transceiver with lightpipe coupler	8,121,447	21-Feb-12
110.	Integrated control system for laser and mach-zehnder interferometer	7,916,377	29-Mar-11
111.	Method and system for bandwidth enhancement using hybrid inductors	8,289,067	16-Oct-12
112.	Method and system for optoelectronic receivers for uncoded data	8,358,940	22-Jan-13
113.	Novel low-cost transceiver approach	8,577,191	5-Nov-13
114.	Method and system for optoelectronic receivers utilizing waveguide heterojunction phototransistors integrated in a cmos soi wafer	8,592,745	26-Nov-13
115.	Method and system for integrated power combiners	8,625,935	7-Jan-14
116.	Method and system for waveguide mode filters	8,649,639	11-Feb-14
117.	Method and system for multi-mode integrated receivers	13/156,990	9-Jun-11
118.	Method and system for hybrid integration of optical communication systems	13/568,406	7-Aug-12
119.	Method and system for encoding multi-level pulse amplitude modulated signals using integrated optoelectronic devices	13/568,616	7-Aug-12
120.	Method and system for optoelectronic receivers for uncoded data	8,626,002	7-Jan-14
121.	Method and system for bandwidth enhancement using hybrid inductors	8,604,866	10-Dec-13
122.	Method and system for a light source assembly supporting direct coupling to an integrated circuit	8,440,989	14-May-13
123.	Method and system for coupling optical signals into silicon optoelectronic chips	8,433,162	30-Apr-13

EXHIBIT C

Trademarks

Description	Serial/Registration No.	File Date
DESIGN ONLY	78583030	3/8/05
LUXTERA	78583028	3/8/05
LUXTERA	78582939	3/8/05
VideoLynx	77378412	1/23/08
OptoPHY	77516061	7/7/08
LUXTERA	86150245	12/20/13
LUXTERA	85884907	3/25/13