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[ ]Yes [X]No

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Execution Date: March 25, 2008

2. Name and address of receiving party(ies):

Name: Numonyx B.V.

Street Address: A-1 Business Centre,
Z.A. Vers la Piece Rte.

City: De l'Etraz, Rolle, 1180
Country: Switzerland

Additional name(s) & address(es) attached? [ ]Yes [X]No

4. Application number(s) or patent number(s):

If this document is being filed together with a new application, the execution date of the application is:

A. Patent Application No.(s)	B. Patent No.(s)
Serial No. 10/424,899	6,791,414

Additional numbers attached? [ ]Yes [X]No

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: Mark V. Muller

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Schwegman, Lundberg & Woessner, P.A.
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Minneapolis, MN 55402--0938

6. Total number of applications and patents involved: 1

7. Total fee (37 CFR 3.41):$ 40.00

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Mark V. Muller/Reg. No. 37,509 /Mark V. Muller/ FEBRUARY 25, 2014
Name of Person Signing Signature Date

Total number of pages including cover sheet: 54

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ASSIGNMENT

For good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, Intel Corporation, a Delaware Corporation, having an address of 2200 Mission College Boulevard, Santa Clara, CA 95052, U.S.A. ("Assignor"), hereby sells, assigns, transfers and conveys to Numonyx B.V., Acting Through Its Swiss Branch, having an address of A-1 Business Centre, Z.A. Vers la Piece, Rte de l'Etraz, 1180 Rolle, Switzerland ("Assignee"), its successors, assigns and legal representatives, Assignor's entire right, title and interest in and to the U.S. Patents and U.S. Patent Applications listed on Schedule A, and any and all causes of action for past, present, and future infringement of any of said Letters Patents, subject to prior encumbrances,

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IN TESTIMONY WHEREOF, Assignor and Assignee having caused this Assignment to be duly executed in their respective names and behalves by affixing their hands thereto by their respective designated officer, director, or agent, whose names and titles appear below.

Executed at SANTA CLARA, CA, this 25th day of MARCH, 2008

Signature: Cary Klafter

Name: Cary I. Klafter

(Intel Corporation)

VICE PRESIDENT, LEGAL & CORPORATE SECRETARY

LEGAL OK

Signature: _____

Name: _____

(Numonyx B.V.)

Not for recording

CALIFORNIA ALL-PURPOSE ACKNOWLEDGMENT

State of California
County of SANTA CLARA }

On MARCH 25, 2008 (Date) before me, ANN CUNNINGHAM NOTARY PUBLIC (Here Insert Name and Title of the Officer),

personally appeared CARY I. KLAFTER (Name(s) of Signer(s))

who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) (is)/~~are~~ subscribed to the within instrument and acknowledged to me that (he)/~~she/they~~ executed the same in (his)/~~her/their~~ authorized capacity(ies), and that by (his)/~~her/their~~ signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

ANN CUNNINGHAM
Commission # 1759138
Notary Public - California
Santa Clara County
MyComm. Expires Jul 28, 2011

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

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Schedule A

Country	Patent Number	Publication Number	Serial Number	Title
US	5,202,291		07/883,067	HIGH CF4-FLOW REACTIVE ION ETCH FOR ALUMINUM PATTERNING
US	5,216,843		07/950,812	POLISHING PAD CONDITIONING APPARATUS FOR WAFER PLANARIZATION PROCESS
US	5,218,636		07/665,970	DIAL PULSE DIGIT DETECTOR
US	5,219,791		07/712,119	TEOS INTERMETAL DIELECTRIC PRECLEAN FOR VIA FORMATION
US	5,222,244		07/630,497	METHOD OF MODIFYING A MICROINSTRUCTION WITH OPERANDS SPECIFIED BY AN INSTRUCTION HELD IN AN ALIAS REGISTER
US	5,232,871		07/869,227	METHOD FOR FORMING A TITANIUM NITRIDE BARRIER LAYER
US	5,237,202		07/803,724	LEAD FRAME AND SEMICONDUCTOR DEVICE USING SAME
US	5,237,535		07/773,228	METHOD OF REPAIRING OVERERASED CELLS IN A FLASH MEMORY
US	5,242,864		07/893,765	POLYMIDE PROCESS FOR PROTECTING INTEGRATED PRODUCTS
US	5,244,843		07/809,971	NOVEL PROCESS FOR FORMING A THIN OXIDE LAYER
US	5,255,230		07/816,635	METHOD AND APPARATUS FOR TESTING THE CONTINUITY OF STATIC RANDOM ACCESS MEMORY CELLS
US	5,255,378		07/981,943	METHOD OF TRANSFERRING BURST DATA IN A MICROPROCESSOR
US	5,256,994		07/948,215	PROGRAMMABLE SECONDARY CLOCK GENERATOR
US	5,265,059		07/698,547	CIRCUITRY AND METHOD FOR DISCHARGING A DRAIN OF A CELL OF A NON-VOLATILE SEMICONDUCTOR MEMORY
US	5,267,213		07/861,093	BIAS CIRCUITRY FOR CONTENT ADDRESSABLE MEMORY CELLS OF A FLOATING GATE NONVOLATILE MEMORY
US	5,270,264		07/917,465	PROCESS FOR FILLING SUBMICRON SPACES WITH DIELECTRIC
US	5,274,277		07/938,934	HIGH SPEED OR CIRCUIT CONFIGURATION
US	5,274,281		07/875,661	STATIC PLA WITH STATE MACHINE CONTROLLED BY MODEL OF BOTH MINTERM AND AN OUTPUT LINE
US	5,274,678		07/815,819	CLOCK SWITCHING APPARATUS AND METHOD FOR COMPUTER SYSTEMS

Schedule A

US	5,276,690	07/830,209	APPARATUS UTILIZING DUAL COMPARE LOGIC FOR SELF CHECKING OF FUNCTIONAL REDUNDANCY CHECK (FRC) LOGIC
US	5,276,704	07/971,689	SAWC PHASE DETECTION METHOD AND APPARATUS
US	5,276,833	07/544,821	DATA CACHE MANAGEMENT SYSTEM WITH TEST MODE USING INDEX REGISTERS AND CAS DISABLE AND POSTED WRITE DISABLE
US	5,279,865	07/722,861	HIGH THROUGHPUT INTERLEVEL DIELECTRIC GAP FILLING PROCESS
US	5,280,590	07/902,317	LOGIC SUPPORT CHIP FOR AT-TYPE COMPUTER WITH IMPROVED BUS ARCHITECTURE
US	5,286,678	07/951,945	SINGLE STEP SALICIDATION PROCESS
US	5,289,026	07/744,969	ASYMMETRIC FLOATING GATE OVERLAP FOR IMPROVED DEVICE CHARACTERISTICS IN BURIED BIT-LINE DEVICES
US	5,289,412	07/901,395	HIGH-SPEED BIAS-STABILIZED CURRENT MIRROR REFERENCING CIRCUIT FOR NON-VOLATILE MEMORIES
US	5,290,735	08/011,944	THIN, HIGH LEAD COUNT PACKAGE
US	5,291,060	07/984,841	LEAD FRAME AND SEMICONDUCTOR DEVICE USING SAME
US	5,291,071	07/881,843	HIGH SPEED, LOW POWER OUTPUT CIRCUIT WITH TEMPERATURE COMPENSATED NOISE CONTROL
US	5,296,094	07/897,768	PROCESS FOR ETCHING SILICON DIOXIDE LAYER WITHOUT MICRO MASKING EFFECT
US	5,298,807	07/813,148	BUFFER CIRCUITRY FOR TRANSFERRING SIGNALS FROM TTL CIRCUITRY TO DUAL RANGE CMOS CIRCUITRY
US	5,301,097	07/896,195	MULTI-STAGED CHARGE-PUMP WITH STAGGERED CLOCK PHASES FOR PROVIDING HIGH CURRENT CAPABILITY
US	5,309,012	07/971,074	PROTECTED ERASE VOLTAGE DISCHARGE TRANSISTOR IN A NONVOLATILE SEMICONDUCTOR MEMORY
US	5,313,605	07/630,534	HIGH BANDWIDTH OUTPUT HIERARCHICAL MEMORY STORE INCLUDING A CACHE, FETCH BUFFER AND ROM
US	5,317,535	07/901,110	GATE/SOURCE DISTURB PROTECTION FOR SIXTEEN-BIT FLASH EEPROM MEMORY ARRAYS
US	5,317,750	07/984,280	MICROCONTROLLER PERIPHERAL EXPANSION BUS FOR ACCESS TO INTERNAL SPECIAL FUNCTION REGISTERS

Schedule A

US	5,321,583	07/984,335	ELECTRICALLY CONDUCTIVE INTERPOSER AND ARRAY PACKAGE CONCEPT FOR INTERCONNECTING TO A CIRCUIT BOARD
US	5,339,442	07/954,743	IMPROVED SYSTEM OF RESOLVING CONFLICTING DATA PROCESSING MEMORY ACCESS REQUESTS
US	5,340,370	08/146,923	NOVEL SLURRIES FOR CHEMICAL MECHANICAL POLISHING
US	5,341,330	08/145,732	METHOD FOR WRITING TO A FLASH MEMORY ARRAY DURING ERASE SUSPEND INTERVALS
US	5,345,577	07/981,329	DRAM REFRESH CONTROLLER WITH IMPROVED BUS ARBITRATION SCHEME
US	5,350,484	07/941,412	A METHOD FOR THE ANISOTROPIC ETCHING OF METAL FILMS IN THE FABRICATION OF INTERCONNECTS
US	5,358,891	08/084,795	TRENCH ISOLATION WITH PLANAR TOPOGRAPHY AND METHOD OF FABRICATION
US	5,365,128	08/036,219	HIGH-RESOLUTION SYNCHRONOUS DELAY LINE
US	5,367,679	07/998,555	ROUND ROBIN SCHEDULER USING A SCHEDULER CARRY OPERATION FOR ARBITRATION
US	5,373,508	07/923,853	DETECTING VALID DATA FROM A TWISTED PAIR MEDIUM
US	5,379,443	08/133,771	MICROPROCESSOR PROVIDING ENCODED INFORMATION ON BYTE ENABLE LINES INDICATING WHETHER READING CODE OR DATA, LOCATION OF CODE DATA ON DATA LINES, AND BIT WIDTH OF CODE DATA
US	5,398,075	08/154,955	ANALOG CHROMA KEYING ON COLOR DATA
US	5,404,400	08/024,402	OUTCALLING APPARATUS
US	5,410,263	08/023,673	DELAY LINE LOOP FOR ON-CHIP CLOCK SYNTHESIS WITH ZERO SKEW AND 50% DUTY CYCLE
US	5,412,793	08/277,369	METHOD FOR TESTING ERASE CHARACTERISTICS OF A FLASH MEMORY ARRAY
US	5,416,782	07/969,465	METHOD AND APPARATUS FOR IMPROVING DATA FAILURE RATE TESTING FOR MEMORY ARRAYS
US	5,421,021	08/047,696	A CIRCUIT INCLUDING A LATCHING UNIT FOR HOLDING INSTRUCTIONS DURING EXECUTION FOR RE-EXECUTION FOLLOWING EXCEPTION HANDLING
US	5,422,586	08/119,423	METHOD AND APPARATUS FOR A TWO PHASE BOOTSTRAP CHARGE PUMP
US	5,426,462	08/319,779	APPARATUS FOR ENCODING SIGNALS USING A CONFIGURABLE TRANSFORM CIRCUIT

Schedule A

US	5,428,565	08/212,350	SINGLE STAGE SENSING APPARATUS FOR A CONTENT ADDRESSABLE MEMORY
US	5,432,469	08/248,419	METHOD AND APPARATUS FOR A TWO PHASE BOOTSTRAP CHARGE PUMP
US	5,434,534	08/158,418	CMOS VOLTAGE REFERENCE CIRCUIT
US	5,434,892	08/307,502	A THROTTLING CIRCUIT FOR A DATA TRANSFER SYSTEM
US	5,436,585	08/242,790	BINMOS DRIVER CIRCUIT WITH INTEGRATED VOLTAGE SUPPLY CONVERSION
US	5,437,021	07/897,897	PROCESSOR SPEED/TYPE INDEPENDENT BIOS TIMER
US	5,442,586	08/119,425	METHOD AND APPARATUS FOR CONTROLLING THE OUTPUT CURRENT PROVIDED BY A CHARGE PUMP CIRCUIT
US	5,442,694	08/226,678	RING TONE DETECTION FOR A TELEPHONE SYSTEM
US	5,444,602	08/201,895	ELECTRONIC PACKAGE THAT HAS A DIE COUPLED TO A LEAD FRAME BY A DIELECTRIC TAPE AND A HEAT SINK THAT PROVIDES BOTH AN ELECTRICAL AND A THERMAL PATH BETWEEN THE DIE AND THE LEAD FRAME
US	5,446,839	08/067,858	METHOD FOR CONTROLLING DATAFLOW BETWEEN A PLURALITY OF CIRCULAR BUFFERS
US	5,446,867	07/890,937	MICROPROCESSOR PLL CLOCK CIRCUIT WITH SELECTABLE DELAYED FEEDBACK
US	5,450,544	08/357,544	METHOD AND APPARATUS FOR DATA BUFFERING AND QUEUE MANAGEMENT OF DIGITAL MOTION VIDEO SIGNALS
US	5,453,708	08/368,335	CLOCKING SCHEME FOR LATCHING OF A DOMINO OUTPUT
US	5,454,089	08/141,685	BRANCH LOOK AHEAD ADDER FOR USE IN AN INSTRUCTION PIPELINE SEQUENCER
US	5,455,794	08/403,633	METHOD AND APPARATUS FOR CONTROLLING THE OUTPUT CURRENT PROVIDED BY A CHARGE PUMP CIRCUIT
US	5,455,800	08/329,773	APPARATUS FOR IMPROVING THE PROGRAM AND ERASE PERFORMANCE OF A FLASH EEPROM MEMORY ARRAY
US	5,455,957	08/394,560	METHOD AND APPARATUS FOR CONDUCTING BUS TRANSACTIONS BETWEEN TWO CLOCK INDEPENDENT BUS AGENTS OF A COMPUTER SYSTEM

Schedule A

US	5,457,648	08/208,800	RANDOM ACCESS MEMORY WITH DIGITAL SIGNALS RUNNING OVER THE SMALL SIGNAL REGION OF THE ARRAY
US	5,459,355	08/285,495	MULTIPLE LAYER PROGRAMMABLE LAYOUT FOR VERSION IDENTIFICATION
US	5,463,658	08/216,668	LOW IMPACT COLLISION DETECTION METHOD
US	5,463,748	08/085,637	INSTRUCTION BUFFER FOR ALIGNING INSTRUCTION SETS USING BOUNDARY DETECTION
US	5,463,757	08/185,449	COMMAND INTERFACE BETWEEN USER COMMANDS AND A MEMORY DEVICE
US	5,467,460	08/234,587	METHOD AND APPARATUS FOR MINIMIZING THE DATA TRANSFER FROM A MEMORY DURING A CACHE MISS
US	5,469,093	08/333,264	CURRENT MIRROR DRIVE CIRCUIT WITH HIGH BREAKDOWN VOLTAGE
US	5,469,164	08/129,899	CIRCUIT AND METHOD FOR DIGITAL TO ANALOG SIGNAL CONVERSION
US	5,471,604	07/969,780	METHOD FOR LOCATING SECTOR DATA IN A MEMORY DISK BY EXAMINING A PLURALITY OF HEADERS NEAR AN INITIAL POINTER
US	5,471,637	08/429,658	METHOD AND APPARATUS FOR CONDUCTING BUS TRANSACTIONS BETWEEN TWO CLOCK INDEPENDENT BUS AGENTS OF A COMPUTER SYSTEM USING A TRANSACTION BY TRANSACTION DETERMINISTIC REQUEST/RESPONSE PROTOCOL AND BURST TRANSFER
US	5,473,190	08/167,531	TAB TAPE
US	5,473,753	07/969,749	METHOD OF MANAGING DEFECTS IN FLASH DISK MEMORIES
US	5,475,633	08/252,320	CACHE MEMORY UTILIZING PSEUDO STATIC FOUR TRANSISTOR MEMORY CELL
US	5,475,693	08/364,546	ERROR MANAGEMENT FOR FLASH PROCESSES FOR FLASH EEPROM MEMORY ARRAYS
US	5,477,418	08/275,599	IMPROVED I/O CONNECTOR FOR ADD IN PRINTED CIRCUIT CARDS FOR COMPUTER SYSTEMS
US	5,479,633	07/969,763	A METHOD OF CONTROLLING CLEAN-UP OF A SOLID STATE MEMORY DISK STORING FLOATING SECTOR DATA
US	5,485,422	08/252,684	DRAIN BIAS MULTIPLEXING FOR MULTIPLE BIT FLASH CELL
US	5,488,570	08/268,270	ENCODING AND DECODING VIDEO SIGNALS USING ADAPTIVE FILTER SWITCHING CRITERIA

Schedule A

US	5,488,639	08/171,554	PARALLEL MULTISTAGE SYNCHRONIZATION METHOD AND APPARATUS
US	5,490,102	08/260,044	LOW CAPACITANCE CONTENT ADDRESSABLE MEMORY CELL
US	5,490,109	08/267,472	METHOD AND APPARATUS FOR PREVENTING OVER ERASURE OF FLASH EEPROM MEMORY DEVICES
US	5,490,264	08/130,023	GENERALLY DIAGONAL MAPPING OF ADDRESS SPACE FOR ROW/COLUMN ORGANIZER MEMORIES
US	5,495,453	08/326,689	A LOW POWER VOLTAGE DETECTOR CIRCUIT INCLUDING A FLASH MEMORY CELL
US	5,497,354	08/253,902	BIT MAP ADDRESSING SCHEMES FOR FLASH MEMORY
US	5,497,355	08/253,842	SYNCHRONOUS ADDRESS LATCHING FOR MEMORY ARRAYS
US	5,503,959	08/046,477	LITHOGRAPHIC TECHNIQUE FOR PATTERNING A SEMICONDUCTOR DEVICE
US	5,504,875	08/032,686	NONVOLATILE MEMORY WITH A PROGRAMMABLE OUTPUT OF SELECTABLE WIDTH AND A METHOD FOR CONTROLLING THE NONVOLATILE MEMORY TO SWITCH BETWEENDIFFERENT OUTPUT WIDTHS
US	5,506,803	08/361,872	APPARATUS AND METHOD FOR MINIMIZING VERIFY TIME IN A SEMICONDUCTOR MEMORY BY CONSTANTLY CHARGING N-WELL CAPACITANCE
US	5,506,885	08/289,315	METHOD OF ADAPTING PROCESSING PARAMETERS IN A CALL PROCESSING SYSTEM
US	5,510,740	08/272,879	METHOD FOR SYNCHRONIZING CLOCKS UPON RESET
US	5,511,195	08/152,348	DRIVER, COMPUTER IMPLEMENTED PROCESS AND COMPUTER SYSTEM FOR PROCESSING DATA USING LOADABLE MICROCODE RUNNING ON A PROGRAMMABLE PROCESSOR
US	5,513,136	08/358,978	NONVOLATILE MEMORY WITH BLOCKS AND CIRCUITRY FOR SELECTIVELY PROTECTING THE BLOCKS FROM MEMORY OPERATIONS
US	5,513,331	08/412,607	METHOD AND APPARATUS FOR AUTOMATICALLY CONFIGURING SYSTEM MEMORY ADDRESS SPACE OF A COMPUTER SYSTEM HAVING A MEMORY SUBSYSTEM WITH INDETERMINISTIC NUMBER OF MEMORY UNITS OF INDETERMINISTIC SIZES DURING SYSTEM RESET
US	5,517,138	08/316,546	DUAL ROW SELECTION USING MULTIPLEXED TRI-LEVEL DECODER

Schedule A

US	5,517,452	08/403,407	METHOD AND APPARATUS FOR COMPENSATING FOR SUBTHRESHOLD CURRENT IN A STATIC RAM
US	5,524,231	08/086,043	NONVOLATILE MEMORY CARD WITH AN ADDRESS TABLE AND AN ADDRESS TRANSLATION LOGIC FOR MAPPING OUT DEFECTIVE BLOCKS WITHIN THE MEMORY CARD
US	5,524,266	08/246,779	SYSTEM HAVING MULTIPLE PHASE BOOSTED CHARGE PUMP WITH A PLURALITY OF STAGES
US	5,525,913	08/325,879	POWER VALIDATION TOOL FOR MICROPROCESSOR SYSTEMS
US	5,526,311	08/175,599	METHOD AND CIRCUITRY FOR ENABLING AND PERMANENTLY DISABLING TEST MODE ACCESS IN A FLASH MEMORY DEVICE
US	5,532,940	08/234,978	PROCESS, APPARATUS AND SYSTEM FOR SELECTING QUANTIZATION LEVELS FOR ENCODING VIDEO SIGNALS
US	5,535,369	08/485,661	METHOD FOR ALLOCATING MEMORY IN A SOLID STATE MEMORY DISK
US	5,535,397	08/085,409	METHOD AND APPARATUS FOR PROVIDING A CONTEXT SWITCH IN RESPONSE TO AN INTERRUPT IN A COMPUTER PROCESS
US	5,537,069	08/413,951	APPARATUS AND METHOD FOR SELECTING A TAP RANGE IN A DIGITAL DELAY LINE
US	5,538,141	08/312,831	TEST FLOW ASSURANCE USING MEMORY IMPRINTING
US	5,544,071	08/174,729	CRITICAL PATH PREDICTION FOR DESIGN OF CIRCUITS
US	5,546,447	08/268,265	DISPLAYING CALLER IDENTIFICATION INFORMATION IN A COMPUTER SYSTEM
US	5,546,539	08/542,039	METHOD AND APPARATUS FOR UPDATING FILES OF A PLURALITY OF STORAGE DEVICES THROUGH PROPAGATION OF FILES OVER A NETWORK
US	5,546,568	08/176,944	CPU CLOCK CONTROL UNIT
US	5,552,832	08/329,524	RUN LENGTH ENCODING SEQUENCE FOR VIDEO SIGNALS
US	5,553,030	08/491,792	METHOD AND APPARATUS FOR CONTROLLING THE OUTPUT VOLTAGE PROVIDED BY A CHARGE PUMP CIRCUIT
US	5,556,811	08/468,972	UTILIZING HIGH PERFORMANCE, LOW ESR AND LOW INDUCTANCE CAPACITORS TO IMPROVE TRANSIENT RESPONSE OF ON-BOARD VOLTAGE REGULATED PACKAGES
US	5,557,075	08/266,150	PARALLEL FLEXIBLE TRANSMISSION CABLE

Schedule A

US	5,557,330	08/332,583	ENCODING VIDEO SIGNALS USING SELECTIVE PRE FILTERING
US	5,557,749	07/961,475	SYSTEM FOR AUTOMATICALLY COMPRESSING AND DECOMPRESSING DATA FOR SENDER AND RECEIVERPROCESSES UPON DETERMINATIONOF A COMMON COMPRESSION/DECOMPRESSION METHOD UNDERSTOOD BY BOTH SENDER AND RECEIVER PROCESSES
US	5,559,722	08/234,976	PROCESS, APPARATUS AND SYSTEM FOR TRANSFORMING SIGNALS USING PSEUDO SIMD PROCESSING
US	5,565,759	08/356,905	SMART BATTERY PROVIDING BATTERY LIFE AND RECHARGE TIME PREDICTION
US	5,568,569	08/258,613	METHOD AND APPARATUS FOR ANALYZING DIGITAL VIDEO IMAGES BY MERGING DISPLACEMENT VECTORS
US	5,570,050	08/590,726	ZERO STANDBY CURRENT POWER UP RESET CIRCUIT
US	5,572,198	08/279,954	METHOD AND APPARATUS FOR ROUTING IN REDUCED SWITCH MATRICES TO PROVIDE ONE HUNDRED PERCENT COVERAGE
US	5,572,465	08/451,037	POWER SUPPLY CONFIGURED SENSING SCHEME FOR FLASH EEPROM
US	5,576,636	08/515,248	LOW POWER PROGRAMMABLE LOGIC ARRAYS
US	5,579,530	08/389,078	METHOD AND APPARATUS FOR DYNAMICALLY ALLOCATING ACCESS TIME TO A RESOURCE SHARED BETWEEN A PERIPHERAL BUS AND A HOST BUS BY DYNAMICALLY CONTROLLING THE SIZE OF BURST DATA TRANSFERS ON THE PERIPHERAL BUS
US	5,581,594	08/599,032	METHOD AND APPARATUS FOR INITIATING COMMUNICATION VIA PAGING A MOBILE COMPUTING DEVICE
US	5,589,829	08/329,340	DECODING VARIABLE LENGTH ENCODED SIGNALS
US	5,590,289	08/384,472	METHOD AND APPARATUS FOR INITIALIZING A COMPUTER SYSTEM HAVING CENTRAL AND DISTRIBUTED ADDRESS DECODE MEMORY BUS RESOURCES
US	5,592,425	08/576,705	METHOD AND APPARATUS FOR TESTING A MEMORY WHERE DATA IS PASSED THROUGH THE MEMORY FOR COMPARISON WITH DATA READ FROM THE MEMORY
US	5,594,360	08/607,521	LOW CURRENT REDUCED AREA PROGRAMMING VOLTAGE DETECTOR FOR FLASH MEMORY

Schedule A

US	5,595,526	08/347,813	METHOD AND APPARATUS FOR ENDPOINT DETECTION IN A CHEMICAL/MECHANICAL PROCESS FOR POLISHING A SUBSTRATE
US	5,596,734	08/575,178	METHOD AND APPARATUS FOR PROGRAMMING EMBEDDED MEMORIES OF A VARIETY OF INTEGRATED CIRCUITS USING THE IEEE TEST ACCESS PORT
US	5,600,375	08/302,595	RENDERING AN INTER VERSES INTRA VIDEO ENCODING DECISION BASED UPON A VERTICAL GRADIENT MEASURE OF TARGET VIDEO FRAMES
US	5,602,502	08/536,853	CIRCUIT FOR DETECTING WHEN A SUPPLY OUTPUT VOLTAGE EXCEEDS A PREDETERMINED LEVEL
US	5,602,719	08/558,032	NO HANDLE ZIP SOCKET
US	5,602,902	08/410,212	FOUR WIRE MODEM SIGNAL SWITCHING FOR VOICE AND DATA APPLICATIONS
US	5,603,036	08/019,617	POWER MANAGEMENT SYSTEM FOR COMPONENTS USED IN BATTERY POWERED APPLICATIONS
US	5,603,412	08/595,796	APPARATUS AND SEMICONDUCTOR COMPONENT FOR ASSURING TEST FLOW COMPLIANCE
US	5,608,741	08/156,427	FAST PARITY GENERATOR USING COMPLEMENT PASS-TRANSISTOR LOGIC
US	5,611,054	08/567,405	METHOD AND APPARATUS FOR DECODING AND RECODING OF ADDRESSES
US	5,612,916	08/707,925	MEMORY BYPASS MODE
US	5,612,991	08/414,914	USE OF RSSI INDICATION FOR IMPROVED DATA TRANSMISSION OVER AMPS NETWORK
US	5,621,245	08/741,526	APPARATUS FOR OPTIMIZING OPERATING PARAMETERS OF AN INTEGRATED CIRCUIT PACKAGE HAVING A VOLTAGE REGULATOR MOUNTED THEREON
US	5,621,798	08/423,306	METHOD AND APPARATUS FOR COOPERATIVE MESSAGING
US	5,623,620	08/085,542	SPECIAL TEST MODES SHARED RESOURCE IN A MEMORY DEVICE
US	5,625,303	08/534,485	MULTIPLEXER HAVING A PLURALITY OF INTERNAL DATA PATHS THAT OPERATE AT DIFFERENT SPEEDS
US	5,627,788	08/437,090	MEMORY UNIT WITH BIT LINE DISCHARGER
US	5,633,102	08/396,926	LITHOGRAPHY USING A NEW PHASE-SHIFTING RETICLE

Schedule A

US	5,636,362	08/314,418	PROGRAMMABLE HIGH WATERMARK IN STACK FRAME CACHE USING SECOND REGION AS A STORAGE IF FIRST REGION IS FULL AND AN EVENT HAVING A PREDETERMINED MINIMUM PRIORITY
US	5,637,018	08/333,139	HI-JACK HINGED CONNECTION ADAPTER FOR INPUT/OUTPUT CARDS
US	5,638,436	08/524,111	VOICE DETECTION
US	5,640,083	08/458,805	METHOD AND APPARATUS FOR IMPROVING POWER UP TIME OF FLASH EEPROM MEMORY ARRAYS
US	5,640,519	08/528,914	METHOD AND APPARATUS TO IMPROVE LATENCY EXPERIENCED BY AN AGENT UNDER A ROUND ROBIN ARBITRATION SCHEME
US	5,642,263	08/689,698	CIRCUIT BOARD RETENTION SYSTEM
US	5,643,000	08/691,859	METHOD AND APPARATUS FOR PROVIDING PROCESSOR FIELD UPGRADABILITY TO A MOTHERBOARD
US	5,666,556	08/710,572	A METHOD AND APPARATUS FOR REDIRECTING REGISTER ACCESS REQUESTS WHEREIN THE REGISTER SET IS SEPARATE FROM A CENTRAL PROCESSOR UNIT
US	5,668,949	08/545,374	SYSTEM UTILIZING MULTIPLE ADDRESS DECODE RESOURCES AND DECODER RECEIVEING ADDRESS DETERMINES ADDRESS CORRESPONDING TO RESOURCES BASED ON SELECT AND READY SIGNALS BY THAT PARTICULAR RESOURCE
US	5,671,179	08/764,666	LOW POWER PULSE GENERATOR FOR SMART VOLTAGE FLASH EEPROM
US	5,687,360	08/431,016	BRANCH PREDICTOR USING MULTIPLE PREDICTION HEURISTICS AND A HEURISTIC IDENTIFIER IN THE BRANCH INSTRUCTION
US	5,691,883	08/578,984	MULTIPLE INTAKE DUCT MICROPROCESSOR COOLING SYSTEM
US	5,694,149	08/253,737	VERTICALLY SCALING IMAGE SIGNALS USING DIGITAL DIFFERENTIAL ACCUMULATOR PROCESSING
US	5,706,218	08/648,553	RANDOM NUMBER GENERATOR
US	5,710,902	08/524,065	INSTRUCTION DEPENDENCY CHAIN INDENTIFIER
US	5,712,578	08/579,095	PLA ARCHITECTURE HAVING IMPROVED CLOCK SIGNAL TO OUTPUT TIMING USING A TYPE-I DOMINO AND PLANE
US	5,712,857	08/536,112	METHODS AND APPARATUS FOR CORRELATING STUCK-AT FAULT TEST COVERAGE AND CURRENT LEAKAGE FAULT TEST COVERAGE

Schedule A

US	5,721,882	08/807,212	METHOD AND APPARATUS FOR INTERFACING MEMORY DEVICES OPERATING AT DIFFERENT SPEEDS TO A COMPUTER SYSTEM BUS
US	5,721,927	08/689,357	METHOD FOR VERIFYING CONTIQUITY OF A BINARY TRANSLATED BLOCK OF INSTRUCTIONS BY ATTACHING A COMPARE AND/OR BRANCH INSTRUCTION TO PREDECESSOR BLOCK OF INSTRUCTIONS
US	5,726,865	08/665,405	CIRCUIT BOARD RETENTION SYSTEM
US	5,735,701	08/570,239	LOCKING POWER CABLE INTERFACE GUARD
US	5,740,385	08/358,359	LOW LOAD HOST/PCI BUS BRIDGE
US	5,745,786	08/188,555	METHOD AND APPARATUS FOR ASSIGNING MEMORY SPACE ADDRESSES TO MEMORY ON COMPUTER INTERFACE BOARDS
US	5,752,013	08/085,508	METHOD AND APPARATUS FOR PROVIDING PRECISE FAULT TRACING IN A SUPERSCALAR MICROPROCESSOR
US	5,754,162	08/253,374	HORIZONTALLY SCALING IMAGE SIGNALS USING SELECTED WEIGHT FACTORS
US	5,757,217	08/672,412	SLOW SPEED DRIVER WITH CONTROLLED SLEW RATE
US	5,764,548	08/537,260	FAST FLOATING-POINT TO INTEGER CONVERSION
US	5,764,759	08/319,159	CALL PROCESSING USING PREVIOUSLY OBTAINED LINE CHARACTERISTICS
US	5,768,289	08/862,006	DYNAMICALLY CONTROLLING THE NUMBER OF BOUNDARY-SCAN CELLS IN A BOUNDARY-SCAN PATH
US	5,768,351	08/831,578	METHOD AND APPARATUS FOR CONNECTING A TELEPHONE TO A VOICE CAPABLE MODEM
US	5,771,183	08/672,678	APPARATUS AND METHOD FOR COMPUTATION OF STICKY BIT IN A MULTI-STAGE SHIFTER USED FOR FLOATING POINT ARITHMETIC
US	5,773,895	08/627,058	ANCHOR PROVISIONS TO PREVENT MOLD DELAMINATION IN AN OVERMOLDED PLASTIC ARRAY PACKAGE
US	5,775,951	08/724,625	HI-JACK HINGED CONNECTION ADAPTER FOR INPUT/OUTPUT CARDS
US	5,777,624	08/582,200	METHOD AND APPARATUS FOR ELIMINATING VISUAL ARTIFACTS CAUSED BY DIFFUSING ERRORS IN A DECIMATED VIDEO SIGNAL
US	5,778,097	08/610,582	TABLE-DRIVEN BI-DIRECTIONAL MOTION ESTIMATION USING SCRATCH AREA AND OFFSET VALVES

Schedule A

US	5,784,046	08/254,364	HORIZONTALLY SCALING IMAGE SIGNALS USING DIGITAL DIFFERENTIAL ACCUMULATOR PROCESSING
US	5,784,263	08/584,330	CONNECTOR WITH ATTACHABLE DAUGHTER CARD RETENTION SYSTEM
US	5,787,159	08/607,796	USE OF CALLER ID INFORMATION
US	5,787,454	08/578,964	RECORDER BUFFER WITH INTERLEAVING MECHANISM FOR ACCESSING A MULTI-PORTED CIRCULAR MEMORY ARRAY
US	5,793,069	08/672,411	APPARATUS FOR PROTECTING GATE ELECTRODES OF TARGET TRANSISTORS IN A GATE ARRAY FROM GATE CHARGING BY EMPLOYING FREE TRANSISTORS IN THE GATE ARRAY
US	5,794,007	08/553,017	SYSTEM AND METHOD FOR PROGRAMMING PROGRAMMABLE ELECTRONIC COMPONENTS USING BOARD-LEVEL AUTOMATED TEST EQUIPMENT
US	5,795,172	08/768,961	PRODUCTION PRINTED CIRCUIT BOARD (PCB) EDGE CONNECTOR TEST CONNECTOR
US	5,796,282	08/700,613	LATCHING MECHANISM FOR PULSED DOMINO LOGIC WITH INHERENT RACE MARGIN AND TIME BORROWING
US	5,796,639	08/778,305	METHOD AND APPARATUS FOR VERIFYING THE INSTALLATION OF STRAPPING DEVICES ON A CIRCUIT BOARD ASSEMBLY
US	5,801,821	08/497,321	PHOTOLITHOGRAPHY METHOD USING COHERENCE DISTANCE CONTROL
US	5,802,074	08/715,857	METHOD AND APPARATUS FOR THE NON-INVASIVE TESTING OF PRINTED CIRCUIT BOARD ASSEMBLIES
US	5,802,213	08/324,923	ENCODING VIDEO SIGNALS USING LOCAL QUANTIZATION LEVELS
US	5,802,674	08/849,031	FIBRE METERING ARRANGEMENT
US	5,804,771	08/721,268	ORGANIC SUBSTRATE (PCB) SLIP PLANE "STRESS DEFLECTOR" FOR FLIP CHIP DEVICES
US	5,809,110	08/594,411	TECHNIQUE OF CONTROLLING TELEPHONE CALLS
US	5,809,247	08/685,952	METHOD AND APPARATUS FOR GUIDED TOURING OF INTERNET/INTRANET WEBSITES
US	5,815,372	08/822,743	PACKAGING MULTIPLE DIES ON A BALL GRID ARRAY SUBSTRATE
US	5,818,969	08/854,770	INTELLIGENT START FOR MOTION ESTIMATION SEARCH
US	5,832,241	08/878,660	DATA CONSISTENCY ACROSS A BUS TRANSACTIONS THAT IMPOSE ORDERING CONSTRAINTS

Schedule A

US	5,835,927	08/719,583	SPECIAL TEST MODES FOR A PAGE BUFFER SHARED RESOURCE IN A MEMORY DEVICE
US	5,838,941	08/774,659	OUT-OF-ORDER SUPERSCALAR MICROPROCESSOR WITH A RENAMING DEVICE THAT MAPS INSTRUCTIONS FROM MEMORY TO REGISTERS
US	5,843,846	08/775,573	ETCH PROCESS TO PRODUCE ROUNDED TOP CORNERS FOR SUB-MICRON SILICON TRENCH APPLICATIONS
US	5,844,852	08/907,754	MEMORY ARRAYS WITH INTEGRATED BIT LINE VOLTAGE STABILIZATION CIRCUITRY
US	5,847,366	08/668,045	APPARATUS AND METHOD FOR CONTROLLING THE TEMPERATURE OF AN INTEGRATED CIRCUIT UNDER TEST
US	5,848,288	08/530,076	METHOD AND APPARATUS FOR ACCOMMODATING DIFFERENT ISSUE WIDTH IMPLEMENTATIONS OF VLIW ARCHITECTURES
US	5,867,367	08/984,766	QUAD FLAT PACK INTEGRATED CIRCUIT PACKAGE
US	5,867,721	08/978,998	SELECTING AN INTEGRATED CIRCUIT FROM DIFFERENT INTEGRATED CIRCUIT ARRAY CONFIGURATIONS
US	5,880,622	08/768,297	METHOD AND APPARATUS FOR CONTROLLING A CHARGE PUMP FOR RAPID INITIALIZATION
US	5,881,076	08/682,108	COMPARATOR UTILIZING REDUNDANCY
US	5,881,146	08/828,000	METHOD AND APPARATUS FOR DETERMINING DIGITS DIALED USING A SELECTED ALGORITHM
US	5,888,897	08/739,879	PROCESS FOR FORMING AN INTEGRATED STRUCTURE COMPRISING A SELF-ALIGNED VIA/CONTACT AND INTERCONNECT
US	5,889,408	08/670,545	DELTA IDDQ TESTING
US	5,889,409	08/721,685	LEAKAGE TRACKING DEVICE SAMPLE FOR IDDQ MEASUREMENT AND DEFECT RESOLUTION
US	5,889,950	08/771,709	METHOD AND APPARATUS FOR DISTRIBUTION OF BROADCAST DATA
US	5,889,988	08/748,551	DEBUGGER FOR DEBUGGING TASKS IN AN OPERATING SYSTEM VIRTUAL DEVICE DRIVER
US	5,894,408	09/024,860	ELECTRONIC CARTRIDGE WHICH ALLOWS DIFFERENTIAL THERMAL EXPANSION BETWEEN COMPONENTS OF THE CARTRIDGE
US	5,900,770	08/874,496	VARIABLE LOADING APPARATUS FOR OUTPUT LOADING OF INTEGRATED CIRCUITS
US	5,903,432	08/933,405	COMPUTER PACKAGE WITH A POLYGONAL SHAPED MOTHERBOARD

Schedule A

US	5,903,500	08/834,032	1.8 VOLT OUTPUT BUFFER ON FLASH MEMORIES
US	5,909,635	08/673,277	CLADDING OF AN INTERCONNECT FOR IMPROVED ELECTROMIGRATION PERFORMANCE
US	5,912,950	08/594,016	TELEPHONE NETWORK WITH NORMALLY OFF HOOK TELEPHONES
US	5,915,018	08/740,976	KEY MANAGEMENT SYSTEM FOR DVD COPYRIGHT MANAGEMENT
US	5,917,239	08/835,228	RECESSED OR RAISED CHARACTERS ON A CERAMIC LID
US	5,918,025	08/775,807	METHOD AND APPARATUS FOR CONVERTING A FIVE WIRE ARBITRATION/BUFFER MANAGEMENT PROTOCOL INTO A TWO WIRE PROTOCOL
US	5,918,033	08/780,675	METHOD AND APPARATUS FOR DYNAMIC LOCATION AND CONTROL OF PROCESSSOR RESOURCES TO INCREASE RESOLUTION OF DATA DEPENDENCY STALLS
US	5,918,192	08/787,865	A METHOD FOR CALIBRATING A DIGITAL CAMERA TO A PC MONITOR TO ENHANCE PICTURE QUALITY OF A PICTURE CAPTURED BY THE DIGITAL CAMERA AND DISPLAYED ON THE PC MONITOR
US	5,920,870	912,380	MULTI-LAYER ABSTRACTION BUCKET MECHANISM
US	5,931,944	08/996,756	BRANCH INSTRUCTION HANDLING IN A SELF-TIMED MARKING SYSTEM
US	5,941,982	08/997,461	EFFICIENT SELF-TIMED MARKING OF LENGTHY VARIABLE LENGTH INSTRUCTIONS
US	5,943,487	08/679,197	METHOD FOR EXTRACTING A RESISTOR NETWORK FROM AN INTEGRATED CIRCUIT POLYGON LAYOUT
US	5,943,693	08/412,555	ALGORITHMIC ARRAY MAPPING TO DECREASE DEFECT SENSITIVITY OF MEMORY DEVICES
US	5,945,988	08/866,707	METHOD AND APPARATUS FOR AUTOMATICALLY DETERMINING AND DYNAMICALLY UPDATING USER PREFERENCES IN AN ENTERTAINMENT SYSTEM
US	5,946,079	08/962,138	PHOTOLITHOGRAPHY METHOD USING COHERENCE DISTANCE CONTROL
US	5,946,258	09/040,523	PUMP SUPPLY SELF REGULATION FOR FLASH MEMORY CELL PAIR REFERENCE CIRCUIT
US	5,946,396	08/738,086	A SYSTEM AND METHOD FOR ENSURING INTEGRITY OF AUDIO
US	5,948,096	08/997,462	APPARATUS AND METHOD FOR SELF-TIMED MARKING OF VARIABLE LENGTH INSTRUCTIONS HAVING LENGTH-AFFECTING PREFIX BYTES
US	5,948,960	09/020,661	HTMU TEST HANDLER THROW MEASURING UNIT

Schedule A

US	5,949,651	09/179,016	QUAD FLAT PACK INTEGRATED CIRCUIT PACKAGE
US	5,951,667	08/778,192	METHOD AND APPARATUS FOR CONNECTING EXPANSION BUSES TO A PERIPHERAL COMPONENT INTERCONNECT BUS
US	5,959,445	09/002,174	STATIC, HIGH-SENSITIVITY, FUSE-BASED STORAGE CELL
US	5,961,728	08/874,388	METHOD AND APPARATUS FOR CLEANING A TEST PROBE
US	5,963,970	08/770,958	METHOD AND APPARATUS FOR TRACKING ERASE CYCLES UTILIZING ACTIVE AND INACTIVE WEAR BAR BLOCKS HAVING FIRST AND SECOND COUNT FIELDS
US	5,964,513	09/085,779	CHASSIS FOR ELECTRONIC COMPONENTS
US	5,964,870	08/934,964	METHOD AND APPARATUS FOR USING FUNCTION CONTEXT TO IMPROVE BRANCH
US	5,965,937	08/990,856	THERMAL INTERFACE ATTACH MECHANISM FOR ELECTRICAL PACKAGES
US	5,966,020	08/741,053	METHOD AND APPARATUS FOR FACILITATING DETECTION OF SOLDER OPENS OF SMT COMPONENTS
US	5,966,544	08/746,547	DATA SPECULATABLE PROCESSOR HAVING REPLY ARCHITECTURE
US	5,970,147	08/938,491	SYSTEM AND METHOD FOR CONFIGURING AND REGISTERING A CRYPTOGRAPHIC DEVICE
US	5,973,957	08/931,247	SENSE AMPLIFIER COMPRISING A PREAMPLIFIER AND A DIFFERENTIAL INPUT LATCH FOR FLASH MEMORIES
US	5,978,224	09/179,125	QUAD FLAT PACK INTEGRATED CIRCUIT PACKAGE
US	5,978,228	08/777,604	APPARATUS FOR MOUNTING A VERY LARGE SCALE INTEGRATION (VLSI) CHIP TO A COMPUTER CHASSIS FOR COOLING
US	5,978,263	08/895,613	NEGATIVE VOLTAGE SWITCH ARCHITECTURE FOR A NONVOLATILE MEMORY
US	5,978,873	08/936,857	COMPUTER SYSTEM INCLUDING RIGHT ANGLE PROCESSOR AND ADD-ON CARD CONNECTORS
US	5,978,909	08/979,579	SYSTEM FOR SPECULATIVE BRANCH TARGET PREDICTION HAVING A DYNAMIC PREDICTION HISTORY BUFFER AND A STATIC PREDICTION HISTORY BUFFER
US	5,982,684	09/086,330	PARALLEL ACCESS TESTING OF A MEMORY ARRAY
US	5,987,504	08/801,508	METHOD AND APPARATUS FOR DELIVERING DATA
US	5,987,552	09/013,774	COHERENT VARIABLE LENGTH READS FROM SYSTEM MEMORY

Schedule A

US	5,987,572	08/937,874	METHOD AND APPARATUS EMPLOYING A DYNAMIC ENCRYPTION INTERFACE BETWEEN A PROCESSOR AND A MEMORY
US	6,002,525	09/110,805	CORRECTING LENS DISTORTION
US	6,002,879	08/829,856	METHOD FOR PERFORMING COMMON SUBEXPRESSION ELIMINATION ON A RACK-N STATIC SINGLE ASSIGNMENT LANGUAGE
US	6,006,282	08/565,953	BLOCKING HOST INPUT WHILE A REMOTE GUEST HAS INPUT CONTROL TO A HOST-EXECUTED SHARED APPLICATION
US	6,009,497	09/189,000	METHOD AND APPARATUS FOR UPDATING FLASH MEMORY RESIDENT FIRMWARE THROUGH A STANDARD DISK DRIVE INTERFACE
US	6,012,082	08/935,742	CPU-CYCLE STEALING FOR MULTI-TASKING OPERATING SYSTEM
US	6,014,755	08/700,676	METHOD OF MANAGING DEFECTS IN FLASH DISK MEMORIES
US	6,016,398	08/831,739	METHOD FOR USING STATIC SINGLE ASSIGNMENT TO COLOR OUT ARTIFICIAL REGISTER DEPENDENCIES
US	6,019,166	09/000,981	PICKUP CHUCK WITH AN INTEGRAL HEATSINK
US	6,021,505	09/105,479	METHOD AND APPARATUS FOR UPDATING A TIMER FROM MULTIPLE TIMING DOMAINS
US	6,024,426	09/329,425	CHASSIS FOR ELECTRONIC COMPONENTS
US	6,026,455	08/201,817	ARCHITECTURE AND METHOD FOR PROVIDING GUARANTEED ACCESS FOR A RETRYING BUS MASTER TO A DATA TRANSFER BRIDGE CONNECTING TWO BUSES IN A COMPUTER SYSTEM
US	6,026,465	08/897,499	FLASH MEMORY INCLUDING A MODE REGISTER FOR INDICATING SYNCHRONOUS OR ASYNCHRONOUS MODE OF OPERATION
US	6,027,191	09/329,426	CHASSIS FOR ELECTRONIC COMPONENTS
US	6,028,696	09/172,615	CHARGE CONTROLLED MIRROR WITH IMPROVED FRAME TIME UTILIZATION AND METHOD OF ADDRESSING THE SAME
US	6,029,730	09/001,021	HOT SHEAR APPARATUS AND METHOD FOR REMOVING A SEMICONDUCTOR CHIP FROM AN EXISTING PACKAGE
US	6,031,656	09/179,933	BEAM-ADDRESSED MICROMIRROR DIRECT VIEW DISPLAY
US	6,031,657	09/208,041	MEMBRANE-ACTUATED CHARGE CONTROLLED MIRROR (CCM) PROJECTION DISPLAY

Schedule A

US	6,047,035	09/103,683	METHOD AND DEVICE FOR QUANTIZING THE INPUT TO SOFT DECODERS
US	6,051,999	09/006,770	LOW VOLTAGE PROGRAMMABLE COMPLEMENTARY INPUT STAGE SENSE AMPLIFIER
US	6,055,095	09/364,142	MICROSCOPE WITH INFRARED IMAGING
US	6,055,614	08/778,015	APPARATUS FOR PERFORMING A USER REQUESTED RESET DURING ALGORITHM EXECUTION
US	6,060,917	09/064,276	FREQUENCY SYNTHESIZER
US	6,061,263	09/221,804	SMALL OUTLINE RAMBUS IN-LINE MEMORY MODULE
US	6,061,265	09/221,233	QUANTUM MAGNETIC MEMORY
US	6,064,571	09/074,951	FAN DUCT MODULE
US	6,069,928	08/885,803	SCALABLE RECEIVER STRUCTURE FOR EFFICIENT BIT SEQUENCE DECODING
US	6,070,252	08/698,465	METHOD AND APPARATUS FOR INTERACTIVE BUILT-IN-SELF-TESTING WITH USER-PROGRAMMABLE TEST PATTERNS
US	6,072,723	09/306,322	METHOD AND APPARATUS FOR PROVIDING REDUNDANCY IN NON-VOLATILE MEMORY DEVICES
US	6,073,030	08/820,129	USE OF RSSI INDICATION FOR IMPROVED DATA TRANSMISSION OVER AMPS NETWORK
US	6,075,751	09/231,725	SIGNAL TRANSITION DETECTOR FOR ASYNCHRONOUS CIRCUITS
US	6,077,337	09/203,432	CHEMICAL-MECHANICAL POLISHING SLURRY
US	6,080,022	08/672,643	MULTIVOLTAGE KEYED ELECTRICAL CONNECTOR
US	6,081,272	08/941,599	MERGING DUMMY STRUCTURE REPRESENTATIONS FOR IMPROVED DISTRIBUTION OF ARTIFACTS IN A SEMICONDUCTOR LAYER
US	6,083,839	09/001,509	UNIQUE CHEMICAL MECHANICAL PLANARIZATION APPROACH WHICH UTILIZES MAGNETIC SLURRY FOR POLISH AND MAGNETIC FIELDS FOR PROCESS CONTROL
US	6,084,773	09/024,921	INTEGRATED PROCESSOR SUBSTRATE PROTECTIVE ENCLOSURE FOR USE IN DESKTOP PC SYSTEMS
US	6,085,341	09/030,522	MEMORY TEST MODE FOR WORLDLINE RESISTIVE DEFECTS
US	6,094,530	09/069,527	REMOTELY MONITORING EXECUTION OF A PROGRAM
US	6,100,709	09/087,753	SILICON WAFER TESTING RIG AND A METHOD FOR TESTING A SILICON WAFER WHEREIN THE SILICON WAFER IS BENT INTO A DOME SHAPE
US	6,102,647	09/105,191	CART FOR TRANSFERRING OBJECTS

Schedule A

US	6,104,720	08/848,554	DYNAMIC COMMUNICATION PATH SELECTION FOR DATA TRANSMISSION BETWEEN COMPUTERS
US	6,108,130	09/393,757	STEREOSCOPIC IMAGE SENSOR
US	6,108,743	09/021,688	TECHNIQUE FOR PERFORMING DMA INCLUDING ARBITRATION BETWEEN A CHAINED LOW PRIORITY DMA AND HIGH PRIORITY DMA OCCURRING BETWEEN TWO LINKS IN THE CHAINED LOW PRIORITY
US	6,113,648	09/024,830	METHOD AND APPARATUS FOR PROTECTING GATE ELECTRODES OF TARGET TRANSISTORS IN THE GATE ARRAY FROM GATE CHARGING BY EMPLOYING FREE TRANSISTORS IN THE GATE ARRAY
US	6,124,168	08/337,131	METHOD FOR FORMING AN ASYMMETRIC FLOATING GATE OVERLAP FOR IMPROVED DEVICE PERFORMANCE IN BURIED BIT-LINE DEVICES
US	6,125,412	08/046,109	A SYSTEM FOR PERFORMING INPUT AND OUTPUT OPERATIONS TO AND FROM A PROCESSOR
US	6,127,696	08/087,140	HIGH VOLTAGE MOS TRANSISTOR FOR FLASH EEPROM APPLICATIONS HAVING A UNI-SIDED LIGHTLY DOPED DRAIN
US	6,130,819	09/015,423	FAN DUCT MODULE
US	6,134,635	08/987,279	METHOD AND APPARATUS OF RESOLVING A DEADLOCK BY COLLAPSING WRITEBACKS TO A MEMORY
US	6,137,354	09/080,812	BYPASSABLE AMPLIFIER
US	6,137,709	09/499,084	SMALL OUTLINE MEMORY MODULE
US	6,144,218	09/012,201	HIGH SPEED ANALOG COMPENSATED INPUT BUFFER
US	6,151,229	09/346,483	CHARGE PUMP WITH GATED PUMPED OUTPUT DIODE AT INTERMEDIATE STAGE
US	6,151,678	08/927,370	ANTI-THEFT MECHANISM FOR MOBILE COMPUTERS
US	6,162,073	09/223,811	HOT PLUG STRUCTURE
US	6,163,474	09/225,927	MEMORY CARD WHICH IS THERMALLY CONTROLLED
US	6,163,838	09/106,857	COMPUTER PROCESSOR WITH A REPLAY SYSTEM
US	6,166,563	09/299,771	METHOD AND APPARATUS FOR DUAL MODE OUTPUT BUFFER IMPEDANCE COMPENSATION
US	6,172,538	09/226,924	UNIVERSAL PULSE SYNCHRONIZER
US	6,172,540	09/374,798	APPARATUS FOR FAST LOGIC TRANSFER OF DATA ACROSS ASYNCHRONOUS CLOCK DOMAINS
US	6,173,489	09/032,628	ORGANIC SUBSTRATE (PCB) SLIP PLANE "STRESS DEFLECTOR" FOR FLIP CHIP DEVICES

Schedule A

US	6,181,180	09/340,417	FLIP-FLOP CIRCUIT
US	6,184,732	09/370,622	SETTING THE COMMON MODE LEVEL OF A DIFFERENTIAL CHARGE PUMP OUTPUT
US	6,184,739	09/205,992	ADVANCED NEAR IDEAL MIXER
US	6,192,044	08/829,608	EMPLOYING A LOOK-UP SERVICE AND A CALLEE CONNECTION SERVICE TO ESTABLISH A NETWORK PHONE CALL BETWEEN A CALLER AND A CALLEE
US	6,195,259	09/358,373	HOT PLUG CARTRIDGE ASSEMBLY
US	6,198,421	09/259,650	NEURAL FLASH ANALOG-TO-DIGITAL CONVERTER USING WEIGHTED CURRENT SIMULATION
US	6,199,149	09/016,790	OVERLAY COUNTER FOR ACCELERATED GRAPHICS PORT
US	6,208,527	09/098,086	RETENTION MECHANISM ASSEMBLY FOR PROCESSOR CARTRIDGES WITH CAPTURED SCREW FASTENERS
US	6,211,718	09/003,908	LOW VOLTAGE DOUBLE BALANCED MIXER
US	6,214,098	09/504,191	CHEMICAL-MECHANICAL POLISHING SLURRY
US	6,221,789	09/124,562	THIN OXIDES OF SILICON
US	6,232,826	09/005,560	CHARGE PUMP AVOIDING GAIN DEGRADATION DUE TO THE BODY EFFECT
US	6,239,605	09/162,912	METHOD TO PERFORM IDDQ TESTING IN THE PRESENCE OF HIGH BACKGROUND LEAKAGE CURRENT
US	6,239,606	09/163,592	METHOD TO PERFORM IDDQ TESTING IN THE PRESENCE OF HIGH BACKGROUND LEAKAGE CURRENT
US	6,240,168	09/240,168	METHOD AND APPARATUS FOR CONTROLLING A COMPUTER TO IMPLEMENT TELEPHONE FUNCTIONS WITH A DISPLAYED TELEPHONE OF VARIABLE SIZE
US	6,246,334	09/299,162	BOARD ID DISPLAY SYSTEM
US	6,247,120	08/912,048	INSTRUCTION BUFFER FOR ISSUING INSTRUCTION SETS TO AN INSTRUCTION DECODER
US	6,250,821	08/787,983	METHOD AND APPARATUS FOR PROCESSING BRANCH INSTRUCTIONS IN AN INSTRUCTION BUFFER
US	6,255,135	09/179,014	QUAD FLAT PACK INTEGRATED CIRCUIT PACKAGE
US	6,255,873	09/665,339	SETTING THE COMMON MODE LEVEL OF A DIFFERENTIAL CHARGE PUMP OUTPUT
US	6,255,896	09/406,329	METHOD AND APPARATUS FOR RAPID INITIALIZATION OF CHARGE PUMP CIRCUITS
US	6,256,059	09/003,732	AUTOMATIC TRANSFER OF IMAGE INFORMATION BETWEEN IMAGING DEVICE AND HOST SYSTEM

Schedule A

US	6,256,673	09/213,220	CYCLIC MULTICASTING OR ASYNCHRONOUS BROADCASTING OF COMPUTER FILES
US	6,268,774	09/434,250	SELF-TUNING AMPLIFIER
US	6,272,676	09/006,276	METHOD AND APPARATUS FOR FINDING LOOP-LEVER PARALLELISM IN A POINTER BASED APPLICATION
US	6,282,228	08/821,611	SPREAD SPECTRUM CODES FOR USE IN COMMUNICATION
US	6,284,091	09/352,634	UNIQUE CHEMICAL MECHANICAL PLANARIZATION APPROACH WHICH UTILIZES MAGNETIC SLURRY FOR POLISH AND MAGNETIC FIELDS FOR PROCESS CONTROL
US	6,292,048	09/438,186	GATE ENHANCEMENT CHARGE PUMP FOR LOW VOLTAGE POWER SUPPLY
US	6,297,492	09/003,477	FAST BICMOS ACTIVE-PIXEL SENSOR CELL WITH FAST NPN EMITTER-FOLLOWER READOUT
US	6,307,355	09/148,033	METHOD AND APPARATUS FOR REDUCING THE POWER CONSUMPTION OF A VOLTAGE REGULATOR
US	6,308,278	09/001,102	SUPPLYING STANDBY VOLTAGE TO MEMORY AND WAKEUP CIRCUITRY TO WAKE A COMPUTER FROM A LOW POWER MODE
US	6,311,212	09/270,287	SYSTEMS AND METHODS FOR ON-CHIP STORAGE OF VIRTUAL CONNECTION DESCRIPTORS
US	6,314,506	09/221,626	METHOD AND APPARATUS FOR DETERMINING A NEXT ADDRESS WITHIN A BINARY SEARCH ALGORITHM
US	6,317,452	09/307,646	METHOD AND APPARATUS FOR WIRELESS SPREAD SPECTRUM COMMUNICATION WITH PREAMBLE SOUNDING GAP
US	6,324,263	09/144,511	DIGITAL TELEPHONE SYSTEM WITH AUTOMATIC ROUTING BASED UPON CALLER ID
US	6,346,144	09/723,092	CHEMICAL-MECHANICAL POLISHING SLURRY
US	6,351,387	09/606,893	SYSTEM AND METHOD OF HEAT EXTRACTION FROM AN INTEGRATED CIRCUIT DIE
US	6,351,555	09/482,551	EFFICIENT COMPANDING ALGORITHM SUITABLE FOR COLOR IMAGING
US	6,359,814	09/753,351	NEGATIVE OUTPUT VOLTAGE CHARGE PUMP AND METHOD THEREFOR
US	6,361,007	09/483,215	MOUNTING BRACKET FOR PCS AND OTHER ANTENNAS

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US	6,364,331	09/410,400	METHOD AND APPARATUS FOR TRANSFERRING WAFER CASSETTES IN MICROELECTRONIC MANUFACTURING ENVIRONMENT
US	6,365,441	09/694,802	PARTIAL UNDERFILL FOR FLIP-CHIP ELECTRONIC PACKAGES
US	6,366,158	09/752,247	SELF INITIALIZATION FOR CHARGE PUMPS
US	6,366,516	09/753,005	MEMORY SUBSYSTEM EMPLOYING POOL OF REFRESH CANDIDATES
US	6,369,642	09/748,611	OUTPUT SWITCH FOR CHARGE PUMP RECONFIGURATION
US	6,370,685	09/226,804	DATA-FLOW METHOD OF ANALYZING DEFINITIONS AND USES OF L VALUES IN PROGRAMS
US	6,373,324	09/475,459	VOLTAGE BLOCKING METHOD AND APPARATUS FOR A CHARGE PUMP WITH DIODE CONNECTED PULL-UP AND PULL-DOWN ON BOOT NODES
US	6,374,278	09/276,366	METHOD AND APPARATUS FOR THE GENERATION OF STATISTICALLY RANDOM NUMBERS
US	6,377,576	08/541,678	TELEPHONE CALL SETUP PROCEDURE
US	6,378,061	08/150,784	APPARATUS FOR ISSUING INSTRUCTIONS AND REISSUING A PREVIOUS INSTRUCTIONS BY RECIRCULATING USING THE DELAY CIRCUIT
US	6,384,658	09/676,313	CLOCK SPLITTER CIRCUIT TO GENERATE SYNCHRONIZED CLOCK AND INVERTED CLOCK
US	6,384,838	08/425,231	OPTIMIZED LOOKUP TABLE METHOD FOR CONVERTING YUV PIXEL VALUES TO RGB PIXEL VALUES
US	6,384,872	09/395,000	METHOD AND APPARATUS FOR INTERLACED IMAGE ENHANCEMENT
US	6,388,475	09/474,566	VOLTAGE TOLERANT HIGH DRIVE PULL-UP DRIVER FOR AN I/O BUFFER
US	6,400,370	09/393,477	STOCHASTIC SAMPLING WITH CONSTANT DENSITY IN OBJECT SPACE FOR ANISOTROPIC TEXTURE MAPPING
US	6,400,709	09/204,607	DTMF DETECTION IN INTERNET TELEPHONY
US	6,407,632	09/611,720	RADIO FREQUENCY AMPLIFIER
US	6,418,201	09/510,311	MULTIPLE PLATFORM VOICE PROCESSING SYSTEM WITH OPTIMIZED RESOURCE ALLOCATION
US	6,421,432	09/497,970	METHOD AND APPARATUS FOR CONTROLLING A COMPUTER TO IMPLEMENT TELEPHONE FUNCTIONS WITH A DISPLAYED TELEPHONE OF VARIABLE SIZE

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US	6,425,067		09/340,282	SYSTEMS AND METHODS FOR IMPLEMENTING POINTER MANAGEMENT
US	6,438,275		09/296,451	METHOD FOR MOTION COMPENSATED FRAME RATE UPSAMPLING BASED ON PIECEWISE AFFINE WARPING
US	6,441,678		10/051,696	SELF INITIALIZATION FOR CHARGE PUMPS
US	6,445,230		09/750,671	PROGRAMMABLE DIGITAL PHASE LOCK LOOP
US	6,449,211		09/945,021	VOLTAGE DRIVER FOR A MEMORY
US	6,449,308		09/318,287	HIGH-SPEED DIGITAL DISTRIBUTION SYSTEM
US	6,452,438		09/751,695	TRIPLE WELL NO BODY EFFECT NEGATIVE CHARGE PUMP
US	6,456,110		09/750,110	VOLTAGE LEVEL SHIFTER HAVING ZERO DC CURRENT AND STATE RETENTION IN DROWSY MODE
US	6,461,169		09/849,506	INTERCONNECTING CIRCUIT MODULES TO A MOTHERBOARD USING AN EDGE CONNECTOR WITH CONDUCTIVE POLYMER CONTACTS
US	6,462,612		09/894,151	CHOPPER STABILIZED BANDGAP REFERENCE CIRCUIT TO CANCEL OFFSET VARIATION
US	6,465,358		09/684,550	POST ETCH CLEAN SEQUENCE FOR MAKING A SEMICONDUCTOR DEVICE
US	6,471,170		09/804,489	KEYBOARD HOLDER
US	6,480,066		09/705,499	AMPLIFIERS
US	6,484,092	US-2002-0152020-A1	09/818,993	METHOD AND SYSTEM FOR DYNAMIC AND INTERACTIVE ROUTE FINDING
US	6,484,309	TNT	09/168,592	ENABLING SOFTWARE DESIGNED FOR ONE OPERATING SYSTEM TO OPERATE ON ANOTHER OPERATING SYSTEM
US	6,486,791		09/872,490	DRIVING A VISUAL INDICATOR ARRAY IN AN ELECTRONIC SIGNALING SYSTEM
US	6,488,571		09/746,470	APPARATUS FOR ENHANCED RATE CHEMICAL MECHANICAL POLISHING WITH ADJUSTABLE SELECTIVITY
US	6,489,557		09/385,924	IMPLEMENTING MICRO BGA.TM. ASSEMBLY TECHNIQUES FOR SMALL DIE
US	6,489,955		09/327,015	RAY INTERSECTION REDUCTION USING DIRECTIONALLY CLASSIFIED TARGET LISTS
US	6,493,233		09/934,871	PCB-TO-CHASSIS MOUNTING SCHEMES
US	6,496,055		09/753,045	GATE ENHANCED TRI-CHANNEL POSITIVE CHARGE PUMP
US	6,498,305		09/713,702	INTERCONNECT MECHANICS FOR ELECTROMAGNETIC COUPLER

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US	6,498,605	09/442,663	PIXEL SPAN DEPTH BUFFER
US	6,499,085	09/752,846	METHOD AND SYSTEM FOR SERVICING CACHE LINE IN RESPONSE TO PARTIAL CACHE LINE REQUEST
US	6,504,760	09/888,252	CHARGING A CAPACITANCE OF A MEMORY CELL AND CHARGER
US	6,507,061	09/945,331	MULTIPLE LAYER PHASE-CHANGE MEMORY
US	6,512,861	09/892,921	PACKAGING AND ASSEMBLY METHOD FOR OPTICAL COUPLING
US	6,514,805	09/896,532	TRENCH SIDEWALL PROFILE FOR DEVICE ISOLATION
US	6,515,586	09/216,580	TACTILE TRACKING SYSTEMS AND METHODS
US	6,515,901	09/751,514	METHOD AND APPARATUS FOR ALLOWING CONTINUOUS APPLICATION OF HIGH VOLTAGE TO A FLASH MEMORY DEVICE POWER PIN
US	6,515,906	09/752,714	METHOD AND APPARATUS FOR MATCHED-REFERENCE SENSING ARCHITECTURE FOR NON-VOLATILE MEMORIES
US	6,522,180	09/745,970	BI-VOLTAGE LEVELS SWITCHES
US	6,525,726	09/432,134	METHOD AND APPARATUS FOR ADAPTIVE HIERARCHICAL VISIBILITY IN A TILED THREE-DIMENSIONAL GRAPHICS ARCHITECTURE
US	6,533,586	09/751,527	ELECTROMAGNETIC COUPLER SOCKET
US	6,539,366	09/071,049	CODEC WITH GENETIC ADAPTATION
US	6,542,584	09/144,186	DIGITAL TELEPHONE SYSTEM WITH AUTOMATIC VOICE MAIL REDIRECTION
US	6,544,047	09/821,114	DUAL-SWIPING INTERCONNECTION CLIP, AND HOOK AND SLOT ARRANGEMENT FOR PRINTED CIRCUIT BOARD (PCB) ATTACHMENT
US	6,548,399	09/996,215	METHOD OF FORMING A SEMICONDUCTOR DEVICE USING A CARBON DOPED OXIDE LAYER TO CONTROL THE CHEMICAL MECHANICAL POLISHING OF A DIELECTRIC LAYER
US	6,552,600	09/809,623	INITIALIZATION OF NEGATIVE CHARGE PUMP
US	6,552,898	09/566,185	FAN DUCT MODULE
US	6,556,128	09/458,715	METHOD FOR REDUCING POWER CONSUMPTION IN WAIT-MODE
US	6,560,286	09/474,183	FIELD FRAME MOTION DESIGN FOR DIGITAL VIDEO DECODER
US	6,560,317	10/038,411	RECEIVING CALLER IDENTIFICATION INFORMATION WITH A TELECOMMUNICATIONS DEVICE FOR THE DEAF

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US	6,564,811		09/818,177	METHOD OF REDUCING RESIDUE DEPOSITION ONTO ASH CHAMBER BASE SURFACES
US	6,569,705		09/745,835	METAL STRUCTURE FOR A PHASE-CHANGE MEMORY DEVICE
US	6,570,789		09/752,535	LOAD FOR NON-VOLATILE MEMORY DRAIN BIAS
US	6,573,747		09/965,627	DIGITAL UPDATE SCHEME FOR ADAPTIVE IMPEDANCE CONTROL OF ON-DIE INPUT/OUTPUT CIRCUITS
US	6,574,141		09/982,246	DIFFERENTIAL REDUNDANCY MULTIPLEXOR FOR FLASH MEMORY DEVICES
US	6,574,386		09/839,848	DYNAMICALLY RECONFIGURABLE OPTICAL SWITCHING SYSTEM
US	6,576,847		09/751,442	CLAMP TO SECURE CARRIER TO DEVICE FOR ELECTROMAGNETIC COUPLER
US	6,577,274		10/028,472	METHOD AND APPARATUS FOR CONTROLLING ACCESS TO MOBILE DEVICES
US	6,580,837		09/457,058	UP-SAMPLING DECIMATED COLOR PLANE DATA
US	6,586,761	TNT	09/948,830	PHASE CHANGE MATERIAL MEMORY DEVICE
US	6,586,836		09/516,652	PROCESS FOR FORMING MICROELECTRONIC PACKAGES AND INTERMEDIATE STRUCTURES FORMED THEREWITH
US	6,590,807		09/921,853	METHOD FOR READING A STRUCTURAL PHASE-CHANGE MEMORY
US	6,593,650		10/050,463	PLASMA INDUCED DEPLETION OF FLUORINE FROM SURFACES OF FLUORINATED LOW-K DIELECTRIC MATERIALS
US	6,594,329		09/432,050	ELASTIC BUFFER
US	6,594,344		09/749,610	AUTO LATENCY TEST TOOL
US	6,595,798		09/280,171	TEST FIXTURE FOR TESTING A MULTI-PORT VOICE PROCESSING CARD AND THE LIKE
US	6,596,614		10/246,273	USE OF MEMBRANE PROPERTIES TO REDUCE RESIDUAL STRESS IN AN INTERLAYER REGION
US	6,597,606		10/154,019	CHARGING A CAPACITANCE OF A MEMORY CELL AND CHARGER
US	6,598,133	US-2003-0005240-A1	09/894,755	SUCCESSIVE TEMPLATE GENERATION USING MINIMAL RANDOM ACCESS MEMORY BANDWIDTH
US	6,603,768		09/344,672	MULTI-PROTOCOL CONVERSION ASSISTANCE METHOD AND SYSTEM FOR A NETWORK ACCELERATOR
US	6,603,893		09/819,160	METHOD AND APPARATUS FOR SWITCHING AN OPTICAL BEAM IN A SEMICONDUCTOR SUBSTRATE

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US	6,604,136		09/337,025	APPLICATION PROGRAMMING INTERFACES AND METHODS ENABLING A HOST TO INTERFACE WITH A NETWORK PROCESSOR
US	6,605,527		09/896,531	REDUCED AREA INTERSECTION BETWEEN ELECTRODE AND PROGRAMMING ELEMENT
US	6,605,984		10/038,499	CHARGE PUMP RIPPLE REDUCTION
US	6,614,065		10/238,081	USE OF MEMBRANE PROPERTIES TO REDUCE RESIDUAL STRESS IN AN INTERLAYER REGION
US	6,617,593		09/730,206	ION IMPLANTATION SYSTEM
US	6,621,287	AMM	09/858,224	CONNECTOR ASSEMBLY WITH DECOUPLING CAPACITORS
US	6,622,802	WWN	09/821,247	FASTENER INSTALLATION TOOL AND METHODS OF USE
US	6,625,052		09/966,014	WRITE-ONCE POLYMER MEMORY WITH E-BEAM WRITING AND READING
US	6,625,650		09/340,068	SYSTEM FOR MULTI-LAYER BROADBAND PROVISIONING IN COMPUTER NETWORKS
US	6,628,552		08/834,029	SELF-CONFIGURING INPUT BUFFER ON FLASH MEMORIES
US	6,628,865		09/738,800	ALIGNMENT OF OPTICAL FIBERS TO AN ETCHED ARRAY WAVEGUIDE
US	6,629,271		09/472,839	TECHNIQUE FOR SYNCHRONIZING FAULTS IN A PROCESSOR HAVING A REPLAY SYSTEM
US	6,630,390		10/354,361	METHOD OF FORMING A SEMICONDUCTOR DEVICE USING A CARBON DOPED OXIDE LAYER TO CONTROL THE CHEMICAL MECHANICAL POLISHING OF A DIELECTRIC LAYER
US	6,631,339		09/834,016	DATA PATH EVALUATION SYSTEM AND METHOD
US	6,631,444		09/894,513	CACHE ARCHITECTURE FOR PIPELINED OPERATION WITH ON-DIE PROCESSOR
US	6,633,972		09/878,062	METHOD AND APPARATUS FOR UTILIZING STATIC QUEUES IN PROCESSOR STAGING
US	6,636,671		09/741,642	MARKINGS FOR ALIGNING FIBER OPTIC BUNDLE
US	6,637,719		10/006,502	CARRIER FOR DISK DRIVE HOT SWAPPING
US	6,642,102		09/896,530	BARRIER MATERIAL ENCAPSULATION OF PROGRAMMABLE MATERIAL
US	6,643,161		10/282,534	WRITE-ONCE POLYMER MEMORY WITH E-BEAM WRITING AND READING
US	6,643,367		09/301,855	DYNAMIC AND SCHEDULED COMPUTER TELEPHONY RESOURCE ALLOCATION
US	6,646,991		09/470,189	MULTI-LINK EXTENSIONS AND BUNDLE SKEW MANAGEMENT

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US	6,647,455		09/893,779	ON-DIE CACHE MEMORY WITH REPEATERS
US	6,647,545		09/503,879	METHOD AND APPARATUS FOR BRANCH TRACE MESSAGE SCHEME
US	6,650,802		09/470,574	METHOD AND APPARATUS FOR SWITCHING AN OPTICAL BEAM
US	6,650,823		09/741,520	METHOD OF CREATING A PHOTONIC VIA USING FIBER OPTIC
US	6,654,369		09/322,152	METHOD FOR DIRECTING THE ROUTE OF A CELL TRANSMITTING A NETWORK
US	6,655,022		09/160,535	IMPLEMENTING MICRO BGA ASSEMBLY TECHNIQUES FOR SMALL DIE
US	6,661,264	TNT	09/967,180	RELEASING FUNCTIONAL BLOCKS IN RESPONSE TO A DETERMINATION OF A SUPPLY VOLTAGE PREDETERMINED LEVEL AND A LOGIC PREDETERMINED INITIAL STATE
US	6,662,200		09/754,684	MULTIPLIERLESS PYRAMID FILTER
US	6,662,271		09/894,638	CACHE ARCHITECTURE WITH REDUNDANT SUB ARRAY
US	6,665,792		09/475,029	INTERFACE TO A MEMORY SYSTEM FOR A PROCESSOR HAVING A REPLAY SYSTEM
US	6,668,298		09/474,750	SHIFTING AN INPUT SIGNAL FROM A HIGH-SPEED DOMAIN TO A LOWER-SPEED DOMAIN
US	6,671,172	WWN	09/950,100	ELECTRONIC ASSEMBLIES WITH HIGH CAPACITY CURVED FIN HEAT SINKS
US	6,671,771		09/468,477	HASH CAM HAVING A REDUCED WIDTH COMPARISON CIRCUITRY AND ITS APPLICATION
US	6,671,847		09/709,000	I/O DEVICE TESTING METHOD AND APPARATUS
US	6,672,891	2003-0064617	09/967,060	ZERO INSERTION FORCE CONNECTOR FOR SUBSTRATES WITH EDGE CONTACTS
US	6,674,115	TNT	10/309,633	MULTIPLE LAYER PHRASE-CHANGE MEMORY
US	6,675,057	WWN	09/842,389	INTEGRATED CIRCUIT ANNEALING METHODS AND APPARATUS
US	6,683,509	US 2003/0048145 A1	10/223,869	VOLTAGE CONTROLLED OSCILLATORS
US	6,683,884		09/541,048	SHARED CREDIT ROUND ROBIN QUEUING
US	6,686,793		10/273,689	GATE ENHANCED TRI-CHANNEL POSITIVE CHARGE PUMP
US	6,687,840		09/557,099	MULTI-LINK EXTENSIONS AND BUNDLE SKEW MANAGEMENT
US	6,689,057		09/773,174	METHOD AND APPARATUS FOR COMPRESSING CALORIE BURN CALCULATION DATA USING POLYNOMIAL COEFFICIENTS

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US	6,694,076		09/822,380	METHOD FOR CENTERING A CORE OF A WAVEGUIDE AMPLIFIER
US	6,699,798	US-2003-0203647-A1	10/131,017	PROMOTING ADHESION OF FLUOROPOLYMER FILMS TO SEMICONDUCTOR SUBSTRATES
US	6,700,209		09/474,746	PARTIAL UNDERFILL FOR FLIP-CHIP ELECTRONIC PACKAGES
US	6,703,299	JNG	10/032,115	UNDERFILL PROCESS FOR FLIP-CHIP DEVICE
US	6,707,712		10/458,828	METHOD FOR READING A STRUCTURAL PHASE-CHANGE MEMORY
US	6,707,970		09/738,799	ALIGNMENT OF FIBER OPTIC BUNDLE TO ARRAY WAVEGUIDE USING AN EPOXY
US	6,710,845		09/752,938	PURGING GAS FROM A PHOTOLITHOGRAPHY ENCLOSURE BETWEEN A MASK PROTECTIVE DEVICE AND A PATTERNED MASK
US	6,717,855		10/318,464	METHOD AND APPARATUS FOR ALLOWING CONTINUOUS APPLICATION OF HIGH VOLTAGE TO A FLASH MEMORY DEVICE POWER PIN
US	6,719,920		10/002,855	SLURRY FOR POLISHING A BARRIER LAYER
US	6,723,167		09/746,435	SPINDLE SLEEVE FOR COATER/DEVELOPER
US	6,724,442		09/277,637	OPTICALLY SWITCHABLE INFRARED DETECTOR
US	6,724,767		09/271,061	TWO-DIMENSIONAL QUEUING/DE-QUEUING METHODS AND SYSTEMS FOR IMPLEMENTING THE SAME
US	6,724,814		09/598,934	PAD AND CODEC DETECTION
US	6,728,249		09/344,608	SYSTEM AND METHOD FOR PERFORMING CUT-THROUGH FORWARDING IN AN ATM NETWORK SUPPORTING LAN EMULATION
US	6,734,118		10/252,295	DIELECTRIC MATERIAL TREATMENT
US	6,734,443		09/850,766	APPARATUS AND METHOD FOR REMOVING PHOTOMASK CONTAMINATION AND CONTROLLING ELECTROSTATIC DISCHARGE
US	6,741,978		09/547,624	ACCESSING FILE DATA STORED IN NON-VOLATILE RE-PROGRAMMABLE SEMICONDUCTOR MEMORIES
US	6,744,671		09/752,550	KICKER FOR NON-VOLATILE MEMORY DRAIN BIAS
US	6,747,598		10/417,540	METHOD AND APPARATUS FOR CONTROLLING ACCESS TO MOBILE DEVICES
US	6,748,118		09/507,399	METHOD OF QUANTIZING SIGNAL SAMPLES OF AN IMAGE DURING SAME
US	6,748,513		09/665,922	METHOD AND APPARATUS FOR A LOW LATENCY SOURCE-SYNCHRONOUS ADDRESS RECEIVER FOR A HOST SYSTEM BUS IN A MEMORY CONTROLLER

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US	6,751,640		09/718,877	METHOD AND APPARATUS FOR MULTIPLY-ACCUMULATE TWO-DIMENSIONAL SEPARABLE SYMMETRIC FILTERING
US	6,751,837	us-220-0051343-A1	10/025,434	METHOD OF HEAT EXTRACTION FROM AN INTEGRATED CIRCUIT DIE
US	6,754,407		10/158,250	FLIP-CHIP PACKAGE INTEGRATING OPTICAL AND ELECTRICAL DEVICES AND COUPLING TO A WAVEGUIDE ON A BOARD
US	6,754,764		09/468,965	METHOD AND APPARATUS FOR MAINTAINING ORDER IN A PIPELINED PROCESS AND ITS APPLICATION
US	6,759,646		09/199,836	COLOR INTERPOLATION FOR A FOUR COLOR MOSAIC PATTERN
US	6,765,681		10/119,501	MEASURING OPTICAL PHASE
US	6,766,286		09/820,108	PYRAMID FILTER
US	6,768,665		10/212,630	REFRESHING MEMORY CELLS OF A PHASE CHANGE MATERIAL MEMORY DEVICE
US	6,770,531		09/896,008	ADHESIVE MATERIAL FOR PROGRAMMABLE DEVICE
US	6,772,366		09/802,451	METHOD AND APPARATUS FOR DETECTING AC REMOVAL
US	6,776,493		10/126,106	TUNABLE OPTICAL DISPERSION COMPENSATOR
US	6,777,970	VVT	09/838,730	AC TESTING OF LEAKAGE CURRENT IN INTEGRATED CIRCUITS USING RC TIME CONSTANT
US	6,778,548		09/603,957	DEVICE TO RECEIVE, BUFFER, AND TRANSMIT PACKETS OF DATA IN A PACKET SWITCHING NETWORK
US	6,779,089		10/042,905	LOCKED CONTENT ADDRESSABLE MEMORY FOR EFFICIENT ACCESS
US	6,784,004		10/662,021	METHOD OF DETERMINING POST-ETCH OFFSET IN EXPOSED-TO-EMBEDDED OVERLAY
US	6,787,443		10/442,834	PCB DESIGN AND METHOD FOR PROVIDING VENTED BLIND VIAS
US	6,791,414	2003/0206055	10/424,899	SIGNAL PROCESSING STAGE AND RADIO FREQUENCY TUNER
US	6,792,102		09/750,030	MATCHING ROUTED CALL TO AGENT WORKSTATION
US	6,792,179		10/334,749	OPTICAL THUMBTACK
US	6,797,979		10/418,530	METAL STRUCTURE FOR A PHASE-CHANGE MEMORY DEVICE
US	6,798,901		09/411,697	METHOD OF COMPRESSING A COLOR IMAGE
US	6,801,143		10/186,564	A METHOD AND APPARATUS FOR GENERATING GRAY CODE FOR ANY EVEN COUNT VALUE TO ENABLE EFFICIENT POINTER EXCHANGE MECHANISMS IN ASYNCHRONOUS FIFO'S

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US	6,801,436		09/964,747	EXTENSION MECHANISM AND METHOD FOR ASSEMBLING OVERHANGING COMPONENTS
US	6,807,600	US-2004-0019707-A1	10/205,546	METHOD, SYSTEM, AND PROGRAM FOR MEMORY BASED DATA TRANSFER
US	6,810,443		10/335,049	OPTICAL STORAGE TRANSFER PERFORMANCE
US	6,826,100		10/404,405	PUSH BUTTON MODE AUTOMATIC PATTERN SWITCHING FOR INTERCONNECT BUILT-IN SELF TEST
US	6,828,512		10/267,158	APPARATUS AND METHODS FOR INTERCONNECTING COMPONENTS TO VIA-IN-PAD INTERCONNECTS
US	6,830,470	US-2004-0259405-A1	10/600,668	ELECTRICAL DEVICE CONNECTOR
US	6,831,862		10/330,469	METHOD AND APPARATUS FOR MATCHED-REFERENCE SENSING ARCHITECTURE FOR NON-VOLATILE MEMORIES
US	6,832,268		10/324,863	MECHANISM TO GUARANTEE FORWARD PROGRESS FOR INCOMING COHERENT INPUT/OUTPUT (I/O) TRANSACTIONS FOR CACHING I/O AGENT ON ADDRESS CONFLICT WITH PROCESSOR TRANSACTIONS
US	6,836,176	US-2003-0122610-A1	10/185,419	CHARGE PUMP RIPPLE REDUCTION
US	6,842,452		09/712,185	METHOD FOR SWITCHING DATA STREAMS
US	6,844,738		10/007,672	COAXIAL RADIO FREQUENCY ADAPTER AND METHOD
US	6,846,737		09/639,625	PLASMA-INDUCED DEPLETION OF FLUORINE FROM SURFACES OF FLUORINATED LOW-K DIELECTRIC MATERIALS
US	6,851,027	2003-0056074	09/953,356	MEMORY SYSTEM ORGANIZED INTO BLOCKS OF DIFFERENT SIZES AND ALLOCATION METHOD THEREFOR
US	6,853,720		09/967,367	SOFTWARE CALL CONTROL AGENT
US	6,853,723		09/417,161	HIGH IMPEDANCE POLARITY DETECTOR
US	6,856,733	JEG	10/008,922	1 X N FANOUT WAVEGUIDE PHOTODETECTOR
US	6,861,267	US-2003-0052351-A1	09/953,833	FORMATION OF SHUNT-LAYER FREE OVONIC UNIFIED MEMORY (OUM) DEVICES
US	6,861,917	US-2004-0233000-A1	10/444,311	OSCILLATOR SYSTEM WITH SWITCHED-CAPACITOR NETWORK AND METHOD FOR GENERATING A PRECISION TIME REFERENCE
US	6,862,341		09/834,713	DEVICE AND METHOD OF INTERFACING VOICE DATA BETWEEN A SWITCH AND A COMPUTER SYSTEM
US	6,862,714	US-2003-0200514-A1	10/126,402	ACCURATELY TUNING RESISTORS
US	6,863,564		10/645,229	COAXIAL RADIO FREQUENCY ADAPTER AND METHOD

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US	6,865,344		09/712,822	CODE-SWITCHED OPTICAL NETWORK
US	6,868,071		09/714,382	SYSTEM AND METHOD OF TRANSMITTING DATA FRAMES IN A MESH OF DATA SWITCHES
US	6,873,380	US-2003-0011303-A1	09/904,268	PROVIDING OPTICAL ELEMENTS OVER EMISSIVE DISPLAYS
US	6,876,843	US 2002/0137486 A1	10/056,155	RADIO FREQUENCY AMPLIFIER WITH IMPROVED INTERMODULATION PERFORMANCE
US	6,877,060		09/933,547	DYNAMIC DELAYED TRANSACTION BUFFER CONFIGURATION BASED ON BUS FREQUENCY
US	6,886,989		09/738,686	ALIGNMENT OF FIBER OPTIC BUNDLE TO ARRAY WAVEGUIDE USING PINS
US	6,889,237		09/823,212	TWO-DIMENSIONAL PYRAMID FILTER ARCHITECTURE
US	6,891,889		09/947,331	SIGNAL TO NOISE RATIO OPTIMIZATION FOR VIDEO COMPRESSION BIT-RATE CONTROL
US	6,894,801		10/199,382	RECOVERY OF BIT-ROTATED FRAMES DURING FACSIMILE TRANSMISSIONS IN A GLOBAL SYSTEM FOR MOBILE COMMUNICATIONS (GSM) NETWORK
US	6,898,852	US-2004-0043662-A1	10/647,396	CONNECTOR ASSEMBLY WITH DECOUPLING CAPACITORS
US	6,904,201		10/142,329	PHASE-CONTROLLED FIBER BRAGG GRATINGS AND MANUFACTURING METHODS
US	6,904,482		10/086,410	A COMMON BOOT ENVIRONMENT FOR A MODULAR SERVER SYSTEM
US	6,904,504		09/991,128	METHOD AND APPARATUS FOR SOFTWARE SELECTION OF PROTECTED REGISTER SETTINGS
US	6,905,397		10/213,776	APPARATUS FOR ENHANCED RATE CHEMICAL MECHANICAL POLISHING WITH ADJUSTABLE SELECTIVITY
US	6,908,812	US-2003-0201469-A1	10/426,380	PHASE CHANGE MATERIAL MEMORY DEVICE
US	6,909,645	US-2004-0013007-A1	10/196,401	CLUSTER BASED REDUNDANCY SCHEME FOR SEMICONDUCTOR MEMORIES
US	6,915,407		10/813,145	METHOD AND APPARATUS FOR A LOW LATENCY SOURCE-SYNCHRONOUS ADDRESS RECEIVER FOR A HOST SYSTEM BUS IN A MEMORY CONTROLLER
US	6,915,522		10/055,528	SYSTEM AND METHOD TO SYNCHRONIZE TWO OR MORE OBJECT MANAGEMENT SYSTEMS
US	6,917,381	US-2002-0063789-A1	09/727,038	COLOR FILTER ARRAY AND COLOR INTERPOLATION ALGORITHM
US	6,917,524	US-2005-0014419-A1	10/918,081	EXTENSION MECHANISM AND METHOD FOR ASSEMBLING OVERHANGING COMPONENTS
US	6,927,346	US-2004-0118606-A1	10/326,901	SURFACE MOUNT TECHNOLOGY TO VIA-IN-PAD INTERCONNECTIONS

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US	6,927,497	US-2004-0036163-A1	10/226,070	MULTI-DIE SEMICONDUCTOR PACKAGE
US	6,928,200	SWL	10/265,873	ULTRA-THIN POLARIZATION MODE CONVERTERS BASED ON LIQUID CRYSTAL MATERIALS
US	6,928,216		10/672,329	MARKINGS FOR ALIGNING FIBER OPTIC BUNDLE
US	6,931,121		09/362,425	DUAL PERSONALITY ANALOG PORT
US	6,931,151		09/991,629	METHOD AND APPARATUS FOR MODIFYING GRAPHICS CONTENT PRIOR TO DISPLAY FOR COLOR BLIND USE
US	6,933,944		10/104,042	DYNAMIC COMPUTATION OF CHIPSET-SUPPORTED ACCELERATED GRAPHICS PORT APERTURE SIZES
US	6,934,953		09/997,669	DEFERRED PROCEDURE CALL IN INTERFACE DESCRIPITON LANGUAGE
US	6,937,794		10/409,287	USING A TRANSVERSAL FILTER TO COMPENSATE FOR DISPERSION
US	6,937,948	US-2003-0093233-A1	09/993,336	FLASH MEMORY PROGRAM AND ERASE OPERATIONS
US	6,950,952		10/211,465	DYNAMIC POWER LEVEL CONTROL BASED ON A BOARD LATCH STATE
US	6,952,122	US-2003-0062933-A1	09/966,481	GENERATING PULSES FOR RESETTING INTEGRATED CIRCUITS
US	6,952,764		10/039,588	STOPPING REPLAY TORNADOES
US	6,958,450		10/405,098	CONNECTION APPARATUS, SYSTEMS, AND METHODS
US	6,961,472		09/507,213	METHOD OF INVERSE QUANTIZING QUANTIZED SIGNAL SAMPLES OF AN IMAGE DURING IMAGE DECOMPRESSION
US	6,967,496	US-2004-0246017-A1	10/889,417	AC TESTING OF LEAKAGE CURRENT IN INTEGRATED CIRCUITS USING RC TIME CONSTANT
US	6,975,720		09/523,935	METHOD OF PROCESSING AN INBOUND CALL IN A CALL CENTER
US	6,976,172		09/752,882	SYSTEM AND METHOD FOR PROTECTED MESSAGING
US	6,982,988		10/044,766	PROGRAMMABLE FRAME SPLITTER
US	6,998,289	US-2003-0071289-A1	10/302,421	MULTIPLE LAYER PHASE-CHANGE MEMORY
US	7,000,109		10/002,541	METHOD AND APPARATUS FOR UNLOCKING A COMPUTER SYSTEM HARD DRIVE
US	7,000,434		09/741,237	METHOD OF CREATING AN ANGLED WAVEGUIDE USING LITHOGRAPHIC TECHNIQUES
US	7,002,873	2005-0135178	10/739,268	MEMORY ARRAY WITH STAGED OUTPUT
US	7,003,059		09/500,524	JABBER COUNTER MECHANISM FOR ELASTIC BUFFER OPERATION

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US	7,007,304		09/665,826	METHOD AND APPARATUS TO IMPROVE THE PROTECTION OF INFORMATION PRESENTED BY A COMPUTER
US	7,010,780		09/953,277	METHOD AND SYSTEM FOR SOFTWARE MODULARIZATION AND AUTOMATIC CODE GENERATION FOR EMBEDDED SYSTEMS
US	7,013,120		10/043,746	WALKING WEAVER IMAGE REJECT MIXER FOR RADIO
US	7,017,062		09/751,601	METHOD AND APPARATUS FOR RECOVERING FROM AN OVERHEATED MICROPROCESSOR
US	7,024,575		10/294,271	APPARATUS AND METHOD FOR TIME SYNCHRONIZATION OF A PLURALITY OF MULTIMEDIA STREAMS
US	7,029,978	US-2005-0032319-A1	10/633,869	CONTROLLING THE LOCATION OF CONDUCTION BREAKDOWN IN PHASE CHANGE MEMORIES
US	7,031,881	US-2005-0137831-A1	10/742,218	METHOD, SYSTEM, AND ARTICLE OF MANUFACTURE FOR RUNNING DIAGNOSTICS RELATED TO A DEVICE
US	7,032,149	US-2004-0243898-A1	10/449,332	APPARATUS AND METHOD FOR ADAPTING A LEVEL SENSITIVE DEVICE TO PRODUCE EDGE-TRIGGERED BEHAVIOR
US	7,036,071	AMM	10/214,630	PRACTICAL CODING AND METRIC CALCULATION FOR THE LATTICE INTERFERED CHANNEL
US	7,045,408	US-2004-0235236-A1	10/443,152	AN INTEGRATED CIRCUIT WITH IMPROVED CHANNEL STRESS PROPERTIES AND A METHOD FOR MAKING IT
US	7,047,458		10/319,517	TESTING METHODOLOGY AND APPARATUS FOR INTERCONNECTS
US	7,048,073	WWN	10/655,822	FASTENER INSTALLATION TOOL AND METHODS OF USE
US	7,049,704		10/840,017	A FLIP-CHIP PACKAGE INTEGRATING OPTICAL AND ELECTRICAL DEVICES AND COUPLING TO A WAVEGUIDE ON A BOARD
US	7,050,063		09/502,994	3D RENDERING TEXTURE CACHING SCHEME
US	7,064,344	US-2003-0205809-A1	10/418,548	BARRIER MATERIAL ENCAPSULATION OF PROGRAMMABLE MATERIAL
US	7,065,298		09/454,164	CODE-BASED OPTICAL NETWORKS, METHODS AND APPARATUS
US	7,072,352		10/080,093	INVERSE MULTIPLEXING OF UNMANAGED TRAFFIC FLOWS OVER A MULTI-STAR INFINIBAND NETWORK
US	7,073,070		09/895,738	METHOD AND APPARATUS TO IMPROVE THE PROTECTION OF INFORMATION PRESENTED BY A COMPUTER
US	7,080,236		10/262,214	A STACK-POINTER UPDATE TECHNIQUE

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US	7,089,409	2004-0083351	10/690,634	INTERFACE TO A MEMORY SYSTEM FOR A PROCESSOR HAVING A REPLAY SYSTEM
US	7,091,108	US-2005-0059221-A1	10/661,738	METHODS AND APPARATUSES FOR MANUFACTURING ULTRA THIN DEVICE LAYERS FOR INTEGRATED CIRCUIT DEVICES
US	7,093,124		10/002,337	A MECHANISM TO IMPROVE AUTHENTICATION FOR REMOTE MANAGEMENT OF A COMPUTER SYSTEM
US	7,099,180	US-2006-0181922-A1	11/058,797	RESETTING PHASE CHANGE MEMORY BITS
US	7,105,408	US-2006-0073655-A1	10/948,884	PHASE CHANGE MEMORY WITH A SELECT DEVICE HAVING A BREAKDOWN LAYER
US	7,107,202		09/495,150	METHOD AND APPARATUS FOR HARDWARE AND SOFTWARE CO-SIMULATION
US	7,111,103		10/104,341	METHOD AND APPARATUS FOR GENERATING TRAFFIC IN AN ELECTRONIC BRIDGE VIA A LOCAL CONTROLLER
US	7,112,970	US-2004-0239334-A1	10/820,693	COAXIAL RADIO FREQUENCY ADAPTER AND METHOD
US	7,120,904		09/552,292	DATA-FLOW METHOD FOR OPTIMIZING EXCEPTION-HANDLING INSTRUCTIONS IN PROGRAMS
US	7,122,391		10/659,898	WAFER-LEVEL TEST STRUCTURE FOR EDGE-EMITTING SEMICONDUCTOR LASERS
US	7,123,265		09/741,599	METHOD & APPARATUS FOR ADDING REAL-TIME PRIMITIVES
US	7,123,712		09/277,286	COMPUTER TELEPHONY SERVER WITH IMPROVED FLEXIBILITY
US	7,124,412		09/737,140	EXTENSIBLE BIOS ERROR LOG
US	7,125,762	US-2006-0024892-A1	10/900,666	COMPENSATING THE WORKFUNCTION OF A METAL GATE TRANSISTOR FOR ABSTRACTION BY THE GATE DIELECTRIC LAYER
US	7,133,585	US-2006-0198597-A1	11/410,591	METHOD TO REALIZE FAST SILICON-ON-INSULATOR (SOI) OPTICAL DEVICE
US	7,133,586	US-2006-0198572-A1	11/411,059	METHOD TO REALIZE FAST SILICON-ON-INSULATOR (SOI) OPTICAL DEVICE
US	7,135,696	US-2006-0073631-A1	10/949,090	PHASE CHANGE MEMORY WITH DAMASCENE MEMORY ELEMENT
US	7,139,842		09/823,215	METHOD AND APPARATUS FOR INTERSYSTEM CUT/COPY AND PASTE
US	7,140,023	US-2005-0097295-A1	10/699,638	SYMBOLIC BUFFER ALLOCATION IN LOCAL CACHE AT A NETWORK PROCESSING ELEMENT
US	7,141,454	US-2004-0266068-A1	10/731,177	WIRE-BONDED PACKAGE WITH ELECTRICALLY INSULATING WIRE ENCAPSULANT AND THERMALLY CONDUCTIVE OVERMOLD

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US	7,143,279	US-2004-0243798-A1	10/448,696	DYNAMIC BIOS EXECUTION AND CONCURRENT UPDATE FOR A BLADE SERVER
US	7,145,481	US-2005-0068203-A1	10/676,888	METHOD AND APPARATUS FOR TRUSTED KEYBOARD SCANNING
US	7,154,175	US-2005-0280138-A1	10/873,817	GROUND PLANE FOR INTEGRATED CIRCUIT PACKAGE
US	7,154,853		10/137,753	RATE POLICING ALGORITHM FOR PACKET FLOWS
US	7,155,370		10/393,223	REUSABLE, BUILT-IN SELF-TEST METHODOLOGY FOR COMPUTER SYSTEMS
US	7,155,599	2002-0087836	09/750,095	RECOVERY SCHEMES FOR REGISTER RENAMING STRUCTURES IN THE PRESENCE OF EXCEPTIONS
US	7,155,615		09/608,117	METHOD AND APPARATUS FOR PROVIDING A SECURE-PRIVATE PARTITION ON A HARD DISK DRIVE OF A COMPUTER SYSTEM VIA IDE CONTROLLER
US	7,158,631		10/284,724	EFFICIENT ECHO CANCELLATION TECHNIQUES
US	7,159,154		10/614,215	A TECHNIQUE FOR SYNCHRONIZING FAULTS IN A PROCESS HAVING A REPLAY SYSTEM
US	7,160,127	US-2004-0183558-A1	10/391,893	A VARIABLE LATCH
US	7,161,225	US-2005-0136557-A1	11/038,336	FORMATION OF SHUNT-LAYER FREE OVONIC UNIFIED MEMORY (OUM) DEVICES
US	7,161,908	US-2004-0062253-A1	10/256,475	DETERMINISTIC BANDWIDTH THROTTLING TO FACILITATE OPERATION OF A CONTROL UNIT
US	7,161,999	US-2003-0123588-A1	10/038,956	SYNCHRONIZING DATA OR SIGNAL TRANSFER ACROSS CLOCKED LOGIC DOMAINS
US	7,162,028		09/996,255	UNIVERSAL TELEPHONY INTERFACE POLARITY DETECTOR
US	7,162,564		10/190,851	CONFIGURABLE MULTI-PORT MULTI-PROTOCOL NETWORK INTERFACE TO SUPPORT PACKET PROCESSING
US	7,162,614	US-2004-0268092 A1	10/608,121	ELIMINATION OF POTENTIAL RENAMING STALLS DUE TO USE OF PARTIAL REGISTERS
US	7,168,074		09/675,286	RUNTIME PREDICTION FRAMEWORK FOR CPU INTENSIVE APPLICATIONS
US	7,171,545		10/747,625	PREDICTIVE FILTERING OF REGISTER CACHE ENTRY
US	7,173,817	US-2005-0068722-A1	10/748,385	FRONT SIDE HOT-SWAP CHASSIS MANAGEMENT MODULE
US	7,174,060	US-2006-0018585-A1	11/189,543	ULTRA-THIN POLARIZATION MODE CONVERTERS BASED ON LIQUID CRYSTAL MATERIALS
US	7,176,122	US-2004-0175925-A1	10/379,061	DIELECTRIC WITH SIDEWALL PASSIVATING LAYER
US	7,177,502	US-2005-0232543-A1	11/151,010	HEATING OPTICAL DEVICES
US	7,180,429		10/076,817	SLOW MOTION DETECTION SYSTEM

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US	7,180,523		09/539,343	TRIMMING SURFACES
US	7,180,929		10/126,348	WAFER-LEVEL TEST STRUCTURE FOR EDGE-EMITTING SEMICONDUCTOR LASERS
US	7,181,601	US-2005-0125645-A1	10/731,567	METHOD AND APPARATUS FOR PREDICTION FOR FORK AND JOIN INSTRUCTIONS IN SPECULATIVE EXECUTION
US	7,183,500	US-2006-0000353-A1	10/883,610	ELECTROMAGNETIC INTERFERENCE (EMI) FILTER WITH PASSIVE NOISE CANCELLATION
US	7,184,050	US-2005-0237331-A1	11/172,342	DYNAMIC COMPUTATION OF CHIPSET-SUPPORTED ACCELERATED GRAPHICS PORT APERTURE SIZES
US	7,184,536		09/967,108	INTELLIGENT FORWARDED TELEPHONE CALL HANDLING WITH A CALL ANSWERING SYSTEM
US	7,185,253	US-2003-0188269-A1	10/107,628	COMPACTING CIRCUIT RESPONSES
US	7,193,965		09/565,215	MULTI-WIRELESS NETWORK CONFIGURABLE BEHAVIOR
US	7,194,182		10/304,195	METHODS AND APPARATUSES USING A FIBER-FLEXURE INDUCTION SOLDERING STATION
US	7,194,559		10/231,863	SLAVE I/O DRIVER CALIBRATION USING ERROR-NULLING MASTER REFERENCE
US	7,197,174		09/396,407	MAGNETIC INK ENCODING PEN
US	7,197,498	US-2004-0267772-A1	10/609,954	APPARATUS, SYSTEM AND METHOD FOR UPDATING A SORTED LIST
US	7,197,659		09/965,223	GLOBAL I/O TIMING ADJUSTMENT USING CALIBRATED DELAY ELEMENTS
US	7,200,060	US-2005-0013190-A1	10/620,469	A MEMORY DRIVER ARCHITECTURE AND ASSOCIATED METHODS
US	7,203,631	US-2004-0049371-A1	10/334,113	SYSTEM AND METHOD TO ANALYZE VLSI DESIGNS
US	7,203,767	US-2006-0168311-A1	11/351,991	CONSOLE REDIRECTION AMONG LINKED COMPUTERS
US	7,203,825		09/970,485	SHARING INFORMATION TO REDUCE REDUNDANCY IN HYBRID BRANCH PREDICTION
US	7,205,074		10/334,841	VENTING OF PELLICLE CAVITY FOR A MASK
US	7,205,562		10/318,984	PHASE CHANGE MEMORY AND METHOD THEREFOR
US	7,206,865		10/402,125	APPARATUS AND METHOD FOR COMBINING WRITES TO I/O
US	7,206,955		10/745,903	BUNDLE SKEW MANAGEMENT AND CELL SYNCHRONIZATION
US	7,207,039	US-2005-0149924-A1	10/746,975	SECURE BOOTING AND PROVISIONING
US	7,210,079	US-2006-0123275-A1	11/321,012	APPARATUS AND METHOD FOR ADAPTING A LEVEL SENSITIVE DEVICE TO PRODUCE EDGE-TRIGGERED BEHAVIOR
US	7,211,501		10/319,310	METHOD AND APPARATUS FOR LASER ANNEALING

US	7,212,021		10/097,136	MANUFACTURING INTEGRATED CIRCUITS AND TESTING ON-DIE POWER SUPPLIES USING DISTRIBUTED PROGRAMMABLE DIGITAL CURRENT SINKS
US	7,212,497		09/741,405	METHOD AND DRIVER FOR DETECTING GLITCHES
US	7,213,142		10/421,287	SYSTEM AND METHOD TO INITIALIZE REGISTERS WITH AN EEPROM STORED BOOT SEQUENCE
US	7,215,173	US-2006-0170481-A1	11/047,442	A LOW-SWING LEVEL SHIFTER
US	7,215,383	US-2004-0183954-A1	10/767,324	COHERENT LIGHT DESPECKLING
US	7,216,140		09/676,556	EFFICIENT IMPLEMENTATION OF N-POINT DCT, N-POINT IDCT, SA-DCT AND SA-IDCT ALGORITHMS
US	7,216,201		11/327,454	PARALLEL CACHELETS
US	7,218,491	DJP1	10/329,058	ELECTROSTATIC DISCHARGE PROTECTION UNIT INCLUDING EQUALIZATION
US	7,223,660	US-2004-0023418-A1	10/210,866	FLASH ASSISTED ANNEALING
US	7,223,701	US-2004-0048485-A1	10/236,203	IN-SITU SEQUENTIAL HIGH DENSITY PLASMA DEPOSITION AND ETCH PROCESSING FOR GAP FILL
US	7,231,083		09/430,282	CONTROLLING PROCESSOR-BASED SYSTEMS USING A DIGITAL CAMERA
US	7,231,468	US-2005-0033869-A1	10/456,185	FUTURE ACTIVITY LIST FOR PERIPHERAL BUS HOST CONTROLLER
US	7,231,552		10/280,458	METHOD AND APPARATUS FOR INDEPENDENT CONTROL OF DEVICES UNDER TEST CONNECTED IN PARALLEL
US	7,233,725	US-2005-0145783-A1	11/042,537	1 X N FANOUT WAVEGUIDE PHOTODETECTOR
US	7,236,059		11/172,133	APPARATUS, SYSTEM, AND METHOD FOR OSCILLATOR NETWORK WITH MUTLIPLE PARALLEL OSCILLATOR CIRCUITS
US	7,237,102		10/283,920	METHODS AND APPARATUS FOR CONFIGURING HARDWARE RESOURCES IN A PRE-BOOT ENVIRONMENT WITHOUT REQUIRING A SYSTEM RESET
US	7,239,999	2004-0019491	10/200,328	SPEED CONTROL PLAYBACK OF PARAMETRIC SPEECH ENCODED DIGITAL AUDIO
US	7,240,247		10/133,625	PROVIDING A CHAIN OF TOKENIZED ERROR AND STATE INFORMATION FOR A CALL STACK
US	7,240,260		10/317,605	STIMULUS GENERATION
US	7,240,342		09/608,616	USER TRANSPARENT CONTINUOUS COMPILATION
US	7,242,760		09/750,025	AUTOMATIC DETECTING WHEN AN AGENT IS AVAILABLE

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US	7,245,945		10/289,081	PORTABLE COMPUTING DEVICE ADAPTED TO UPDATE DISPLAY INFORMATION WHILE IN A LOW POWER MODE
US	7,246,135	US-2002-0091867-A1	09/756,579	SHARING CLASSES BETWEEN PROGRAMS
US	7,248,475	US-2006-0268534-A1	11/140,769	WIRELESS DEVICE ENCLOSURE USING PIEZOELECTRIC COOLING STRUCTURES
US	7,249,230	US-2005-0289305-A1	10/874,998	QUEUE STRUCTURE WITH VALIDITY VECTOR AND ORDER ARRAY
US	7,251,880	AMM	09/964,746	METHOD AND STRUCTURE FOR IDENTIFYING LEAD-FREE SOLDER
US	7,256,872		10/759,641	PURGING GAS FROM A PHOTOLITHOGRAPHY ENCLOSURE BETWEEN A MASK PROTECTIVE DEVICE AND A PATTERNED MASK
US	7,257,538		10/266,226	GENERATING ANIMATION FROM VISUAL AND AUDIO INPUT
US	7,259,023	US-2006-0054991-A1	10/939,145	FORMING PHASE CHANGE MEMORY ARRAYS
US	7,259,982	US-2006-0146600-A1	11/029,981	READING PHASE CHANGE MEMORIES TO REDUCE READ DISTURBS
US	7,260,661	US-2006-0050694-A1	10/934,640	PROCESSING REPLIES TO REQUEST PACKETS IN AN ADVANCED SWITCHING CONTEXT
US	7,270,056	Us-2006-0042482	10/930,251	PRINT STRIPPER FOR ESD CONTROL
US	7,271,403	US-2004-0113154-A1	10/319,183	ISOLATING PHASE CHANGE MEMORY DEVICES
US	7,271,673	US-2007-0001775-A1	11/171,860	VOLTAGE CONTROLLED OSCILLATOR (VCO) TUNING
US	7,272,211		10/038,917	PROPERTY MANAGEMENT SYSTEM PROTOCOL AUTO-DETECTION
US	7,272,623	2003-0191787-A1	10/118,349	METHODS AND APPARATUS FOR DETERMINING A FLOATING-POINT EXPONENT ASSOCIATED WITH AN UNDERFLOW CONDITION OR AN OVERFLOW CONDITION
US	7,272,701	US-2005-0091475-A1	10/692,436	METHOD AND APPARATUS FOR LIMITING PORTS IN A REGISTER ALIAS TABLE HAVING HIGH-BANDWIDTH AND LOW-BANDWIDTH STRUCTURES
US	7,275,254		09/717,579	METHOD AND APPARATUS FOR DETERMINING AND DISPLAYING THE SERVICE LEVEL OF A DIGITAL TELEVISION BROADCAST SIGNAL
US	7,275,312	US-2004-0261262-A1	10/611,215	APPARATUS FOR PRECISE ALIGNMENT OF PACKAGING CAPS ON A SUBSTRATE
US	7,277,066	US-2003-0011724-A1	09/906,342	REPAIRABLE TILED DISPLAYS
US	7,282,730	US-2006-0157689-A1	11/037,850	FORMING A CARBON LAYER BETWEEN PHASE CHANGE LAYERS OF A PHASE CHANGE MEMORY

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US	7,289,382	US-2005-0135170-A1	10/744,664	REWRITABLE FUSE MEMORY
US	7,289,455	US-2005-0025055-A1	10/628,997	NETWORK STATISTICS
US	7,289,945	US-2004-0082230-A1	10/281,857	ANALYZING INTERCONNECT STRUCTURES
US	7,296,060	2002-0107924	09/220,910	SYSTEM AND METHOD FOR AUTOMATICALLY IDENTIFYING AND ATTACHING RELATED DOCUMENTS
US	7,299,425	US-2004-0268273-A1	10/606,868	METHOD AND APPARATUS TO CREATE BYPASS LOGIC IN A DIGITAL CIRCUIT DESIGN
US	7,299,433	US-2004-0250224-A1	10/458,537	TIMING ANALYSIS APPARATUS, SYSTEMS, AND METHODS
US	7,302,652		10/404,937	LEAKAGE CONTROL IN INTEGRATED CIRCUITS
US	7,302,756	US-2004-0262039-A1	10/612,281	BOND FINGER ON VIA SUBSTRATE, PROCESS OF MAKING SAME, PACKAGE MADE THEREBY, AND METHOD OF ASSEMBLING SAME
US	7,304,373	US-2006-0091508-A1	10/977,908	IMPROVED POWER DISTRIBUTION WITHIN A FOLDED FLEX PACKAGE METHOD AND APPARATUS
US	7,307,295	US-2005-0130363-A1	11/049,524	A METHOD AND AN APPARATUS FOR A HARD-CODED BIT VALUE CHANGEABLE IN ANY LAYER OF METAL
US	7,308,470	US-2005-0125478-A1	10/728,395	SMALLER AND LOWER POWER STATIC MUX CIRCUITRY IN GENERATING MULTIPLIER PARTIAL PRODUCT SIGNALS
US	7,308,563		09/968,278	DUAL-TARGET BLOCK REGISTER ALLOCATION
US	7,310,790		10/309,529	AUTOMATIC SYMBOLIC INDEXING METHODS FOR FORMAL VERIFICATION ON A SYMBOLIC LATTICE DOMAIN
US	7,313,016	US-2006-0256613-A1	11/486,872	RESETTING PHASE CHANGE MEMORY BITS
US	7,317,310		09/954,402	EMBEDDED PCB IDENTIFICATION
US	7,317,737	US-2005-0053083-A1	10/655,565	SYSTEMS AND METHODS FOR USING HDLC CHANNEL CONTEXT TO SIMULTANEOUSLY PROCESS MULTIPLE HDLC CHANNELS
US	7319947		09/470,875	METHOD AND APPARATUS FOR PERFORMING DISTRIBUTED SIMULATION UTILIZING A SIMULATION BACKPLANE
US	7,320,033		09/917,320	DYNAMIC LOCAL DRIVE AND PRINTER SHARING
US	7,323,707	US-2006-0001016-A1	10/881,664	INITIALIZING PHASE CHANGE MEMORIES
US	7,324,516		10/217,644	DATA PACKET HEADER CONVERSION
US	7,325,025	2003-0115237	10/020,447	IMPROVED LOOK-AHEAD CARRY ADDER CIRCUIT
US	7,326,972	US-2006-0001103-A1	10/880,988	INTERCONNECT STRUCTURE IN INTEGRATED CIRCUITS
US	7,326,973	US-2005-0127506-A1	11/049,435	A METHOD AND AN APPARATUS FOR A HARD-CODED BIT VALUE CHANGEABLE IN ANY LAYER OF METAL

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US	7,327,370	US-2005-0243096-A1	11/174,662	MEMORY CONTROLLER HUB INTERFACE
US	7,328,313	US-2006-0224834-A1	11/094687	WRITE-BACK CACHE METHODS AND APPARATUS
US	RE38,674	5,244,843	08/528,188	PROCESS FOR FORMING A THIN OXIDE LAYER
US			07/999,148	METHOD AND APPARATUS FOR ANALYZING DIGITAL VIDEO IMAGES BY MERGING DISPLACEMENT VECTORS
US			08/623,672	CLEANING STEP WHICH IMPROVES ELECTROMIGRATION PERFORMANCE OF INTERLAYER CONNECTION IN INTEGRATED CIRCUITS
US			08/772,016	METHOD AND APPARATUS FOR PERFORMING BLOCK BASED FREQUENCY DOMAIN FILTERING
US			08/799,654	METHOD AND APPARATUS FOR SCALING IMAGE DATA
US			08/874,821	METHOD AND APPARATUS FOR SCRUBBING THE BOND PADS OF AN INTEGRATED CIRCUIT DURING WAFER SORT
US			08/944,041	POLYSILICON POLISH FOR PATTERNING IMPROVEMENT
US			08/965,592	METHOD AND APPARATUS FOR SEARCHING A MASS STORAGE MEDIUM
US			09/000,712	METHOD AND APPARATUS FOR CHANGING THE FONT USED TO DISPLAY TEXT ENTERED INTO AN INFORMATION INPUT FIELD
US			09/004,052	PORTABLE DIGITAL PHOTOGRAPH VIEWING APPARATUSES
US			09/122,270	ADVANCED REGISTER RENAMING SYSTEM FOR IMPROVED INSTRUCTION LEVEL PARALLELISM
US			09/148,392	SELECTING DESIGN POINTS ON PARAMETER FUNCTIONS HAVING FIRST SUM OF CONSTRAINT SET AND SECOND SUM OF OPTIMIZING SET TO IMPROVE SECOND SUM WITHIN DESIGN CONSTRAINTS
US			09/156,272	PHOTOLITHOGRAPHY METHOD USING COHERENCE DISTANCE CONTROL
US			09/250,940	SYSTEM AND METHOD FOR CONTROLLING AN ELECTRONIC DEVICE
US			09/258,060	CALIBRATING PROJECTION DISPLAYS
US			09/259,394	CORRECTING NON-UNIFORMITY IN DISPLAYS
US			09/344,453	NETWORK ACCELERATOR SUBSYSTEM BASED ON SINGLE-CHIP NETWORK
US			09/350,269	TRANSMITTING DATA AND COMMANDS OVER A BUS
US			09/409,522	AUTOMATICALLY RECORDING VIDEO

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US		09/471,964	REAL-TIME PERFORMANCE ASSESSMENT OF LARGE AREA NETWORK USER EXPERIENCE
US		09/478,994	SYSTEM AND METHOD FOR STALLING A DISPLAY CONTROLLER UPON REQUEST
US		09/515,556	OBSCURING VIDEO SIGNALS FOR CONDITIONAL ACCESS
US		09/524,701	MICROSCOPE WITH INFRARED IMAGING
US		09/533,024	METHOD AND APPARATUS TO PROVIDE CLIENT-SIDE FILTERING IN A BROADCAST SYSTEM
US		09/603,800	COMBINED PROPAGATE/GENERATE/PARTIAL SUM CIRCUIT FOR SINGLE-RAIL ADDERS
US		09/608,637	METHODS FOR FORMAL VERIFICATION ON A SYMBOLIC LATTICE DOMAIN
US		09/609,496	METHOD AND APPARATUS FOR FAST ARGUMENT REDUCTION IN A COMPUTING SYSTEM
US		09/611,938	DYNAMICALLY LOCATING ICONS ON A VIDEO DISPLAY SCREEN
US		09/676,175	METHOD AND APPARATUS FOR GENERATING AN EXPECTED TOP OF STACK DURING INSTRUCTION TRANSLATION
US		09/715,529	METHOD AND APPARATUS FOR SYNCHRONIZING NETWORK POLICIES
US		09/723,210	PROVIDING A VALID INITIAL FRAME
US	JCS	09/732,115	APPARATUS FOR SHIELDING TRANSMISSION LINE EFFECTS ON A PRINTED CIRCUIT BOARD
US	DJP1	09/735,358	CLOCK NETWORK
US	2002-0087852	09/749,405	METHOD AND APPARATUS FOR PREDICTING BRANCHES USING A META PREDITOR
US	2002-0087833	09/749,725	A METHOD AND APPARATUS FOR DISTRIBUTED DISPERSAL LOGIC FOR PIPELINED PROCESSORS
US		09/817,711	TWO-DIMENSIONAL PYRAMID FILTER ARCHITECTURE
US		09/835,034	TIMING MULTIPLE EVENTS WITH A SINGLE TIMER
US	US-2002-0154098-A1	09/836,978	LOCATING A POSITION ON A DISPLAY SCREEN
US	US-2002-0163301-A1	09/847,447	LARGE FORMAT EMISSIVE DISPLAY
US	2002-0188806	09/891,523	PARALLEL CACHELETS
US	2003-0014459	09/893,868	CASCADED DOMINO FOUR-TO-TWO REDUCER CIRCUIT AND METHOD
US		09/894,136	SYSTEM FOR SHARING CHANNELS BY INTERLEAVING FLITS
US		09/895,113	METHOD OF SCHEDULING MODULES ON A CAROUSEL

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US	US-2003-0011108-A1	09/904,269	ASSEMBLING DISPLAY MODULES
US		09/951,904	SYSTEM AND METHOD FOR SPLIT AUTOMATIC GAIN CONTROL
US	2003-0126179	09/956,903	SYMMETRIC CASCADED DOMINO CARRY GENERATE CIRCUIT
US		09/964,502	NETWORK COMMUNICATION CASING
US		09/982,242	METHOD AND APPARATUS TO EMULATE EXTERNAL IO INTERCONNECTION
US	US-2003-0077076-A1	09/999,784	PORTABLE DOWNLOAD UNIT INCLUDING A MEMORY CHIP-TO-CD BURNER
US		10/027,053	BIT ERROR RATE TEST SYSTEM FOR MULTI-SOURCE AGREEMENT COMPLIANT TRANSCEIVERS
US		10/041,543	METHOD AND APPARATUS FOR HEADER UPDATING
US		10/061,907	DIGITAL CAMERA WITH ISO PICKUP SENSITIVITY ADJUSTMENT
US	US-2003-0142058-A1	10/062,268	LCD CONTROLLER ARCHITECTURE FOR HANDLING FLUCTUATING BANDWIDTH CONDITIONS
US		10/062,863	A PROTOCOL DRIVER APPLICATION PROGRAMMING INTERFACE FOR OPERATING SYSTEMS
US		10/112,194	TELEPHONE CONFERENCE BRIDGE PROVIDED VIA A PLURALITY OF COMPUTER TELEPHONY RESOURCE ALGORITHMS
US	AMM	10/154,948	SEARCH RECEIVER USING ADAPTIVE DETECTION THRESHOLDS
US	US-2003-0224535-A1	10/160,641	FORMING FERROELECTRIC POLYMER MEMORIES
US		10/179,790	CONTROLLING SNOOP ACTIVITIES USING TASK TABLE IN MULTIPROCESSOR SYSTEM
US	US-2004-0015763-A1	10/202,624	TEST INTERFACE, SYSTEM, AND METHOD FOR TESTING COMMUNICATIONS DEVICES WITH NON-DETERMINISTIC LATENCY
US	US-2004-0031031-A1	10/215,549	EXECUTING APPLICATIONS FROM A SEMICONDUCTOR NONVOLATILE MEMORY
US		10/228,617	PROCESS AND APPARATUS FOR PACKAGING A TAPE SUBSTRATE
US	US-2004-0047408-A1	10/238,669	DATA LINK ANALYZER
US		10/253,229	LOW LATENCY MEMORY ACCESS METHOD USING UNIFIED QUEUE MECHANISM
US	US-2004-0079388-A1	10/278,535	REMOVING FLUORINE-BASED PLASMA ETCH RESIDUES
US	US-2004-0080356-A1	10/280,926	COMPACT INPUT/OUTPUT SIGNAL DRIVER FOR ELECTROSTATIC DISCHARGE PROTECTION
US		10/288,021	PHOTOACTIVE ADHESION PROMOTER

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US	JNG	10/299,135	PROTECTIVE FILM FOR THE FABRICATION OF DIRECT BUILD-UP LAYERS ON AN ENCAPSULATED DIE PACKAGE
US		10/304,303	USE OF CHROMELESS PHASE SHIFT MASKS TO PATTERN CONTACTS
US	US-2004-0102013-A1	10/306,320	CODOPING OF SOURCE DRAINS USING CARBON OR FLUORINE ION IMPLANTS TO IMPROVE POLYSILICON DEPLETION
US		10/309,472	PARAMETRIC REPRESENTATION METHODS FOR FORMAL VERIFICATION ON A SYMBOLIC LATTICE DOMAIN
US	WWN	10/322,902	SUBSTRATE-IMPRINTING APPARATUS, METHODS OF MANUFACTURE, AND PRODUCTS FORMED THEREFROM
US		10/324,692	PORTABLE DIGITAL PHOTOGRAPH VIEWING APPARATUSES
US		10/331,122	ON-CHIP JITTER TESTING
US		10/335,012	DIGITAL PHASE DETECTION WITH JITTER FILTER
US	US-2004-0132503-A1	10/336,629	THERMAL MANAGEMENT FOR TELECOMMUNICATION DEVICES
US	2003-0135715	10/351,444	ENHANCED VIRTUAL RENAMING SCHEME AND DEADLOCK PREVENTION THEREFOR
US	2005-0262332	10/404,384	METHOD AND SYSTEM FOR BRANCH TARGET PREDICTION USING PATH INFORMATION
US		10/425,987	LOW POWER ADDER
US		10/426,044	LOW POWER ADDER CIRCUIT UTILIZING BOTH STATIC AND DYNAMIC LOGIC
US		10/427,168	INTERCONNECTION DESIGNS AND MATERIALS HAVING IMPROVED STRENGTH AND FATIGUE LIFE
US		10/427,377	SMART CONTROL POINTS
US	US 2004-0220877 A1	10/428,286	MEDIA CENTER STORAGE DEVICE PROXY
US	US-2004-0243896-A1	10/436,775	TEST SCAN CELLS
US		10/438,146	REDUCED AREA INTERSECTION BETWEEN ELECTRODE AND PROGRAMMING ELEMENT
US	US-2004-0236562-A1	10/445,272	USING MULTIPLE SIMULATION ENVIRONMENTS
US		10/453,115	METHOD AND APPARATUS FOR PREFETCHING BASED UPON TYPE IDENTIFIER TAGS
US	US-2004-0246955-A1	10/454,790	A METHOD AND PROCESS FOR DETERMINING A QUOTIENT
US	US-2004-0254775-A1	10/461,217	METHOD AND APPARTUS TO CHARACTERIZE AN ELECTRONIC DEVICE

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US	US-2004-0258389-A1	10/463,651	PASS THROUGH MODE FOR A PERSONAL VIDEO RECORDER
US		10/465,666	SYSTEM AND PROCESS TO CONTROL ELECTROPLATING A METAL ONTO A SUBSTRATE
US	2004-0098565	10/601,172	INSTRUCTION QUEUE FOR AN INSTRUCTION PIPELINE
US	US-2004-0264413-A1	10/603,859	DEVICE, SYSTEM AND METHOD FOR CHANNEL SCANNING
US	US-2004-0268032-A1	10/609,714	A MODULAR CONTENT ADDRESSABLE MEMORY
US	US-2004-0266184-A1	10/609,963	POST-DEPOSITION MODIFICATION OF INTERLAYER DIELECTRICS
US	US 2005-0010683 A1	10/610,104	APPARATUS, SYSTEM AND METHOD FOR PERFORMING TABLE MAINTENANCE
US		10/610,713	A METHOD AND APPARATUS FOR INTEGRATED CIRCUIT SELF-DESCRIPTION
US	2004 0267977	10/610,855	TOPOLOGY BASED REPLACEMENT ROUTING OF SIGNAL PATHS
US	US-2005-0050303-A1	10/611,380	HIERARCHICAL REORDER BUFFERS FOR CONTROLLING SPECULATIVE EXECUTION IN A MULTI-CLUSTER SYSTEM
US	US-2004-0267914-A1	10/611,617	METHOD, APPARATUS AND SYSTEM FOR CREATING EFFICIENT UNIVERSAL PLUG AND PLAY CONTROL POINTS
US	US-2004-0267480-A1	10/612,293	SELECTIVE CONTROL OF TEST-ACCESS PORTS IN INTEGRATED CIRCUITS
US		10/628,597	FASTENER INSTALLATION TOOL AND METHODS OF USE
US	US-2005-0102465-A1	10/629,093	MANAGING A CACHE WITH PINNED DATA
US		10/641,614	PROCESSING INSTRUCTIONS
US		10/654,252	METHOD AND APPARATUS FOR MULTI-LINK EXTENSIONS AND BUNDLE SKEW MANAGEMENT
US	US-2005-0060376-A1	10/660,876	SECURE COMPUTER TELEPHONY INTEGRATION ACCESS
US	US 2004-0162105 A1	10/663,165	ENHANCED GENERAL PACKET RADIO SERVICE (GPRS) MOBILITY MANAGEMENT
US	US-2005-0086508-A1	10/666,077	REGISTER ALIAS TABLE CACHE
US	US-2005-066328-A1	10/669,309	METHOD AND APPARATUS TO PERFORM TASK SCHEDULING
US	US-2005-0071795-A1	10/676,893	A METHOD AND APPARATUS FOR INTEGRATED CIRCUIT DATAPATH LAYOUT USING A VECTOR EDITOR
US	US-2005-0071846-A1	10/677,081	PASSING PARAMETERS BY IMPLICIT REFERENCE

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US	US-2005-0077180-A1	10/682,275	MODIFIED ELECTROPLATING SOLUTION COMPONENTS IN A HIGH-ACID ELECTROLYTE SOLUTION
US	US-2005-0077181-A1	10/682,276	MODIFIED ELECTROPLATING SOLUTION COMPONENTS IN A LOW-ACID ELECTROLYTE SOLUTION
US	US-2005-0122389-A1	10/723,413	MULTI-CONFERENCE STREAM MIXING
US		10/743,397	SHIFTING AN INPUT SIGNAL FROM A HIGH-SPEED DOMAIN TO A LOWER-SPEED DOMAIN
US	2005-0147036	10/749,271	METHOD AND APPARATUS FOR ENABLING AN ADAPTIVE REPLAY LOOP IN A PROCESSOR
US	CES	10/758,055	SOCKET WARPAGE REDUCTION APPARATUS AND METHOD
US		10/761,394	DEVICE TO RECEIVE, BUFFER, AND TRANSMIT PACKETS OF DATA IN A PACKET SWITCHING NETWORK
US		10/761,395	DEVICE TO RECEIVE, BUFFER, AND TRANSMIT PACKETS OF DATA IN A PACKET SWITCHING NETWORK
US	US-2004-0159945-A1	10/774,869	UNDERFILL PROCESS FOR FLIP-CHIP DEVICE
US		10/774,952	DIE-IN-HEAT SPREADER MICROELECTRONIC PACKAGE
US	US-2005-0188156-A1	10/783,621	METHOD AND APPARATUS FOR DEDICATING CACHE ENTRIES TO CERTAIN STREAMS FOR PERFORMANCE OPTIMIZATION
US	US-2005-0204099-A1	10/799,555	METHOD AND APPARATUS TO WRITE BACK DATA
US	US-2005-0202252-A1	10/799,928	USE OF ALTERNATIVE POLYMER MATERIALS FOR "SOFT" POLYMER PELLICLES
US	US-2005-0251795-A1	10/805,106	METHOD, SYSTEM, AND PROGRAM FOR OPTIMIZING CODE
US	US-2005-0210225-A1	10/805,947	HYBRID BRANCH PREDICTION
US		10/814,398	METHOD AND APPARATUS FOR ANALOG COMPENSATION OF DRIVER OUTPUT SIGNAL SLEW RATE AGAINST DEVICE IMPEDANCE VARIATION
US	US-2005-0240820-A1	10/815,904	A METHOD AND APPARATUS FOR MULTIPROCESSOR DEBUG SUPPORT
US		10/817,263	PRESBYOPIC BRANCH TARGET PREFETCH METHOD AND APPARATUS
US	US-2005-0239275-A1	10/832,178	COMPLIANT MULTI-COMPOSITION INTERCONNECTS
US		10/842,752	DEVICE TO RECEIVE, BUFFER, AND TRANSMIT PACKETS OF DATA IN A PACKET SWITCHING NETWORK

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US	US-2005-0270983-A1	10/863,661	A METHOD AND APPARATUS TO MANAGE EXCEPTIONS IN NETWORK PROCESSORS
US		10/868,703	APPARATUS AND METHOD OF DYNAMIC USAGE PROFILE ACQUISITION AND UTILIZATION IN A WIRELESS MOBILE DEVICE
US	US-2004-0231886-A1	10/870,506	PCB DESIGN AND METHOD FOR PROVIDING VENTED BLIND VIAS
US	US-2006-0002172-A1	10/880,692	PROVIDING CURRENT FOR PHASE CHANGE MEMORIES
US	US-2006-0002425-A1	10/883,107	DETERMINING AVAILABLE BANDWIDTH IN A NETWORK
US	US-2006-0000806-A1	10/883,404	SUBSTRATE CARRIER FOR SURFACE PLANARIZATION
US	US-2006-0007855-A1	10/885,821	PRIORITIZATION OF NETWORK TRAFFIC
US		10/893,015	METHOD, SYSTEM, AND APPARATUS FOR TRACKING DEFECTIVE CACHE LINES
US	US-2006-0033217-A1	10/915,293	FLIP-CHIPS ON FLEX SUBSTRATES, FLIP-CHIP AND WIRE-BONDED CHIP STACKS, AND METHODS OF ASSEMBLING SAME
US	US-2005-0014096-A1	10/917,679	PHOTOACTIVE ADHESION PROMOTER
US	20060053328	10/935,902	TRAINING PATTERN BASED DE-SKEW MECHANISM AND FRAME ALIGNMENT
US	US-2005-0054143-A1	10/939,226	USING BENZOCYCLOBUTENE BASED POLYMERS AS UNDERFILL MATERIALS
US	US-2006-0054996-A1	10/939,237	BREAK DOWN FORMED MEMORY DEVICE WITH SELF ALIGNED GLUE LAYER
US	US 2006-0062174 A1	10/945,797	DEVICE AND METHODS FOR INCREASING WIRELESS CONNECTION SPEEDS
US		10/954,947	OVERHEAD PROCESSING AND GENERATION TECHNIQUES
US	US-2006-0072634-A1	10/955,394	CALIBRATION METHODS FOR TUNABLE LASERS
US	US-2006-0075296-A1	10/956,994	METHOD, APPARATUS AND SYSTEM FOR DATA INTEGRITY OF STATE RETENTIVE ELEMENTS UNDER LOW POWER MODES
US	2005-0060154	10/962,685	VOICE DRIVEN WIRELESS POINTER
US	2005-0060502-A1	10/970,015	MECHANISM TO GUARANTEE FORWARD PROGRESS FOR INCOMING COHERENT INPUT/OUTPUT (I/O) TRANSACTIONS FOR CACHING I/O AGENT ON ADDRESS CONFLICT WITH PROCESSOR TRANSACTIONS
US	US-2005-0112793-A1	10/973,161	METHODS OF FORMING A HIGH CONDUCTIVITY DIAMOND FILM AND STRUCTURES FORMED THEREBY

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US	US 2006-0117231 A1	10/976,572	ADAPTIVE COMMUNICATION INTERFACE
US	US-2006-0091492-A1	10/977,186	DEPOSITING TITANIUM SILICON NITRIDE FILMS FOR FORMING PHASE CHANGE MEMORIES
US	US-2006-0106954-A1	10/988,417	MEMORY REUSE FOR MULTIPLE ENDPOINTS IN USB DEVICE
US	US-2006-0105764-A1	10/989,539	ADAPTIVE WIRELESS NETWORKS AND METHODS FOR COMMUNICATING MULTIMEDIA IN A PROACTIVE ENTERPRISE
US	US-2006-0107077-A1	10/989,948	PROGRAMMABLE POWER TRANSITION COUNTER
US	US-2006-0106962-A1	10/992,250	METHOD FOR IMPLEMENTATION OF USB ON-THE-GO
US	US-2005-0100266-A1	10/994,021	METHOD AND APPARATUS FOR WAFER LEVEL TESTING OF INTEGRATED OPTICAL WAVEGUIDE CIRCUITS
US	US-2006-0110883-A1	10/997,609	METHOD FOR FORMING A MEMORY DEVICE
US	US-2005-0099762-A1	11/003956	CAPACITOR
US	US-2005-0083349-A1	11/005,694	PHYSICALLY INTERACTING WITH A PROCESSOR-BASED DISPLAY
US	US-2006-0129701-A1	11/012,316	COMMUNICATING AN ADDRESS TO A MEMORY DEVICE
US		11/015,965	METHOD AND APPARATUS FOR CHANNEL HEALTH ENCODING
US		11/015,967	METHOD AND APPARATUS FOR PROVIDING A CONNECTION MATRIX
US	US-2006-0136679-A1	11/018958	PROTECTED PROCESSING APPARATUS, SYSTEMS, AND METHODS
US	US-2006-0143411-A1	11/021,323	TECHNIQUES TO MANAGE PARTITION PHYSICAL MEMORY
US	US-2006-0143554-A1	11/022,212	SCALABLE TRACEBACK TECHNIQUE FOR CHANNEL DECODER
US	US-2006-019931-A1	11/024,164	RUNAHEAD EXECUTION IN A CENTRAL PROCESSING UNIT
US	US-2006-0140226-A1	11/024,928	TECHNIQUES FOR PROCESSING TRAFFIC TRANSMITTED OVER ADVANCED SWITCHING COMPATIBLE SWITCH FABRICS
US	US-2006-0161688-A1	11/024956	SYSTEMS AND METHODS FOR EFFICIENT OPERATIONS OF COMPONENTS IN A WIRELESS COMMUNICATIONS DEVICE
US	US-2006-0142991-A1	11/025,116	REMOTE USB NETWORK DEVICE CONTROL
US	US-2006-0149917-A1	11/027,784	SECURE MEMORY CONTROLLER
US	US-2006-0143687-A1	11/027,913	SECURE CONTROLLER FOR BLOCK ORIENTED STORAGE

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US	US-2005-0206807-A1	11/032,828	PROVIDING OPTICAL ELEMENTS OVER EMISSIVE DISPLAYS
US	US-2006-0190517-A1	11/050,369	TECHNIQUES FOR TRANSPOSITION OF A MATRIX ARRANGED IN A MEMORY AS MULTIPLE ITEMS PER WORD
US		11/053,786	NON STROBE SENSING CIRCUIT
US	US-2005-0145885-A1	11/063,963	I/O ARCHITECTURE FOR INTEGRATED CIRCUIT PACKAGE
US	US-2006-0200684-A1	11/069,924	Power Mode Change Voltage Control In A Computerized System
US	US-2006-0215567-A1	11/090,571	METHOD AND APPARATUS FOR MONITORING PATH STATISTICS
US	US-2006-0224857-A1	11/092,432	LOCKING ENTRIES INTO TRANSLATION LOOKASIDE BUFFERS
US	US-2006-0221944-A1	11/093,907	DIFFERENTIAL DELAY COMPENSATION
US	US-2006-0228858-A1	11/095,330	FLASH MEMORY CELL HAVING REDUCED FLOATING GATE TO FLOATING GATE COUPLING
US	US-2006-0223068-A1	11/095,414	Sorting Of Carbon Nanotubes Through Selective DNA Delamination Of DNA/Carbon Nanotube Hybrid Structures
US	US-2006-0224337-A1	11/095,950	PROGRAMMABLE CURRENT LOAD SYSTEMS AND METHODS
US	US-2005-0189544-A1	11/100,885	METHODS OF FORMING A HIGH CONDUCTIVITY DIAMOND FILM AND STRUCTURES FORMED THEREBY
US	US-2006-0230235-A1	11/101,785	LOW LOCALITY-OF-REFERENCE SUPPORT IN A MULTI-LEVEL CACHE HIERACHY
US	US-2006-0226410-A1	11/103,188	HEATING PHASE CHANGE MATERIAL
US	US-2006-0239800-A1	11/114,261	PULSED DC AND RF PHYSICAL VAPOR DEPOSITION CLUSTER TOOL
US	US-2005-0192789-A1	11/124,315	METHODS FOR FORMAL VERIFICATION ON A SYMBOLIC LATTICE DOMAIN
US		11/137,314	DEVICE AND METHOD FOR MAXIMIZING PERFORMANCE ON A MEMORY INTERFACE WITH A VARIABLE NUMBER OF CHANNELS
US	US-2005-0248579-A1	11/137,700	METHOD AND APPARATUS FOR REORDERING MEMORY REQUESTS FOR PAGE COHERENCY
US	US-2005-0225860-A1	11/144,583	SEGMENTED COMPLEX DIFFRACTION GRATINGS
US	US-2005-0231804-A1	11/145,251	SEGMENTED COMPLEX DIFFRACTION GRATINGS
US	US-2005-0225861-A1	11/145,291	SEGMENTED COMPLEX DIFFRACTION GRATINGS
US	US-2006-0288098-A1	11/156,838	PERIPHERAL INTERFACE ALERT MESSAGE FOR DOWNSTREAM DEVICE

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US	US-2006-0293039-A1	11/166,143	METHOD AND SYSTEM FOR TRANSFERRING MESSAGES TO A MOBILE STATION ACCORDING TO SPECIFIC PARAMETERS
US		11/167,495	METHOD OF FORMING A MULTI-DIE SEMICONDUCTOR PACKAGE
US	US-2006-0289848-A1	11/168,780	REDUCING OXIDATION OF PHASE CHANGE MEMORY ELECTRODES
US	US-2007-0002059-A1	11/169,537	PIXEL DATA COMPRESSION FROM CONTROLLER TO DISPLAY
US	US-2007-0002017-A1	11/170,110	DEVICE, SYSTEM AND METHOD FOR WIRELESS COMMUNICATION AND CURSOR POINTING
US	US-2007-0006007-A1	11/173,218	FREQUENCY-DEPENDENT VOLTAGE CONTROL IN DIGITAL LOGIC
US	US-2007-0001762-A1	11/173,760	CURRENT SENSING METHOD FOR INTEGRATED SWITCHING TRANSISTORS
US	US-2007-0018148-A1	11/185,488	PHASE CHANGE MEMORY WITH U-SHAPED CHALCOGENIDE CELL
US	US-2005-0273603-A1	11/188,420	A MECHANISM TO IMPROVE AUTHENTICATION FOR REMOTE MANAGEMENT OF A COMPUTER SYSTEM
US	US-2007-0028031-A1	11/189,448	Universal Nonvolatile Memory Boot Mode
US	2005-0268083	11/192,025	METHOD AND SYSTEM FOR USING INTERNAL FIFO RAM TO IMPROVE SYSTEM BOOT TIMES
US	US-2007-0023857-A1	11/193,952	FABRICATING SUB-LITHOGRAPHIC CONTACTS
US	US-2005-0270088-A1	11/197,806	ACTIVE PHASE CANCELLATION FOR INDUCTOR / CAPACITOR NETWORKS
US	US-2005-0274619-A1	11/207,305	MODIFIED ELECTROPLATING SOLUTION COMPONENTS IN A LOW-ACID ELECTROLYTE SOLUTION
US	US-2007-0055816-A1	11/218,371	POWER LOSS RECOVERY IN NON-VOLATILE MEMORY
US	US-2007-0058584-A1	11/225,303	TECHNIQUES TO TRANSMIT AND DUPLEX WITH CHANNEL KNOWLEDGE AT A BASE STATION
US	US-2007-0079054-A1	11/240,004	METHOD AND APPARATUS FOR OPTIMIZING FLASH DEVICE ERASE DISTRIBUTION
US	US-2007-0076708-A1	11/241,339	ERROR PROTECTION TECHNIQUES FOR FRAMES ON A WIRELESS NETWORK
US	US-2007-0082469-A1	11/248,488	FORMING HEATERS FOR PHASE CHANGE MEMORIES
US	US-2006-0036985-A1	11/251,664	COMPACTING CIRCUIT RESPONSES
US	US-2006-0033522-A1	11/253,377	AC TESTING OF LEAKAGE CURRENT IN INTEGRATED CIRCUITS USING RC TIME CONSTANT
US	US-2007-0106871-A1	11/271,778	PROCESSOR MULTI-PARTITION SECURITY ARCHITECTURE

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US	US-2007-0111492-A1	11/274,622	A STRUCTURED, ELECTRICALLY-FORMED FLOATING GATE FOR FLASH MEMORIES
US	US-2006-0078198-A1	11/283,375	APPARATUS AND METHOD FOR IMAGER DEVICE COLOR CALIBRATION USING SPECTRAL LIGHT SOURCE
US	US-2006-0074619-A1	11/285,565	RECOGNIZING SIGNALS IN DESIGN SIMULATION
US	US-2007-0120588-A1	11/291,204	LOW-JITTER CLOCK DISTRIBUTION
US	US-2006-0098524-A1	11/303,417	FORMING PLANARIZED SEMICONDUCTOR STRUCTURES
US	US-2006-0106993-A1	11/321,632	MECHANISM FOR HANDLING EXPLICIT WRITEBACK IN A CACHE COHERENT MULT-NODE ARCHITECTURE
US	US-2006-0149918-A1	11/323,473	MEMORY WITH MODIFIABLE ADDRESS MAP
US		11/325,961	LARGE FORMAT EMISSIVE DISPLAY
US		11/334,729	REPAIRABLE TILED DISPLAYS
US	US-2006-0121936-A1	11/338,932	PORTABLE COMPUTING DEVICE ADAPTED TO UPDATE DISPLAY INFORMATION WHILE IN A LOW POWER MODE
US	US-2006-0168442-A1	11/351,934	CONSOLE REDIRECTION AMONG LINKED COMPUTERS
US	US-2007-0192830-A1	11/354,676	SECURITY MODULE HAVING ACCESS LIMITED BASED UPON SECURITY LEVEL OF CODE SEEKING ACCESS
US	US-2007-0204121-A1	11/361,228	MOVEABLE LOCKED LINES IN A MULTI-LEVEL CACHE
US	US-2007-0227878-A1	11/392,135	FORMING OVONIC THRESHOLD SWITCHES WITH REDUCED DEPOSITION CHAMBER GAS PRESSURE
US	US-2007-0230638-A1	11/394,533	METHOD AND APPARATUS TO EFFICIENTLY CONFIGURE MULTI-ANTENNA EQUALIZERS
US	US-2007-0230804-A1	11/394,929	ENCODING TECHNIQUES EMPLOYING NOISE-BASED ADAPTATION
US	US-2007-0230539-A1	11/394,994	WIRELESS COMMUNICATIONS WITH AUXILIARY ANTENNAS
US	US-2007-0234189-A1	11/396,329	SYSTEM AND METHOD FOR REDUCING FALSE ALARM IN THE PRESENCE OF RANDOM SIGNALS
US	US-2006-0175068-A1	11/396,769	FASTENER INSTALLATION TOOLS, SYSTEMS, AND METHODS OF USE

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US	US-2007-0254446-A1	11/411,311	SELF-ALIGNED BIPOLAR JUNCTION TRANSISTORS
US	US-2006-0186924-A1	11/411,647	VOLTAGE-LEVEL CONVERTER
US	US-2006-0225031-A1	11/437,352	METHOD AND APPARATUS FOR ACCESSING THREAD-PRIVATIZED GLOBAL STORAGE OBJECTS
US	US-2006-0265541-A1	11/462,264	METHOD AND APPARATUS FOR GENERATING TRAFFIC IN AN ELECTRONIC BRIDGE VIA A LOCAL CONTROLLER
US	US-2006-0294321-A1	11/514,802	COMMUNICATION REGISTERS FOR PROCESSING ELEMENTS
US		11/527,895	COMPOSITE ORGANIC INORGANIC NANOCLUSTERS AS CARRIERS AND IDENTIFIERS OF TESTER MOLECULES
US		11/529,022	AUTHENTICATING DATA RETURNED FROM NON-VOLATILE MEMORY COMMANDS
US		11/529,987	ARCHITECTURE FOR VIRTUAL SECURITY MODULE
US	US-2007-0026566-A1	11/542,712	PHASE CHANGE MEMORY WITH DAMASCENE MEMORY ELEMENT
US		11/545,234	ASYMMETRIC CHALCOGENIDE DEVICE
US	US-2007-0050181-A1	11/553,905	ANTECEDENT STRENGTHENING TO PERFORM GENERALIZED TRAJECTORY EVALUATION
US	US-2007-0093103-A1	11/561,684	VARIABLE LATCH
US	US-2007-0037350-A1	11/582,881	FLASH MEMORY CELL HAVING REDUCED FLOATING GATE TO FLOATING GATE COUPLING
US		11/595,055	READ WINDOW IN CHALCOGENIDE SEMICONDUCTOR MEMORIES
US		11/606,800	A PHASE CHANGE MEMORY CELL HAVING A TAPERED MICROTRENCH
US	US-2007-0105312-A1	11/615,862	MEMORY CELL WITH NANOCRYSTAL AS DISCRETE STORAGE ELEMENT
US	US-2007-0102817-A1	11/616,164	METHOD AND APPARATUS FOR REDUCING ELECTRICAL INTERCONNECTION FATIGUE
US		11/823,518	HIGH DENSITY NOR FLASH ARRAY ARCHITECTURE
US		60/090,939	SINGLE-CHIP NETWORK PROCESSOR & INTERFACE SYSTEM
US		60/140,705	DIGITAL IMPAIRMENT LEARNING SEQUENCE
US		60/282,961	COMPOSITE DIFFRACTION GRATINGS FOR SIGNAL PROCESSING AND OPTICAL CONTROL APPLICATIONS
US		60/287,707	PARALLEL CACHELETS
US		60/315,797	UNIVERSAL TELEPHONY INTERFACE POLARITY DETECTOR

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US	60/317,802	TIME VARYING FILTER WITH ZERO AND/OR POLE MIGRATION
US	60/447,665	ENHANCED GPRS MOBILITY MANAGEMENT