PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT2912014

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
AMERICAN CAPITAL, LTD.	06/20/2014

RECEIVING PARTY DATA

Name:	CONTOUR SEMICONDUCTOR, INC.
Street Address:	85 RANGEWAY ROAD
Internal Address:	BLDG. 1
City:	N. BILLERICA
State/Country:	MASSACHUSETTS
Postal Code:	01862

PROPERTY NUMBERS Total: 48

Property Type	Number
Patent Number:	5673218
Patent Number:	5889694
Patent Number:	RE41733
Patent Number:	RE42310
Patent Number:	6586327
Patent Number:	7183206
Patent Number:	7507663
Patent Number:	6598164
Patent Number:	6956757
Patent Number:	7460384
Patent Number:	7593246
Patent Number:	7826244
Patent Number:	8358525
Patent Number:	7149934
Patent Number:	8108735
Patent Number:	7376008
Patent Number:	7652916
Patent Number:	7916530
Patent Number:	7548454
Patent Number:	7593256

Property Type	Number
Patent Number:	7548453
Patent Number:	7667996
Patent Number:	7813157
Patent Number:	7933133
Patent Number:	8116109
Patent Number:	8000129
Patent Number:	7682981
Patent Number:	8358526
Patent Number:	8351238
Patent Number:	8325556
Patent Number:	8325557
Patent Number:	8035416
Patent Number:	8526217
Patent Number:	8455298
Patent Number:	8451024
Patent Number:	8635426
Patent Number:	8537618
Patent Number:	8378456
Application Number:	12720843
Application Number:	13373205
Application Number:	13707895
Application Number:	13714499
Application Number:	12924167
Application Number:	12930655
Application Number:	13135235
Application Number:	13385371
Application Number:	61725620
Application Number:	14282444

CORRESPONDENCE DATA

Fax Number: (617)248-4000

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

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Address Line 4: BOSTON, MASSACHUSETTS 02110

ATTORNEY DOCKET NUMBER:	2009744-0002
NAME OF SUBMITTER:	ELIZABETH A. WALKER

SIGNATURE:	/Elizabeth A. Walker/
DATE SIGNED:	06/24/2014

Total Attachments: 4
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source=Release of Security Interest in Patents (Bridge Note Security Release)#page4.tif

RELEASE OF SECURITY INTEREST IN PATENTS

THIS RELEASE OF SECURITY INTEREST IN PATENTS (this "**Release**") is made as of June 20, 2014 ("**Effective Date**") by and between Contour Semiconductor, Inc., a Delaware corporation, with a principal office located at 85 Rangeway Road, Bldg. 1, N. Billerica, MA 01862 (the "**Grantor**") and American Capital, Ltd., a Delaware regulated investment corporation ("**Grantee**").

WHEREAS, pursuant to the terms and conditions of the certain Security Agreement (the "**Security Agreement**") dated May 30, 2014 (as the same may have been amended, modified, extended or restated from time to time) to which Grantor and Grantee were parties, Grantor and Grantee entered into a certain Grant of Security Interest in U.S. Patents, also executed on May 30, 2014 (the "**Patent Security Agreement**");

WHEREAS, pursuant to the terms and conditions of the Patent Security Agreement, and the Security Agreement, Grantor granted to Grantee a continuing security interest in and to, and lien on, all of Grantor's right, title and interest in, to and under certain Patents (as defined in the Patent Security Agreement), including, without limitation, the patents set forth on Schedule A attached hereto (the "**Patents**");

WHEREAS, the Patent Security Agreement was recorded with the U.S. Patent and Trademark Office ("**USPTO**") on May 30, 2014 at Reel/Frame 033063/0617;

WHEREAS, Grantee desires to terminate all such security interests granted pursuant to the Security Agreement and the Patent Security Agreement, and to execute and deliver to Grantor all deeds, assignments and other instruments as may be reasonably necessary to release the security interests relating to the Patents granted pursuant to the Security Agreement and the Patent Security Agreement.

NOW, THEREFORE, for and in consideration of the foregoing, and other good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, Grantee hereby confirms that it has terminated the Patent Security Agreement, and the Security Agreement, and relinquishes unto Grantor the continuing security interest in, and lien on, the Patents granted pursuant to the Security Agreement and the Patent Security Agreement and, in furtherance of (and for purposes of only) the foregoing, otherwise assigns, grants and conveys to Grantor, without recourse, any and all right, title and interest the Grantee may have in, to or under to the Patents in order to revest in Grantor full and unencumbered title to said Patents.

[Signature page follows.]

IN WITNESS WHEREOF, Grantee has caused this Release of Security Interest in Patents to be executed by its duly authorized signatory as of the date first written above.

AMERICAN CAPITAL, LTD.

By: _____

Name: Tim Huelskamp

Title: Vice president

[Signature Page to Release of Security Interest in Patents]

Schedule A

ISSUED PATENTS

Patent No.	Issue Date	Title
5,673,218	09/30/1997	Dual-Addressed Rectifier Storage Device
5,889,694	03/30/1999	Dual-Addressed Rectifier Storage Device
RE41,733	09/21/2010	Dual-Addressed Rectifier Storage Device
RE42,310	04/26/2011	Dual-Addressed Rectifier Storage Device
6,586,327	07/01/2003	Fabrication of Semiconductor Devices
7,183,206	02/27/2007	Fabrication of Semiconductor Devices
7,507,663	03/24/2009	Fabrication of Semiconductor Devices
ZL01819463X	11/19/2008	Fabrication of Semiconductor Devices
6,598,164	07/22/2003	Device & Method for Reducing Piracy of Digitized Information
6,956,757	10/18/2005	Low Cost High Density Rectifier Matrix Memory
7,460,384	12/02/2008	Low Cost High Density Rectifier Matrix Memory
7,593,246	09/22/2009	Low Cost High Density Rectifier Matrix Memory
7,826,244	11/02/2010	Low Cost High Density Rectifier Matrix Memory
8,358,525	01/22/2013	Low Cost High Density Rectifier Matrix Memory
7,149,934	12/12/2006	Error Correcting Memory Access Means and Method
8,108,735	01/31/2012	Error Correcting Memory Access Means and Method
7,376,008	05/20/2008	SCR Matrix Storage Device
7,652,916	01/26/2010	SCR Matrix Storage Device
7,916,530	03/29/2011	SCR Matrix Storage Device
7,548,454	06/16/2009	Memory Array with Readout Isolation
7,593,256	09/22/2009	Memory Array with Readout Isolation
7,548,453	06/16/2009	Memory Array with Readout Isolation
7,667,996	02/23/2010	Nano-Vacuum Tubes and their Application in Storage Devices
7,813,157	10/12/2010	Non-Linear Conductor Memory
7,933,133	04/26/2011	Low Cost, High-Density Rectifier Matrix Memory
8,116,109	02/14/2012	Low-Cost High Density Rectifier Matrix Memory

8,000,129	08/16/2011	Field-Emitter-Based Memory Array with Phase-Change Storage Devices
7,682,981	03/23/2010	Topography Transfer Method with Aspect Ratio Scaling
8,358,526	01/22/2013	Diagonal Connection Storage Array
8,351,238	01/08/2013	Low-Complexity Electronic Circuits & Methods for Forming the Same
8,325,556	12/04/2012	Sequencing Decoder Circuit
8,325,557	12/04/2012	Methods and Apparatus for Disabling a Memory-Array Portion
8,035,416	10/11/2011	Bipolar-MOS Driver Circuit
8,526,217	09/03/2013	Low-Complexity Electronic Circuits & Methods for Forming the Same
8,455,298	06/04/2013	Method for Forming Self-aligned Phase-Change Semiconductor Diode Memory
8,451,024	05/28/2013	Bipolar-MOS Driver Circuit
8,635,426	01/21/2014	Diagonally Accessed Memory Array Circuit
8,537,618	09/17/2013	RAM Memory Device with Nand Type Interface
8,378,456	02/19/2013	UNIFIED SWITCH ARRAY FOR MEMORY DEVICES
12/720,843	03/10/2010	[ISSUE FEE PAID] Vertical Switch Three-Dimensional Memory Array
13/373,205	11/08/2011	[ISSUE FEE PAID] PINCHED CENTER RESISTIVE CHANGE MEMORY CELL (NUP-052US)
13/707,895	12/07/2012	[ALLOWED] EMBEDDED NON-VOLATILE MEMORY

PENDING PATENTS

Applctn No.	Filing Date	Title
13/714,499	12/14/2012	Bipolar-CMOS Driver Circuit
12/924,167	09/22/2010	Method of Phase Change Memory Programming
12/930,655	01/13/2011	Diode Polarity for Diode Array
13/135,235	06/29/2011	3-D Resistor Array and Method of Operation
13/385,371	02/15/2012	CURRENT STEERING ELEMENT FORMATION FOR MEMORY CELLS (NUP-055US)
61/725,620	11/13/2012	Solid State Devices Having Fine Pitch Structures
14/282,444	05/20/2014	Vertical Switch Three-Dimensional Memory Array
CONTINUED	05/21/2014	PINCHED CENTER RESISTIVE CHANGE MEMORY CELL (NUP-052C1)
CONTINUATION PLANNED		EMBEDDED NON-VOLATILE MEMORY (NUP-058C1)