PATENT ASSIGNMENT COVER SHEET

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EPAS ID: PAT3056792

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
RENESAS ELECTRONICS CORPORATION	06/19/2014

RECEIVING PARTY DATA

Name:	TESSERA ADVANCED TECHNOLOGIES, INC.
Street Address:	3025 ORCHARD PARKWAY
City:	SAN JOSE
State/Country:	CALIFORNIA
Postal Code:	95134

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	14176328

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

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ATTORNEY DOCKET NUMBER:	TA139-0015-US-07
NAME OF SUBMITTER:	JENNIFER KOSTIC
SIGNATURE:	/Jennifer Kostic/
DATE SIGNED:	10/08/2014

Total Attachments: 5
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FORM OF
DEED OF ASSIGNMENT

THIS DEED OF ASSIGNMENT ("**Assignment**"), EFFECTIVE AS OF JANUARY 1, 2014, IS MADE BY AND BETWEEN

RENESAS ELECTRONICS CORPORATION (hereinafter "**ASSIGNOR**"), a corporation organized under the laws of Japan with its principal place of business located at 1753 Shimonumabe, Nakahara-ku, Kawasaki, Kanagawa 211-8668, Japan; and

TESSERA ADVANCED TECHNOLOGIES, INC. (hereinafter "**ASSIGNEE**"), a Delaware corporation having a place of business at 3025 Orchard Parkway, San Jose, California 95134, United States.

WHEREAS:

A **ASSIGNOR** is the sole owner in respect of the patents and patent applications listed in the attached Appendix (hereinafter "the **PATENTS**"); and

B **ASSIGNEE** is desirous of acquiring all of the worldwide right, title and interest in and to the **PATENTS** and the inventions disclosed therein.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, **ASSIGNOR** has sold, assigned and transferred, and does hereby sell, assign and transfer to **ASSIGNEE** all of the worldwide right, title and interest in (i) the **PATENTS** and the inventions and improvements disclosed therein; (ii) all reissues, divisionals, continuations, continuations-in-part, extensions, renewals, reexaminations and foreign counterparts thereof, and other patents, patent applications, certificates of invention other governmental grants resulting from the **PATENTS**; (iii) all patents and applications which claim priority to or have common disclosure or common priority with any such patents or patent applications, and (iv) all rights corresponding to any of the foregoing throughout the world (including the right to claim the priority date of any of the **PATENTS** and the right to sue for and recover damages for any past, present or future infringement of the Patents), the same to be held and enjoyed by **ASSIGNEE** for its own use and enjoyment, and for the use and enjoyment of its successors, assigns and other legal representatives, to the end of the term or terms of said **PATENTS** granted or reissued or reexamined as fully and entirely as the same would have been held and enjoyed by **ASSIGNOR**, if this assignment and sale had not been made.

IN WITNESS WHEREOF, **ASSIGNOR** has caused these presents to be signed by its duly appointed trustee having full authority to convey its property; and **ASSIGNEE** has caused these presents to be signed by its duly appointed trustee.

If the issue date and/or patent number of any of the **PATENTS** is unknown to **ASSIGNOR** and **ASSIGNEE** at the time this Assignment is executed, **ASSIGNOR** does hereby authorize its attorneys to insert on this Assignment the issue date and patent number of said any patent when known.

ASSIGNOR hereby declares that **ASSIGNEE** may take the steps for recordal of this assignment in the sole name of **ASSIGNEE**.

SIGNATURE PAGE FOLLOWS

SIGNED for and on behalf of

ASSIGNOR: **RENESAS ELECTRONICS CORPORATION**

By _____ on June 19, 2014

(Signature) (Date)

Yasushi Adachi, General Manager, Intellectual Property Division

(Print Name and Title)

SIGNED for and on behalf of

ASSIGNEE: **TESSERA ADVANCED TECHNOLOGIES, INC.**

by _____ on June 25, 2014

(Signature) (Date)

Robert Davis, Chairman of the Board (acting)

(Print Name and Title)

SIGNATURE PAGE TO DEED OF ASSIGNMENT

APPENDIX TO DEED OF ASSIGNMENT

LISTED PATENTS AND PATENT APPLICATIONS

Country	Patent Number	Filing Date	Application Number	Issue Date	Title
DE	69534313.0	09/13/1995	69534313.0	07/13/2005	Polierverfahren
EP (FR, GB, IT)	1308243	09/13/1995	2025724.2	07/13/2005	Polishing method
JP		10/27/1999	2009-287566		Semiconductor device
JP		10/27/1999	2013-235987		Semiconductor device
JP		09/28/2001	2014-038734		Semiconductor device and method for manufacturing the same
JP	3992439	02/20/1996	2001-7146	08/03/2007	Semiconductor integrated circuit device for connecting semiconductor region and electrical wiring metal via titanium silicide layer and method of fabrication thereof
JP	4224000	03/19/1997	2004-207132	11/28/2008	A nonvolatile semiconductor memory device and a method of manufacture thereof
JP	4372749	08/28/1997	2005-368913	09/11/2009	Package construction of semiconductor device
JP	4237777	03/17/1999	2006-108401	12/26/2008	Semiconductor device
JP	4566283	06/04/1999	2010-63153	08/13/2010	Semiconductor device and method of manufacturing the same
JP	4272175	01/25/2002	2005-82073	03/06/2009	Semiconductor device
KR	392239	09/13/1995	1998-701691	07/09/2003	Polishing method

Country	Patent Number	Filing Date	Application Number	Issue Date	Title
KR	306409	02/06/1998	1998-3534	08/09/2001	Semiconductor device and method for manufacturing the same
KR	494520	03/13/1998	1998-8572	06/01/2005	A semiconductor device and its manufacturing method
KR	604960	02/20/1998	1999-7008647	7/19/2006	The nonvolatile semiconductor memory device and its manufacturing method and a semiconductor device and its manufacturing method
KR	286746	05/19/1998	1998-18023	01/16/2001	Semiconductor device
KR	755912	09/22/1998	2000-7005174	08/30/2007	Semiconductor device
KR	277250	09/12/1998	1998-37689	10/09/2000	A semiconductor device and its manufacturing method
KR	281351	09/30/1998	1998-40783	11/17/2000	Semiconductor device
KR	277324	12/09/1998	1998-53928	10/09/2000	Semiconductor device and method of designing a semiconductor device
KR	686681	01/19/2000	2001-7009651	02/16/2007	Semiconductor intergrated circuit and nonvolatile memory element
KR	322439	03/14/2000	2000-12853	01/16/2002	Etching and cleaning methods and etching and cleaning apparatuses used therefor
KR	704244	10/04/1997	1997-51057	03/30/2007	Semiconductor memory and a method of manufacturing the same.
KR	475256	12/24/1997	1997-73666	02/25/2005	Semiconductor device having nonvolatile memory and its manufacturing method
KR	564180	03/13/1999	1999-8456	03/20/2006	Semiconductor integrated circuit device and process for manufacturing the same

Country	Patent Number	Filing Date	Application Number	Issue Date	Title
KR	570241	01/22/1999	2001-7009213	04/05/2006	Semiconductor integrated circuit and manufacture thereof
KR	324708	03/15/2000	2000-13157	02/02/2002	A semiconductor device
KR	888533	12/26/2002	2002-83912	03/05/2009	Semiconductor device
TW	289164	11/17/1995	84112279	10/21/1996	Non-volatile semiconductor device and process thereof
TW	314656	11/14/1996	85113942	09/01/1997	Seminconductor integrated circuit device
TW	377495	09/17/1997	86113459	12/21/1999	Method of manufacturing semiconductor memory cells and the same apparatus
US		04/08/1997	14/176,328		Method of forming a cmos structure having gate insulation films of different thickness