PATENT ASSIGNMENT COVER SHEET

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Stylesheet Version v1.2

EPAS ID: PAT3079113

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
FREESCALE SEMICONDUCTOR, INC.	06/29/2012

RECEIVING PARTY DATA

Name:	ZOZO MANAGEMENT, LLC
Street Address:	1209 ORANGE STREET
City:	WILMINGTON
State/Country:	DELAWARE
Postal Code:	19801

PROPERTY NUMBERS Total: 86

Property Type	Number
Patent Number:	6020261
Patent Number:	5615473
Patent Number:	6211530
Patent Number:	6248459
Patent Number:	6270568
Patent Number:	6709989
Patent Number:	6087267
Patent Number:	6477692
Patent Number:	6801322
Patent Number:	5666288
Patent Number:	5619418
Patent Number:	5796985
Patent Number:	5790416
Patent Number:	5901065
Patent Number:	5506450
Patent Number:	6709312
Patent Number:	5774358
Patent Number:	5799172
Patent Number:	6944755
Patent Number:	7086027
Patent Number:	6246973

Property Type	Number
Patent Number:	5554889
Patent Number:	5410548
Patent Number:	5587883
Patent Number:	5596172
Patent Number:	5480835
Patent Number:	5508230
Patent Number:	5617035
Patent Number:	5587605
Patent Number:	5589402
Patent Number:	6254685
Patent Number:	5517141
Patent Number:	5583747
Patent Number:	5724557
Patent Number:	5532175
Patent Number:	5968849
Patent Number:	5783475
Patent Number:	5940779
Patent Number:	5743788
Patent Number:	6263605
Patent Number:	6514126
Patent Number:	6361675
Patent Number:	6726826
Patent Number:	6480998
Patent Number:	6952812
Patent Number:	6931611
Patent Number:	6910025
Patent Number:	6536026
Patent Number:	6651227
Patent Number:	7007253
Patent Number:	6925622
Patent Number:	6944806
Patent Number:	7093223
Patent Number:	6925542
Patent Number:	6933614
Patent Number:	6924232
Patent Number:	6933599
Patent Number:	6894937
Patent Number:	7039883
Patent Number:	6920586

Property Type	Number
Patent Number:	7287194
Patent Number:	7195963
Patent Number:	7176133
Patent Number:	7717060
Patent Number:	7402472
Patent Number:	5790415
Patent Number:	5751593
Patent Number:	5920484
Patent Number:	5984510
Patent Number:	6006024
Patent Number:	5987086
Patent Number:	5899745
Patent Number:	5754454
Patent Number:	5903471
Patent Number:	6075934
Patent Number:	6174810
Patent Number:	5966306
Patent Number:	5999717
Patent Number:	5985748
Patent Number:	6221537
Patent Number:	6321186
Patent Number:	6493854
Patent Number:	6165567
Patent Number:	6378112
Patent Number:	6326301
Patent Number:	6551919

CORRESPONDENCE DATA

Fax Number: (512)853-8801

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

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ATTORNEY DOCKET NUMBER:	6686-00000
NAME OF SUBMITTER:	B. NOEL KIVLIN
SIGNATURE:	/B. Noel Kivlin/

DATE SIGNED:	10/23/2014

Total Attachments: 14
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ASSIGNMENT

This Assignment by **Freescale Semiconductor, Inc.**, a corporation duly authorized under the laws of the State of Delaware (hereinafter the "Assignor") witnesseth:

WHEREAS, Assignor is the owner of certain rights, title and interest in and to the patents and patent applications set forth on Schedule A hereto (hereinafter the "Patents and Applications");

WHEREAS, **ZOZO Management, LLC**, a corporation duly organized under and pursuant to the laws of the State of Deleware, and having a principal place of business at 1209 Orange Street, Wilmington, DE 19801 (hereinafter the "Assignee"), is desirous of acquiring the entire right, title and interest in and to said Patents and Applications for Letters Patent of the United States or foreign, and in and to any Letters Patent or Patents, United States or foreign, to be obtained therefor and thereon;

NOW, THEREFORE, for good and valuable consideration, the receipt and adequacy of which is hereby acknowledged, said Assignor has sold, assigned, transferred and set over, and by these presents does sell, assign, transfer and set over, unto said Assignee, its successors, legal representatives and assigns, Assignor's interest in the entire right, title and interest in and to the above-mentioned Patents and Applications, application for Letters Patent, and any and all Letters Patent or Patents in the United States of America and all foreign countries which may be granted therefor and thereon, and in and to any and all divisions, continuations, and continuations-in-part of said application, or reissues or extensions of said Letters Patent or Patents, and all rights under the International Convention for the Protection of Industrial Property, the same to be held and enjoyed by said Assignee, for its own use and behalf and the use and behalf of its successors, legal representatives and assigns, to the full end of the term or terms for which Letters Patent or Patents may be granted, as fully and entirely as the same would have been held and enjoyed by the Assignor, had this sale and assignment not been made. Assignor does hereby sell, assign, transfer, and convey to Assignee, its successors, legal representatives, and assigns all claims for damages and all remedies arising out of any violation of the rights assigned hereby that may have accrued prior to the date of assignment to Assignee, or may accrue hereafter including, but not limited to, the right to sue for, collect, and retain damages for past infringement of the said Patents and Applications before or after issuance.

IN TESTIMONY WHEREOF, 29 day of June 2012.

Freescale Semiconductor, Inc.

By: _____

Changhae Park, PhD
Vice President
Freescale Semiconductor, Inc.

SCHEDULE "A" to Assignment

	Patent	Docket #	Cntry	App #	FilDate	IssDate	Inventors	Title	Status
1	5395740	CM00596L-US	US	08/010224	27-Jan-1993	07-Mar-1995	SWIRBEL, THOMAS J.; DAVIS, JAMES L.; ARLEDGE, JOHN K	METHOD FOR FABRICATING ELECTRODE PATTERNS	Dropped
	5480822	CM00596L-USD01	US	08/275147	18-Jul-1994	24-Oct-1995	SWIRBEL, THOMAS J.; DAVIS, JAMES L.; ARLEDGE, JOHN K	METHOD FOR FABRICATING ELECTRODE PATTERNS	Granted
2	5372188	CM00731L-US	US	08/085807	06-Jul-1993	03-Jan-1995	GOLD, GLENN; SUPPELSA, ANTHONY B; SUPPELSA, ANTHONY J.	ENCAPSULATED ELECTRONIC COMPONENT HAVING A HEAT DIFFUSING LAYER	Granted
3	6021051	CM02709JK-US	US	09/323258	01-Jun-1999	01-Feb-2000	WEISMAN, DOUGLAS H	PROCESS FOR FORMING HIGH ASPECT RATIO CIRCUIT FEATURES	Granted
4	69438186.8	CR07978-DE	DE	94111748.7	28-Jul-1994	25-Oct-2000	WETZEL, CHARLES E; HALCHIN, DAVID J	HALBLEITERBAUELEMENT GESCHUETZT DURCH DIODEN	Dropped
	EP0648517	CR07978-EP	EP	94111748.7	28-Jul-1994	25-Oct-2000	WETZEL, CHARLES E; HALCHIN, DAVID J	DIODE PROTECTED SEMICONDUCTOR DEVICE	Inactive
	EP0648517	CR07978-FR	FR	94111748.7	28-Jul-1994	25-Oct-2000	WETZEL, CHARLES E; HALCHIN, DAVID J	DIODE PROTECTED SEMICONDUCTOR DEVICE	Dropped
	EP0648517	CR07978-GB	GB	94111748.7	28-Jul-1994	25-Oct-2000	WETZEL, CHARLES E; HALCHIN, DAVID J	DIODE PROTECTED SEMICONDUCTOR DEVICE	Dropped
		CR07978-JP	JP	6-202803	05-Aug-1994		WETZEL, CHARLES E; HALCHIN, DAVID J	DIODE PROTECTED SEMICONDUCTOR DEVICE	Inactive
	EP0648517	CR07978-SE	SE	94111748.7	28-Jul-1994	25-Oct-2000	WETZEL, CHARLES E; HALCHIN, DAVID J	DIODE PROTECTED SEMICONDUCTOR DEVICE	Dropped
	5399893	CR07978-US	US	08/111226	24-Aug-1993	21-Mar-1995	WETZEL, CHARLES E; HALCHIN, DAVID J	DIODE PROTECTED SEMICONDUCTOR DEVICE	Granted
5	4142114	CR08321-JP	JP	5-221932	26-Aug-1994	20-Jun-2008	TEHRANI, SAIED NIKOO; ZHU, X THEODORE; GORONKIN, HERBERT; SHEN, JUN	COMPLEMENTARY HETEROJUNCTION DEVICE AND METHOD OF FABRICATING	Granted
	5349214	CR08321-US	US	08/119554	13-Sep-1993	20-Sep-1994	TEHRANI, SAIED NIKOO; ZHU, X THEODORE; GORONKIN, HERBERT; SHEN, JUN	COMPLEMENTARY HETEROJUNCTION D EVICE	Granted
	5427965	CR08321-USD01	US	08/282292	29-Jun-1994	27-Jun-1995	TEHRANI, SAIED NIKOO; ZHU, X THEODORE; GORONKIN, HERBERT; SHEN, JUN	METHOD OF FABRICATING A COMPLE MENTARY HETEROJUNCTION FET	Granted
6	5424698	CR08391-US	US	08/161908	06-Dec-1993	13-Jun-1995	DYDYK, MICHAEL; GOLIO, JOHN MICHAEL; HIGGINS JR, ROBERT J; ARVANITIS, ARISTOTELIS S	A FERRITE/SEMICONDUCTOR RESONATOR/FILTER AND METHOD OF FABRI CATION	Dropped
	5616473	CR08391-USD01	US	08/453855	30-May-1995	01-Apr-1997	DYDYK, MICHAEL; GOLIO, JOHN MICHAEL; HIGGINS JR, ROBERT J; ARVANITIS, ARISTOTELIS S	METHOD OF MAKING A FERRITE/SEM ICONDUCTOR RESONATOR/FILTER	Granted
7	4066973	CR08518-JP	JP	5-271805	12-Oct-1984	21-Mar-2008	TSUI, RAYMOND K	METHOD OF FORMING A QUANTUM MULTI-FUNCTION SEMICONDUCTOR DEVICE	Granted
	5371038	CR08518-US	US	08/139180	21-Oct-1993	06-Dec-1994	TSUI, RAYMOND K	METHOD OF FORMING A QUANTUM MU LTI-FUNCTION SEMICONDUCTOR DEV ICE	Granted
8	6211530	CR98-004-US	US	09/097025	12-Jun-1998	03-Apr-2001	GORONKIN, HERBERT; TSUI, RAYMOND K; ZHANG, RUTH Y.; SHIRALAGI, KUMAR	SPARSE-CARRIER DEVICES AND MET HOD OF FABRICATION	Granted
9	ZL00120218.8	JG99-003-CN	CN	00120218.8	13-Jul-2000	07-Apr-2004	WANG, JUN NMI; OOMS, WILLIAM JAY; HALLMARK, JERALD A	SEMICONDUCTOR STRUCTURE HAVING A CRYSTALLINE ALKALINE EARTH METAL OXIDE INTERFACE WITH SIL ICON	Granted
		JG99-003-EP	EP	00106237.3	22-Mar-2000		WANG, JUN NMI; OOMS, WILLIAM JAY; HALLMARK, JERALD A	SEMICONDUCTOR STRUCTURE HAVING A CRYSTALLINE ALKALINE EARTH METAL OXIDE INTERFACE WITH SIL ICON	Inactive
		JG99-003-HK	HK	02104104.3	31-May-2002		WANG, JUN NMI; OOMS, WILLIAM JAY; HALLMARK, JERALD A	SEMICONDUCTOR STRUCTURE HAVING A CRYSTALLINE ALKALINE EARTH METAL OXIDE INTERFACE WITH SIL ICON	Inactive
		JG99-003-JP	JP	2000-85098	09-Mar-2000		WANG, JUN NMI; OOMS, WILLIAM JAY; HALLMARK, JERALD A	SEMICONDUCTOR STRUCTURE HAVING A CRYSTALLINE ALKALINE EARTH METAL OXIDE INTERFACE WITH SILICON	Inactive
		JG99-003-KR	KR	10-2000-0012758	14-Mar-2000		WANG, JUN NMI; OOMS, WILLIAM JAY; HALLMARK, JERALD A	SEMICONDUCTOR STRUCTURE HAVING A CRYSTALLINE ALKALINE EARTH METAL OXIDE INTERFACE WITH SIL ICON	Inactive
		JG99-003-SG	SG	200001965-3	17-Jul-2000		WANG, JUN NMI; OOMS, WILLIAM JAY; HALLMARK, JERALD A	SEMICONDUCTOR STRUCTURE HAVING A CRYSTALLINE ALKALINE EARTH METAL OXIDE INTERFACE WITH SIL ICON	Inactive
	90-158099	JG99-003-TW	TW	89104672	15-Mar-2000	01-Jul-2002	WANG, JUN NMI; OOMS, WILLIAM JAY; HALLMARK, JERALD A	SEMICONDUCTOR STRUCTURE HAVING A CRYSTALLINE ALKALINE EARTH METAL OXIDE INTERFACE WITH SIL ICON	Granted
	6248459	JG99-003-US	US	09/274268	22-Mar-1999	19-Jun-2001	WANG, JUN NMI; OOMS, WILLIAM JAY; HALLMARK, JERALD A	SEMICONDUCTOR STRUCTURE HAVING A CRYSTALLINE ALKALINE EARTH METAL OXIDE INTERFACE WITH SIL ICON	Granted

	ZL00120285.3	JG99-010-CN	CN	00120285.3	14-Jul-2000	07-Apr-2004	DROOPAD, RAVINDRANATH; YU, ZHIYI JIMMY; RAMDANI, JAMAL	METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE WITH REDUCED LEAKAGE CURRENT DENSITY	Granted
		JG99-010-EP	EP	00115127.3	12-Jul-2000		DROOPAD, RAVINDRANATH; YU, ZHIYI JIMMY; RAMDANI, JAMAL	METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE WITH REDUCED LEAKAGE CURRENT DENSITY	Inactive
		JG99-010-JP	JP	2000-213805	14-Jul-2000		DROOPAD, RAVINDRANATH; YU, ZHIYI JIMMY; RAMDANI, JAMAL	METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE WITH REDUCED LEAKAGE CURRENT DENSITY	Inactive
10		JG99-010-KR	KR	10-2000-0039467	11-Jul-2000		DROOPAD, RAVINDRANATH; YU, ZHIYI JIMMY; RAMDANI, JAMAL	METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE WITH REDUCED LEAKAGE CURRENT DENSITY	Inactive
	85711	JG99-010-SG	SG	200003682-8	03-Jul-2000	31-Oct-2002	DROOPAD, RAVINDRANATH; YU, ZHIYI JIMMY; RAMDANI, JAMAL	METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE WITH REDUCED LEAKAGE CURRENT DENSITY	Granted
	NI-147864	JG99-010-TW	TW	89114108	14-Jul-2000	01-Jan-2002	DROOPAD, RAVINDRANATH; YU, ZHIYI JIMMY; RAMDANI, JAMAL	METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE WITH REDUCED LEAKAGE CURRENT DENSITY	Granted
	6270568	JG99-010-US	US	09/354173	15-Jul-1999	07-Aug-2001	DROOPAD, RAVINDRANATH; YU, ZHIYI JIMMY; RAMDANI, JAMAL	METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE WITH REDUCED LEAKAGE CURRENT DENSITY	Granted
	ZL00131682.1	JG99-015-CN	CN	00131682.1	24-Oct-2000	06-Apr-2005	RAMDANI, JAMAL; DROOPAD, RAVINDRANATH; YU, ZHIYI JIMMY	METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE INCLUDING A METAL OXIDE INTERFACE WITH SILICON	Granted
		JG99-015-EP	EP	00122869.9	23-Oct-2000		RAMDANI, JAMAL; DROOPAD, RAVINDRANATH; YU, ZHIYI JIMMY	METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE INCLUDING A METAL OXIDE INTERFACE WITH SILICON	Dropped
		JG99-015-JP	JP	2000-323458	23-Oct-2000		RAMDANI, JAMAL; DROOPAD, RAVINDRANATH; YU, ZHIYI JIMMY	METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE INCLUDING A METAL OXIDE INTERFACE WITH SILICON	Inactive
	714078	JG99-015-KR	KR	10-2000-0060223	13-Oct-2000	26-Apr-2007	RAMDANI, JAMAL; DROOPAD, RAVINDRANATH; YU, ZHIYI JIMMY	METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE INCLUDING A METAL OXIDE INTERFACE WITH SILICON	Granted
11	99871	JG99-015-SG	SG	200005662-2	03-Oct-2000	30-Apr-2009	RAMDANI, JAMAL; DROOPAD, RAVINDRANATH; YU, ZHIYI JIMMY	METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE INCLUDING A METAL OXIDE INTERFACE WITH SILICON	Granted
	NI-148130	JG99-015-TW	TW	89120550	03-Oct-2000	11-Dec-2001	RAMDANI, JAMAL; DROOPAD, RAVINDRANATH; YU, ZHIYI JIMMY	METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE INCLUDING A METAL OXIDE INTERFACE WITH SILICON	Granted
		JG99-015-US	US	09/423945	25-Oct-1999		RAMDANI, JAMAL; DROOPAD, RAVINDRANATH; YU, ZHIYI JIMMY	METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE INCLUDING A METAL OXIDE INTERFACE WITH SILICON	Inactive
		JG99-015-USCD1	US	10/160196	11-Jun-2002		RAMDANI, JAMAL; DROOPAD, RAVINDRANATH; YU, ZHIYI JIMMY	METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE INCLUDING A METAL OXIDE INTERFACE WITH SILICON	Inactive
9	6709989	JG99-015-USPO1	US	09/885408	21-Jun-2001	23-Mar-2004	RAMDANI, JAMAL; DROOPAD, RAVINDRANATH; YU, ZHIYI JIMMY	METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE INCLUDING A MONOCRYSTALLINE METAL OXIDE INTERFACE WITH SILICON	Granted
12	5463306	PT00277U-US	US	08/063498	19-Jul-1993	31-Oct-1995	BERRY, JAMES E; FACE, GARY LEE; HEROLD, BARRY W; MCLAUGHLIN, KEVIN T; GRAHAM-MEIGHAN, MARGARET	APPARATUS FOR DETECTING COMPLETION OF ENERGY TRANSFER IN AN INDUCTIVE DC TO DC CONVERTER	Granted
13	5345235	PT00285U-US	US	08/044662	13-Apr-1993	06-Sep-1994	BABCOCK, MARK H	SCALED REFERENCE ANALOG TO DIGITAL CONVERSION CIRCUITRY AND METHOD OF OPERATION	Granted
14	5337027	PT00471U-US	US	08/147235	04-Nov-1993	09-Aug-1994	BARRETT JR, RAYMOND L; HEROLD, BARRY W	HIGH EFFICIENCY CLASS AB TRANS CONDUCTANCE AMPLIFIER	Granted
15	6057257	SC00088A-US	US	08/838648	04-Mar-1986	11-Jul-2000	DOCKREY, J. WILLIAM; THOMAS, PATRICK K.; HARTMAN, DENNIS C.	PROCESS FOR FORMING AN INTEGRATED CIRCUIT	Granted
		SC00088A-WO	WO	86-02723	19-Dec-1986		DOCKREY, J. WILLIAM; THOMAS, PATRICK K.; HARTMAN, DENNIS C.	SELECTIVE ETCH PROCESS HAVING REDUCED CARBON EFFECT	Inactive
16	69732287.8	SC00027WR.DE	DE	97919783.8	23-Jan-1997	21-May-2003	MARCHENKO, ALEXANDER MICHAILOVITCH; PLIS, ANDREY PETROVITCH; SHIRO, EUGENE; SOTNIKOV, MIKHAIL ANATOLEVITCH; TOPOUZOV, IGOR; MCGUINNESS, PATRICK J.	A METHOD FOR MANUFACTURING AN ELECTRONIC DEVICE HAVING A CHANNEL	Dropped
	EP1010198	SC00027WR.EP	EP	97919783.8	23-Jan-1997	21-May-2003	MARCHENKO, ALEXANDER MICHAILOVITCH; PLIS, ANDREY PETROVITCH; SHIRO, EUGENE; SOTNIKOV, MIKHAIL ANATOLEVITCH; TOPOUZOV, IGOR; MCGUINNESS, PATRICK J.	A METHOD FOR MANUFACTURING AN ELECTRONIC DEVICE HAVING A CHANNEL	Inactive

	EP19101 08	SC0027WR-FR	FR	97919793.8	23-Jan-1997	21-May-2003	MARCHENKO, ALEXANDER MICHAILOVITCH; PLIS, ANDREY PETROVITCH; SHIRO, EUGENE; SOTNIKOV, MIKHAIL ANATOLEVITCH; TOPOUZOV, IGOR; MCGUINNESS, PATRICK J.	A METHOD FOR MANUFACTURING AN ELECTRONIC DEVICE HAVING A CHA NNEL	Dropped
	EP19101 08	SC0027WR-GB	GB	97919793.8	23-Jan-1997	21-May-2003	MARCHENKO, ALEXANDER MICHAILOVITCH; PLIS, ANDREY PETROVITCH; SHIRO, EUGENE; SOTNIKOV, MIKHAIL ANATOLEVITCH; TOPOUZOV, IGOR; MCGUINNESS, PATRICK J.	A METHOD FOR MANUFACTURING AN ELECTRONIC DEVICE HAVING A CHA NNEL	Dropped
		SC0027WR-JP	JP	10-531676	23-Jan-1997		MARCHENKO, ALEXANDER MICHAILOVITCH; PLIS, ANDREY PETROVITCH; SHIRO, EUGENE; SOTNIKOV, MIKHAIL ANATOLEVITCH; TOPOUZOV, IGOR; MCGUINNESS, PATRICK J.	A METHOD FOR MANUFACTURING AN ELECTRONIC DEVICE HAVING A CHANNEL	Inactive
	6477592	SC0027WR-US	US	09/355144	22-Jul-1999	05-Nov-2002	MARCHENKO, ALEXANDER MICHAILOVITCH; PLIS, ANDREY PETROVITCH; SHIRO, EUGENE; SOTNIKOV, MIKHAIL ANATOLEVITCH; TOPOUZOV, IGOR; MCGUINNESS, PATRICK J.	METHOD AND APPARATUS FOR CHANNEL ROUTING OF AN ELECTRONIC DEVICE	Granted
		SC0027WR-WO	WO	PCT/IB97/0 0038	23-Jan-1997		MARCHENKO, ALEXANDER MICHAILOVITCH; PLIS, ANDREY PETROVITCH; SHIRO, EUGENE; SOTNIKOV, MIKHAIL ANATOLEVITCH; TOPOUZOV, IGOR; MCGUINNESS, PATRICK J.	A METHOD FOR MANUFACTURING AN ELECTRONIC DEVICE HAVING A CHA NNEL	Inactive
17	2268648	SC0170E1-GB	GB	9214161.1	02-Jul-1992	21-Aug-1996	BARON, NATAN; ADELMAN, JUDAH L.; VOLPERT, YEHUDA	A LOCK DETECTION CIRCUIT FOR A PHASE LOCK LOOP	Dropped
	5327103	SC0170E1-US	US	08/086263	29-Jun-1993	05-Jul-1994	BARON, NATAN; ADELMAN, JUDAH L.; VOLPERT, YEHUDA	A LOCK DETECTION CIRCUIT FOR A PHASE LOCK LOOP	Granted
	P6940860 41.0	SC0175DA-DE	DE	9410468.0	24-Mar-1994	08-Oct-1997	YU, CHRIS CHANG	POLISHING PAD AND METHOD OF PO LISHING A SEMICONDUCTOR SUBSTR ATE	Inactive
	EP0832188	SC0175DA-EP	EP	9410468.0	24-Mar-1994	08-Oct-1997	YU, CHRIS CHANG	POLISHING PAD AND METHOD OF PO LISHING A SEMICONDUCTOR SUBSTR ATE	Inactive
	EP0832188	SC0175DA-FR	FR	9410468.0	24-Mar-1994	08-Oct-1997	YU, CHRIS CHANG	POLISHING PAD AND METHOD OF PO LISHING A SEMICONDUCTOR SUBSTR ATE	Inactive
	EP0832188	SC0175DA-GB	GB	9410468.0	24-Mar-1994	08-Oct-1997	YU, CHRIS CHANG	POLISHING PAD AND METHOD OF PO LISHING A SEMICONDUCTOR SUBSTR ATE	Inactive
18	EP0832188	SC0175DA-IT	IT	9410468.0	24-Mar-1994	08-Oct-1997	YU, CHRIS CHANG	POLISHING PAD AND METHOD OF PO LISHING A SEMICONDUCTOR SUBSTR ATE	Dropped
	3425216	SC0175DA-JP	JP	6-101749	18-Apr-1994	02-May-2003	YU, CHRIS CHANG	METHOD OF POLISHING A SEMICOND UCTOR SUBSTRATE	Dropped
		SC0175DA-KR	KR	94-6232	26-Apr-1994		YU, CHRIS CHANG	POLISHING PAD AND METHOD OF PO LISHING A SEMICONDUCTOR SUBSTR ATE	Inactive
	88-87316	SC0175DA-TW	TW	83102934	06-Mar-1994	06-Dec-1994	YU, CHRIS CHANG	POLISHING PAD AND METHOD OF PO LISHING A SEMICONDUCTOR SUBSTR ATE	Granted
	5328734	SC0175DA-US	US	08/054188	30-Apr-1993	19-Jul-1994	YU, CHRIS CHANG	POLISHING PADS USED TO CHEMICA L-MECHANICAL POLISH A SEMICOND UCTOR SUBSTRATE	Granted
	368604	SC0229BA-KR	KR	10-1995-0007691	31-Mar-1995	06-Jan-2003	FILIPIAK, STANLEY M.; GELATOS, AVGERINOS V.	METHOD FOR CAPPING COPPER IN S EMICONDUCTOR DEVICES	Granted
19	Nr. 078046	SC0229BA-TW	TW	84101465	17-Feb-1995	06-May-1998	FILIPIAK, STANLEY M.; GELATOS, AVGERINOS V.	METHOD FOR CAPPING COPPER IN S EMICONDUCTOR DEVICES	Granted
	5447887	SC0229BA-US	US	08/222759	01-Apr-1994	05-Sep-1995	FILIPIAK, STANLEY M.; GELATOS, AVGERINOS V.	METHOD FOR CAPPING COPPER IN S EMICONDUCTOR DEVICES	Granted
		SC0232WD-TW	TW	091139979	13-Dec-2002		MAUTZ, KARL EMERSON	METHOD AND APPARATUS FOR MEASURING A REQUIRED CHARACTERISTIC OF A LAYER AND MEASURING APPARATUS	Inactive
20	6801322	SC0232WD-US	US	10/021756	13-Dec-2001	05-Oct-2004	MAUTZ, KARL EMERSON	METHOD AND APPARATUS FOR MEASURING A REQUIRED FEATURE OF A LAYER DURING A POLISHING PROCESS	Granted
		SC0232WD-WO	WO	PCT/US02/3 9563	03-Dec-2002		MAUTZ, KARL EMERSON	METHOD FOR MEASURING A REQUIRED CHARACTERISTIC OF A LAYER AND MEASURING APPARATUS	Inactive
21	5966298	SC0252BA-US	US	08/428211	21-Apr-1995	59-Sep-1997	JONES, LARRY G.; MAZIASZ, ROBERT L.; GURUSWAMY, MOHANKUMAR; BLAAUW,	METHOD AND APPARATUS FOR DESIG NING AN INTEGRATED CIRCUIT	Granted

								DAVID T.	
22		5819418	SC02563A-US	US	08/382210	16-Feb-1995	06-Apr-1997	BLAAUW, DAVID T.; NORTON, JOSEPH W.; JONES, LARRY G.; MISRA, SUSANTA; BAHAR, RUTH I.	LOGIC GATE SIZE OPTIMIZATION P ROCESS FOR AN INTEGRATED CIRCU IT WHEREBY CIRCUIT SPEED IS IM PROVED WHILE CIRCUIT AREA IS O PTIMIZED	Granted
23		5795985	SC02707A-US	US	08/839393	29-Apr-1997	18-Aug-1998	O'BRIEN, PETER R.; WILEY, RICHARD P.	METHOD AND APPARATUS FOR INCORP ORATING A MILLER COMPENSATION FOR MODELING ELECTRICAL CIRCU ITS	Granted
24		5790418	SC02758A-US	US	08/529772	18-Sep-1995	04-Aug-1998	NORTON, JOSEPH W.; BLAAUW, DAVID T.; JONES, LARRY G.	UPDATING HIERARCHICAL DAG REPR ESENTATIONS THROUGH A BOTTOM U P METHOD	Granted
25		5801585	SC02760A-US	US	08/697768	07-Feb-1996	04-May-1999	GUSUSWAMY, MOHANKUMAR; GULITZ, DANIEL W.; MAZIASZ, ROBERT L.	APPARATUS AND METHOD FOR AUTOM ATICALLY PLACING TRS AND CONN ECTION ELEMENTS WITHIN AN INTE GRATED CIRCUIT	Granted
26		5506450	SC02772A-US	US	08/435107	04-May-1995	09-Apr-1996	LEE, CHIL-CHANG; KAWASAKI, HISAO	SEMICONDUCTOR DEVICE WITH IMPR OVED ELECTOMIGRATION RESISTANC E AND METHOD FOR MAKING THE SA ME	Granted
		I275449	SC0302WD-TW	TW	092116540	18-Jun-2003	11-Mar-2007	MAUTZ, KARL EMERSON	METHOD AND APPARATUS FOR MONITORING A POLISHING CONDITION OF A SURFACE OF A WAFER IN A POLISHING PROCESS	Granted
27	a	6769212	SC0302WD-US	US	10/180740	26-Jun-2002	03-Mar-2004	MAUTZ, KARL EMERSON	METHOD AND APPARATUS FOR MONITORING A POLISHING CONDITION OF A SURFACE OF A WAFER IN A POLISHING PROCESS	Granted
			SC0302WD-WO	WO	PCT/US03/1 9464	23-Apr-2003		MAUTZ, KARL EMERSON	METHOD AND APPARATUS FOR MONITORING A POLISHING CONDITION OF A SURFACE OF A WAFER IN A POLISHING PROCESS	Inactive
28		5774368	SC0304A-US	US	08/825153	01-Apr-1997	30-Jun-1998	SHROTE, CURTIS K.	METHOD AND APPARATUS FOR GENER ATING INSTRUCTION/DATA STREAMS EMPLOYED TO VERIFY HARDWARE IM PLEMENTATIONS OF INTEGRATED CI RCUIT DESIGNS	Granted
29		5798172	SC0317A-US	US	08/711638	10-Sep-1996	25-Aug-1998	GULLAPALLI, KIRAN K.; BECKERICH, STEVEN; HAMM, STEVE; MULVANEY, BRIAN J.	METHOD OF SIMULATING AN INTEGR ATED CIRCUIT	Granted
30	a	6944795	SC0338W1-US	US	09/910554	20-Jul-2001	13-Sep-2005	GUR, AMIT; RIZI, HAIM; HALAHMI, DROR	METHOD AND APPARATUS FOR EXTRACTING A PORTION OF DATA IN A SOURCE REGISTER AND ARRANGING IT ON ONE SIDE OF A DESTINATION REGISTER	Granted
31	a	7086027	SC0348WR-US	US	10/632111	29-Oct-2003	01-Aug-2006	CHILUVURI, VENKATA K. R.; MARCHENKO, ALEXANDER MICHAILOVITCH; SOTNIKOV, MIKHAIL ANATOLEVITCH	METHOD AND APPARATUS FOR CONSTRAINT GRAPH BASED LAYOUT COMPACTION FOR INTEGRATED CIRCUITS	Granted
			SC0348WR-WO	WO	PCT/RU03/0 0280	05-Jul-2003		CHILUVURI, VENKATA K. R.; MARCHENKO, ALEXANDER MICHAILOVITCH; SOTNIKOV, MIKHAIL ANATOLEVITCH	METHOD AND APPARATUS FOR CONSTRAINT GRAPH BASED LAYOUT COMPACTION FOR INTEGRATED CIRCUITS	Inactive
32		3402528	SC0834AJ-JP	JP	10-244418	14-Aug-1998	14-Nov-2003	SEKINE, SATOSHI	A MODELING METHOD OF MOSFET EL ECTRIC CHARACTERISTICS	Dropped
		6346973	SC0834AJ-US	US	09/373980	12-Aug-1999	12-Jun-2001	SEKINE, SATOSHI	MODELING METHOD OF MOSFET	Granted
			SC0772IP-US	US	882710	03-Apr-1992		SHIN, HANK HYUN KYOO; TRACY, CLARENCE J.; DUFFIN, ROBERT L.; FREEMAN, JR., JOHN L.; GRIVNA, GORDON M.; WILSON, SYD ROBERT	STRUCTURE AND METHOD FOR METAL LIZATION OF SEMICONDUCTOR DEVI CES	Inactive
33		5701721	SC0772IP-USDIV1	US	08/668041	04-Jun-1996	23-Dec-1997	SHIN, HANK HYUN KYOO; TRACY, CLARENCE J.; DUFFIN, ROBERT L.; FREEMAN, JR., JOHN L.; GRIVNA, GORDON M.; WILSON, SYD ROBERT	STRUCTURE AND METHOD FOR METAL LIZATION OF SEMICONDUCTOR DEVI CES	Expired
		5554869	SC0772IP-USFW01	US	08/430105	27-Apr-1995	10-Sep-1996	SHIN, HANK HYUN KYOO; TRACY, CLARENCE J.; DUFFIN, ROBERT L.; FREEMAN, JR., JOHN L.; GRIVNA, GORDON M.; WILSON, SYD ROBERT	STRUCTURE AND METHOD FOR METAL LIZATION OF SEMICONDUCTOR DEVI CES	Granted
34		5340993	SC0778CT-US	US	08/054483	30-Apr-1993	23-Aug-1994	SALINA, JOHN; BROWN, CLEM N	OPTOCOUPLER PACKAGE WITH INTEG RAL VOLTAGE ISOLATION BARRIER	Granted
35		5410548	SC0807SS-US	US	07/987311	28-Oct-1992	25-Apr-1995	MILLMAN, STEVEN D.	TEST PATTERN FAULT EQUIVALENCE	Granted
36		5276368	SC0808BC-US	US	07/865567	02-Oct-1992	04-Jan-1994	GUDGLEY, JOHN R.; CARAVELLA, JAMES S.	DIGITAL VOLTAGE LEVEL TRANSLAT OR CIRCUIT	Granted
37			SC0810IP-JP	JP	5-343367	17-Dec-1993		LEISK, ISRAEL ARNOLD	METHOD OF PROCESSING A POLYCIDE STRUCTURE	Inactive

	5369578	SC09108P-US	US	07/957425	28-Dec-1992	14-Feb-1995	LESK, ISRAEL ARNOLD	METHOD OF PROCESSING A POLYOID E STRUCTURE	Granted
39	5398932	SC09124T-US	US	08/080168	04-Jun-1993	16-Aug-1994	THEODORE, N. DAVID; CARREJO, JUAN PABLO	METHOD AND APPARATUS FOR MEASU RING THE TOPOLOGY OF A SEMICON DUCTOR DEVICE	Granted
36	5397917	SC09134T-US	US	08/051954	26-Apr-1993	14-Mar-1995	OMMEN, DENISE MARIE; BAIRD, JOHN; TSAI, CHI-TAO LI	SEMICONDUCTOR PACKAGE CAPABLE OF SPREADING HEAT AND METHOD O F FORMING	Granted
40	5352926	SC09166T-US	US	08/080080	04-Jun-1993	04-Oct-1994	ANDREWS, JAMES A	FLIP CHIP PACKAGE AND METHOD F OR MAKING	Granted
41	5341884	SC09169T-US	US	07/988411	07-Dec-1992	30-Aug-1994	ADAMS, VICTOR J; GRIEST, SIDNEY H; HART JR, JOHN WILLIAM	PRESSURE SENSOR BUILT INTO A C ABLE CONNECTOR	Granted
	PI9303868 7.3	SC09173P-DE	DE	8310875D.8	01-Jun-1993	18-Dec-1996	BENNETT, PAUL THOMAS; GUTTERIDGE, RONALD JAMES; KOURY, DANIEL N., JR.; MIETUS, DAVID FRANCIS; RISTIC, LJUBISA	LATERALLY SENSITIVE ACCELEROME TER AND METHOD FOR MAKING	Dropped
	EP0562792	SC09173P-EP	EP	8310875D.8	01-Jun-1993	18-Dec-1996	BENNETT, PAUL THOMAS; GUTTERIDGE, RONALD JAMES; KOURY, DANIEL N., JR.; MIETUS, DAVID FRANCIS; RISTIC, LJUBISA	LATERALLY SENSITIVE ACCELEROME TER AND METHOD FOR MAKING	Inactive
	EP0562792	SC09173P-FR	FR	8310875D.8	01-Jun-1993	18-Dec-1996	BENNETT, PAUL THOMAS; GUTTERIDGE, RONALD JAMES; KOURY, DANIEL N., JR.; MIETUS, DAVID FRANCIS; RISTIC, LJUBISA	LATERALLY SENSITIVE ACCELEROME TER AND METHOD FOR MAKING	Dropped
42	EP0562792	SC09173P-GB	GB	8310875D.8	01-Jun-1993	18-Dec-1996	BENNETT, PAUL THOMAS; GUTTERIDGE, RONALD JAMES; KOURY, DANIEL N., JR.; MIETUS, DAVID FRANCIS; RISTIC, LJUBISA	LATERALLY SENSITIVE ACCELEROME TER AND METHOD FOR MAKING	Dropped
	HK1004293	SC09173P-HK	HK	98102985.8	06-Apr-1998	28-Nov-1998	BENNETT, PAUL THOMAS; GUTTERIDGE, RONALD JAMES; KOURY, DANIEL N., JR.; MIETUS, DAVID FRANCIS; RISTIC, LJUBISA	LATERALLY SENSITIVE ACCELEROME TER AND METHOD FOR MAKING	Dropped
		SC09173P-JP	JP	5-203212	21-Jul-1993		BENNETT, PAUL THOMAS; GUTTERIDGE, RONALD JAMES; KOURY, DANIEL N., JR.; MIETUS, DAVID FRANCIS; RISTIC, LJUBISA	LATERALLY SENSITIVE ACCELEROME TER AND METHOD FOR MAKING	Inactive
	5337606	SC09173P-US	US	07/923618	10-Aug-1992	16-Aug-1994	BENNETT, PAUL THOMAS; GUTTERIDGE, RONALD JAMES; KOURY, DANIEL N., JR.; MIETUS, DAVID FRANCIS; RISTIC, LJUBISA	LATERALLY SENSITIVE ACCELEROME TER AND METHOD FOR MAKING	Granted
43	5381159	SC09193T-US	US	08/017158	12-Feb-1993	10-Jan-1995	PHIPPS, JOHN P	METHOD OF TESTING A SEMICONDUC TOR DEVICE	Granted
	3036248	SC09212T-JP	JP	5-338977	03-Dec-1993	03-Mar-2000	OLSON, TIMOTHY LEE; CARNEY, LAURIANN TUCKER; JOHNSON, GARY C; STROM, WILLIAM M.	LEAD FRAME ASSEMBLY FOR SURFACE MOUNT INTEGRATED CIRCUIT POWER PACKAGE	Granted
		SC09212T-KR	KR	93-19859	25-Sep-1993		OLSON, TIMOTHY LEE; CARNEY, LAURIANN TUCKER; JOHNSON, GARY C; STROM, WILLIAM M.	LEAD FRAME ASSEMBLY FOR SURFAC E MOUNT INTEGRATED CIRCUIT POW ER PACKAGE	Inactive
		SC09212T-US	US	985095	03-Dec-1992		OLSON, TIMOTHY LEE; CARNEY, LAURIANN TUCKER; JOHNSON, GARY C; STROM, WILLIAM M.	LEAD FRAME ASSEMBLY FOR SURFAC E MOUNT INTEGRATED CIRCUIT POW ER PACKAGE	Inactive
44		SC09212T-USPW01	US	08/215009	18-Mar-1994		OLSON, TIMOTHY LEE; CARNEY, LAURIANN TUCKER; JOHNSON, GARY C; STROM, WILLIAM M.	LEAD FRAME ASSEMBLY FOR SURFAC E MOUNT INTEGRATED CIRCUIT POW ER PACKAGE	Inactive
		SC09212T-USPW02	US	08/379638	23-Jan-1995		OLSON, TIMOTHY LEE; CARNEY, LAURIANN TUCKER; JOHNSON, GARY C; STROM, WILLIAM M.	LEAD FRAME ASSEMBLY FOR SURFAC E MOUNT INTEGRATED CIRCUIT POW ER PACKAGE	Inactive
	5587883	SC09212T-USPW03	US	08/557667	13-Nov-1995	24-Dec-1996	OLSON, TIMOTHY LEE; CARNEY, LAURIANN TUCKER; JOHNSON, GARY C; STROM, WILLIAM M.	LEAD FRAME ASSEMBLY FOR SURFAC E MOUNT INTEGRATED CIRCUIT POW ER PACKAGE	Granted
		SC09217P-EP	EP	93117874.3	04-Nov-1993		GRUPEN-SHEMANSKY, MELISSA E	METHOD FOR THINNING A SEMICOND UCTOR WAFER	Inactive
		SC09217P-JP	JP	5-343287	17-Dec-1993		GRUPEN-SHEMANSKY, MELISSA E	METHOD FOR THINNING A SEMICOND UCTOR WAFER	Inactive
45		SC09217P-SG	SG	9602148-9	04-Nov-1993		GRUPEN-SHEMANSKY, MELISSA E	METHOD FOR THINNING A SEMICOND UCTOR WAFER	Inactive
	5368685	SC09217P-US	US	07/982854	31-Dec-1992	07-Dec-1993	GRUPEN-SHEMANSKY, MELISSA E	METHOD FOR THINNING A SEMICOND UCTOR WAFER	Granted
		SC09239P-US	US	08/057936	07-May-1993		RASKIN, GLENN DAVID; COLE, SETSUKO JEANNIE; HOGGATT, MARK CHARLES	PLANAR ENCAPSULATION PROCESS	Inactive
46	5696172	SC09239P-USPW01	US	08/560828	17-Nov-1995	21-Jan-1997	RASKIN, GLENN DAVID; COLE, SETSUKO JEANNIE; HOGGATT, MARK CHARLES	PLANAR ENCAPSULATION PROCESS	Granted
		SC09255P-US	US	08/057396	06-May-1993		CARNEY, JR., FRANCIS JOSEPH; CARNEY, GEORGE FRANCIS; MITCHELL, DOUGLAS G	AN ELECTRICAL INTERCONNECT AND METHOD FOR FORMING THE SAME	Inactive
47	5460318	SC09255P-USPW01	US	08/350395	05-Dec-1994	03-Jan-1996	CARNEY, JR., FRANCIS JOSEPH; CARNEY, GEORGE FRANCIS; MITCHELL, DOUGLAS G	AN ELECTRICAL INTERCONNECT AND METHOD FOR FORMING THE SAME	Granted
48	5389579	SC09280P-US	US	08/043117	05-Apr-1993	14-Feb-1995	WELLS, RAYMOND G	METHOD FOR SINGLE SIDED POLISH ING OF A	Granted

								SEMICONDUCTOR WAFER	
49	5373467	SC083628-US	US	08/038385	29-Mar-1993	13-Dec-1994	GEORGE, BINAY J; WILCKA, MARKUS; TYLER, SEAN	METHOD FOR DERIVING A PIECEWISE LINEAR MODEL	Granted
50	5372512	SC083577-US	US	08/082841	28-Jun-1993	13-Dec-1994	CRONIN, WAYNE ALLEN; BARTON JR, FRANCIS W; KOETZ, KIRBY FERDINAND	SEMICONDUCTOR MATERIAL CONTACT ING MEMBER	Granted
51	5304953	SC083844C-US	US	08/082012	01-Jun-1993	19-Apr-1994	HEIM, BARRY S; RODEL, MICHAEL W; HU, TZU-HUI (PAUL)	LOCK RECOVERY CIRCUIT FOR A PH ASE LOCKED LOOP	Granted
52		SC083787-EP	EP	94109608.1	27-Jun-1994		ANDERSON JR, GEORGE P; POLLOCK, RANDY L.	A SEMICONDUCTOR DEVICE WITH IM PROVED HEAT DISSIPATION	Inactive
		SC083787-JP	JP	6-193891	27-Jul-1994		ANDERSON JR, GEORGE P; POLLOCK, RANDY L.	A SEMICONDUCTOR DEVICE WITH IM PROVED HEAT DISSIPATION	Inactive
		SC083787-US	US	098883	28-Jul-1993		ANDERSON JR, GEORGE P; POLLOCK, RANDY L.	A SEMICONDUCTOR DEVICE WITH IM PROVED HEAT DISSIPATION	Inactive
	5508230	SC083787-US2D1	US	08/418236	04-Apr-1995	16-Apr-1996	ANDERSON JR, GEORGE P; POLLOCK, RANDY L.	METHOD OF MAKING A SEMICONDUCT OR DEVICE WITH DIAMOND HEAT DI SSIPATION	Granted
53	5381095	SC083790-US	US	08/089912	08-Jul-1993	10-Jan-1995	FISCHER, LYNN ROY	PHASE LOCK LOOP WITH SELF TEST CIRCUITRY AND METHOD FOR USING THE SAME	Granted
54	3308743	SC084057-JP	JP	6-326552	16-Nov-1994	17-May-2002	CERGEL, LUBOMIR; JOHNSON, BARRY C; STAFFORD, JOHN W	AN ELECTRICAL CONTACT AND METHOD FOR MAKING AN ELECTRICAL CONTACT	Granted
	338187	SC084057-KR	KR	10-1994-0029128	08-Nov-1994	14-May-2002	CERGEL, LUBOMIR; JOHNSON, BARRY C; STAFFORD, JOHN W	AN ELECTRICAL CONTACT AND METHOD FOR MAKING AN ELECTRICAL CONTACT	Granted
	5448047	SC084057-US	US	08/154575	19-Nov-1993	29-Aug-1995	CERGEL, LUBOMIR; JOHNSON, BARRY C; STAFFORD, JOHN W	AN ELECTRICAL CONTACT AND METH OD FOR MAKING AN ELECTRICAL CO NTACT	Granted
55	5396019	SC084177-US	US	08/023407	25-Feb-1993	03-May-1994	MOLINE, DANIEL D; WEIR, BERNARD EDWARD III	LOW INDUCTANCE LEAD FRAME FOR A SEMICONDUCTOR PACKAGE	Granted
56	5467024 X	SC084557-US	US	08/143849	01-Nov-1993	14-Nov-1995	SWAPP, MAVIN CLIFF	METHOD AND APPARATUS FOR TESTI NG INTEGRATED DEVICES	Dropped
	5617038	SC084607-US2D1	US	08/582518	02-Nov-1995	01-Apr-1997	SWAPP, MAVIN CLIFF	METHOD FOR TESTING INTEGRATED DEVICES	Granted
57	ZL94119960.0	SC084657-CN	CN	94119960.0	22-Nov-1994	05-Nov-2003	RAMSEY, KENNETH C.; MILLER, WILLIAM JOSEPH; STROM, WILLIAM M.	PACKAGE FOR MATING WITH A SEMI CONDUCTOR DIE AND METHOD OF MA NUFACTURE	Granted
		SC084657-EP	EP	94117750.3	10-Nov-1994		RAMSEY, KENNETH C.; MILLER, WILLIAM JOSEPH; STROM, WILLIAM M.	PACKAGE FOR MATING WITH A SEMI CONDUCTOR DIE AND METHOD OF MA NUFACTURE	Inactive
	3934689	SC084657-JP	JP	6-309437	21-Nov-1994	30-Mar-2007	RAMSEY, KENNETH C.; MILLER, WILLIAM JOSEPH; STROM, WILLIAM M.	PACKAGE FOR MATING WITH A SEMICONDUCTOR DIE AND METHOD OF MANUFACTURE	Granted
		SC084657-US	US	08/155880	23-Nov-1993		RAMSEY, KENNETH C.; MILLER, WILLIAM JOSEPH; STROM, WILLIAM M.	PACKAGE FOR MATING WITH A SEMI CONDUCTOR DIE AND METHOD OF MA NUFACTURE	Inactive
	5567600	SC084657-US2D1	US	08/473633	07-Jun-1995	24-Dec-1996	RAMSEY, KENNETH C.; MILLER, WILLIAM JOSEPH; STROM, WILLIAM M.	PACKAGE FOR MATING WITH A SEMI CONDUCTOR DIE	Granted
	5989402	SC084657-US2PW01	US	08/650419	30-Oct-1995	31-Dec-1998	RAMSEY, KENNETH C.; MILLER, WILLIAM JOSEPH; STROM, WILLIAM M.	PROCESS FOR MANUFACTURING A PA CKAGE FOR MATING WITH A BARE S EMICONDUCTOR DIE	Granted
58		SC085180-JP	JP	6-220778	24-Aug-1994		HICKMAN, PAT; LAI, STEPHEN WAI-YAN	MEMORY EFFICIENT GATE ARRAY CE LL	Inactive
	5452246	SC085180-US	US	08/134851	07-Sep-1993	19-Sep-1995	HICKMAN, PAT; LAI, STEPHEN WAI-YAN	MEMORY EFFICIENT GATE ARRAY CE LL	Granted
59	5381065	SC085180-US	US	08/089963	29-Jul-1993	10-Jan-1995	LAI, STEPHEN WAI-YAN; DJAJA, GREGORY; MESKEL, SOLOMON G.	CMOS DRIVER USING OUTPUT FEEDB ACK PRE-DRIVE	Granted
60	5346190	SC085220-US	US	08/102833	03-Aug-1993	06-Sep-1994	KAYLOR, SCOTT ALAN	MODULAR LOW VOLTAGE FILTER WIT H COMMON MODE FEEDBACK	Granted
61	95101855.8	SC085340-CN	CN	95101855.8	25-Feb-1995	13-Mar-2002	DE FRESART, EDOUARD D.; STEELE, JOHN W; THEODORE, N. DAVID	METHOD FOR MAKING A SEMICONDUC TOR STRUCTURE	Granted
	19520949.7	SC085340-DE	DE	19520567.5	23-Feb-1995	09-May-2001	DE FRESART, EDOUARD D.; STEELE, JOHN W; THEODORE, N. DAVID	VERFAHREN ZUR HERSTELLUNG EINES BIPOLAREN TRANSISTORS	Dropped
	EP0669647	SC085340-EP	EP	95102567.5	23-Feb-1995	09-May-2001	DE FRESART, EDOUARD D.; STEELE, JOHN W; THEODORE, N. DAVID	METHOD FOR MAKING A SEMICONDUC TOR STRUCTURE	Inactive
	EP0669647	SC085340-FR	FR	95102567.5	23-Feb-1995	09-May-2001	DE FRESART, EDOUARD D.; STEELE, JOHN W; THEODORE, N. DAVID	METHOD FOR MAKING A SEMICONDUC TOR STRUCTURE	Granted
	EP0669647	SC085340-GB	GB	95102567.5	23-Feb-1995	09-May-2001	DE FRESART, EDOUARD D.; STEELE, JOHN W; THEODORE, N. DAVID	METHOD FOR MAKING A SEMICONDUC TOR STRUCTURE	Dropped
	3530254	SC085340-JP	JP	7-60012	24-Feb-1995	09-Mar-2004	DE FRESART, EDOUARD D.; STEELE, JOHN W; THEODORE, N. DAVID	METHOD FOR MAKING A SEMICONDUC TOR STRUCTURE	Granted
	5436190	SC085340-US	US	08/200084	28-Feb-1994	25-Jul-1995	DE FRESART, EDOUARD D.; STEELE, JOHN W; THEODORE, N. DAVID	METHOD FOR MAKING A SEMICONDUC TOR STRUCTURE	Granted
62	5519648	SC085403-US	US	08/154059	18-Nov-1993	21-May-1996	WILCKA, MARKUS; GEORGE, BINAY J; TYLER, SEAN	A METHOD OF CELL CHARACTERIZAT ION IN A DISTRIBUTED SIMULATIO N	Granted

								SYSTEM	
63	5254885	SC08633T-US	US	08/181936	18-Jan-1994	03-Jul-2001	KRAFT, DONALD; HOWARD, EMMETT; HIBBEN, SCOTT	CHEMICAL VAPOR DEPOSITION TRAP WITH TAPERED INLET	Granted
64		SC08639C-EP	EP	94117927.7	14-Nov-1994		BENNETT, PAUL THOMAS; GRAY, RANDALL C; PIGOTT, JOHN M	TEMPERATURE STABLE SQUARE WAVE OSCILLATOR	Inactive
		SC08639C-JP	JP	6-309893	18-Nov-1994		BENNETT, PAUL THOMAS; GRAY, RANDALL C; PIGOTT, JOHN M	OSCILLATOR CIRCUIT	Inactive
	5386201	SC08639C-US	US	08/157548	26-Nov-1993	31-Jan-1995	BENNETT, PAUL THOMAS; GRAY, RANDALL C; PIGOTT, JOHN M	TEMPERATURE STABLE SQUARE WAVE OSCILLATOR	Granted
65		SC08667C-US	US	08/147256	05-Nov-1993		ABDI, BEHROOZ L; STUHLMILLER, GARY	DIFFERENTIAL HIGH SPEED TRACK AND HOLD AMPLIFIER	Inactive
	5517141	SC08667C-USPW01	US	08/420866	18-Mar-1995	14-May-1996	ABDI, BEHROOZ L; STUHLMILLER, GARY	DIFFERENTIAL HIGH SPEED TRACK AND HOLD AMPLIFIER	Granted
66	5338246	SC08670C-US	US	08/140850	25-Oct-1993	13-Jul-1994	MAHABADI, JOHN KOUROS	CIRCUIT AND METHOD OF SETTING A BIAS POINT FOR A SINGLE-ENDED AMPLIFIER DURING POWER UP	Granted
67		SC08683T-US	US	08/143959	01-Nov-1993		BAIRD, JOHN; CARNEY, JR., FRANCIS JOSEPH	THERMOPLASTIC INTERCONNECT FOR ELECTRONIC DEVICE AND METHOD FOR MAKING	Inactive
	5563747	SC08683T-USPW01	US	08/438055	08-May-1995	10-Dec-1996	BAIRD, JOHN; CARNEY, JR., FRANCIS JOSEPH	THERMOPLASTIC INTERCONNECT FOR ELECTRONIC DEVICE AND METHOD FOR MAKING	Granted
68		SC08704P-EP	EP	95111164.0	17-Jul-1995		VARKER, CHARLES J; DREYER, MICHAEL; ZIRKLE, THOMAS E	SEMICONDUCTOR DEVICE INTERCONNECT LAYOUT METHOD AND STRUCTURE FOR REDUCING PREMATURE ELECTROMIGRATION FAILURE DUE TO HIGH LOCALIZED CURRENT DENSITY	Dropped
		SC08704P-JP	JP	7-206772	31-Jul-1995		VARKER, CHARLES J; DREYER, MICHAEL; ZIRKLE, THOMAS E	SEMICONDUCTOR DEVICE INTERCONNECT LAYOUT METHOD AND STRUCTURE FOR REDUCING PREMATURE ELECTROMIGRATION FAILURE DUE TO HIGH LOCALIZED CURRENT DENSITY	Inactive
	5461260	SC08704P-US	US	08/283238	01-Aug-1994	24-Oct-1995	VARKER, CHARLES J; DREYER, MICHAEL; ZIRKLE, THOMAS E	SEMICONDUCTOR DEVICE INTERCONNECT LAYOUT METHOD AND STRUCTURE FOR REDUCING PREMATURE ELECTROMIGRATION FAILURE DUE TO HIGH LOCALIZED CURRENT DENSITY	Granted
		SC08704P-USD01	US	08/473802	07-Jun-1995		VARKER, CHARLES J; DREYER, MICHAEL; ZIRKLE, THOMAS E	SEMICONDUCTOR DEVICE INTERCONNECT LAYOUT METHOD AND STRUCTURE FOR REDUCING PREMATURE ELECTROMIGRATION FAILURE DUE TO HIGH LOCALIZED CURRENT DENSITY	Inactive
	5780478	SC08704P-USD02	US	08/736200	15-Oct-1996	02-Jun-1998	VARKER, CHARLES J; DREYER, MICHAEL; ZIRKLE, THOMAS E	AN INTERCONNECT RUN BETWEEN A FIRST POINT AND A SECOND POINT IN A SEMICONDUCTOR DEVICE FOR REDUCING ELECTROMIGRATION FAILURE	Dropped
69	5439567	SC08758P-US	US	08/234205	28-Apr-1994	25-Apr-1995	LYTLE, WILLIAM H; CHANG, KEVIN HANN; EAST, PETER CHARLES	METHOD OF ETCHING COPPER LAYER S	Granted
70	5534039	SC08827P-US	US	08/283351	29-Jul-1994	02-Apr-1996	GRIVNA, GORDON M	A METHOD FOR MAKING A SELF-ALIGNED OXIDE GATE CAP	Granted
71	5724587	SC08183D-US	US	08/499638	10-Jul-1995	03-Mar-1998	MCBEAN, SR, RONALD V.	METHOD FOR DESIGNING A SIGNAL DISTRIBUTION NETWORK	Granted
72		SC08208P-EP	EP	96105709.8	11-Apr-1996		RACANELLI, MARCO; HWANG, BOR-YUAN	METHOD OF ADJUSTING A THRESHOLD VOLTAGE FOR A SEMICONDUCTOR DEVICE FABRICATED ON A SEMICONDUCTOR ON INSULATOR SUBSTRATE	Inactive
		SC08208P-JP	JP	8-138857	09-Apr-1996		RACANELLI, MARCO; HWANG, BOR-YUAN	METHOD OF ADJUSTING A THRESHOLD VOLTAGE FOR A SEMICONDUCTOR DEVICE FABRICATED ON A SEMICONDUCTOR ON INSULATOR SUBSTRATE	Inactive
	5832175	SC08208P-US	US	08/423614	17-Apr-1995	03-Jul-1998	RACANELLI, MARCO; HWANG, BOR-YUAN; HUANG, WEN LING MARGARET; FOERSTNER, JUERGEN A	METHOD OF ADJUSTING A THRESHOLD VOLTAGE FOR A SEMICONDUCTOR DEVICE FABRICATED ON A SEMICONDUCTOR ON INSULATOR SUBSTRATE	Granted
73		SC08324T-EP	EP	96108992.9	30-Jun-1996		BELLO, GERNANDO ALBERTO; HALL, JAMES B; ONEAL, EARL W.; PARSONS, JAMES STANLEY; WELT, CYNTHIA ANN; BAILEY, GEORGE W	METHOD FOR PRE-SHAPING A SEMICONDUCTOR SUBSTRATE FOR POLISHING AND STRUCTURE	Inactive

		SC093247-JP	JP	8-195246	04-Jun-1996		BELLO, GERNANDO ALBERTO; HALL, JAMES B; O'NEAL, EARL W.; PARSONS, JAMES STANLEY; WELT, CYNTHIA ANN; BAILEY, GEORGE W.	METHOD FOR PRE-SHAPING A SEMIC ONDUCTOR SUBSTRATE FOR POLISHI NG AND STRUCTURE	Inactive
		SC093247-KR	KR	10-1996-0013566	30-Apr-1996		BELLO, GERNANDO ALBERTO; HALL, JAMES B; O'NEAL, EARL W.; PARSONS, JAMES STANLEY; WELT, CYNTHIA ANN; BAILEY, GEORGE W.	METHOD FOR PRE-SHAPING A SEMIC ONDUCTOR SUBSTRATE FOR POLISHI NG AND STRUCTURE	Inactive
	NI-102587	SC093247-TW	TW	85102917	11-Mar-1996	01-May-1999	BELLO, GERNANDO ALBERTO; HALL, JAMES B; O'NEAL, EARL W.; PARSONS, JAMES STANLEY; WELT, CYNTHIA ANN; BAILEY, GEORGE W.	METHOD FOR PRE-SHAPING A SEMIC ONDUCTOR SUBSTRATE FOR POLISHI NG AND STRUCTURE	Granted
		SC093247-US	US	08/496510	28-Jun-1995		BELLO, GERNANDO ALBERTO; HALL, JAMES B; O'NEAL, EARL W.; PARSONS, JAMES STANLEY	METHOD FOR PRE-SHAPING A SEMIC ONDUCTOR SUBSTRATE FOR POLISHI NG AND STRUCTURE	Inactive
	5963849	SC093247-US01	US	08/512050	07-Aug-1995	19-Oct-1999	BELLO, GERNANDO ALBERTO; HALL, JAMES B; O'NEAL, EARL W.; PARSONS, JAMES STANLEY; WELT, CYNTHIA ANN; BAILEY, GEORGE W.	METHOD FOR PRE-SHAPING A SEMIC ONDUCTOR SUBSTRATE FOR POLISHI NG AND STRUCTURE	Granted
74		SC094988P-US	US	08/509848	13-Nov-1996		RAMASWAMI, SHRINATH	METHOD OF FORMING A SPACER	Inactive
	5783475	SC094988P-US/FW01	US	08/974694	20-Nov-1997	21-Jul-1998	RAMASWAMI, SHRINATH	METHOD OF FORMING A SPACER	Granted
75		SC098913-EP	EP	98103605.0	02-Mar-1998		GAITONDE, DINESH D.; REYES, ALBERTO J; XIE, HONG; RIGG, DANA MARK	ARCHITECTURAL POWER ESTIMATION METHOD AND APPARATUS	Inactive
		SC098913-JP	JP	10-66644	04-Mar-1998		GAITONDE, DINESH D.; REYES, ALBERTO J; XIE, HONG; RIGG, DANA MARK	ARCHITECTURAL POWER ESTIMATION METHOD AND APPARATUS	Inactive
		SC098913-KR	KR	10-1998-0031803	22-Jan-1998		GAITONDE, DINESH D.; REYES, ALBERTO J; XIE, HONG; RIGG, DANA MARK	ARCHITECTURAL POWER ESTIMATION METHOD AND APPARATUS	Inactive
		SC098913-SG	SG	9800371-8	19-Feb-1998		GAITONDE, DINESH D.; REYES, ALBERTO J; XIE, HONG; RIGG, DANA MARK	ARCHITECTURAL POWER ESTIMATION METHOD AND APPARATUS	Inactive
	NI-105831	SC098913-TW	TW	86118601	10-Dec-1997	21-Aug-1999	GAITONDE, DINESH D.; REYES, ALBERTO J; XIE, HONG; RIGG, DANA MARK	ARCHITECTURAL POWER ESTIMATION METHOD AND APPARATUS	Granted
	5940778	SC098913-US	US	08/813875	05-Mar-1997	17-Aug-1999	GAITONDE, DINESH D.; REYES, ALBERTO J; XIE, HONG; RIGG, DANA MARK	ARCHITECTURAL POWER ESTIMATION METHOD AND APPARATUS	Granted
76	ZL97123123.5	SC099787-CN	CN	97123123.5	14-Nov-1997	11-Aug-2004	VANELL, JAMES F	PLATEN COATING STRUCTURE FOR CHEMICAL MECHANICAL POLISHING AND METHOD	Granted
	69716662.4	SC099787-DE	DE	97119782.7	12-Nov-1997	06-Nov-2002	VANELL, JAMES F	PLATEN COATING STRUCTURE FOR CHEMICAL MECHANICAL POLISHING AND METHOD	Granted
	EP0839625	SC099787-EP	EP	97119782.7	12-Nov-1997	06-Nov-2002	VANELL, JAMES F	PLATEN COATING STRUCTURE FOR CHEMICAL MECHANICAL POLISHING AND METHOD	Inactive
	EP0839625	SC099787-FR	FR	97119782.7	12-Nov-1997	06-Nov-2002	VANELL, JAMES F	PLATEN COATING STRUCTURE FOR CHEMICAL MECHANICAL POLISHING AND METHOD	Granted
	EP0839625	SC099787-GB	GB	97119782.7	12-Nov-1997	06-Nov-2002	VANELL, JAMES F	PLATEN COATING STRUCTURE FOR CHEMICAL MECHANICAL POLISHING AND METHOD	Granted
		SC099787-JP	JP	9-342029	27-Nov-1997		VANELL, JAMES F	PLATEN COATING STRUCTURE FOR CHEMICAL MECHANICAL POLISHING AND METHOD	Inactive
	501981	SC099787-KR	KR	10-1997-0066581	02-Dec-1997	08-Jul-2005	VANELL, JAMES F	PLATEN COATING STRUCTURE FOR CHEMICAL MECHANICAL POLISHING AND METHOD	Granted
	NI-100621	SC099787-TW	TW	86115033	21-Oct-1997	01-Feb-1999	VANELL, JAMES F	PLATEN COATING STRUCTURE FOR CHEMICAL MECHANICAL POLISHING AND METHOD	Granted
	6743768	SC099787-US	US	08/755670	02-Dec-1996	25-Apr-1998	VANELL, JAMES F	PLATEN COATING STRUCTURE FOR CHEMICAL MECHANICAL POLISHING AND METHOD	Granted
77		SC103157-JP	JP	11-356851	16-Dec-1999		VANELL, JAMES F	PAD CONDITIONER COUPLING AND END EFFECTOR FOR A CHEMICAL MECHANICAL PLANARIZATION SYSTEM AND METHOD THEREFOR	Inactive
	102569	SC103157-SG	SG	9908345-5	10-Dec-1999	31-May-2004	VANELL, JAMES F	PAD CONDITIONER COUPLING AND END EFFECTOR FOR A CHEMICAL MECHANICAL PLANARIZATION SYSTEM AND METHOD THEREFOR	Granted
	NI-191781	SC103157-TW	TW	88122399	28-Dec-1999	11-Mar-2002	VANELL, JAMES F	PAD CONDITIONER COUPLING AND E ND EFFECTOR FOR A CHEMICAL MEC HANICAL PLANARIZATION SYSTEM A ND METHOD THEREFOR	Granted
	6263608	SC103157-US	US	09/216830	21-Dec-1998	24-Jul-2001	VANELL, JAMES F	PAD CONDITIONER COUPLING AND END EFFECTOR FOR A CHEMICAL MECHANICAL PLANARIZATION SYSTEM A ND METHOD THEREFOR	Granted

	®	6914125	SC10315T-USD01	US	09/686189	02-Jun-2005	04-Feb-2003	VANELL, JAMES F	PAD CONDITIONER DOUPLING AND END EFFECTOR FOR A CHEMICAL MECHANICAL PLANARIZATION SYSTEM AND METHOD THEREFOR	Granted
		6796885	SC10315T-USD02	US	10/298744	18-Nov-2002	28-Sep-2004	VANELL, JAMES F	PAD CONDITIONER DOUPLING AND END EFFECTOR FOR A CHEMICAL MECHANICAL PLANARIZATION SYSTEM AND METHOD THEREFOR	Dropped
		3467012	SC10775T-JP	JP	2000-357160	24-Nov-2000	29-Aug-2003	JOHNSON, TIMOTHY LEE; ENGLISH, JOSEPH; AUSTIN, DAVID; CARNEY, GEORGE FRANCIS; KNOBLAUCH, KANDIS MAE; MITCHELL, DOUGLAS G	METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND PLATING TOOL THEREFOR	Granted
		424859	SC10775T-KR	KR	10-2000-0067382	14-Nov-2000	17-Mar-2004	JOHNSON, TIMOTHY LEE; ENGLISH, JOSEPH; AUSTIN, DAVID; CARNEY, GEORGE FRANCIS; KNOBLAUCH, KANDIS MAE; MITCHELL, DOUGLAS G	METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND PLATING TOOL THEREFOR	Granted
78		90-154858	SC10775T-TW	TW	89123098	02-Nov-2000	16-Aug-2002	JOHNSON, TIMOTHY LEE; ENGLISH, JOSEPH; AUSTIN, DAVID; CARNEY, GEORGE FRANCIS; KNOBLAUCH, KANDIS MAE; MITCHELL, DOUGLAS G	METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND PLATING TOOL THEREFOR	Granted
		6361675	SC10775T-US	US	09/451552	01-Dec-1999	26-Mar-2002	JOHNSON, TIMOTHY LEE; ENGLISH, JOSEPH; AUSTIN, DAVID; CARNEY, GEORGE FRANCIS; KNOBLAUCH, KANDIS MAE; MITCHELL, DOUGLAS G	METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND PLATING TOOL THEREFOR	Granted
	®	6726838	SC10775T-USD01	US	10/011228	05-Nov-2001	27-Apr-2004	JOHNSON, TIMOTHY LEE; ENGLISH, JOSEPH; AUSTIN, DAVID; CARNEY, GEORGE FRANCIS; KNOBLAUCH, KANDIS MAE; MITCHELL, DOUGLAS G	METHOD OF MANUFACTURING A SEMICONDUCTOR COMPONENT AND PLATING TOOL THEREFOR	Granted
79		6460988	SC10910TS-US	US	09/561322	18-Apr-2000	12-Nov-2002	MUKHERJEE, PRADIPTO; DASGUPTA, AUROBINDO; BLAAUW, DAVID T.; SEARLES, DAVID	ITERATIVE, NOISE SENSITIVE METHOD OF ROUTING SEMICONDUCTOR NETS	Granted
80	®	6952812	SC11403TS-US	US	09/781482	13-Feb-2001	04-Oct-2005	ABADIR, MAGDY S.; ZENG, JING; BHADRA, JAYANTA	DESIGN ANALYSIS TOOL FOR PATH EXTRACTION AND FALSE PATH IDENTIFICATION AND METHOD THEREOF	Granted
81	®	6931611	SC11522TS-US	US	10/025289	19-Dec-2001	16-Aug-2005	MARTIN, ANDREW; KRISHNAMURTHY, NARAYANAN	DESIGN VERIFICATION SYSTEM FOR AVOIDING FALSE FAILURES AND METHOD THEREFOR	Granted
82	®	6910025	SC11668TS-US	US	09/993226	20-Nov-2001	21-Jun-2005	CAO, LIPENG	MODELING BEHAVIOR OF AN ELECTRICAL CURRENT	Granted
83	®	6536025	SC11745TC-US	US	09/886079	20-Jun-2001	18-Mar-2003	GULLAPALLI, KIRAN K.	METHOD AND APPARATUS FOR ANALYZING SMALL SIGNAL RESPONSE AND NOISE IN NONLINEAR CIRCUITS	Granted
84	®	6651227	SC11835TS-US	US	09/965211	22-Oct-2001	18-Nov-2003	ABADIR, MAGDY S.; ZHU, JUNHAO	METHOD FOR GENERATING TRANSITION DELAY FAULT TEST PATTERNS	Granted
85	®	7007253	SC12003TS-US	US	10/657304	08-Sep-2003	28-Feb-2006	GULLAPALLI, KIRAN K.; GOURARY, MARK M.; RUSAKOV, SERGEI G.; ULYANOV, SERGEI L.; ZHAROV, MIKHAIL M.	METHOD AND APPARATUS FOR DISTORTION ANALYSIS IN NONLINEAR CIRCUITS	Granted
			SC12003TS-WO	WO	PCT/RU02/00474	31-Oct-2002		GULLAPALLI, KIRAN K.; GOURARY, MARK M.; RUSAKOV, SERGEI G.; ULYANOV, SERGEI L.; ZHAROV, MIKHAIL M.	METHOD AND APPARATUS FOR DISTORTION ANALYSIS IN NONLINEAR CIRCUITS	Inactive
86	®	6925622	SC12023ZS-US	US	10/282251	30-Sep-2002	02-Aug-2005	REYES, ALBERTO J.	SYSTEM AND METHOD FOR CORRELATED CLOCK NETWORKS	Granted
87	®	6944808	SC12034TC-US	US	10/150897	24-May-2002	13-Sep-2005	FLYNN, CINDA L.; SHOFNER, ORMAN G.	METHOD AND APPARATUS TO DATA LOG AT-SPEED MARCH C+ MEMORY BIST	Granted
88	®	7082323	SC12394TS-US	US	10/304423	26-Nov-2002	15-Aug-2006	SEGER, MURAT; ALGOR, ILAN; PANDA, RAJENDRAN V.; BLAAUW, DAVID T.	NOISE ANALYSIS FOR AN INTEGRATED CIRCUIT MODEL	Granted
89			SC12446TH-EP	EP	04708107.8	09-Sep-2005		MOYER, WILLIAM C.; MARSHALL, RAY	MEMORY MANAGEMENT IN A DATA PROCESSING SYSTEM	Dropped
		4710654	SC12446TH-JP	JP	2006-506855	25-Sep-2005	11-Mar-2011	MOYER, WILLIAM C.; MARSHALL, RAY	MEMORY MANAGEMENT IN A DATA PROCESSING SYSTEM	Granted
			SC12446TH-KR	KR	10-2005-7017279	15-Sep-2005		MOYER, WILLIAM C.; MARSHALL, RAY	MEMORY MANAGEMENT IN A DATA PROCESSING SYSTEM	Inactive
		I359771	SC12446TH-TW	TW	093103578	16-Dec-2003	11-May-2009	MOYER, WILLIAM C.; MARSHALL, RAY	MEMORY MANAGEMENT IN A DATA PROCESSING SYSTEM	Granted
	®	6925542	SC12446TH-US	US	10/393592	21-Mar-2003	02-Aug-2005	MOYER, WILLIAM C.; MARSHALL, RAY	MEMORY MANAGEMENT IN A DATA PROCESSING SYSTEM	Granted
			SC12446TH-WO	WO	PCT/US04/08309	04-Feb-2004		MOYER, WILLIAM C.; MARSHALL, RAY	MEMORY MANAGEMENT IN A DATA PROCESSING SYSTEM	Inactive
90			SC12481TK-CN	CN	200480009283.1	08-Oct-2005		LEE, CHU CHUNG (STEPHEN); HARLIN, RUANDA; HESS, KEVIN J.; TAN, LAN CHU; YONG, CHENG CHOI	INTEGRATED CIRCUIT DIE HAVING A COPPER CONTACT AND METHOD THEREFOR	Inactive
			SC12481TK-JP	JP	2006-508606	27-Sep-2005		LEE, CHU CHUNG (STEPHEN); HARLIN, RUANDA; HESS, KEVIN J.;	INTEGRATED CIRCUIT DIE HAVING A COPPER CONTACT AND METHOD THEREFOR	Inactive

								TAN, LAN CHU; YONG, CHENG CHOI		
		SC12481TK-KR	KR	10-2005-7018580	30-Sep-2005			LEE, CHU-CHUNG (STEPHEN); HARUN, FUAIDA; HESS, KEVIN J.; TAN, LAN CHU; YONG, CHENG CHOI	INTEGRATED CIRCUIT DIE HAVING A COPPER CONTACT AND METHOD THEREFOR	Inactive
	MY-134518-A	SC12481TK-MY	MY	PI20031227	03-Apr-2003	31-Dec-2007		LEE, CHU-CHUNG (STEPHEN); HARUN, FUAIDA; HESS, KEVIN J.; TAN, LAN CHU; YONG, CHENG CHOI	INTEGRATED CIRCUIT DIE HAVING A COPPER CONTACT AND METHOD THEREFOR	Granted
		SC12481TK-TW	TW	092109252	02-Apr-2004			LEE, CHU-CHUNG (STEPHEN); HARUN, FUAIDA; HESS, KEVIN J.; TAN, LAN CHU; YONG, CHENG CHOI	INTEGRATED CIRCUIT DIE HAVING A COPPER CONTACT AND METHOD THEREFOR	Inactive
8	8923814	SC12481TK-US	US	10/862541	15-Sep-2003	23-Aug-2005		LEE, CHU-CHUNG (STEPHEN); HARUN, FUAIDA; HESS, KEVIN J.; TAN, LAN CHU; YONG, CHENG CHOI	INTEGRATED CIRCUIT DIE HAVING A COPPER CONTACT AND METHOD THEREFOR	Granted
		SC12481TK-WO	WO	PCT/US04/08816	31-Mar-2004			LEE, CHU-CHUNG (STEPHEN); HARUN, FUAIDA; HESS, KEVIN J.; TAN, LAN CHU; YONG, CHENG CHOI	INTEGRATED CIRCUIT DIE HAVING A COPPER CONTACT AND METHOD THEREFOR	Inactive
		SC12804TP-JP	JP	2004-242474	23-Aug-2004			MATHEW, VARUGHESE; GARCIA, SAM S.; PRINDLE, CHRISTOPHER M.	SEMICONDUCTOR PROCESS AND COMPOSITION FOR FORMING A BARRIER MATERIAL OVERLYING COPPER	Inactive
91										
8	8924232	SC12804TP-US	US	10/650002	27-Aug-2003	02-Aug-2005		MATHEW, VARUGHESE; GARCIA, SAM S.; PRINDLE, CHRISTOPHER M.	SEMICONDUCTOR PROCESS AND COMPOSITION FOR FORMING A BARRIER MATERIAL OVERLYING COPPER	Granted
	200480028846.8	SC12810TK-CN	CN	200480028846.8	08-Oct-2004	02-Jul-2008		JOINER, BENNETT A.; ZHOU, YAPING; HERBERG, BEN W.	ELECTROMATIC NOISE SHIELDING IN SEMICONDUCTOR PACKAGES USING CAGED INTERCONNECT STRUCTURES	Granted
		SC12810TK-EP	EP	04794587.7	28-May-2006			JOINER, BENNETT A.; ZHOU, YAPING; HERBERG, BEN W.	ELECTROMATIC NOISE SHIELDING IN SEMICONDUCTOR PACKAGES USING CAGED INTERCONNECT STRUCTURES	Dropped
	234224	SC12810TK-IN	IN	538/CELNP/2006	17-Feb-2006	11-May-2009		JOINER, BENNETT A.; ZHOU, YAPING; HERBERG, BEN W.	ELECTROMATIC NOISE SHIELDING IN SEMICONDUCTOR PACKAGES USING CAGED INTERCONNECT STRUCTURES	Granted
		SC12810TK-JP	JP	2006-536656	14-Apr-2006			JOINER, BENNETT A.; ZHOU, YAPING; HERBERG, BEN W.	ELECTROMATIC NOISE SHIELDING IN SEMICONDUCTOR PACKAGES USING CAGED INTERCONNECT STRUCTURES	Inactive
92										
	10-1113414	SC12810TK-KR	KR	10-2006-7008137	27-Apr-2006	31-Jan-2012		JOINER, BENNETT A.; ZHOU, YAPING; HERBERG, BEN W.	ELECTROMATIC NOISE SHIELDING IN SEMICONDUCTOR PACKAGES USING CAGED INTERCONNECT STRUCTURES	Granted
	I360038	SC12810TK-TW	TW	093131320	14-Oct-2004	21-May-2012		JOINER, BENNETT A.; ZHOU, YAPING; HERBERG, BEN W.	ELECTROMATIC NOISE SHIELDING IN SEMICONDUCTOR PACKAGES USING CAGED INTERCONNECT STRUCTURES	Granted
9	8923569	SC12810TK-US	US	10/694146	27-Oct-2003	23-Aug-2005		JOINER, BENNETT A.; ZHOU, YAPING; HERBERG, BEN W.	ELECTROMATIC NOISE SHIELDING IN SEMICONDUCTOR PACKAGES USING CAGED INTERCONNECT STRUCTURES	Granted
		SC12810TK-WO	WO	PCT/US04/35284	08-Oct-2004			JOINER, BENNETT A.; ZHOU, YAPING; HERBERG, BEN W.	ELECTROMATIC NOISE SHIELDING IN SEMICONDUCTOR PACKAGES USING CAGED INTERCONNECT STRUCTURES	Inactive
	200480024434.0	SC12922TC-CN	CN	200480024434.0	24-Feb-2006	14-Oct-2009		GARNI, BRAD J.; ANDRE, THOMAS W.; NAHAS, JOSEPH J.	ACCELERATED LIFE TEST OF MRAM CELLS	Granted
		SC12922TC-EP	EP	04783696.6	26-Apr-2006			GARNI, BRAD J.; ANDRE, THOMAS W.; NAHAS, JOSEPH J.	ACCELERATED LIFE TEST OF MRAM CELLS	Dropped
	4588796	SC12922TC-JP	JP	2006-528548	24-Mar-2006	17-Sep-2010		GARNI, BRAD J.; ANDRE, THOMAS W.; NAHAS, JOSEPH J.	ACCELERATED LIFE TEST OF MRAM CELLS	Granted
93	10-1094675	SC12922TC-KR	KR	10-2006-7006886	24-Mar-2006	01-Aug-2011		GARNI, BRAD J.; ANDRE, THOMAS W.; NAHAS, JOSEPH J.	ACCELERATED LIFE TEST OF MRAM CELLS	Granted
	I349935	SC12922TC-TW	TW	093128880	23-Sep-2004	01-Oct-2011		GARNI, BRAD J.; ANDRE, THOMAS W.; NAHAS, JOSEPH J.	ACCELERATED LIFE TEST OF MRAM CELLS	Granted
8	8884937	SC12922TC-US	US	10/667959	26-Sep-2003	17-May-2005		GARNI, BRAD J.; ANDRE, THOMAS W.; NAHAS, JOSEPH J.	ACCELERATED LIFE TEST OF MRAM CELLS	Granted
		SC12922TC-WO	WO	PCT/US04/28648	14-Sep-2004			GARNI, BRAD J.; ANDRE, THOMAS W.; NAHAS, JOSEPH J.	ACCELERATED LIFE TEST OF MRAM CELLS	Inactive
94	8 7039883	SC12951TS-US	US	10/729622	05-Dec-2003	02-May-2006		KRISHNAMURTHY,	DERIVATION OF CIRCUIT	Granted

								NARAYANAN	BLOCK CONSTRAINTS	
		200480040728.2	SC13158TH-CN	CN	200480040735.2	20-Jul-2006	03-Dec-2008	MOYER, WILLIAM C.	REAL-TIME DEBUG SUPPORT FOR A DMA DEVICE AND METHOD THEREOF	Granted
		4531773	SC13158TH-JP	JP	2006-551090	21-Jul-2006	18-Jun-2010	MOYER, WILLIAM C.	REAL-TIME DEBUG SUPPORT FOR A DMA DEVICE AND METHOD THEREOF	Granted
		10-1045475	SC13158TH-KR	KR	10-2006-7014758	21-Jul-2006	03-Jun-2011	MOYER, WILLIAM C.	REAL-TIME DEBUG SUPPORT FOR A DMA DEVICE AND METHOD THEREOF	Granted
95		1354605	SC13158TH-TW	TW	094100177	04-Jan-2005	21-Dec-2011	MOYER, WILLIAM C.	REAL-TIME DEBUG SUPPORT FOR A DMA DEVICE AND METHOD THEREOF	Granted
	§	6922586	SC13158TH-US	US	10/764110	23-Jan-2004	19-Jul-2005	MOYER, WILLIAM C.	REAL-TIME DEBUG SUPPORT FOR A DMA DEVICE AND METHOD THEREOF	Granted
	§	7287194	SC13158TH-USC01	US	11/099899	06-Apr-2005	23-Oct-2007	MOYER, WILLIAM C.	REAL-TIME DEBUG SUPPORT FOR A DMA DEVICE AND METHOD THEREOF	Granted
			SC13158TH-WO	WO	PCT/US04/43491	21-Dec-2004		MOYER, WILLIAM C.	REAL-TIME DEBUG SUPPORT FOR A DMA DEVICE AND METHOD THEREOF	Inactive
			SC13324TP-TW	TW	094115448	13-May-2005		ORLOWSKI, MARIUS K.; LIU, CHUN-LI YEAP, CHOH-FEI	METHOD FOR MAKING A SEMICONDUCTOR STRUCTURE USING SILICON GERMANIUM	Pending
96	§	7195963	SC13324TP-US	US	10/851347	21-May-2004	27-Mar-2007	ORLOWSKI, MARIUS K.; LIU, CHUN-LI YEAP, CHOH-FEI	METHOD FOR MAKING A SEMICONDUCTOR STRUCTURE USING SILICON GERMANIUM	Granted
			SC13324TP-WO	WO	PCT/US05/17391	13-Apr-2005		ORLOWSKI, MARIUS K.; LIU, CHUN-LI YEAP, CHOH-FEI	METHOD FOR MAKING A SEMICONDUCTOR STRUCTURE USING SILICON GERMANIUM	Inactive
			SC13660TP-TW	TW	094138131	31-Oct-2005		HUEB, STEVEN M.; LOVEJOY, MICHAEL L.; MATHEW, VARUGHESE	CONTROLLED ELECTROLESS PLATING	Pending
97	§	7176133	SC13660TP-US	US	10/994725	22-Nov-2004	13-Feb-2007	HUEB, STEVEN M.; LOVEJOY, MICHAEL L.; MATHEW, VARUGHESE	CONTROLLED ELECTROLESS PLATING	Granted
	§	7717060	SC13660TP-USC01	US	11/610799	14-Dec-2006	18-May-2010	HUEB, STEVEN M.; LOVEJOY, MICHAEL L.; MATHEW, VARUGHESE	CONTROLLED ELECTROLESS PLATING	Granted
		200680001528.4	SC13662TP-CN	CN	200680001528.4	21-Jun-2007	09-Sep-2009	LIM, SANGWOO; GRUDOWSKI, PAUL A.; LUO, TIEN YING; ADETUTU, OLUBUNMI O.; TSENG, HSING-HUANG	METHOD OF MAKING A NITRIDED GATE DIELECTRIC	Granted
			SC13662TP-EP	EP	06733384.3	04-Jul-2007		LIM, SANGWOO; GRUDOWSKI, PAUL A.; LUO, TIEN YING; ADETUTU, OLUBUNMI O.; TSENG, HSING-HUANG	METHOD OF MAKING A NITRIDED GATE DIELECTRIC	Dropped
			SC13662TP-JP	JP	2007-557034	31-May-2007		LIM, SANGWOO; GRUDOWSKI, PAUL A.; LUO, TIEN YING; ADETUTU, OLUBUNMI O.; TSENG, HSING-HUANG	METHOD OF MAKING A NITRIDED GATE DIELECTRIC	Pending
98			SC13662TP-KR	KR	10-2007-7019458	24-Aug-2007		LIM, SANGWOO; GRUDOWSKI, PAUL A.; LUO, TIEN YING; ADETUTU, OLUBUNMI O.; TSENG, HSING-HUANG	METHOD OF MAKING A NITRIDED GATE DIELECTRIC	Pending
			SC13662TP-TW	TW	095106163	23-Feb-2006		LIM, SANGWOO; GRUDOWSKI, PAUL A.; LUO, TIEN YING; ADETUTU, OLUBUNMI O.; TSENG, HSING-HUANG	METHOD OF MAKING A NITRIDED GATE DIELECTRIC	Pending
	§	7402472	SC13662TP-US	US	11/067257	25-Feb-2005	22-Jul-2008	LIM, SANGWOO; GRUDOWSKI, PAUL A.; LUO, TIEN YING; ADETUTU, OLUBUNMI O.; TSENG, HSING-HUANG	METHOD OF MAKING A NITRIDED GATE DIELECTRIC	Granted
			SC13662TP-WO	WO	PCT/US06/04198	08-Feb-2006		LIM, SANGWOO; GRUDOWSKI, PAUL A.; LUO, TIEN YING; ADETUTU, OLUBUNMI O.; TSENG, HSING-HUANG	METHOD OF MAKING A NITRIDED GATE DIELECTRIC	Inactive
99		5784615	SC3001DA-US	US	08/830199	10-Apr-1997	04-Aug-1998	PULLELA, SATYA; DHARCHOUDHURY, ABHIJIT; BLAAUW, DAVID T.; EDWARDS, TIM; NORTON, JOSEPH W.	COMPLEMENTARY NETWORK REDUCTIO N FOR LOAD MODELING	Granted
100		5761083	SC3075A-US	US	08/629457	10-Apr-1996	12-May-1998	PULLELA, SATYA; DHARCHOUDHURY, ABHIJIT; BLAAUW, DAVID T.; EDWARDS, TIM; NORTON, JOSEPH W.	ACCURATE DELAY PREDICTION BASE D ON MULTI-MODEL ANALYSIS	Granted
101		5920484	SC3014A-US	US	08/753635	02-Dec-1996	06-Jul-1999	NGUYEN, TUYEN VAN; LI, JING	METHOD FOR GENERATING A REDUCED ORDER MODEL OF AN ELECTRONIC CIRCUIT	Granted
102			SC3022DA-AU	AU	38231/97	25-Sep-1997		GURUSWAMY, MOHANKUMAR; DULITZ, DANIEL W.; MAZIASZ, ROBERT L.; RAMAN, SRILATA; CHILUVURI, VENKATA K. R.; FERNANDES, ANDREA	AUTOMATIC SYNTHESIS OF STANDAR D CELL LAYOUTS	Inactive

	5966518	SC302223A-US	US	08/740720	01-Nov-1996	16-Nov-1999	GURUSWAMY, MOHANKUMAR; DULITZ, DANIEL W.; MAZIASZ, ROBERT L.; RAMAN, SRILATA; CHILUVURI, VENKATA K. R.; FERNANDEZ, ANDREA	AUTOMATIC SYNTHESIS OF STANDARD CELL LAYOUTS	Granted
103	6006024	SC302224A-US	US	08/740768	01-Nov-1996	21-Dec-1999	GURUSWAMY, MOHANKUMAR; DULITZ, DANIEL W.; FERNANDEZ, ANDREA; RAMAN, SRILATA; MAZIASZ, ROBERT L.	METHOD OF ROUTING AN INTEGRATED CIRCUIT	Granted
104	5987086	SC303116A-US	US	08/740721	01-Nov-1996	16-Nov-1999	RAMAN, SRILATA; GURUSWAMY, MOHANKUMAR; DULITZ, DANIEL W.; CHILUVURI, VENKATA K. R.; MAZIASZ, ROBERT L.	AUTOMATIC LAYOUT STANDARD CELL ROUTING	Granted
105	4288344	SC303777A-JP	JP	10-196845	28-Jun-1998	03-Apr-2009	KIM, SUNG; LAI, LEI PING; BAJAJ, RAJEEV; MANZONIE, ADAM W.	METHOD OF CHEMICAL MECHANICAL POLISHING (CMP) USING AN UNDER PAD WITH DIFFERENT COMPRESSIO N REGIONS AND POLISHING PAD TH EREFOR	Granted
	5899745	SC303777A-US	US	08/887095	03-Jul-1997	04-May-1999	KIM, SUNG; LAI, LEI PING; BAJAJ, RAJEEV; MANZONIE, ADAM W.	METHOD OF CHEMICAL MECHANICAL POLISHING (CMP) USING AN UNDER PAD WITH DIFFERENT COMPRESSIO N REGIONS AND POLISHING PAD TH EREFOR	Granted
106	5754454	SC303428A-US	US	08/808759	03-Mar-1997	19-May-1998	PIXLEY, CARL; PARK, JAEHONG	METHOD FOR DETERMINING FUNCTIO NAL EQUIVALENCE BETWEEN DESIGN MODELS	Granted
107		SC304668A-JP	JP	10-67746	02-Mar-1998		PULLELA, SATYA; EDWARDS, TIM; NORTON, JOSEPH W.; DHARCHOUDHURY, ABHIJIT; BLAAUW, DAVID T.	METHOD FOR OPTIMIZING ELEMENT SIZES IN A SEMICONDUCTOR DEVIC E	Inactive
	462594	SC304668A-KR	KR	10-1998-0005703	02-Mar-1998	04-Apr-2005	PULLELA, SATYA; EDWARDS, TIM; NORTON, JOSEPH W.; DHARCHOUDHURY, ABHIJIT; BLAAUW, DAVID T.	METHOD FOR OPTIMIZING ELEMENT SIZES IN A SEMICONDUCTOR DEVIC E	Granted
	NI-134804	SC304668A-TW	TW	87101868	11-Feb-1998	12-Nov-2001	PULLELA, SATYA; EDWARDS, TIM; NORTON, JOSEPH W.; DHARCHOUDHURY, ABHIJIT; BLAAUW, DAVID T.	METHOD FOR OPTIMIZING ELEMENT SIZES IN A SEMICONDUCTOR DEVIC E	Granted
	5903471	SC304668A-US	US	08/805662	03-Mar-1997	11-May-1999	PULLELA, SATYA; EDWARDS, TIM; NORTON, JOSEPH W.; DHARCHOUDHURY, ABHIJIT; BLAAUW, DAVID T.	METHOD FOR OPTIMIZING ELEMENT SIZES IN A SEMICONDUCTOR DEVIC E	Granted
108	6078884	SC304988A-US	US	08/848867	01-May-1997	13-Jun-2000	CHILUVURI, VENKATA K. R.; GURUSWAMY, MOHANKUMAR; RAMAN, SRILATA; MAZIASZ, ROBERT L.	METHOD FOR OPTIMIZING CONTACT PIN PLACEMENT IN AN INTEGRATED CIRCUIT	Granted
109	ZL98105825.X	SC305124A-CN	CN	98104825X	06-Apr-1998	05-Nov-2003	ISLAM, RABIUL; GELATOS, AVGERINOS V.; LUCAS, KEVIN D.; FILIPIAK, STANLEY M.; VENKATRAMAN, RAMNATH	COPPER INTERCONNECT STRUCTURE AND METHOD OF FORMATION	Granted
	4302231	SC305124A-JP	JP	11-97403	06-Apr-1998	01-May-2009	ISLAM, RABIUL; GELATOS, AVGERINOS V.; LUCAS, KEVIN D.; FILIPIAK, STANLEY M.; VENKATRAMAN, RAMNATH	COPPER INTERCONNECT STRUCTURE AND METHOD OF FORMATION	Granted
	531561	SC305124A-KR	KR	10-1998-0011824	02-Apr-1998	22-Nov-2005	ISLAM, RABIUL; GELATOS, AVGERINOS V.; LUCAS, KEVIN D.; FILIPIAK, STANLEY M.; VENKATRAMAN, RAMNATH	COPPER INTERCONNECT STRUCTURE AND METHOD OF FORMATION	Granted
	74130	SC305124A-SG	SG	9801925-9	01-Apr-1998	28-Oct-2002	ISLAM, RABIUL; GELATOS, AVGERINOS V.; LUCAS, KEVIN D.; FILIPIAK, STANLEY M.; VENKATRAMAN, RAMNATH	COPPER INTERCONNECT STRUCTURE AND METHOD OF FORMATION	Granted
	NI-125658	SC305124A-TW	TW	88105369	30-Jun-1999	14-May-2001	ISLAM, RABIUL; GELATOS, AVGERINOS V.; LUCAS, KEVIN D.; FILIPIAK, STANLEY M.; VENKATRAMAN, RAMNATH	COPPER INTERCONNECT STRUCTURE AND METHOD OF FORMATION	Granted
	6174810	SC305124A-US	US	09/055510	06-Apr-1998	16-Jan-2001	ISLAM, RABIUL; GELATOS, AVGERINOS V.; LUCAS, KEVIN D.; FILIPIAK, STANLEY M.; VENKATRAMAN, RAMNATH	COPPER INTERCONNECT STRUCTURE AND METHOD OF FORMATION	Granted
		SC305124A-USCD1	US	09/686698	11-Oct-2000		ISLAM, RABIUL; GELATOS, AVGERINOS V.; LUCAS, KEVIN D.; FILIPIAK, STANLEY M.; VENKATRAMAN, RAMNATH	COPPER INTERCONNECT STRUCTURE AND METHOD OF FORMATION	Inactive
110	5966306	SC305984A-US	US	08/886585	07-Jul-1997	12-Oct-1999	MCGINE, MARK HOWARD; MARTIN, HAROLD MACK; NGUYEN, ANHTU	METHOD FOR VERIFYING PROTOCOL CONFORMANCE OF AN ELECTRICAL INTERFACE	Granted
111	5999717	SC306693A-US	US	09/001791	31-Dec-1997	07-Dec-1999	KAUFMAN, MATTHEW J.; MARTIN, ANDREW; PIXLEY, CARL	METHOD FOR PERFORMING MODEL CHECKING IN INTEGRATED CIRCUIT DESIGN	Granted

112	5985748	SC907602A-US	US	08/988782	01-Dec-1997	16-Nov-1999	WATTS, DAVID; MKANSAH, FRANKLIN D.; MENDONCA, JOHN	METHOD OF MAKING A SEMICONDUCTOR DEVICE USING CHEMICAL-MECHANICAL POLISHING HAVING A COMBINATION STEP PROCESS	Granted
113	6221537	SC907664A-US	US	09/064369	19-Dec-1997	24-Apr-2001	THOMPSON, MATTHEW A.; MANGAT, PAWITTER J. S.	SEMICONDUCTOR DEVICE AND METHO D OF FORMATION	Granted
114	6321186	SC908756-US	US	09/303995	03-May-1999	20-Nov-2001	YUAN, JUN; PIRLEY, CARL; SHULTZ, STEPHEN K.; MILLER, HILLEL	METHOD AND APPARATUS FOR INTEGRATED CIRCUIT DESIGN VERIFICATION	Granted
115	6493854	SC909531A-US	US	09/411725	01-Oct-1999	10-Dec-2002	CHOWDHURY, SALIM; BEARDEN, DAVID	METHOD AND APPARATUS FOR PLACING REPEATERS IN A NETWORK OF AN INTEGRATED CIRCUIT	Granted
116	6169587	SC911086A-US	US	09/290396	12-Apr-1999	06-Dec-2000	VENTZEK, PETER L. G.; CORONELL, DANIEL GENE; HARTIG, MICHAEL J.; ARMOUR, JOHN C.	PROCESS OF FORMING A SEMICONDUCTOR DEVICE	Granted
117	6378112	SC911162A-US	US	09/322817	14-Jun-1999	23-Apr-2002	MARTIN, ANDREW; KRISHNAMURTHY, NARAYANAN; ABADIR, MAGDY S.; WANG, LI-CHUNG	VERIFICATION OF DESIGN BLOCKS AND METHOD OF EQUIVALENCE CHECKING OF MULTIPLE DESIGN VIEWS	Granted
118	6326301	SC911771A-US	US	09/352134	13-Jul-1999	04-Dec-2001	VENKATESAN, SURESH; SMITH, BRADLEY P; ISLAM, RASIUL	A METHOD FOR FORMING A DUAL INLAID COPPER INTERCONNECT STRUCTURE	Granted
	6551919	SC911771A-US001	US	09/970284	03-Oct-2001	22-Apr-2003	VENKATESAN, SURESH; SMITH, BRADLEY P; ISLAM, RASIUL	A METHOD FOR FORMING A DUAL INLAID COPPER INTERCONNECT STRUCTURE	Granted