PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT3083774

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	PATENT SECURITY AGREEMENT

CONVEYING PARTY DATA

Name	Execution Date
PLX TECHNOLOGY, INC.	10/27/2014

RECEIVING PARTY DATA

Name:	DEUTSCHE BANK AG NEW YORK BRANCH, AS COLLATERAL AGENT
Street Address:	60 WALL STREET
City:	NEW YORK
State/Country:	NEW YORK
Postal Code:	10005

PROPERTY NUMBERS Total: 57

Property Type	Number
Patent Number:	6091705
Patent Number:	6581126
Patent Number:	7003613
Patent Number:	7028126
Patent Number:	6742076
Patent Number:	7145934
Patent Number:	7039750
Patent Number:	7233602
Patent Number:	7177294
Patent Number:	7167484
Patent Number:	6954616
Patent Number:	7212297
Patent Number:	6898751
Patent Number:	7215659
Patent Number:	7277451
Patent Number:	7222201
Patent Number:	6851009
Patent Number:	7287257
Patent Number:	7015842
Patent Number:	7075471
Patent Number:	7132965

Property Type	Number
Patent Number:	7409476
Patent Number:	7660944
Application Number:	11938525
Patent Number:	7834709
Patent Number:	8468301
Patent Number:	7869356
Patent Number:	8738812
Patent Number:	8196013
Patent Number:	8504755
Patent Number:	8370411
Patent Number:	8201010
Patent Number:	8417985
Patent Number:	8145949
Application Number:	12837730
Application Number:	12837778
Patent Number:	8327042
Patent Number:	8457247
Patent Number:	8797857
Patent Number:	8548011
Patent Number:	8521941
Patent Number:	8683285
Patent Number:	8015330
Patent Number:	8553683
Patent Number:	8554976
Patent Number:	8645605
Patent Number:	8543890
Patent Number:	8332681
Patent Number:	8785246
Application Number:	13624781
Application Number:	13660791
Application Number:	13741180
Application Number:	14073491
Application Number:	14106579
Application Number:	14203149
Application Number:	14231079
Application Number:	14244634

CORRESPONDENCE DATA

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ATTORNEY DOCKET NUMBER:	040981-0072
NAME OF SUBMITTER:	RHONDA DELEON
SIGNATURE:	/Rhonda DeLeon/
DATE SIGNED:	10/28/2014

Total Attachments: 6
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PATENT SECURITY AGREEMENT dated as of October 27, 2014 (this "Agreement"), among PLX Technology, Inc. (the "Grantor") and Deutsche Bank AG New York Branch, as Collateral Agent (in such capacity, the "Collateral Agent").

Reference is made to (a) the Credit Agreement dated as of May 6, 2014 (as amended, supplemented or otherwise modified from time to time, the "Credit Agreement"), among Avago Technologies Finance Pte. Ltd., a company incorporated under the Singapore Companies Act ("Holdings"), Avago Technologies Cayman Ltd., an exempted company incorporated with limited liability in the Cayman Islands (the "Borrower"), Avago Technologies Holdings Luxembourg S.à r.l., a private limited liability company incorporated under the laws of Luxembourg, having its registered office at 2-8, avenue Charles de Gaulle, L-1653 Luxembourg, in the process of being registered with the Trade and Companies Register and with a share capital of $20,000 (the "Luxco Borrower"), the Lenders party thereto and Deutsche Bank AG New York Branch, as Collateral Agent and (b) the Collateral Agreement dated as of May 6, 2014 (as amended, supplemented or otherwise modified from time to time, the "Collateral Agreement"), among the grantors from time to time party thereto and the Collateral Agent. The Lenders and have agreed to extend credit to the Borrower Parties subject to the terms and conditions set forth in the Credit Agreement. The Grantor is an Affiliate of the Borrower Parties and is willing to execute and deliver this Agreement in order to induce the Lenders to make additional Loans and as consideration for Loans previously made. Accordingly, the parties hereto agree as follows:

SECTION 1.   Terms.   Capitalized terms used in this Agreement and not otherwise defined herein have the meanings specified in the Collateral Agreement or the Credit Agreement, as applicable. The rules of construction specified in Section 1.01(b) of the Collateral Agreement also apply to this Agreement.

SECTION 2.   Grant of Security Interest.   As security for the payment or performance, as the case may be, in full of the Secured Obligations, the Grantor hereby grants to the Collateral Agent, its successors and assigns, for the benefit of the Secured Parties, a security interest (the "Security Interest") in all of such Grantor's right, title and interest in, to and under any Patents now owned or at any time hereafter acquired by such Grantor, including those listed on Schedule I (the "Patent Collateral"); provided that notwithstanding anything to the contrary contained in the foregoing clause, the security interest created hereby shall not extend to, and the term "Patent Collateral" shall not include, any Excluded Assets.

SECTION 3.   Collateral Agreement.   The Security Interest granted to the Collateral Agent herein is granted in furtherance, and not in limitation, of the security interests granted to the Collateral Agent pursuant to the Collateral Agreement. The Grantor hereby acknowledges and affirms that the rights and remedies of the Collateral Agent with respect to the Patent Collateral are more fully set forth in the Collateral Agreement, the terms and provisions of which are hereby incorporated herein by reference as if fully set forth herein. In the event of any conflict between the terms of this Agreement and the Collateral Agreement, the terms of the Collateral Agreement shall govern.

SECTION 4.   Counterparts.   This Agreement may be executed in counterparts (and by different parties hereto on different counterparts), each of which shall constitute an original but all of which when taken together shall constitute a single contract. Delivery of an executed signature page to this Agreement by facsimile or other electronic transmission shall be effective as delivery of a manually signed counterpart of this Agreement.

[Remainder of this page intentionally left blank]

IN WITNESS WHEREOF, the parties hereto have duly executed this Agreement as of the day and year first above written.
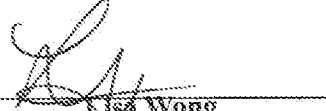
PLX TECHNOLOGY, INC.

By: _____

    Name: Anthony E. Maslowski
    Title: Vice President, Chief Financial Officer and Secretary

Patent Security Agreement

DEUTSCHE BANK AG NEW YORK BRANCH,
as Collateral Agent

By: _____
Name: **Anca Trifan**
Title: **Managing Director**

By: _____
Name: Lisa Wong
Title: Vice President

Patent Security Agreement

Schedule I

Title	Application No. Filing Date	Patent No. Issue Date
Method and apparatus for a fault tolerant, software transparent and high data integrity extension to a backplane bus or interconnect	08/771581 12/20/1996	6091705 7/18/2000
Method, system and apparatus for a computer subsystem interconnection using a chain of bus repeaters	09/315412 5/19/1999	6581126 6/17/2003
System for transferring data using a USB host system with a dedicated processor	09/490263 1/24/2000	7003613 2/21/2006
Universal serial bus for mobile devices having expansion modules	09/667091 9/21/2000	7028126 4/11/2006
Systems and methods for batched USB data transfers	09/754828 1/2/2001	6742076 5/25/2004
Multichannel signal transmission and reception for bluetooth systems	09/798482 3/3/2001	7145934 12/5/2006
On-chip switch fabric	09/912231 7/24/2001	7039750 5/2/2006
Coordination architecture for wireless communication devices using multiple protocols	10/003703 10/23/2001	7233602 6/19/2007
Collision rectification in wireless communication devices	10/053860 10/25/2001	7177294 2/13/2007
Centralized coordination point for wireless communication devices using multiple protocols	10/066284 2/1/2002	7167484 1/23/2007
Top-level controller for wireless communication devices and protocols	10/106515 3/22/2002	6954616 10/11/2005
Universal printing system	10/164148 6/5/2002	7212297 5/1/2007
Method and system for optimizing polling in systems using negative acknowledgement protocols	10/209541 7/31/2002	6898751 5/24/2005
Remotely-cooperative scheduling solution for moderating wireless protocols	10/211954 7/31/2002	7215659 5/8/2007
Recognition scheme for moderating wireless protocols	10/211976 7/31/2002	7277451 10/2/2007
Virtual endpoint for USB devices	10/338067 1/6/2003	7222201 5/22/2007
Method, system and apparatus for a computer subsystem interconnection using a chain of bus repeaters	10/446402 5/28/2003	6851009 2/1/2005
Automatic embedded host configuration system and method	10/680285 10/7/2003	7287257 10/23/2007
High-speed sampling architectures	11/033661 1/12/2005	7015842 3/21/2006
Double-sampled, time-interleaved analog to digital converter	11/056028 2/11/2005	7075471 7/11/2006
High-speed sampling architectures	11/284985 11/21/2005	7132965 11/7/2006

Title	Application No. Filing Date	Patent No. Issue Date
System and method for USB controllers	11/362320 2/24/2006	7409476 8/5/2008
Random number generation	11/880880 7/24/2007	7660944 2/9/2010
Adjustment of Data Storage Capacity Provided by a Storage System	11/938525 11/12/2007	
Circuit for voltage controlled oscillator	12/245078 10/3/2008	7834709[1] 11/16/2010
Writing of data on an array of storage devices with controlled granularity	12/227449 11/18/2008	8468301 6/18/2013
Dynamic buffer pool in PCIExpress switches	12/336402 12/16/2008	7869356 1/11/2011
Transfer of commands and storage data to a data storage device	12/472901 5/27/2009	8738812 5/27/2014
Supporting global input/output interconnect features on ports of a midpoint device	12/605110 10/23/2009	8196013 6/5/2012
USB 3 bridge with embedded hub	12/716584 3/3/2010	8504755 8/6/2013
Generating unique random numbers for multiple instantiations	12/723403 3/12/2010	8370411 2/5/2013
Automatic reference frequency compensation	12/782499 5/18/2010	8201010 6/12/2012
Adjusting system clock to faster speed upon receiving mass storage command and back to lower speed upon completion of all commands	12/782501 5/18/2010	8417985 4/9/2013
Automated regression failure management system	12/816573 6/16/2010	8145949 3/27/2012
RUNTIME REPROGRAMMING OF A PROCESSOR CODE SPACE MEMORY AREA	12/837730 7/16/2010	
CACHING USING VIRTUAL MEMORY	12/837778 7/16/2010	
Automatic port accumulation	12/875500 9/3/2010	8327042 12/4/2012
In-band generation of low-frequency periodic signaling	12/949706 11/18/2010	8457247 6/4/2013
Dynamic buffer pool in PCIExpress switches	12/957237 11/30/2010	8797857 8/5/2014
Dynamic host clock compensation	12/959239 12/2/2010	8548011 10/1/2013
Multi-root sharing of single-root input/output virtualization	12/979904 12/28/2010	8521941 8/27/2013
Parallel packetized interconnect with simplified data link layer	12/980602 12/29/2010	8683285 3/25/2014

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[1] To be assigned from Oxford Semiconductor Pte. Ltd. to PLX Technology, Inc.

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Title	Application No. Filing Date	Patent No. Issue Date
Read control in a computer I/O interconnect	13/020702 2/3/2011	8015330 9/6/2011
Three dimensional fat tree networks	13/176350 7/5/2011	8553683 10/8/2013
Single pipe non-blocking architecture	13/179074 7/8/2011	8554976 10/8/2013
Sharing multiple virtual functions to a host using a pseudo physical function	13/212700 8/18/2011	8645605 2/4/2014
Supporting global input/output interconnect features on ports of a midpoint device	13/457275 4/26/2012	8543890 9/24/2013
Automatic reference frequency compensation	13/461358 5/1/2012	8332681 12/11/2012
Multiple seal-ring structure for the design, fabrication, and packaging of integrated circuits	13/566332 8/3/2012	8785246 7/22/2014
PCI EXPRESS SWITCH WITH LOGICAL DEVICE CAPABILITY	13/624781 9/21/2012	
METHOD AND APPARATUS FOR SECURING AND SEGREGATING HOST TO HOST MESSAGING ON PCIE FABRIC	13/660791 10/25/2012	
GENERATING UNIQUE RANDOM NUMBERS FOR MULTIPLE INSTANTIATIONS	13/741180 1/14/2013	
	14/073491 11/16/2014	
	14/106579 12/13/2013	
	14/203149 3/10/2014	
MULTI-PATH ID ROUTING IN A PCIE EXPRESS FABRIC ENVIRONMENT	14/231079 3/31/2014	
	14/244634 4/3/2014	