PATENT ASSIGNMENT COVER SHEET

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Stylesheet Version v1.2

EPAS ID: PAT3196117

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
FREESCALE SEMICONDUCTOR, INC.	12/18/2014

RECEIVING PARTY DATA

Name:	INTEL CORPORATION
Street Address:	2200 MISSION COLLEGE BLVD.
City:	SANTA CLARA
State/Country:	CALIFORNIA
Postal Code:	95054

PROPERTY NUMBERS Total: 17

Property Type	Number
Patent Number:	5889788
Patent Number:	6134675
Patent Number:	6769076
Patent Number:	6845419
Patent Number:	7013409
Patent Number:	7248069
Patent Number:	7296137
Patent Number:	7299335
Patent Number:	7444568
Patent Number:	7681078
Patent Number:	8041901
Patent Number:	8341301
PCT Number:	WO2005020280
PCT Number:	WO2006130207
PCT Number:	WO2006130208
PCT Number:	WO2007103591
PCT Number:	WO2008081346

CORRESPONDENCE DATA

Fax Number: (612)677-3572

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent

using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

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Correspondent Name:	JENNY KATHMAN
Address Line 1:	C/O CPA GLOBAL
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Address Line 4:	MINNEAPOLIS, MINNESOTA 55402

ATTORNEY DOCKET NUMBER:	G01240 - FREESCALE
NAME OF SUBMITTER:	JENNY KATHMAN
SIGNATURE:	/Jenny Kathman/
DATE SIGNED:	01/23/2015

Total Attachments: 6

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Patent Assignment

Freescale Semiconductor, Inc., a Delaware corporation, with an office at 6501 William Cannon Drive West, Austin, TX 78735 ("Assignor") is the sole owner of the patents and patent applications listed in Schedule 1 hereto (collectively the "Listed Patents"); and

Intel Corporation, a Delaware corporation, with an office at 2200 Mission College Boulevard, Santa Clara, CA 95054 ("Assignee"), desires to acquire all right, title and interest in the Listed Patents and the other patents and related rights described below.

For good and valuable consideration, the receipt of which is hereby acknowledged, Assignor does hereby sell, assign, transfer and convey to Assignee and its successors and assigns all right, title and interest that may exist today and in the future to any and all:

(1) Listed Patents;

(2) patents and patent applications to which any of the Listed Patents directly or indirectly claims, or forms the basis for, priority anywhere in the world;

(3) reissues, reexaminations, extensions, continuations, continuations-in-part, continuing prosecution applications and divisions of any of the items covered by (1) or (2) above;

(4) foreign counterparts to any of the items covered by (1), (2) or (3) above, including utility models, inventors' certificates, industrial design protection and any other form of governmental grants or issuances for the protection of inventions, designs or discoveries;

(5) inventions, invention disclosures, designs and discoveries described, disclosed or claimed in the items covered by (1) through (4) above;

(6) patents that issue from any of the items covered by (1) through (5) above;

(7) claims, causes of action and enforcement rights of any kind, whether currently pending, filed or otherwise, and whether known or unknown, under or arising from any of the items covered by (1) through (6) above, including all rights to pursue and collect damages, costs, injunctive relief and other remedies for past, current or future infringement thereof and including rights afforded under 35 U.S.C. § 154(d);

(8) royalties, income and other payments due as of the date hereof or hereafter (except as otherwise provided in the purchase agreement between Assignor and Assignee) under or arising from any of the items covered by (1) through (7) above; and

(9) rights to apply for, file, register, maintain, extend and renew in any or all countries of the world patents, certificates of invention, utility models, industrial design protection, design patent protection and other governmental grants or issuances of

any kind related to any of the items covered by (1) through (7) above.

Assignor shall execute and deliver any instruments, and do and perform any other acts and things as may be reasonably necessary or desirable for effecting and evidencing the assignments contemplated hereby, including the execution, acknowledgment and recordation of any instruments.

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks and any other patent office to issue any and all patents, utility models or other governmental grants or issuances pertaining to any of the items assigned hereunder in the name of Assignee.

The assignments and rights pursuant hereto will inure to the benefit of Assignee and its successors, assigns and other legal representatives and is binding upon Assignor and its successors, assigns, heirs and legal representatives.

Assignor, by its duly authorized representative, has executed this assignment on the date set forth below.

DATE: 12/18, 2014

By: Freescale Semiconductor, Inc.
Changhae Park
Vice President

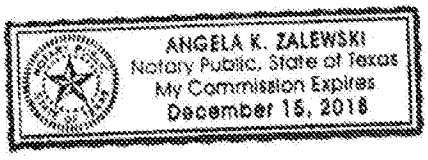
Signature

STATE OF Texas)
) ss.
COUNTY OF Travis)

ANGELA K. ZALEWSKI
Notary Public, State of Texas
My Commission Expires
December 15, 2018

On this 18th day of December, 2014, personally appeared before me, Changhae Park to me known and known to me to be the person aforesaid, who duly acknowledged the signing of the foregoing instrument to be his or her voluntary act and deed, and as VP of Freescale Semiconductor, Inc. did execute the same for the uses and purposes therein set forth.

WITNESS my hand and official seal.
(Seal)



Notary Public in and for the state of Texas

Angela K Zalewski
Print Name

My appointment expires on: December 15, 2018

ACCEPTED:

DATE: 1/13, 2015

Intel Corporation

By: J. PATRICK TOHER
Printed/Typed Name

Title: MANAGING COUNSEL

Signature

Schedule 1
to
Patent Assignment

Filing Date	Status	Country	Patent number	Title	Publication date	Priority date
2/3/1997	Granted	US	5,889,788	WRAPPER CELL ARCHITECTURE FOR PATH DELAY TESTING OF EMBEDDED CORE MICROPROCESSORS AND METHOD OF OPERATION		2/3/1997
1/14/1998	Granted	US	6,134,675	METHOD OF TESTING MULTI-CORE PROCESSORS AND MULTI-CORE PROCESSOR TESTING DEVICE		1/14/1998
2/7/2000	Granted	US	6,769,076	REAL-TIME PROCESSOR DEBUG SYSTEM		2/7/2000
2/6/2001	Granted	CN	ZL01103095.X	REAL-TIME PROCESSOR DEBUG SYSTEM	8/15/2001	2/7/2000
2/6/2001	Granted	JP	4916617	REAL-TIME PROCESSOR DEBUG SYSTEM	4/18/2012	2/7/2000
2/7/2001	Granted	KR	856336	REAL-TIME PROCESSOR DEBUG SYSTEM	9/4/2008	2/7/2000
1/31/2001	Granted	TW	NI-153858	REAL-TIME PROCESSOR DEBUG SYSTEM	4/21/2002	2/7/2000
1/24/2000	Granted	US	6,845,419	FLEXIBLE INTERRUPT CONTROLLER THAT INCLUDES AN INTERRUPT FORCE REGISTER		1/24/2000
1/22/2001	Granted	CN	ZL01101691.4	FLEXIBLE INTERRUPT CONTROLLER THAT INCLUDES AN INTERRUPT FORCE REGISTER	8/22/2001	1/24/2000
1/24/2001	Granted	JP	4749556	FLEXIBLE INTERRUPT CONTROLLER THAT INCLUDES AN INTERRUPT FORCE REGISTER	8/17/2011	1/24/2000
1/22/2001	Granted	KR	734158	FLEXIBLE INTERRUPT CONTROLLER THAT INCLUDES AN INTERRUPT FORCE REGISTER	7/3/2007	1/24/2000
1/5/2001	Granted	TW	NI-190461	FLEXIBLE INTERRUPT CONTROLLER THAT INCLUDES AN INTERRUPT FORCE REGISTER	11/21/2003	1/24/2000
7/25/2002	Granted	US	7,013,409	METHOD AND APPARATUS FOR DEBUGGING A DATA PROCESSING SYSTEM	1/29/2004	7/25/2002

Filing Date	Status	Country	Patent number	Title	Publication date	Priority date
8/11/2003	Granted	US	7,248,069	METHOD AND APPARATUS FOR PROVIDING SECURITY FOR DEBUG CIRCUITRY	2/17/2005	8/11/2003
8/6/2004	Granted	TW	I360991	METHOD AND APPARATUS FOR PROVIDING SECURITY FOR DEBUG CIRCUITRY	3/21/2012	8/11/2003
1/30/2006	Granted	JP	4728237	METHOD AND APPARATUS FOR PROVIDING SECURITY FOR DEBUG CIRCUITRY	7/20/2011	8/11/2003
2/10/2006	Granted	KR	10-1022639	METHOD AND APPARATUS FOR PROVIDING SECURITY FOR DEBUG CIRCUITRY		8/11/2003
1/9/2006	Granted	CN	200480019583.7	METHOD AND APPARATUS FOR PROVIDING SECURITY FOR DEBUG CIRCUITRY	8/16/2006	8/11/2003
5/27/2005	Granted	US	7,296,137	MEMORY MANAGEMENT CIRCUITRY TRANSLATION INFORMATION RETREIVAL DURING DEBUGGING	11/30/2006	5/27/2005
5/27/2005	Granted	US	7,299,335	TRANSLATION INFORMATION RETRIEVAL TRANSPARENT TO PROCESSOR CORE	11/30/2006	5/27/2005
11/12/2007	Granted	CN	200680016232	TRANSLATION INFORMATION RETRIEVAL TRANSPARENT TO PROCESSOR CORE	7/29/2009	5/27/2005
2/16/2006	Granted	US	7,444,568	METHOD AND APPARATUS FOR TESTING A DATA PROCESSING SYSTEM	11/8/2007	2/16/2006
1/25/2007	Granted	TW	I403744	METHOD AND APPARATUS FOR TESTING A DATA PROCESSING SYSTEM	8/1/2013	2/16/2006
7/30/2008	Granted	JP	5373403	METHOD AND APPARATUS FOR TESTING A DATA PROCESSING SYSTEM	12/18/2013	2/16/2006
8/14/2008	Granted	KR	10-1318697	METHOD AND APPARATUS FOR TESTING A DATA PROCESSING SYSTEM	10/16/2013	2/16/2006
5/18/2007	Granted	US	7,681,078	DEBUGGING A PROCESSOR THROUGH A RESET EVENT	11/20/2008	5/18/2007
3/5/2007	Granted	US	8,041,901	PERFORMANCE MONITORING DEVICE AND METHOD THEREOF	9/11/2008	3/5/2007
1/2/2007	Granted	US	8,341,301	DEVICE AND METHOD FOR TESTING A DIRECT MEMORY ACCESS CONTROLLER	2/11/2010	1/2/2007

Filing Date	Status	Country	Publication number/Serial number	Title	Publication date	Priority date
7/15/2004	Inactive	WO	WO2005/020280	METHOD AND APPARATUS FOR PROVIDING SECURITY FOR DEBUG CIRCUITRY	3/3/2005	8/11/2003
12/7/2005	Abandoned	IN		METHOD AND APPARATUS FOR PROVIDING SECURITY FOR DEBUG CIRCUITRY	1/4/2008	8/11/2003
3/13/2006	Dropped	EP	1656762	METHOD AND APPARATUS FOR PROVIDING SECURITY FOR DEBUG CIRCUITRY	5/17/2006	8/11/2003
3/24/2006	Inactive	WO	WO2006/130207	TRANSLATION INFORMATION RETRIEVAL	12/7/2006	5/27/2005
3/24/2006	Inactive	WO	WO2006/130208	TRANSLATION INFORMATION RETRIEVAL	12/7/2006	5/27/2005
1/18/2007	Inactive	WO	WO2007/103591	METHOD AND APPARATUS FOR TESTING A DATA PROCESSING SYSTEM	9/13/2007	2/16/2006
1/2/2007	Inactive	WO	WO2008/081346	DEVICE AND METHOD FOR TESTING A DIRECT MEMORY ACCESS CONTROLLER	7/10/2008	1/2/2007