PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
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EPAS ID: PAT3207696

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
CONVERSANT INTELLECTUAL PROPERTY MANAGEMENT INC.	01/29/2015

RECEIVING PARTY DATA

Name:	NOVACHIPS CANADA INC.
Street Address:	303 TERRY FOX DRIVE, SUITE 106
City:	OTTAWA
State/Country:	CANADA
Postal Code:	K2K 3J1

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	13643317

CORRESPONDENCE DATA

Fax Number: (888)480-9618

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 2077784870
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Correspondent Name: DENNIS R. HASZKO
Address Line 1: 499 MOSHER HILL ROAD
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ATTORNEY DOCKET NUMBER:	50908.97.MD01342_US_NPE
NAME OF SUBMITTER:	DENNIS R. HASZKO
SIGNATURE:	/Dennis R. Haszko, Reg. No. 39,575/
DATE SIGNED:	02/02/2015

Total Attachments: 25
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Form of Patent Assignment

ASSIGNMENT

WHEREAS, Conversant Intellectual Property Management Inc. ("Seller") is the owner of the patents and patent applications listed in Schedule A (the "Patents");

WHEREAS NovaChips Canada Inc., a Canadian corporation, with an address at 303 Terry Fox Drive, Suite 106, Ottawa ON K2K 3J1 ("Buyer"), is desirous of acquiring all of Seller's right, title, and interest in the Patent(s) that exist today; and

WHEREAS Buyer and Seller entered into that certain Technology Agreement dated January 16, 2015 (the "**Technology Agreement**") in respect to thereto.

NOW, THEREFORE, for and in consideration of the sum of one dollar ($1.00) and other good and valuable consideration, the receipt of which is hereby acknowledged, Seller has sold, assigned and transferred to Buyer, and does hereby sell, assign and transfer to Buyer, all of Seller's right, title and interest in and to the Patents, the same to be held and enjoyed by Buyer for its own use and enjoyment and the use and enjoyment of its successors, assigns or other legal representatives, to the end of the term for which the Patents are granted or reissued or extended as fully and entirely as the same would have been held and enjoyed by Seller if this assignment and sale had not been made, as assignee of the Seller's right, title and interest therein and in and to all damages now or hereafter due or payable (except amounts to be paid to Buyer or its Affiliates pursuant to Encumbrance Agreements as provided in the Technology Agreement) with respect thereto in and to all causes of action (either in law or in equity and whether known or unknown) and the right to sue, counterclaim, and recover for past, present and future infringement of the rights assigned or to be assigned under this Assignment.

This Assignment shall also include, to the extent that Seller had such rights, (A) the right to (i) file continuations, continuations-in-part, divisionals, reissues, reexaminations and extensions of the Patents, and to file future applications claiming priority from any of the Patents or any inventions, invention disclosures, and discoveries described or disclosed in any of the Patents; and (ii) file foreign patents, patent applications and counterparts relating to any of the Patents and items in the foregoing category (A)(i), to the extent that the right to pursue the additional applications and patents contemplated in items (i) and (ii) are available pursuant to applicable patent law(s), and (B) all enforcement rights under, or on account of, any of the Patents, including, without limitation, all causes of action and other enforcement rights for (i) damages, (ii) injunctive relief, and (iii) any other remedies of any kind for past, current and future infringement of the Patents and any foregoing items that may be available pursuant to applicable patent law.

This Assignment is executed and delivered pursuant to the Technology Agreement. Nothing contained in this instrument shall be deemed to modify, supersede, enlarge, limit or affect the rights or obligations of any person under the Technology Agreement. In the event of any conflict between this Assignment and the Technology Agreement, the provisions of the Technology Agreement shall prevail. Capitalized terms not otherwise defined herein shall have the respective meanings set forth in the Technology Agreement. This Assignment shall be governed by, and construed and enforced in accordance with, the laws of the Province of Ontario and the federal laws of Canada applicable therein.

IN TESTIMONY WHEREOF, Seller, has caused this Assignment to be executed by its duly authorized representative this 29 day of January, 2015.

CONVERSANT INTELLECTUAL PROPERTY MANAGEMENT INC.

Scott Burt
SVP and Chief Intellectual Property Officer

ATTESTATION OF SIGNATURE PURSUANT TO 28 U.S.C. § 1746

The undersigned witnessed the signature of Scott Burt to the above Assignment on behalf of Seller and makes the following statements:

1. I am over the age of 18 and competent to testify as to the facts in this Attestation block if called upon to do so.
2. Scott Burt is personally known to me (or proved to me on the basis of satisfactory evidence) and appeared before me on January 27, 2015 to execute the above Assignment on behalf of Seller.
3. Scott Burt subscribed to the above Assignment on behalf of Seller.

I declare under penalty of perjury under the laws of the United States of America that the statements made in the three (3) numbered paragraphs immediately above are true and correct.

EXECUTED on January 29, 2015 at Ottawa, ON Canada

Print Name: Edwin Faulder

Conversant HLNAND Patent(s)

Reference #	Country ID	Title	Status	Serial #	Filed Date	Publication #	Publication Date	Patent #	Issue Date
01238-TW-PAT	TW	APPARATUS AND METHOD FOR PRODUCING DEVICE IDENTIFIERS FOR SERIALLY INTERCONNECTED DEVICES OF MIXED TYPE	PUBLISHED	096146276	12/5/2007	200834318	8/16/2008		
01238-US DIV	US	APPARATUS AND METHOD FOR PRODUCING DEVICE IDENTIFIERS FOR SERIALLY INTERCONNECTED DEVICES OF MIXED TYPE	ISSUED	13/671,248	11/7/2012	2013-0067118	3/14/2013	8,694,692	4/8/2014
01238-US-PAT	US	APPARATUS AND METHOD FOR PRODUCING DEVICE IDENTIFIERS FOR SERIALLY INTERCONNECTED DEVICES OF MIXED TYPE	ISSUED	11/692,452	3/28/2007	2008-0181214	7/31/2008	8,331,361	12/11/2012
01246-TW-PAT	TW	APPARATUS AND METHOD FOR PRODUCING IDENTIFIERS REGARDLESS OF MIXED DEVICE TYPE IN A SERIAL INTERCONNECTION	ALLOWED	096146278	12/5/2007	200836210	9/1/2008		
01246-US-PAT	US	APPARATUS AND METHOD FOR PRODUCING IDENTIFIERS REGARDLESS OF MIXED DEVICE TYPE IN A SERIAL INTERCONNECTION	ISSUED	11/692,446	3/28/2007	US-2008-0192649-A1	8/14/2008	7,853,727	12/14/2010
01295-US-PAT	US	Apparatus and Method for Identifying Device Types of Series-Connected Devices of Mixed Type	ISSUED	12/025,177	2/4/2008	US-2008-0195613-A1	8/14/2008	7,991,925	8/2/2011
01246-US-CON	US	APPARATUS AND METHOD FOR PRODUCING IDENTIFIERS REGARDLESS OF MIXED DEVICE TYPE IN A SERIAL INTERCONNECTION	ISSUED	12/892,215	9/28/2010	2011-0016236 A1	1/20/2011	8,195,839	6/5/2012

Reference #	Country ID	Title	Status	Serial #	Filed Date	Publication #	Publication Date	Patent #	Issue Date
01295-US-CON	US	Apparatus and Method for Identifying Device Types of Series-Connected Devices of Mixed Type	ISSUED	13/168,157	6/24/2011	2011-0258399A1	10/20/2011	8,230,129	7/24/2012
01249-US-PAT	US	APPARATUS AND METHOD FOR IDENTIFYING DEVICE TYPE OF SERIALLY INTERCONNECTED DEVICES	ISSUED	11/692,326	3/28/2007	US-20080215778-A1	9/4/2008	8,010,710	8/30/2011
01251-BE-VALD	BE	METHODS AND APPARATUS FOR CLOCK SIGNAL SYNCHRONIZATION IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ISSUED	11009644.3	2/5/2008	2428960	3/14/2012	2428960	10/9/2013
01251-DE-VAL	DE	METHODS AND APPARATUS FOR CLOCK SIGNAL SYNCHRONIZATION IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ISSUED	602008017274.0	2/5/2008	2118902	11/18/2009	2118902	7/18/2012
01251-DE-VALD	DE	METHODS AND APPARATUS FOR CLOCK SIGNAL SYNCHRONIZATION IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ISSUED	602008028063.2	2/5/2008	2428960	3/14/2012	2428960	10/9/2013
01251-ES-VALD	ES	METHODS AND APPARATUS FOR CLOCK SIGNAL SYNCHRONIZATION IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ISSUED	11009644.3	2/5/2008	2428960	3/14/2012	2428960	10/9/2013
01251-FI-VALD	FI	METHODS AND APPARATUS FOR CLOCK SIGNAL SYNCHRONIZATION IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ISSUED	11009644.3	2/5/2008	2428960	3/14/2012	2428960	10/9/2013

Reference #	Country ID	Title	Status	Serial #	Filed Date	Publication #	Publication Date	Patent #	Issue Date
01251-FR-VAL	FR	METHODS AND APPARATUS FOR CLOCK SIGNAL SYNCHRONIZATION IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ISSUED	08714560.3	2/5/2008	2118902	11/18/2009	2118902	7/18/2012
01251-FR-VALD	FR	METHODS AND APPARATUS FOR CLOCK SIGNAL SYNCHRONIZATION IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ISSUED	11009644.3	2/5/2008	2428960	3/14/2012	2428960	10/9/2013
01251-GB-VAL	GB	METHODS AND APPARATUS FOR CLOCK SIGNAL SYNCHRONIZATION IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ISSUED	08714560.3	2/5/2008	2118902	11/18/2009	2118902	7/18/2012
01251-GB-VALD	GB	METHODS AND APPARATUS FOR CLOCK SIGNAL SYNCHRONIZATION IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ISSUED	11009644.3	2/5/2008	2428960	3/14/2012	2428960	10/9/2013
01251-IE-VALD	IE	METHODS AND APPARATUS FOR CLOCK SIGNAL SYNCHRONIZATION IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ISSUED	11009644.3	2/5/2008	2428960	3/14/2012	2428960	10/9/2013
01251-IT-VALD	IT	METHODS AND APPARATUS FOR CLOCK SIGNAL SYNCHRONIZATION IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ISSUED	11009644.3	2/5/2008	2428960	3/14/2012	2428960	10/9/2013

Reference #	Country ID	Title	Status	Serial #	Filed Date	Publication #	Publication Date	Patent #	Issue Date
01251-JP-NPE	JP	METHODS AND APPARATUS FOR CLOCK SIGNAL SYNCHRONIZATION IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ISSUED	2009-552980	2/5/2008	2010-524277	7/15/2010	5334869	8/9/2013
01251-JP-DIV	JP	METHODS AND APPARATUS FOR CLOCK SIGNAL SYNCHRONIZATION IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ALLOWED	2013-155351	2/5/2008	2013-236398	11/21/2013		
01251-KR-NPE	KR	METHODS AND APPARATUS FOR CLOCK SIGNAL SYNCHRONIZATION IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ISSUED	10-2009-7023268	2/5/2008	10-2010-0015511	2/12/2010	10-1454948	10/20/2014
01251-NL-VALD	NL	METHODS AND APPARATUS FOR CLOCK SIGNAL SYNCHRONIZATION IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ISSUED	11009644.3	2/5/2008	2428960	3/14/2012	2428960	10/9/2013
01251-SE-VALD	SE	METHODS AND APPARATUS FOR CLOCK SYNCHRONIZATION IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ISSUED	11009644.3	2/5/2008			2428960	10/9/2013
01251-TW-PAT	TW	METHODS AND APPARATUS FOR CLOCK SIGNAL SYNCHRONIZATION IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ALLOWED	097105903	2/20/2008	200904110	1/16/2009		

Reference #	Country ID	Title	Status	Serial #	Filed Date	Publication #	Publication Date	Patent #	Issue Date
01251-US-PAT	US	METHODS AND APPARATUS FOR CLOCK SIGNAL SYNCHRONIZATION IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ISSUED	11/959,996	12/19/2007	2008-0226004	9/18/2008	7,865,756	1/4/2011
01251-US-CON	US	METHODS AND APPARATUS FOR CLOCK SIGNAL SYNCHRONIZATION IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ISSUED	12/948,186	11/17/2010	2011-0060934	3/10/2011	8,713,344	4/29/2014
01227-EP-NPE	EP	CIRCUIT AND METHOD FOR TESTING MULTI-DEVICE SYSTEMS	PUBLISHED	07845609.2	11/29/2007	2102869	9/23/2009		
01227-KR-NPE	KR	CIRCUIT AND METHOD FOR TESTING MULTI-DEVICE SYSTEMS	ISSUED	10-2009-7013534	11/29/2007	10-2009-0086616	8/13/2009	10-1445889	9/23/2014
01227-KR-DIV	KR	CIRCUIT AND METHOD FOR TESTING MULTI-DEVICE SYSTEMS	ISSUED	10-2012-7032081	11/29/2007	10-2013-0001338	1/3/2013	10-1404887	5/30/2014
01227-TW-PAT	TW	CIRCUIT AND METHOD FOR TESTING MULTI-DEVICE SYSTEMS	ISSUED	096145535	11/29/2007	200837769	9/16/2008	I462108	11/21/2014
01227-US-PAT	US	CIRCUIT AND METHOD FOR TESTING MULTI-DEVICE SYSTEMS	ISSUED	11/565,327	11/30/2006	2008-0130386	6/5/2008	7,508,724	3/24/2009
01227-US-CON	US	CIRCUIT AND METHOD FOR TESTING MULTI-DEVICE SYSTEMS	ISSUED	12/391,810	2/24/2009	2009-0161458	6/25/2009	7,679,976	3/16/2010
01227-US-CON2	US	CIRCUIT AND METHOD FOR TESTING MULTI-DEVICE SYSTEMS	ISSUED	12/698,585	2/2/2010	2010-0135092	6/3/2010	7,911,860	3/22/2011
01227-US-CON3	US	CIRCUIT AND METHOD FOR TESTING MULTI-DEVICE SYSTEMS	ISSUED	13/030,785	2/18/2011	2011-0141835	6/16/2011	8,081,529	12/20/2011
01268-CN-NPE	CN	RING-OF-CLUSTERS NETWORK TOPOLOGIES	ALLOWED	200880124561.5	11/26/2008	101971574	2/9/2011		
01268-EP-NPE	EP	RING-OF-CLUSTERS NETWORK TOPOLOGIES	PUBLISHED	08869521.8	11/26/2008	2243257	10/27/2010		
01268-JP-DIV	JP	RING-OF-CLUSTERS NETWORK TOPOLOGIES	PUBLISHED	2013-187109	11/26/2008	2014-014160	1/23/2014		

Reference #	Country ID	Title	Status	Serial #	Filed Date	Publication #	Publication Date	Patent #	Issue Date
01268-KR-NPE	KR	RING-OF-CLUSTERS NETWORK TOPOLOGIES	PUBLISHED	10-2010-7016557	11/26/2008	10-2010-0126665	12/2/2010		
01268-TW-PAT	TW	SYSTEM, METHOD AND SEMICONDUCTOR DEVICE FOR RING-OF-CLUSTERS NETWORK TOPOLOGIES	ISSUED	098100742	1/9/2009	200939036	9/16/2009	I457765	10/21/2014
01268-US-PAT	US	RING-OF-CLUSTERS NETWORK TOPOLOGIES	ISSUED	12/013,148	1/11/2008	2009-0180483	7/16/2009	8,594,110	11/26/2013
01268-US-CON	US	RING-OF-CLUSTERS NETWORK TOPOLOGIES	ISSUED	14/057,102	10/18/2013	2014-0115190	4/24/2014	8,902,910	12/2/2014
01266-TW-PAT	TW	SINGLE-STROBE OPERATION OF MEMORY DEVICES	ISSUED	097137924	10/2/2008	200931437	7/16/2009	I396204	5/11/2013
01266-TW-DIV	TW	SINGLE-STROBE OPERATION OF MEMORY DEVICES	PUBLISHED	102101486	10/2/2008	201324529	6/16/2013		
01266-US-PAT	US	SINGLE-STROBE OPERATION OF MEMORY DEVICES	ISSUED	11/873,475	10/17/2007	2009-0103378	4/23/2009	7,889,578	2/15/2011
01266-US-DIV	US	SINGLE-STROBE OPERATION OF MEMORY DEVICES	ISSUED	12/984,987	1/5/2011	2011-0096614	4/28/2011	8,406,070	3/26/2013
01266-US-CON	US	SINGLE-STROBE OPERATION OF MEMORY DEVICES	ISSUED	13/836,702	3/15/2013	2013-0201775	8/8/2013	8,675,425	3/18/2014
01279-US-PAT	US	DATA CHANNEL TEST APPARATUS AND METHOD THEREOF	ISSUED	12/028,335	2/8/2008	2009-0138768	5/28/2009	7,913,128	3/22/2011
01279-US-CON	US	DATA CHANNEL TEST APPARATUS AND METHOD THEREOF	ISSUED	13/033,294	2/23/2011	2011-0154137	6/23/2011	8,392,767	3/5/2013
01281-TW-PAT	TW	SEMICONDUCTOR MEMORY DEVICE SUITABLE FOR INTERCONNECTION IN A RING TOPOLOGY	PUBLISHED	097140432	10/22/2008	200933646	8/1/2009		
01281-US-PAT	US	SEMICONDUCTOR MEMORY DEVICE SUITABLE FOR INTERCONNECTION IN A RING TOPOLOGY	ISSUED	12/141,384	6/18/2008	2009-0154284	6/18/2009	8,825,939	9/2/2014
01282-US-CIP	US	MEMORY CONTROLLER WITH FLEXIBLE DATA ALIGNMENT TO CLOCK	ISSUED	12/325,074	11/28/2008	20090154285	6/18/2009	8,467,486	6/18/2013
01282-US-CON	US	MEMORY CONTROLLER WITH FLEXIBLE DATA ALIGNMENT TO CLOCK	ISSUED	13/887,937	5/6/2013	2013-0243137	9/19/2013	8,837,655	9/16/2014
01282-US-CON2	US	MEMORY CONTROLLER WITH FLEXIBLE DATA ALIGNMENT TO CLOCK	PENDING	14/486,484	9/15/2014				

Reference #	Country ID	Title	Status	Serial #	Filed Date	Publication #	Publication Date	Patent #	Issue Date
01261-CA-NPE	CA	DAISY-CHAIN MEMORY CONFIGURATION AND USAGE	PUBLISHED	2,695,896	8/27/2008	2,695,396	3/5/2009		
01261-EP-NPE	EP	DAISY-CHAIN MEMORY CONFIGURATION AND USAGE	PUBLISHED	08783415.6	8/27/2008	2183748	5/12/2010		
01261-KR-NPE	KR	DAISY-CHAIN MEMORY CONFIGURATION AND USAGE	PUBLISHED	10-2010-7006531	8/27/2008	10-2010-0075860	7/5/2010		
01261-US-PAT	US	DAISY-CHAIN MEMORY CONFIGURATION AND USAGE	PUBLISHED	11/897,105	8/29/2007	2009-0063786	3/5/2009		
01263-TW-PAT	TW	REDUCED PIN COUNT INTERFACE	ISSUED	097128676	7/29/2008	200929246	7/1/2009	I410980	10/1/2013
01263-TW-DIV	TW	REDUCED PIN COUNT INTERFACE	PUBLISHED	101141335	7/29/2008	201316851	4/16/2013		
01263-US-PAT	US	REDUCED PIN COUNT INTERFACE	ISSUED	11/843,024	8/22/2007	2008-0201496	8/21/2008	8,122,202	2/21/2012
01263-US-DIV	US	REDUCED PIN COUNT INTERFACE	ISSUED	13/364,685	2/2/2012	2012-0137050	5/31/2012	8,825,966	9/2/2014
01290-CN-NPE	CN	CLOCK REPRODUCING AND TIMING METHOD IN A SYSTEM HAVING A PLURALITY OF DEVICES AND MEMORY CONTROLLER WITH FLEXIBLE DATA ALIGNMENT	ISSUED	200880120501.6	12/4/2008	101897119	11/24/2010	ZL200880120501.6	4/30/2014
01290-CN-DIV	CN	CLOCK REPRODUCING AND TIMING METHOD IN A SYSTEM HAVING A PLURALITY OF DEVICES AND MEMORY CONTROLLER WITH FLEXIBLE DATA ALIGNMENT	PUBLISHED	201110397274.5	12/4/2008	102623039	8/1/2012		
01290-EP-NPE	EP	CLOCK REPRODUCING AND TIMING METHOD IN A SYSTEM HAVING A PLURALITY OF DEVICES AND MEMORY CONTROLLER WITH FLEXIBLE DATA ALIGNMENT	PUBLISHED	08861510.9	12/4/2008	2220766	8/25/2010		

Reference #	Country ID	Title	Status	Serial #	Filed Date	Publication #	Publication Date	Patent #	Issue Date
01290-HK-FPR	HK	CLOCK REPRODUCING AND TIMING METHOD IN A SYSTEM HAVING A PLURALITY OF DEVICES AND MEMORY CONTROLLER WITH FLEXIBLE DATA ALIGNMENT	PUBLISHED	13101401.6	12/4/2008	1174734	6/14/2013		
01290-JP-NPE	JP	MEMORY CONTROLLER WITH FLEXIBLE DATA AUGNMENT TO CLOCK	ISSUED	2010-537216	12/4/2008	2011-507358	3/3/2011	5523933	4/18/2014
01290-JP-DIV	JP	CLOCK REPRODUCING AND TIMING METHOD IN A SYSTEM HAVING A PLURALITY OF DEVICES AND MEMORY CONTROLLER WITH FLEXIBLE DATA AUGNMENT	ISSUED	2011-251459	12/4/2008	2012-085318	4/26/2012	5662922	6/20/2014
01290-JP-DIV2	JP	CLOCK REPRODUCING AND TIMING METHOD IN A SYSTEM HAVING A PLURALITY OF DEVICES AND MEMORY CONTROLLER WITH FLEXIBLE DATA AUGNMENT	ISSUED	2011-272153	12/4/2008	2012-060677	3/22/2012	5432976	12/13/2013
01290-KR-NPE	KR	CLOCK REPRODUCING AND TIMING METHOD IN A SYSTEM HAVING A PLURALITY OF DEVICES AND MEMORY CONTROLLER WITH FLEXIBLE DATA AUGNMENT	PUBLISHED	10-2010-7009666	12/4/2008	10-2010-0092930	8/23/2010		
01290-KR-DIV	KR	CLOCK REPRODUCING AND TIMING METHOD IN A SYSTEM HAVING A PLURALITY OF DEVICES AND MEMORY CONTROLLER WITH FLEXIBLE DATA AUGNMENT	PUBLISHED	10-2013-7031682	12/4/2008	10-2014-0007468	1/17/2014		

Reference #	Country ID	Title	Status	Serial #	Filed Date	Publication #	Publication Date	Patent #	Issue Date
01290-TW-PAT	TW	CLOCK REPRODUCING AND TIMING METHOD IN A SYSTEM HAVING A PLURALITY OF DEVICES AND MEMORY CONTROLLER WITH FLEXIBLE DATA ALIGNMENT	PUBLISHED	097147841	12/9/2008	200941945	10/1/2009		
01290-TW-DIV	TW	CLOCK REPRODUCING AND TIMING METHOD IN A SYSTEM HAVING A PLURALITY OF DEVICES AND MEMORY CONTROLLER WITH FLEXIBLE DATA ALIGNMENT	PUBLISHED	100144204	12/9/2008	201214975	4/1/2012		
01290-US-PAT	US	CLOCK REPRODUCING AND TIMING METHOD IN A SYSTEM HAVING A PLURALITY OF DEVICES	ISSUED	12/168,091	7/4/2008	US 2009-0154629	6/18/2009	8,781,053	7/15/2014
01290-US-CON	US	CLOCK REPRODUCING AND TIMING METHOD IN A SYSTEM HAVING A PLURALITY OF DEVICES	PUBLISHED	14/294,372	6/3/2014	2014-0341328	11/20/2014		
01291-TW-PAT	TW	OPERATIONAL MODE CONTROL IN SERIAL-CONNECTED MEMORY BASED ON IDENTIFIER	ISSUED	098102586	1/22/2009	200943313	10/16/2009	I406296	8/21/2013
01291-TW-DIV	TW	OPERATIONAL MODE CONTROL IN SERIAL-CONNECTED MEMORY BASED ON IDENTIFIER	PUBLISHED	102121366	1/22/2009	201342391	10/16/2013		
01291-US-REI	US	OPERATIONAL MODE CONTROL IN SERIAL-CONNECTED MEMORY BASED ON IDENTIFIER	ISSUED	13/774,477	1/12/2009			RE44,926	2/22/2011
01294-BE-VAL	BE	SELECTIVE BROADCASTING OF DATA IN SERIES CONNECTED DEVICES	ISSUED	09001914.2	2/11/2009			2251872	4/9/2014
01294-DE-VAL	DE	SELECTIVE BROADCASTING OF DATA IN SERIES CONNECTED DEVICES	ISSUED	602009023043.3	2/11/2009			2251872	4/9/2014
01294-ES-VAL	ES	SELECTIVE BROADCASTING OF DATA IN SERIES CONNECTED DEVICES	ISSUED	09001914.2	2/11/2009			2251872	4/9/2014

Reference #	Country ID	Title	Status	Serial #	Filed Date	Publication #	Publication Date	Patent #	Issue Date
01294-FI-VAL	FI	SELECTIVE BROADCASTING OF DATA IN SERIES CONNECTED DEVICES	ISSUED	09001914.2	2/11/2009			2251872	4/9/2014
01294-FR-VAL	FR	SELECTIVE BROADCASTING OF DATA IN SERIES CONNECTED DEVICES	ISSUED	09001914.2	2/11/2009			2251872	4/9/2014
01294-GB-VAL	GB	SELECTIVE BROADCASTING OF DATA IN SERIES CONNECTED DEVICES	ISSUED	09001914.2	2/11/2009			2251872	4/9/2014
01294-IE-VAL	IE	SELECTIVE BROADCASTING OF DATA IN SERIES CONNECTED DEVICES	ISSUED	09001914.2	2/11/2009			2251872	4/9/2014
01294-IT-VAL	IT	SELECTIVE BROADCASTING OF DATA IN SERIES CONNECTED DEVICES	ISSUED	09001914.2	2/11/2009			2251872	4/9/2014
01294-NL-VAL	NL	SELECTIVE BROADCASTING OF DATA IN SERIES CONNECTED DEVICES	ISSUED	09001914.2	2/11/2009			2251872	4/9/2014
01294-SE-VAL	SE	SELECTIVE BROADCASTING OF DATA IN SERIES CONNECTED DEVICES	ISSUED	09001914.2	2/11/2009			2251872	4/9/2014
01294-TW-PAT	TW	SELECTIVE BROADCASTING OF DATA IN SERIES CONNECTED DEVICES	ISSUED	098104050	2/9/2009	201017414	5/1/2010	I442236	6/21/2014
01294-US-PAT	US	SELECTIVE BROADCASTING OF DATA IN SERIES CONNECTED DEVICES	ISSUED	12/254,315	10/20/2008	2009-0198857	8/6/2009	8,131,913	3/6/2012
01300-CA-NPE	CA	MASS DATA STORAGE SYSTEM WITH NON-VOLATILE MEMORY MODULES	PUBLISHED	2,774,396	8/27/2009	2,774,396	3/25/2010		
01300-CN-NPE	CN	MASS DATA STORAGE SYSTEM WITH NON-VOLATILE MEMORY MODULES	PUBLISHED	200980146068.8	8/27/2009	102216992 A	10/12/2011		
01300-EP-NPE	EP	MASS DATA STORAGE SYSTEM WITH NON-VOLATILE MEMORY MODULES	PUBLISHED	09813922.3	8/27/2009	2342712	7/13/2011		
01300-KR-NPE	KR	MASS DATA STORAGE SYSTEM WITH NON-VOLATILE MEMORY MODULES	PUBLISHED	10-2011-7006236	8/27/2009	10-2011-0081809	7/14/2011		
01300-TW-PAT	TW	MASS DATA STORAGE SYSTEM WITH NON-VOLATILE MEMORY MODULES	PUBLISHED	098128854	8/27/2009	201025017	7/1/2010		
01300-US-PAT	US	MASS DATA STORAGE SYSTEM WITH NON-VOLATILE MEMORY MODULES	PUBLISHED	12/212,902	9/18/2008	2010-0067278	3/18/2010		

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01302-US-PAT	US	MIXED DATA RATES IN MEMORY DEVICES AND SYSTEMS	ISSUED	12/169,115	7/8/2008	2010-0011174	1/14/2010	8,139,390	3/20/2012
01304-CN-NPE	CN	SERIAL-CONNECTED MEMORY SYSTEM WITH OUTPUT DELAY ADJUSTMENT	ALLOWED	200980138194.9	9/17/2009	102165529A	8/24/2011		
01304-EP-NPE	EP	SERIAL-CONNECTED MEMORY SYSTEM WITH OUTPUT DELAY ADJUSTMENT	PUBLISHED	09817125.9	9/17/2009	2329496	6/8/2011		
01304-JP-NPE	JP	SERIAL-CONNECTED MEMORY SYSTEM WITH DUTY CYCLE CORRECTION	PUBLISHED	2011-528145	9/17/2009	2012-504263	2/16/2012		
01304-JP-DIV	JP	SERIAL-CONNECTED MEMORY SYSTEM WITH OUTPUT DELAY ADJUSTMENT	ISSUED	2012-193816	9/17/2009	2013-8386	1/10/2013	5599852	8/22/2014
01304-KR-NPE	KR	SERIAL-CONNECTED MEMORY SYSTEM WITH OUTPUT DELAY ADJUSTMENT	PUBLISHED	10-2011-7006956	9/17/2009	10-2011-0081958	7/15/2011		
01304-TW-PAT	TW	SERIAL-CONNECTED MEMORY SYSTEM WITH OUTPUT DELAY ADJUSTMENT	PUBLISHED	098132332	9/24/2009	201027556	7/16/2010		
01304-US-PAT	US	SERIAL-CONNECTED MEMORY SYSTEM WITH DUTY CYCLE CORRECTION	ISSUED	12/241,960	9/30/2008	2010-0083028	4/1/2010	8,161,313	4/17/2012
01305-US-PAT	US	SERIAL-CONNECTED MEMORY SYSTEM WITH OUTPUT DELAY ADJUSTMENT	ISSUED	12/241,832	9/30/2008	2010-0083027	4/1/2010	8,181,056	5/15/2012
01308-CN-NPE	CN	SEMICONDUCTOR DEVICE WITH MAIN MEMORY UNIT AND AUXILIARY MEMORY UNIT REQUIRING PRESET OPERATION	ISSUED	200980151065.3	12/17/2009	102257568	11/23/2011	ZL200980151065.3	9/18/2013
01308-CN-DIV	CN	SEMICONDUCTOR DEVICE WITH MAIN MEMORY UNIT AND AUXILIARY MEMORY UNIT REQUIRING PRESET OPERATION	PUBLISHED	201310425360.1	12/17/2009	103559905	2/5/2014		
01308-EP-NPE	EP	SEMICONDUCTOR DEVICE WITH MAIN MEMORY UNIT AND AUXILIARY MEMORY UNIT REQUIRING PRESET OPERATION	ALLOWED	09832790.1	12/17/2009	2359369	8/24/2011		
01308-HK-FPD	HK	SEMICONDUCTOR DEVICE WITH MAIN MEMORY UNIT AND AUXILIARY MEMORY UNIT REQUIRING PRESET OPERATION	PENDING	14108020.1	12/17/2009	1194853	24/10/2014		

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01308-JP-NPE	JP	SEMICONDUCTOR DEVICE WITH MAIN MEMORY UNIT AND AUXILIARY MEMORY UNIT REQUIRING PRESET OPERATION	PUBLISHED	2011-541050	12/17/2009	2012-512469	5/31/2012		
01308-KR-NPE	KR	SEMICONDUCTOR DEVICE WITH MAIN MEMORY UNIT AND AUXILIARY MEMORY UNIT REQUIRING PRESET OPERATION	PUBLISHED	10-2011-7009598	12/17/2009	10-2011-0104477	9/22/2011		
01308-TW-PAT	TW	SEMICONDUCTOR DEVICE WITH MAIN MEMORY UNIT AND AUXILIARY MEMORY UNIT REQUIRING PRESET OPERATION	ISSUED	098143317	12/17/2009	201030747	8/16/2010	I443658	7/1/2014
01308-TW-DIV	TW	SEMICONDUCTOR DEVICE WITH MAIN MEMORY UNIT AND AUXILIARY MEMORY UNIT REQUIRING PRESET OPERATION	PUBLISHED	103112465	12/17/2009	201432685	8/16/2014		
01308-US-PAT	US	DEVICE AND METHOD FOR TRANSFERRING DATA TO A NON-VOLATILE MEMORY DEVICE	ISSUED	12/337,841	12/18/2008	2010-0161877	6/24/2010	8,037,235	10/11/2011
01308-US-CIP	US	SEMICONDUCTOR DEVICE WITH MAIN MEMORY UNIT AND AUXILIARY MEMORY UNIT REQUIRING PRESET OPERATION	ISSUED	12/640,388	12/17/2009	US-2010-0157715-A1	6/24/2010	8,194,481	6/5/2012
01306-US-PAT	US	DATA MIRRORING IN SERIAL-CONNECTED MEMORY SYSTEM	ISSUED	12/399,315	3/6/2009	2010-0115217	5/6/2010	8,200,925	6/12/2012
01310-CN-NPE	CN	SOLID STATE DRIVE OR OTHER STORAGE APPARATUS THAT INCLUDES A PLURALITY OF ENCAPSULATED SEMICONDUCTOR CHIPS	ALLOWED	200980144853.X	11/13/2009	102210022 A	10/5/2011		
01310-EP-NPE	EP	SOLID STATE DRIVE OR OTHER STORAGE APPARATUS THAT INCLUDES A PLURALITY OF ENCAPSULATED SEMICONDUCTOR CHIPS	PUBLISHED	09826687.8	11/13/2009	2347442	7/27/2011		

Reference #	Country ID	Title	Status	Serial #	Filed Date	Publication #	Publication Date	Patent #	Issue Date
01310-JP-NPE	JP	SOLID STATE DRIVE OR OTHER STORAGE APPARATUS THAT INCLUDES A PLURALITY OF ENCAPSULATED SEMICONDUCTOR CHIPS	PUBLISHED	2011-535844	11/13/2009	2012508968	4/12/2012		
01310-KR-NPE	KR	SOLID STATE DRIVE OR OTHER STORAGE APPARATUS THAT INCLUDES A PLURALITY OF ENCAPSULATED SEMICONDUCTOR CHIPS	PUBLISHED	10-2011-7010009	11/13/2009	10-2011-0099237	9/7/2011		
01310-US-PAT	US	SYSTEM INCLUDING A PLURALITY OF ENCAPSULATED SEMICONDUCTOR CHIPS	ISSUED	12/367,056	2/6/2009	2010-0118482	5/13/2010	8,472,199	6/25/2013
01310-US-CON	US	SYSTEM INCLUDING A PLURALITY OF ENCAPSULATED SEMICONDUCTOR CHIPS	ISSUED	13/917,728	6/14/2013	2013-0271910	10/17/2013	8,908,378	12/9/2014
01311-CN-NPE	CN	ERROR DETECTION METHOD AND A SYSTEM INCLUDING ONE OR MORE MEMORY DEVICES	ALLOWED	200980151271.4	12/10/2009	102257573	11/23/2011		
01311-EP-NPE	EP	ERROR DETECTION METHOD AND A SYSTEM INCLUDING ONE OR MORE MEMORY DEVICES	PUBLISHED	09832759.6	12/10/2009	2359372	8/24/2011		
01311-JP-NPE	JP	ERROR DETECTION METHOD AND A SYSTEM INCLUDING ONE OR MORE MEMORY DEVICES	PUBLISHED	2011-541038	12/10/2009	2012-512467	5/31/2012		
01311-JP-DIV	JP	ERROR DETECTION METHOD AND A SYSTEM INCLUDING ONE OR MORE MEMORY DEVICES	PENDING	2014-257755	12/10/2009				
01311-KR-NPE	KR	ERROR DETECTION METHOD AND A SYSTEM INCLUDING ONE OR MORE MEMORY DEVICES	PUBLISHED	10-2011-7009393	12/10/2009	10-2011-0103388	9/20/2011		
01311-TW-PAT	TW	ERROR DETECTION METHOD AND A SYSTEM INCLUDING ONE OR MORE MEMORY DEVICES	PUBLISHED	098142289	12/10/2009	201106369	2/16/2011		
01311-US-PAT	US	ERROR DETECTION METHOD AND A SYSTEM INCLUDING ONE OR MORE MEMORY DEVICES	ISSUED	12/418,892	4/6/2009	2010-0162053	6/24/2010	8,880,970	11/4/2014

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01311-US-CON	US	ERROR DETECTION METHOD AND A SYSTEM INCLUDING ONE OR MORE MEMORY DEVICES	PENDING	14/503,714	10/1/2014				
01315-CA-NPE	CA	CONFIGURABLE MODULE AND MEMORY SUBSYSTEM	PUBLISHED	2,738,350	5/20/2010	2,738,350	11/25/2010		
01315-CN-NPE	CN	CONFIGURABLE MODULE AND MEMORY SUBSYSTEM	PUBLISHED	201080003916.0	5/20/2010	102187396 A	9/14/2011		
01315-DE-NPE	DE	CONFIGURABLE MODULE AND MEMORY SUBSYSTEM	PUBLISHED	112010002059.0	5/20/2010	112010002059 T5	9/13/2012		
01315-EP-NPE	EP	CONFIGURABLE MODULE AND MEMORY SUBSYSTEM	PUBLISHED	10777275.8	5/20/2010	2443629	4/25/2012		
01315-IN-NPE	IN	CONFIGURABLE MODULE AND MEMORY SUBSYSTEM	PENDING	421/MUMNP/2011	5/20/2010				
01315-JP-NPE	JP	CONFIGURABLE MODULE AND MEMORY SUBSYSTEM	ALLOWED	2012-511109	5/20/2010	2012-527661	11/8/2012		
01315-KR-NPE	KR	CONFIGURABLE MODULE AND MEMORY SUBSYSTEM	PUBLISHED	10-2011-7009822	5/20/2010	10-2012-0030328	3/28/2012		
01315-US-PAT	US	CONFIGURABLE MODULE AND MEMORY SUBSYSTEM	ISSUED	12/770,376	4/29/2010	2010-0296256	11/25/2010	8,503,211	8/6/2013
01315-US-CON	US	CONFIGURABLE MODULE AND MEMORY SUBSYSTEM	ISSUED	13/957,713	8/2/2013	2013-0322173	12/5/2013	8,767,430	7/1/2014
01318-US-PAT	US	SIMULTANEOUS READ AND WRITE DATA TRANSFER	ISSUED	12/504,156	7/16/2009	2011-0016279	1/20/2011	8,521,980	8/27/2013
01318-US-CON	US	SIMULTANEOUS READ AND WRITE DATA TRANSFER	ISSUED	13/962,062	8/8/2013	2014-0013041	1/9/2014	8,898,415	11/25/2014
01323-US-PAT	US	SEMICONDUCTOR MEMORY WITH MULTIPLE WORDLINE SELECTION	ISSUED	12/564,492	9/22/2009	2011-0032784	2/10/2011	8,068,382	11/29/2011
01332-US-PAT	US	MEMORY SYSTEM HAVING A PLURALITY OF SERIALLY CONNECTED DEVICES	ISSUED	12/782,911	5/19/2010	2011-0235426	9/29/2011	8,582,382	11/12/2013
01332-US-CON	US	MEMORY SYSTEM HAVING A PLURALITY OF SERIALLY CONNECTED DEVICES	ISSUED	14/046,857	10/4/2013	2014-0029347	1/30/2014	8,897,090	11/25/2014
01339-US-PAT	US	SYSTEM OF INTERCONNECTED NONVOLATILE MEMORIES HAVING AUTOMATIC STATUS PACKET	ISSUED	13/048,154	3/15/2011	2011-0264846	10/27/2011	8,843,692	9/23/2014
01340-CA-NPE	CA	STATUS INDICATION IN A SYSTEM HAVING A PLURALITY OF MEMORY DEVICES	PUBLISHED	2,800,612	4/19/2011	2,800,612	10/27/2011		

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01340-CN-NPE	CN	STATUS INDICATION IN A SYSTEM HAVING A PLURALITY OF MEMORY DEVICES	PUBLISHED	201180019962 6	4/19/2011	102859599 A	1/2/2013		
01340-EP-NPE	EP	STATUS INDICATION IN A SYSTEM HAVING A PLURALITY OF MEMORY DEVICES	PUBLISHED	11771440.2	4/19/2011	2561510	2/27/2013		
01340-HK-FPR	HK	STATUS INDICATION IN A SYSTEM HAVING A PLURALITY OF MEMORY DEVICES	PUBLISHED	13107634.2	4/19/2011	1180450A	10/18/2013		
01340-JP-NPE	JP	STATUS INDICATION IN A SYSTEM HAVING A PLURALITY OF MEMORY DEVICES	PUBLISHED	2013-506287	4/19/2011	2013-525889	6/20/2013		
01340-KR-NPE	KR	STATUS INDICATION IN A SYSTEM HAVING A PLURALITY OF MEMORY DEVICES	PUBLISHED	10-2012-7029945	4/19/2011	10-2013-0107195	10/1/2013		
01340-TW-PAT	TW	STATUS INDICATION IN A SYSTEM HAVING A PLURALITY OF MEMORY DEVICES	PUBLISHED	100113549	4/19/2011	201209821	3/1/2012		
01340-US-PAT	US	STATUS INDICATION IN A SYSTEM HAVING A PLURALITY OF MEMORY DEVICES	PUBLISHED	13/023,838	2/9/2011	2011-0258366	10/20/2011		
01341-CA-NPE	CA	HIGH SPEED INTERFACE FOR DAISY-CHAINED DEVICES	PENDING	2,801,153	5/31/2011				
01341-CN-NPE	CN	HIGH SPEED INTERFACE FOR DAISY-CHAINED DEVICES	PUBLISHED	201180026589 7	5/31/2011	102947806	2/27/2013		
01341-EP-NPE	EP	HIGH SPEED INTERFACE FOR DAISY-CHAINED DEVICES	PUBLISHED	11789005.3	5/31/2011	2577473	4/10/2013		
01341-HK-FPR	HK	HIGH SPEED INTERFACE FOR DAISY-CHAINED DEVICES	PUBLISHED	13109960.2	5/31/2011	1182794	12/6/2013		
01341-JP-NPE	JP	HIGH SPEED INTERFACE FOR DAISY-CHAINED DEVICES	ISSUED	2013-512704	5/31/2011	2013-527541	6/27/2013	5643896	11/7/2014
01341-KR-NPE	KR	HIGH SPEED INTERFACE FOR DAISY-CHAINED DEVICES	PENDING	10-2012-7033816	5/31/2011	10-2013-0085956	07/30/2013		
01341-US-PAT	US	HIGH SPEED INTERFACE FOR DAISY-CHAINED DEVICES	ISSUED	13/012,754	1/24/2011	2011-0296056	12/1/2011	8,463,959	6/11/2013
01341-US-CON	US	HIGH SPEED INTERFACE FOR DAISY-CHAINED DEVICES	PUBLISHED	13/914,125	6/10/2013	2013-0275628	10/17/2013		
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01342-US-NPE	US	SERIALLY CONNECTED MEMORY HAVING SUBDIVIDED DATA INTERFACE	ALLOWED	13/643,317	4/26/2011	2013-0086334	4/4/2013		
01346-CA-NPE	CA	METHOD AND APPARATUS FOR CONCURRENTLY READING A PLURALITY OF MEMORY DEVICES USING A SINGLE BUFFER	PENDING	2,798,868	5/6/2011				
01346-CN-NPE	CN	METHOD AND APPARATUS FOR CONCURRENTLY READING A PLURALITY OF MEMORY DEVICES USING A SINGLE BUFFER	PUBLISHED	201180033300	5/6/2011	102971795	3/13/2013		
01346-EP-NPE	EP	METHOD AND APPARATUS FOR CONCURRENTLY READING A PLURALITY OF MEMORY DEVICES USING A SINGLE BUFFER	PUBLISHED	11777075.0	5/6/2011	2567379	3/13/2013		
01346-HK-FPR	HK	METHOD AND APPARATUS FOR CONCURRENTLY READING A PLURALITY OF MEMORY DEVICES USING A SINGLE BUFFER	PUBLISHED	13109959.5	5/6/2011	1182831	12/6/2013		
01346-JP-NPE	JP	METHOD AND APPARATUS FOR CONCURRENTLY READING A PLURALITY OF MEMORY DEVICES USING A SINGLE BUFFER	ALLOWED	2013-508340	5/6/2011	2013-525924	6/20/2013		
01346-KR-NPE	KR	METHOD AND APPARATUS FOR CONCURRENTLY READING A PLURALITY OF MEMORY DEVICES USING A SINGLE BUFFER	PUBLISHED	10-2012-7031992	5/6/2011	10-2013-0071436	6/28/2013		
01346-TW-PAT	TW	METHOD AND APPARATUS FOR CONCURRENTLY READING A PLURALITY FLASH CHIPS USING SINGLE SRAM BUFFER	PUBLISHED	100115972	5/6/2011	201209820	3/1/2012		

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01346-US-PAT	US	METHOD AND APPARATUS FOR CONCURRENTLY READING A PLURALITY OF MEMORY DEVICES USING A SINGLE BUFFER	PUBLISHED	13/102,310	5/6/2011	2011-0276775	11/10/2011		
01355-US-PAT	US	CONNECTION OF MULTIPLE SEMICONDUCTOR MEMORY DEVICES WITH CHIP ENABLE FUNCTION	PUBLISHED	13/588,195	8/17/2012	2013-0094271	4/18/2013		
01373-CA-NPE	CA	FLASH MEMORY MODULE AND MEMORY SUBSYSTEM	PUBLISHED	2,854,118	11/1/2012		5/10/2013		
01373-CN-NPE	CN	FLASH MEMORY MODULE AND MEMORY SUBSYSTEM	PUBLISHED	201280058805 1	11/1/2012	103959386	7/30/2014		
01373-EP-NPE	EP	FLASH MEMORY MODULE AND MEMORY SUBSYSTEM	PUBLISHED	12845812.2	11/1/2012	2774150	9/10/2014		
01373-JP-NPE	JP	FLASH MEMORY MODULE AND MEMORY SUBSYSTEM	PENDING	2014-539194	11/1/2012				
01373-KR-NPE	KR	FLASH MEMORY MODULE AND MEMORY SUBSYSTEM	PUBLISHED	10-2014-7014780	11/1/2012	10-2014-0097270	8/6/2014		
01373-TW-PAT	TW	FLASH MEMORY MODULE AND MEMORY SUBSYSTEM	PUBLISHED	101140318	10/31/2012	201342380	10/16/2013		
01373-US-PAT	US	FLASH MEMORY MODULE AND MEMORY SUBSYSTEM	PUBLISHED	13/665,181	10/31/2012	2013-0107443	5/2/2013		
01374-US-PAT	US	PACKAGE HAVING STACKED MEMORY DIES WITH SERIALLY CONNECTED BUFFER DIES	PUBLISHED	13/675,168	11/13/2012	2013-0119542	5/16/2013		
01356-TW-PAT	TW	POWER SAVING METHODS FOR USE IN A SYSTEM OF SERIALLY CONNECTED SEMICONDUCTOR DEVICES	PUBLISHED	101143273	11/20/2012	201337941	9/16/2013		
01356-US-PAT	US	POWER SAVING METHODS FOR USE IN A SYSTEM OF SERIALLY CONNECTED SEMICONDUCTOR DEVICES	PUBLISHED	13/425,801	3/21/2012	2013-0128678	5/23/2013		
01358-CN-NPE	CN	SOLID STATE MEMORY SYSTEM	PENDING	201280063911 8	12/20/2012				
01358-EP-NPE	EP	SOLID STATE MEMORY SYSTEM	PUBLISHED	12859118.7	12/20/2012	2795621	10/29/2014		
01358-JP-NPE	JP	SOLID STATE MEMORY SYSTEM	PENDING	2014-547653	12/20/2012				
01358-KR-NPE	KR	SOLID STATE MEMORY SYSTEM	PUBLISHED	10-2014-7020758	12/20/2012	2014-0110004	9/16/2014		

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01358-TW-PAT	TW	SOLID STATE MEMORY SYSTEM	PUBLISHED	101148761	12/20/2012	201344692	11/1/2013		
01358-US-PAT	US	SOLID STATE MEMORY SYSTEM	PUBLISHED	13/720,951	12/19/2012	2013-0163175	6/27/2013		
01359-CA-NPE	CA	INDEPENDENT WRITE AND READ CONTROL IN SERIALLY-CONNECTED DEVICES	PUBLISHED	2,856,590	12/6/2012		6/13/2013		
01359-CN-NPE	CN	INDEPENDENT WRITE AND READ CONTROL IN SERIALLY-CONNECTED DEVICES	PUBLISHED	201280060340.2	12/6/2012	103988262	8/13/2014		
01359-EP-NPE	EP	INDEPENDENT WRITE AND READ CONTROL IN SERIALLY-CONNECTED DEVICES	PUBLISHED	12855470.6	12/6/2012	2788985	10/15/2014		
01359-JP-NPE	JP	INDEPENDENT WRITE AND READ CONTROL IN SERIALLY-CONNECTED DEVICES	PENDING	2014-545053	12/6/2012				
01359-KR-NPE	KR	INDEPENDENT WRITE AND READ CONTROL IN SERIALLY-CONNECTED DEVICES	PUBLISHED	10-2014-7018893	12/6/2012	10-2014-0102735	8/22/2014		
01359-TW-PAT	TW	INDEPENDENT WRITE AND READ CONTROL IN SERIALLY-CONNECTED DEVICES	PUBLISHED	101145992	12/6/2012	201344700	11/1/2013		
01359-US-PAT	US	INDEPENDENT WRITE AND READ CONTROL IN SERIALLY-CONNECTED DEVICES	ISSUED	13/401,087	2/21/2012	2013-0151757	6/13/2013	8,825,967	9/2/2014
01376-TW-PAT	TW	METHOD AND APPARATUS FOR CONNECTING MEMORY DIES TO FORM A MEMORY SYSTEM	PUBLISHED	102102899	1/25/2013	201347051	11/16/2013		
01376-US-PAT	US	METHOD AND APPARATUS FOR CONNECTING MEMORY DIES TO FORM A MEMORY SYSTEM	PUBLISHED	13/750,046	1/25/2013	2013-0193582	8/1/2013		
01377-CN-NPE	CN	RING TOPOLOGY STATUS INDICATION	PENDING	TBD	5/28/2013				
01377-EP-NPE	EP	RING TOPOLOGY STATUS INDICATION	PENDING	13796309.6	5/28/2013				
01377-JP-NPE	JP	RING TOPOLOGY STATUS INDICATION	PENDING	TBD	5/28/2013				
01377-KR-NPE	KR	RING TOPOLOGY STATUS INDICATION	PENDING	10-2014-7036568	5/28/2013				
01377-TW-PAT	TW	RING TOPOLOGY STATUS INDICATION	PUBLISHED	102118802	5/28/2013	201411482	3/16/2014		
01377-US-PAT	US	RING TOPOLOGY STATUS INDICATION	PUBLISHED	13/903,418	5/28/2013	2013-0326090	12/5/2013		
01377-WO-PCT	WO	RING TOPOLOGY STATUS INDICATION	PUBLISHED	PCT/CA2013/000518	5/28/2013	2013/177673	12/5/2013		

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01380-CN-NPE	CN	FLASH MEMORY CONTROLLER HAVING DUAL MODE PIN-OUT	PROPOSED						
01380-JP-NPE	JP	FLASH MEMORY CONTROLLER HAVING DUAL MODE PIN-OUT	PROPOSED						
01380-KR-NPE	KR	FLASH MEMORY CONTROLLER HAVING DUAL MODE PIN-OUT	PENDING	10-2014-7036998	9/18/2013				
01380-TW-PAT	TW	FLASH MEMORY CONTROLLER HAVING DUAL MODE PIN-OUT	PUBLISHED	102133883	9/18/2013	201428748	7/16/2014		
01380-US-PAT	US	FLASH MEMORY CONTROLLER HAVING DUAL MODE PIN-OUT	PUBLISHED	13/835,968	3/15/2013	2014-0082260	3/20/2014		
01380-WO-PCT	WO	FLASH MEMORY CONTROLLER HAVING DUAL MODE PIN-OUT	PUBLISHED	PCT/CA2013/000782	9/18/2013	2014/043788	3/27/2014		
01384-JP-NPE	JP	FLASH MEMORY CONTROLLER HAVING MULTI MODE PIN-OUT	PENDING	TBD	10/31/2013				
01384-KR-NPE	KR	FLASH MEMORY CONTROLLER HAVING MULTI MODE PIN-OUT	PENDING	10-2014-7026795	10/31/2013				
01384-TW-PAT	TW	FLASH MEMORY CONTROLLER MULTI MODE PIN-OUT	PUBLISHED	102139555	10/31/2013	201432696	8/16/2014		
01384-US-PAT	US	FLASH MEMORY CONTROLLER MULTI MODE PIN-OUT	PUBLISHED	13/836,113	3/15/2013	2014-0122777	5/1/2014		
01385-TW-PAT	TW	METHOD AND APPARATUS FOR PLL LOCKING CONTROL IN DAISY CHAINED MEMORY SYSTEM	PUBLISHED	102139315	10/30/2013	201439769	10/16/2014		
01385-US-PAT	US	PLL LOCKING CONTROL IN DAISY CHAINED MEMORY SYSTEM	PUBLISHED	14/066,748	10/30/2013	2014-0132318	5/15/2014		
01385-WO-PCT	WO	METHOD AND APPARATUS FOR PLL LOCKING CONTROL IN DAISY CHAINED MEMORY SYSTEM	PUBLISHED	PCT/CA2013/000917	10/30/2013	2014/071497	5/15/2014		
01224-TW-PAT	TW	PACKET BASED ID GENERATION FOR SERIALLY INTERCONNECTED DEVICES	PUBLISHED	096134886	9/19/2007	200830768	7/16/2008		
01224-US-PAT	US	PACKET BASED ID GENERATION FOR SERIALLY INTERCONNECTED DEVICES	ISSUED	11/529,293	9/29/2006	2008-0080492	4/3/2008	8,700,818	4/15/2014
01224-US-CON	US	PACKET DATA ID GENERATION FOR SERIALLY INTERCONNECTED DEVICES	PUBLISHED	14/185,401	2/20/2014	2014-0173322	6/19/2014		

Reference #	Country ID	Title	Status	Serial #	Filed Date	Publication #	Publication Date	Patent #	Issue Date
01231-CA-NPE	CA	APPARATUS AND METHOD FOR CAPTURING SERIAL INPUT DATA	PUBLISHED	2,667,904	12/4/2007	2,667,904	6/12/2008		
01231-CN-NPE	CN	APPARATUS AND METHOD FOR CAPTURING SERIAL INPUT DATA	ISSUED	200780044726.3	12/4/2007	101546328	9/30/2009	ZL200780044726.3	4/23/2014
01231-CN-DIV	CN	APPARATUS AND METHOD FOR CAPTURING SERIAL INPUT DATA	PUBLISHED	201410105789 7	12/4/2007	103823783 A	5/28/2014		
01231-EP-NPE	EP	APPARATUS AND METHOD FOR CAPTURING SERIAL INPUT DATA	PUBLISHED	07855465.6	12/4/2007	2097902	9/9/2009		
01231-JP-DIV	JP	APPARATUS AND METHOD FOR CAPTURING SERIAL INPUT DATA	ISSUED	2010-252824	12/4/2007	2011-028786	2/10/2011	5382861	10/11/2013
01231-JP-DIV2	JP	APPARATUS AND METHOD FOR CAPTURING SERIAL INPUT DATA	ISSUED	2013-131759	12/4/2007	2013-229045		5613789	9/12/2014
01231-KR-NPE	KR	APPARATUS AND METHOD FOR CAPTURING SERIAL INPUT DATA	ISSUED	10-2009-7012104	12/4/2007	10-2009-0094275	9/4/2009	10-1468763	11/27/2014
01231-TW-PAT	TW	APPARATUS AND METHOD FOR CAPTURING SERIAL INPUT DATA	ALLOWED	096146527	12/6/2007	200834327	8/16/2008		
01231-US-PAT	US	APPARATUS AND METHOD FOR CAPTURING SERIAL INPUT DATA	ISSUED	11/567,551	12/6/2006	2008-0137467	6/12/2008	7,818,464	10/19/2010
01231-US-DIV	US	APPARATUS AND METHOD FOR CAPTURING SERIAL INPUT DATA	ISSUED	12/879,543	9/10/2010	2010-0332685	12/30/2010	8,904,046	12/2/2014
01232-CA-NPE	CA	ID GENERATION APPARATUS AND METHOD FOR SERIALLY INTERCONNECTED DEVICES	PUBLISHED	2,671,184	12/3/2007	2,671,184	6/26/2008		
01232-CN-NPE	CN	ID GENERATION APPARATUS AND METHOD FOR SERIALLY INTERCONNECTED DEVICES	PUBLISHED	200780051500.6	12/3/2007	101611454	12/23/2009		
01232-EP-NPE	EP	ID GENERATION APPARATUS AND METHOD FOR SERIALLY INTERCONNECTED DEVICES	PUBLISHED	07855449.0	12/3/2007	2122626	11/25/2009		

Reference #	Country ID	Title	Status	Serial #	Filed Date	Publication #	Publication Date	Patent #	Issue Date
01232-JP-NPE	JP	ID GENERATION APPARATUS AND METHOD FOR SERIALLY INTERCONNECTED DEVICES	ISSUED	2009-541702	12/3/2007	2010-514016	4/30/2010	5398540	11/1/2013
01232-JP-DIV	JP	ID GENERATION APPARATUS AND METHOD FOR SERIALLY INTERCONNECTED DEVICES	PUBLISHED	2013-183052	12/3/2007	2013-239210	11/28/2013		
01232-KR-NPE	KR	ID GENERATION APPARATUS AND METHOD FOR SERIALLY INTERCONNECTED DEVICES	ISSUED	10-2009-7015058	12/3/2007	10-2009-0102809	9/30/2009	10-1392555	4/29/2014
01232-KR-DIV	KR	ID GENERATION APPARATUS AND METHOD FOR SERIALLY INTERCONNECTED DEVICES	ISSUED	10-2013-7033701	12/3/2007	10-2014-0009586		10-1468839	11/27/2014
01232-TW-PAT	TW	ID GENERATION APPARATUS AND METHOD FOR SERIALLY INTERCONNECTED DEVICES	ALLOWED	096148760	12/19/2007	200834310	8/16/2008		
01232-US-PAT	US	ID GENERATION APPARATUS AND METHOD FOR SERIALLY INTERCONNECTED DEVICES	ALLOWED	11/613,563	12/20/2006	2008-0155219	6/26/2008		
01212-US-PAT	US	DATA FLOW CONTROL IN MULTIPLE INDEPENDENT PORT	ISSUED	12/034,686	2/21/2008	2008-0205187	8/28/2008	7,796,462	9/14/2010
01212-US-CON	US	DATA FLOW CONTROL IN MULTIPLE INDEPENDENT PORT	ISSUED	12/851,884	8/6/2010	2010-0306569	12/2/2010	8,159,893	4/17/2012
01212-US-CON2	US	DATA FLOW CONTROL IN MULTIPLE INDEPENDENT PORT	ISSUED	13/418,478	3/13/2012	2012-0170595	7/5/2012	8,493,808	7/23/2013
01213-BE-VAL	BE	PULSE COUNTER WITH CLOCK EDGE RECOVERY	ISSUED	07763856.7	7/6/2007			2050191	9/11/2013
01213-DE-VAL	DE	PULSE COUNTER WITH CLOCK EDGE RECOVERY	ISSUED	602007032810.1	7/6/2007			2050191	9/11/2013
01213-ES-VAL	ES	PULSE COUNTER WITH CLOCK EDGE RECOVERY	ISSUED	07763856.7	7/6/2007	2437586	1/13/2014	2050191	9/11/2013
01213-FI-VAL	FI	PULSE COUNTER WITH CLOCK EDGE RECOVERY	ISSUED	07763856.7	7/6/2007			2050191	9/11/2013

Reference #	Country ID	Title	Status	Serial #	Filed Date	Publication #	Publication Date	Patent #	Issue Date
01213-FR-VAL	FR	PULSE COUNTER WITH CLOCK EDGE RECOVERY	ISSUED	07763856.7	7/6/2007			2050191	9/11/2013
01213-GB-VAL	GB	PULSE COUNTER WITH CLOCK EDGE RECOVERY	ISSUED	07763856.7	7/6/2007			2050191	9/11/2013
01213-IE-VAL	IE	PULSE COUNTER WITH CLOCK EDGE RECOVERY	ISSUED	07763856.7	7/6/2007			2050191	9/11/2013
01213-IT-VAL	IT	PULSE COUNTER WITH CLOCK EDGE RECOVERY	ISSUED	07763856.7	7/6/2007			2050191	9/11/2013
01213-JP-NPE	JP	PULSE COUNTER WITH CLOCK EDGE RECOVERY	ISSUED	2009-522060	7/6/2007	2009-545262	12/17/2009	5355401	9/6/2013
01213-KR-NPE	KR	PULSE COUNTER WITH CLOCK EDGE RECOVERY	ISSUED	10-2009-7003298	7/6/2007	10-2009-0035592	4/9/2009	10-1374916	3/10/2014
01213-NL-VAL	NL	PULSE COUNTER WITH CLOCK EDGE RECOVERY	ISSUED	07763856.7	7/6/2007			2050191	9/11/2013
01213-SE-VAL	SE	PULSE COUNTER WITH CLOCK EDGE RECOVERY	ISSUED	07763856.7	7/6/2007			2050191	9/11/2013
01213-TW-PAT	TW	PULSE COUNTER WITH CLOCK EDGE RECOVERY	ISSUED	096125723	7/13/2007	200826496	6/16/2008	I442704	6/21/2014
01213-US-PAT	US	PULSE COUNTER WITH CLOCK EDGE RECOVERY	ISSUED	11/495,609	7/31/2006	2008-0025457	1/31/2008	7,742,551	6/22/2010
01269-TW-PAT	TW	METHODS AND SYSTEMS FOR FAILURE ISOLATION AND DATA RECOVERY IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ALLOWED	097139347	10/14/2008	200939013	9/16/2009		
01270-US-NPE	US	METHODS AND SYSTEMS FOR FAILURE ISOLATION AND DATA RECOVERY IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ISSUED	11/941,131	11/15/2007	2009-0129184	5/21/2009	7,836,340	11/16/2010
01270-US-DIV	US	METHODS AND SYSTEMS FOR FAILURE ISOLATION AND DATA RECOVERY IN A CONFIGURATION OF SERIES-CONNECTED SEMICONDUCTOR DEVICES	ISSUED	12/945,280	11/12/2010	2011-0060937	3/10/2011	8,443,233	5/14/2013
01401-TW-PAT	TW	METHOD AND APPARATUS FOR TESTING SURFACE MOUNTED DEVICES	PENDING	103132800	9/23/2014				

Reference #	Country ID	Title	Status	Serial #	Filed Date	Publication #	Publication Date	Patent #	Issue Date
01401-US-PRV	US	METHOD AND APPARATUS FOR TESTING SURFACE MOUNTED DEVICES	PENDING	61/883,364	9/27/2013				
01401-US-PAT	US	METHOD AND APPARATUS FOR TESTING SURFACE MOUNTED DEVICES	PENDING	14/478,824	9/5/2014				
01401-WO-PCT	WO	METHOD AND APPARATUS FOR TESTING SURFACE MOUNTED DEVICES	PENDING	PCT/CA2014/000709	9/26/2014				