## PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1 Stylesheet Version v1.2 EPAS ID: PAT3241918

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

### **CONVEYING PARTY DATA**

Name	Execution Date
WILLIAM MAINES	01/30/2015
DAVID MAINES	01/30/2015

#### **RECEIVING PARTY DATA**

Name:	ENDICOTT INTERCONNECT TECHNOLOGIES, INC.
Street Address:	1093 CLARK STREET
City:	ENDICOTT
State/Country:	NEW YORK
Postal Code:	13760

#### **PROPERTY NUMBERS Total: 195**

Property Type	Number
Application Number:	10322527
Application Number:	10370529
Application Number:	10379575
Application Number:	10394107
Application Number:	10394135
Application Number:	10409066
Application Number:	10423877
Application Number:	10423972
Application Number:	10616932
Application Number:	10630722
Application Number:	10643909
Application Number:	10661616
Application Number:	10679302
Application Number:	10737974
Application Number:	10740398
Application Number:	10740500
Application Number:	10790747
Application Number:	10811817
Application Number:	10811915

PATENT REEL: 035098 FRAME: 0968

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Property Type	Number
Application Number:	10812889
Application Number:	10812890
Application Number:	10860067
Application Number:	10860071
Application Number:	10882167
Application Number:	10882170
Application Number:	10900385
Application Number:	10900386
Application Number:	10915483
Application Number:	10920235
Application Number:	10933260
Application Number:	10953923
Application Number:	10955741
Application Number:	10968929
Application Number:	10991451
Application Number:	10991532
Application Number:	11031074
Application Number:	11031085
Application Number:	11086323
Application Number:	11086324
Application Number:	11110901
Application Number:	11110919
Application Number:	11110920
Application Number:	11127160
Application Number:	11128272
Application Number:	11152048
Application Number:	11172786
Application Number:	11172794
Application Number:	11177413
Application Number:	11177442
Application Number:	11215206
Application Number:	11216133
Application Number:	11238960
Application Number:	11242841
Application Number:	11244180
Application Number:	11258092
Application Number:	11259043
Application Number:	11265287

Property Type	Number
Application Number:	11281456
Application Number:	11305073
Application Number:	11324273
Application Number:	11324432
Application Number:	11327493
Application Number:	11334445
Application Number:	11349990
Application Number:	11349998
Application Number:	11350777
Application Number:	11352276
Application Number:	11352279
Application Number:	11390386
Application Number:	11396711
Application Number:	11397713
Application Number:	11401401
Application Number:	11429990
Application Number:	11438424
Application Number:	11454896
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Application Number:	11482945
Application Number:	11492029
Application Number:	11500328
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Application Number:	11607973
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Application Number:	11727314
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Application Number:	11730404
Application Number:	11730761
Application Number:	11730942
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Application Number:	11797232
Application Number:	11797236

Property Type	Number
Application Number:	11802434
Application Number:	11806685
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Application Number:	11882625
Application Number:	11889668
Application Number:	11896786
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Application Number:	11905188
Application Number:	11907004
Application Number:	11907006
Application Number:	11976468
Application Number:	11976629
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Application Number:	12010004
Application Number:	12010335
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Application Number:	12081042
Application Number:	12081051
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Application Number:	12380617
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Application Number:	12380637
Application Number:	12460975
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Application Number:	12720849
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Property Type	Number
Application Number:	12764994
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Application Number:	12837640
Application Number:	12854252
Application Number:	12884392
Application Number:	12884421
Application Number:	12884657
Application Number:	12904305
Application Number:	12909983
Application Number:	12910020
Application Number:	12938759
Application Number:	12939659
Application Number:	12972700
Application Number:	13009922
Application Number:	13022654
Application Number:	13041655
Application Number:	13042578
Application Number:	13082444
Application Number:	13082502
Application Number:	13082599
Application Number:	13090676
Application Number:	13184699
Application Number:	13184882
Application Number:	13189980
Application Number:	13197804
Application Number:	13198756
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Application Number:	13358716
Application Number:	13360935

Property Type	Number
Application Number:	13362135
Application Number:	13442957
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Application Number:	13447701
Application Number:	13448505
Application Number:	13448574
Application Number:	13448778
Application Number:	13456535
Application Number:	13466164
Application Number:	13466181
Application Number:	13476052
Application Number:	13483600
Application Number:	13517776
Application Number:	13523956
Application Number:	13535432
Application Number:	13540645
Application Number:	13594939
Application Number:	13600332
Application Number:	13610976
Application Number:	13622478
Application Number:	13626961
Application Number:	13682805
Application Number:	13723912
Application Number:	13776777

#### **CORRESPONDENCE DATA**

**Fax Number:** (607)723-6605

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 6072316830 Email: amanzer@hhk.com

Correspondent Name: MARK LEVY, HINMAN, HOWARD & KATTELL, LLP

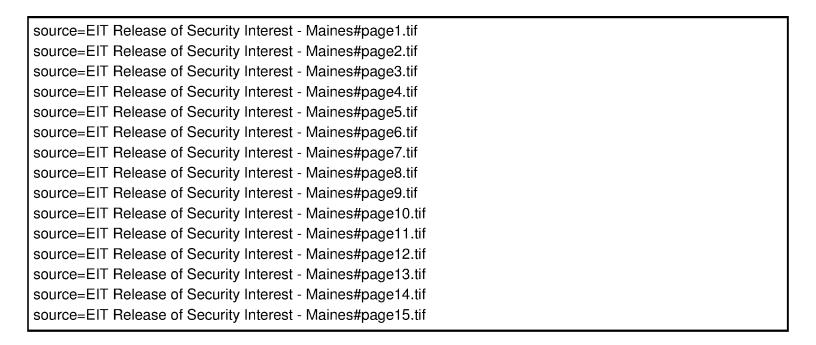
Address Line 1: 80 EXCHANGE STREET

Address Line 2: P.O. BOX 5250

Address Line 4: BINGHAMTON, NEW YORK 13901

NAME OF SUBMITTER:	MARK LEVY
SIGNATURE:	/Mark Levy/
DATE SIGNED:	02/26/2015

**Total Attachments: 15** 



# TERMINATION OF SECURITY INTEREST IN TRADEMARKS AND PATENTS

WHEREAS, Endicott Interconnect Technologies, Inc., a New York corporation with its principal place of business at 1093 Clark Street, Endicott, NY 13760 (the "Grantor"), is the owner of record of the trademarks and applications listed on the attached Exhibit A, now issued or pending in the United States Patent and Trademark Office (the "Trademarks"); and is the owner of record of the patents and patent applications listed on the attached Exhibit B, now issued or pending in the United States Patent and Trademark Office (the "Patents"); and

WHEREAS, the Grantor entered into that certain Security Agreements dated as of June 12, 2013 (the "Security Agreement"), between the Grantor and William Maines and David Maines, ("Secured Party"), true and correct copies of which were recorded by the United States Patent and Trademark Office on June 12, 2013, at Reel 5045, Frame 0951 and Reel 30599, Frame 0918;

WHEREAS, the Secured Party desires to release its security interest in the Trademarks and Patents and terminate the Security Agreement;

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, Secured Party hereby:

- 1. releases and reassigns to the Grantor any and all liens, security interests, right, title and interest of Secured Party pursuant to the Security Agreement in the trademarks and applications more fully described on Exhibit A, without recourse or representation or warranty, express or implied; and
- 2. releases and reassigns to the Grantor any and all liens, security interests, right, title and interest of Secured Party pursuant to the Security Agreement in the patents and applications more fully described on Exhibit B, without recourse or representation or warranty, express or implied; and
- 3. authorizes and requests the Commissioner of Patents and Trademarks of the United States of America to note and record the existence of the release hereby given.

IN WITNESS WHEREOF, Secured Party has caused this Termination of Security Interest in Trademarks and Patents to be signed by its duly authorized representative as of this 20 th day of January, 2015.

Secured Parties:  William Maines
STATE OF NEW YORK )
) ss: COUNTY OF BROOME )
On this 30 day of January, 2015, before me personally came William Maines, to me personally known, and known to me to be the person described in and who executed the foregoing affidavit, and she acknowledged to me that she executed the same as his free act and deed.  **The day of January, 2015, before me personally came William Maines, to me personally known, and who executed the foregoing affidavit, and she acknowledged to me that she executed the same as his free act and deed.  **The day of January, 2015, before me personally came William Maines, to me personally known, and who executed the foregoing affidavit, and she acknowledged to me that she executed the same as his free act and deed.  **The day of January, 2015, before me personally came William Maines, to me personally cam
Karen H. Chier Notary Public, State of New York Qualified in Broome County Commission Expires June 12 20 B #01 Chep43070
STATE OF NEW YORK ) ) ss: COUNTY OF BROOME )
On this day of January, 2015, before me personally came David Maines, to me personally known, and known to me to be the person described in and who executed the foregoing affidavit, and she acknowledged to me that she executed the same as his

Page 2 of 2

free act and deed.

Karen H. Chler
Notary Public, State of New York
Qualified in Brooms County
Commission Expires June 12, 20

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Karen B. Chur Notary

HYPERBGA	HYPERBGA	HYPERBGA	HYPERBGA	HYPERBGA	HYPERBGA	HYPERBGA	HYPERBGA	Endicott Interconnect Technologies	ENDICOTT INTERCONNECT and 3D Design	ENDICOTT INTERCONNECT and 3D Design	ENDICOTT INTERCONNECT 3D Design Only	ENDICOTT INTERCONNECT 3D Design Only	Endicott Interconnect	DRICLAD	DRICLAD	DRICLAD	DRICLAD	DRICLAD	DRICLAD	DRICLAD	DRICLAD	DRICLAD	CoreEZ	COREEZ	Trademark/Service Mark
Europe	Taiwan	Switzerland	Singapore	Canada	Canada	Australia	US	SN	UK	SN	Ę	SN	US	Taiwan	Taiwan	Mexico	Korea	Japan	France	China	Brazil	US	SU	SU	Country
5/9/2000					8/10/2004	2/24/2000	11/9/1999	12/16/2002	8/13/2012	6/20/2012	8/13/2012	6/20/2012	12/16/2002			1/30/1998	9/10/1998	11/14/1997	5/9/2000		1/22/1998	7/31/1997	3/24/2006	3/24/2006	Filing Date
1645605			TOO/10304A	1044049	1226508	824959	75/844,816	76/476,537	2631295	85/656,712	2631552	85/656,675	76/476,536				1998-0023497	H09-177086		9800105902	820508039	75/333,605	76/657,205	76/657,204	Application No.
1645605	950034	477543	T00/10304A		TMA642449	824959	2,632,339	2,829,453					2,831,497	896915	108344	572578	456079	4245007	721563	1435500	820508039	2,594,509	3,564,994	3,619,679	Registration No.
7/23/2001			6/14/2000		6/20/2005	2/16/2001	10/8/2002	4/6/2004					4/13/2004				9/29/1999	2/26/1999	7/23/2001	8/21/2000	1/27/2009	7/16/2002	1/20/2009	5/12/2009	Registration Date
Registered; Renewal Due 5/9/2020	Registered; Renewal Due 7/5/2021	Registered; Renewal Due 5/5/2020	Registered; Renewal Due 6/14/2020	Registered; Renewal Due 6/19/2020	Registered; Renewal Due 12/20/2019	Registered; Renewal Due 2/24/2020	Registered; Renewal Due 10/8/2022	Registered; Renewal Due 4/6/2014	Pending	Pending	Pending	Pending	Registered	Registered; Renewal Due 3/31/2019	Registered; Renewal Due 7/15/2020	Registered; Renewal Due 1/30/2018	Registered; Renewal Due 10/6/2019	Registered; Renewal Due 8/26/2018	Registered; Renewal Due 12/30/2017	Registered; Renewal Due 8/20/2020	Registered; Renewal Due 1/27/2019	Registered; Renewal Due 7/16/2022	Registered; Declaration of Use Due 1/20/2015	Registered; Declaration of Use Due 5/12/2015	

6/12/2013 PATENT REEL: 035098 FRAME: 0977

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Panding				94108442	3/18/2005	DIELECTRIC COMPOSITION FOR FORMING DIELECTRIC LAYER FOR USE IN CIRCUITIZED	Taiwan	TW-2-04-005
Pending				5251747.1		DIELECTRIC COMPOSITION FOR FORMING DIELECTRIC LAYER FOR USE IN CIRCUITIZED SUBSTRATES	Europe	EP-2-04-005
.5 Issued	7,270,845	9/18/2007	2008-0008727	10/812,889	3/31/2004	DIELECTRIC COMPOSITION FOR FORMING DIELECTRIC LAYER FOR USE IN CIRCUITIZED SUBSTRATES	SU	2-04-005
6 Issued	7,508,076	3/24/2009	2006-0125103	11/350,777	2/10/2006	INFORMATION HANDLING SYSTEM UTILIZING A CRCUITIZED SUBSTRATE HAVING A DIELECTRIC LAYER WITHOUT CONTINUOUS FIBERS	US	2-04-003D2
	7,416,996	8/26/2008	2006-0131755	11/349,990	2/9/2006	METHOD OF MAKING CIRCUITIZED SUBSTRATE	US	2-04-003D1
				5251748.9		CIRCUITIZED SUBSTRATE	Europe	EP-2-04-003
6 Issued	7,078,816	7/18/2006	2005-0224985	10/812,890	3/31/2004	CIRCUITIZED SUBSTRATE	US	2-04-002
		8/8/2006	2004-082604	10/423,972	4/28/2003	STRENGTHENED CONDUCTIVE PAD	SU	2-03-005-CIP
Issued	1284967	8/1/2007		93103172	2/11/2004	ELECTRONIC PACKAGE WITH STRENGTHENED	Taiwan	TW-2-03-004-CIP
Pending				4250754.1		ELECTRONIC PACKAGE WITH STRENGTHENED CONDUCTIVE PAD	Europe	EP-2-03-004-CIP
.7 Issued	6,815,837	11/9/2004	2004-0183212	10/423,877	4/28/2003	ELECTRONIC PACKAGE WITH STRENGTHENED CONDUCTIVE PAD	SN	2-03-004-CIP
Pending				93114136		ELECTRONIC CARD	Taiwan	TW-2-03-006
2 Issued	7,109,732	9/19/2006	2005-0022376	10/630,722	7/31/2003	ELECTRONIC COMPONENT TEST APPARATUS	SU	2-03-008
2 Issued	7,332,212	2/19/2008	2006-0029781	11/242,841	10/5/2005	CIRCUITIZED SUBSTRATE WITH CONDUCTIVE POLYMER AND SEED MATERIALS ADHESION LAYER	SN	2-03-009D
2 Issued	7,063,762	6/20/2006	2005-0039840	10/643,909	8/20/2003	CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAME	SN	2-03-009
6 Issued	7,091,066	8/15/2006	2006-0046462	11/259,043	10/27/2005	METHOD OF MAKING CIRCUITIZED SUBSTRATE	SU	2-03-011D2
7 Issued	7,163,847	1/16/2007	2006-0040426	11/258,092	10/26/2005	METHOD OF MAKING CIRCUITIZED SUBSTRATE	SU	2-03-011D1
4 Issued	7,084,014	8/1/2006	2005-0074924	10/679,302	10/7/2003	METHOD OF MAKING CIRCUITIZED SUBSTRATE	SU	2-03-011
6 Issued	6,958,106	10/25/2005	2004-0201136	10/409,066	4/9/2003	MATERIAL SEPARATION TO FORM SEGMENTED PRODUCT	SN	2-03-003
3 Issued	7,013,563	3/21/2006	2005-0005438	10/616,932	7/11/2003	METHOD OF TESTING SPACINGS IN PATTERN OF OPENINGS IN PCB CONDUCTIVE LAYER	US	2-03-007
9 Issued	7,152,319	12/26/2006	2004-0231888	10/811,817	3/30/2004	METHOD OF MAKING HIGH SPEED CIRCUIT BOARD	SU	2-03-001D
7 Issued	7,023,707	4/4/2006	2004-0150101	10/394,135	3/24/2003	INFORMATION HANDLING SYSTEM	SN	2-03-001-CIP2
3 Issued	7,035,113	4/25/2006	2004-0150114	10/394,107	3/24/2003	MULTI-CHIP ELECTRONIC PACKAGE HAVING LAMINATE CARRIER AND METHOD OF MAKING SAME	SU	2-03-001-CIP1
Issued				93101219		HIGH SPEED CIRCUIT BOARD AND METHOD FOR FABRICATION	Taiwan	TW-2-03-001
9 Issued	2,454,289	5/13/2008		2454289	12/29/2003	HIGH SPEED CIRCUIT BOARD AND METHOD FOR FABRICATION	Canada	CA-2-03-001
Issued	7,343,674	3/18/2008	2006-0123626	11/349,998	2/9/2006	METHOD OF MAKING CIRCUITIZED SUBSTRATE ASSEMBLY	SU	2-02-001D3
3 Issued	7,071,423	7/4/2006	2005-0011670	10/915,483	8/11/2004	CIRCUITIZED SUBSTRATE ASSEMBLY AND METHOD OF MAKING SAME	Sn	2-02-001D2
ssued	7,047,630	5/23/2006	2004-0177998	10/811,915	3/30/2004	METHOD OF MAKING CIRCUITIZED SUBSTRATE ASSEMBLY	SN	2-02-001D
Issued	6,900,392	5/31/2005	2005-0023035	10/933,260	9/3/2004	INFORMATION HANDLING SYSTEM UTILIZING CIRCUITIZED SUBSTRATE	SN	2-02-001-CIPD
Issued	6,872,894	3/29/2005	2004-0118598	10/379,575	3/6/2003	INFORMATION HANDLING SYSTEM UTILIZING CIRCUITIZED SUBSTRATE	Sn	2-02-001-CIP
12 Issued	ZL20031012 3253			200310123253.X	12/19/2003	CIRCUITIZED SUBSTRATE ASSEMBLY AND METHOD OF MAKING SAME	China	CN-2-02-001
3 Issued	2,452,178	5/13/2008		2452178	12/5/2003	CIRCUITIZED SUBSTRATE ASSEMBLY AND METHOD OF MAKING SAME	Canada	CA-2-02-001
Issued	6,809,269	10/26/2004	2004-0118596	10/322,527	12/19/2002	CIRCUITIZED SUBSTRATE ASSEMBLY AND METHOD OF MAKING SAME	SU	2-02-001
Issued	2,452,178			2452178		CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAME	Canada	CA-2-03-002
Issued				10707-0701-0	27277	Т	0.000	1

CN-2-04-007	2-04-007	2-04-004	2-03-012	CN-2-07-012	2-07-012	CN-2-07-014	2-07-014	CN-2-07-011	2-07-011	2-04-014	2-04-011D	TW-2-04-011	2-04-011	2-03-001-CIP3CD	2-03-001-CIP3C	TW-2-03-001-CIP3	2-03-001-CIP3	2-04-005D
China	US	S	SU	China	US	China	US	China	US	S	S		US	SU	US	Taiwan	US	US
LOW MOISTURE ABSORPTIVE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	LOW MOISTURE ABSORPTIVE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	LOW MOISTURE ABSORPTIVE CIRCUITIZED SUBSTRATE, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	ITEM IDENTIFICATION CONTROL METHOD	CIRCUITIZED SUBSTRATE WITH INTERNAL COOLING STRUCTURE AND ELECTRICAL ASSEMBLY UTILIZING SAME	CIRCUITIZED SUBSTRATE WITH INTERNAL COOLING STRUCTURE AND ELECTRICAL ASSEMBLY UTILIZING SAME	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH INTERNAL OPTICAL PATHWAY USING PHOTOLITHOGRAPHY	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH INTERNAL OPTICAL PATHWAY USING PHOTOLITHOGRAPHY	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH INTERNAL OPTICAL PATHWAY	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH INTERNAL OPTICAL PATHWAY	ELECTRICAL ASSEMBLY WITH INTERNAL MEMORY CIRCUITIZED SUBSTRATE HAVING ELECTRONIC COMPONENTS POSITIONED THEREON, METHOD OF MAKING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH INTERNAL ORGANIC MEMORY DEVICE	CIRCUITIZED SUBSTRATE WITH INTERNAL ORGANIC MEMORY DEVICE, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME AND INFORMATION HANDLING SYSTEM UTILIZING SAME	CIRCUITIZED SUBSTRATE WITH INTERNAL ORGANIC MEMORY DEVICE, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILITIZING SAME	METHOD OF MAKING A MULTI-CHIP ELECTRONIC PACKAGE HAVING LAMINATE CARRIER	STACKED CHIP ELECTRONIC PACKAGE HAVING LAMINATE CARRIER AND METHOD OF MAKING SAME	STACKED CHIP ELECTRONIC PACKAGE HAVING LAMINATE CARRIER AND METHOD OF MAKING SAME	STACKED CHIP ELECTRONIC PACKAGE HAVING LAMINATE CARRIER AND METHOD OF MAKING SAME	LAYER HAVING DIELECTRIC LAYER HAVING DIELECTRIC COMPOSITION NOT INCLUDING CONTINUOUS OR SEMI-CONTINUOUS FIBERS
	3/23/2005	8/18/2004	12/22/2003	10/22/2008	10/25/2007	10/6/2008	10/19/2007		10/9/2007	7/28/2004	6/12/2007		7/28/2004	6/19/2006	9/30/2005		9/15/2003	9/6/2007
200610057200.6	11/086,323	10/920,235	10/740,500	200810171145.2	11/976,468	200810168238.X	11/907,004	200810168239.4	11/907,006	10/900,386	11/808,596	94124018	10/900,385	11/455,183	11/238,960	93101178	10/661,616	11/896,786
	2005-0218524	2005-0224251	2005-0137890		2009-0109624		2009-0093073		2009-0092353	2006-0022310	2007-0249089		2006-0022303	2006-0240594	2006-0023439		2004-0150095	2008-0003407
	12/30/2008	12/5/2006	9/21/2010		6/15/2010		5/11/2010		6/2/2009	5/16/2006	2/5/2008		8/7/2007	2/23/2010	1/9/2007		1/31/2006	
	7,470,990	7,145,221	7,801,833		7,738,249		7,713,767		7,541,058	7,045,897	7,326,643		7,253,502	7,665,207	7,161,810		6,992,896	F dieni, MO
Pending	issued	Issued	Issued	Pending	Issued	Pending	Issued	Pending	issued	Issued	issued	Pending	Issued	Issued	Issued	Issued	Issued	Allowed

2-04-013	2-04-009D1	2-04-009	2-04-002D	2-04-002	2-03-014D	TW-2-03-014	JP-2-03-014	2-03-014	2-03-013D	TW-2-03-013	JP-2-03-013	EP-2-03-013	2-03-013	2-05-022	2-05-020	2-07-016	2-04-007D	TW-2-04-007	IN-2-04-007	EP-2-04-007
US	S	S	SU	US	US	Taiwan	Japan	SU	SU	Taiwan	Japan	Europe	SN	US	US	SU	SU	Taiwan	India	Europe
CIRCUITIZED SUBSTRATE WITH SPLIT CONDUCTIVE LAYER, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH FILLED ISOLATION BORDER	CIRCUITZED SUBSTRATE WITH FILLED ISOLATION BORDER, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH SIGNAL WIRE SHIELDING	CIRCUITIZED SUBSTRATE WITH SIGNAL WIRE SHIELDING, ELECTRICAL ASSEMBLY UTILIZING SAME AND METHOD OF MAKING.	METHOD OF PROVIDING PRINTED CIRCUIT BOARD WITH CONDUCTIVE HOLES AND BOARD RESULTING THEREFROM	METHOD OF PROVIDING PRINTED CIRCUIT BOARD WITH CONDUCTIVE HOLES AND BOARD RESULTING THEREFROM	METHOD OF PROVIDING PRINTED CIRCUIT BOARD WITH CONDUCTIVE HOLES AND BOARD RESULTING THEREFROM	METHOD OF MAKING MULTILAYERED PRINTED CIRCUIT BOARD WITH FILLED CONDUCTIVE HOLES	METHOD OF MAKING A PRINTED CIRCUIT BOARD WITH LOW CROSS-TALK NOISE	PRINTED CIRCUIT BOARD WITH LOW CROSS- TALK NOISE	METHOD OF MAKING PRINTED CIRCUIT BOARD WITH VARVING DEPTH CONDUCTIVE HOLES ADAPTED FOR RECEIVING PINNED ELECTRICAL COMPONENTS	CIRCUITIZED SUBSTRATE WITH SHIELDED SIGNAL LINES AND PLATED-THRU-HOLES AND METHOD OF MAKING SAME, AND ELECTRICAL ASSEMBLY AND INFORMATION HANDLING SYSTEM UTILIZING SAME	METHOD OF MAKING CIRCUITIZED SUBSTRATES HAVING FILM RESISTORS AS PART THEREOF	METHOD OF MAKING SAME LOW MOISTURE ABSORPTIVE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION	LOW MOISTURE ABSORPTIVE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	LOW MOISTURE ABSORPTIVE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	LOW MOISTURE ABSORPTIVE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME SAME			
7/2/2004	7/10/2006	7/2/2004	5/9/2006	3/3/2004	4/5/2006	12/3/2004		12/18/2003	12/6/2006				12/22/2003	1/19/2006	4/11/2006	1/16/2008	4/5/2007			THE
10/882,167	11/482,945	10/882,170	11/429,990	10/790,747	11/397,713	93137509	2004-355230	10/737,974	11/634,287	93138054	2004-349471	4257721.3	10/740,398	11/334,445	11/401,401	12/007,820	11/730,942	95108059	355/DEL/2006	6251492.2
2006-0000636	2006-0248717	2006-0000639	2006-0200977	2005-0195585	2006-0183316			2005-0136646	2007-0089290				2005-0133257	2006-0121722	2006-0214010	2009-0178271	2007-0182016			
1/2/2007	10/19/2010	1/2/2007	12/9/2008	4/24/2007	3/25/2008	1/1/2012		5/1/2007	5/12/2009				2/13/2007		3/16/2010	8/14/2012	8/26/2008			
7,157,646	7,814,649	7,157,647	7,478,472	7,209,368	7,348,677	1355871		7,211,289	7,530,167				7,176,383		7,679,005	8,240,027	7,416,972			
Issued	issued	issued	Issued	Issued	Issued	Pending	Pending	Issued	ssued	Pending	Pending	Pending	issued	Pending	ssued	Issued	ssued	Pending	Pending	Pending

2-05-001D	2-05-001	2-05-025	TW-2-04-008	IN-2-04-008	2-04-008	2-04-015	2-04-010	2-04-006	2-04-018D	2-04-018	2-04-016D2	2-04-016D	IN-2-04-016	CN-2-04-016	2-04-016	2-04-013DD	2-04-013D	TW-2-04-013	Docket No
SU	SU	US	Taiwan	india	S	S	SU	SU	S	S	SU	SN	India	China	SN	SN	S	Taiwan	India
METHOD OF MAKING AN INTERPOSER	INTERPOSER FOR USE WITH TEST APPARATUS	SUBSTRATE TEST APPARATUS AND METHOD OF TESTING SUBSTRATES	HIGH SPEED CIRCUITIZED SUBSTRATE WIREDUCED THRU-HOLE STUB, METHOD FOR FABRICATION AND INFORMATION HANDLING SYSTEM UTILIZING SAME	HIGH SPEED CIRCUITIZED SUBSTRATE WIREDUCED THAU-HOLE STUB. METHOD FOR FABRICATION AND INFORMATION HANDLING SYSTEM UTILIZING SAME	HIGH SPEED CIRCUITIZED SUBSTRATE WITH REDUCED THRU-HOLE STUB, METHOD FOR FABRICATION AND INFORMATION HANDLING SYSTEM UTILIZING SAME	METHOD OF MAKING A CIRCUITIZED SUBSTRATE HAVING A PLURALITY OF SOLDER CONNECTION SITES THEREON	RADIO FREQUENCY DEVICE FOR TRACKING GOODS	METHOD AND SYSTEM FOR TRACKING GOODS	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH IMPROVED IMPEDANCE CONTROL CIRCUITRY, ELECTRICAL ASSEMBLY AND INFORMATION HANDLING SYSTEM	CIRCUITIZED SUBSTRATE WITH IMPROVED IMPEDANCE CONTROL CIRCUITRY, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY AND INFORMATION HANDLING SYSTEM UTILIZING SAME	CIRCUITIZED SUBSTRATES UTILIZING SMOOTH SIDED CONDUCTIVE LAYERS AS PART THEREOF	CIRCUITIZED SUBSTRATES UTILIZING SMOOTH- SIDED CONDUCTIVE LAYERS AS PART THEREOF	CIRCUITIZED SUBSTRATES UTILIZING SMOOTH- SIDED CONDUCTIVE LAYERS AS PART THEREOF, METHOD OF MAKINIG SAME, AND ELECTRICAL ASSEMBLIES AND INFORMATION HANDLING SYSTEMS UTILIZING SAME	CIRCUITIZED SUBSTRATES UTILIZING SMOOTH- SIDED CONDUCTIVE LAYERS AS PART THEREOF, METHOD OF MAKING SAME, AND ELECTRICAL ASSEMBLIES AND INFORMATION HANDLING SYSTEMS UTILIZING SAME	METHOD OF MAKING CIRCUITIZED SUBSTRATES UTILIZING SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF	INFORMATION HANDLING SYSTEM UTILIZING CIRCUITIZED SUBSTRATE WITH SPLIT CONDUCTIVE LAYER	METHOD OF MAKING CIRCUTIZED SUBSTRATE WITH SPLIT CONDUCTIVE LAYER AND INFORMATION HANDLING SYSTEM UTILIZING SAME	CIRCUITIZED SUBSTRATE WITH SPLIT CONDUCTIVE LAYER, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	CIRCUITIZED SUBSTRATE WITH SPLIT CONDUCTIVE LAYER, METHOD OF MAKING SAME, ELECTRICAL ASSENBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME
9/27/2007	4/21/2005	11/18/2005	***************************************		9/30/2004	10/21/2004	6/4/2004	6/4/2004	8/15/2007	9/29/2004	8/11/2010	4/17/2008			11/19/2004	1/18/2008	12/20/2006	6/20/2005	Ting Date
11/902,976	11/110,901	11/281,456	94132230	1828/DEL/2005	10/955,741	10/968,929	10/860,071	10/860,067	11/889,668	10/953,923	12/854,252	12/148,271	2488/DEL/20058	200510115609.4	10/991,532	12/010,004	11/641,810	94120469	1330/DEU/2005
2008-0020566	2006-0238207				2005-0039950	2006-0099727	2005-0270160	2005-0289019	2007-0284140	2006-0065433	2010-0328868	2008-0259581			2006-0110898	2008-0117583	2007-0144772		FUJIDANOI NO. ISSUEU.
3/31/2009	11/6/2007	10/31/2006			2/7/2006	8/8/2006	11/28/2006	6/23/2009	9/15/2009	11/13/2007	8/14/2012	11/23/2010			6/10/2008	2/17/2009	5/27/2008	10/1/2012	
7,511,518	7,292,055	7,129,732			6,995,322	7,087,441	7,142,121	7,552,091	7,589,283	7,294,791	8,242,376	7,838,776			7,383,629	7,491,896	7,377,033	1373992	raight wy.
Issued	Issued	Issued	Pending	Pending	issued	Issued	Issued	Issued	Issued	Issued	Issued	Issued	Pending	Pending	Issued	Issued	Issued	Issued	Pending

	2489/DEL/2005		AND ELECTRICAL ASSEMBLES AND INFORMATION HANDLING SYSTEMS UTILIZING SAME	India	IN-2-04-019
			CIRCUITIZED SUBSTRATES UTILIZING THREE SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF, METHOD OF MAKING SAME.		
	200510115610.7		CIRCUITIZED SUBSTRATES UTILIZING THREE SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF, METHOD OF MAKING SAME, AND ELECTRICAL ASSEMBLIES AND INFORMATION HANDLING SYSTEMS UTILIZING SAME SAME SAME SAME SAME SAME SAME SAME	China	CN-2-04-019
	10/991,451	11/19/2004	CIRCUITIZED SUBSTRATES UTILIZING THREE SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF, METHOD OF MAKING SAME. AND ELECTRICAL ASSEMBLIES AND INFORMATION HANDLING SYSTEMS UTILIZING SAME	US	2-04-019
2008-0105457	12/007,178	1/8/2008	CIRCUITIZED SUBSTRATE WITH SINTERED PASTE CONNECTIONS AND MULTILAYERED SUBSTRATE ASSEMBLY HAVING SAID SUBSTRATE AS PART THEREOF	sn	2-05-013D
2007-0006452	11/177,413	7/11/2005	METHOD OF MAKING MULTILAYERED CIRCUITIZED SUBSTRATE ASSEMBLY HAVING SINTERED PASTE CONNECTIONS	S	2-05-013
2008-0022520	11/905,188	9/28/2007	METHOD OF MAKING MULTILAYERED CIRCUITIZED SUBSTRATE ASSEMBLY	SU	2-05-012D
2007-0007032	11/177,442	7/11/2005	CIRCUITIZED SUBSTRATE WITH SINTERED PASTE CONNECTIONS, MULTILAYERED SUBSTRATE ASSEMBLY, ELECTRICAL ASSEMBLY AND INFORMATION HANDLING SYSTEM UTILIZING SAME	SN	2-05-012
2008-0054476	11/976,629	10/26/2007	CIRCUITIZED SUBSTRATE WITH INCREASED ROUGHNESS CONDUCTIVE LAYER AS PART THEREOF	US	2-05-016D
2006-0121738	11/327,493	1/9/2006	METHOD OF TREATING CONDUCTIVE LAYER FOR USE IN A CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAID SUBSTRATE HAVING SAID CONDUCTIVE LAYER AS PART THEREOF	SN	2-05-016
2006-0255009	11/128,272	5/13/2005	PLATING METHOD FOR CIRCUITIZED SUBSTRATES	SU	2-05-006
	3154/DEL/2005		CAPACITOR MATERIAL FOR USE IN CIRCUITIZED SUBSTRATES, CIRCUITIZED SUBSTRATE UTILIZING SAME, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND INFORMATION HANDLING SYSTEM UTILIZING SAID CIRCUITIZED SUBSTRATES	India	IN-2-04-017
	200510097424.5	12/28/2005 2	CIRCUITIZED SUBSTRATES, CAPACITOR MATERIAL THEREFOR, THEIR PREPARATION METHOD, AND INFORMATION HANDLING SYSTEM COMPRISING SAME	China	CN-2-04-017
2006-0151863	11/031,085	1/10/2005	CAPACITOR MATERIAL FOR USE IN CIRCUITIZED SUBSTRATES, CIRCUITIZED SUBSTRATES, CIRCUITIZED SUBSTRATE, AUD OF MAKING SAME CIRCUITIZED SUBSTRATE, AND INFORMATION HANDLING SYSTEM UTILIZING SAID CIRCUITIZED SUBSTRATE	S	2-04-017
2008-0102562	12/003,299	12/21/2007	METHOD OF MAKING MULTI-CHIP ELECTRONIC PACKAGE WITH REDUCED LINE SKEW	SU	2-05-010D
2006-0255460	11/127,160	5/12/2005	MULTI-CHIP ELECTRONIC PACKAGE WITH REDUCED LINE SKEW AND CIRCUITIZED SUBSTRATE FOR USE THEREIN	Sn	2-05-010
2007-0254408	11/822,573	7/9/2007	METHOD OF MAKING WIREBOND ELECTRONIC PACKAGE WITH ENHANCED CHIP PAD DESIGN	SU	2-05-014D
2006-0284304	11/152,048	6/15/2005	WIREBOND ELECTRONIC PACKAGE WITH ENHANCED CHIP PAD DESIGN, METHOD DO MAKING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	S	2-05-014
Publication No. Issued	Appl. No.	Filing Date	Title	Country	Docket No.

JP-2-05-023	2-08-009	2-06-004D	2-06-004	2-05-028	2-06-001	2-05-015	2-05-018	2-05-009D2	2-05-009D	2-05-009	2-05-008	2-04-020D	2-04-020	TW-2-05-017	CN-2-05-017	2-05-017	2-05-005D	2-05-005	2-05-003D	2-05-003	2-04-019D	Docket No.
Japan	SU	US	SU	SU	US	SU	SU	US	US	US	S	S	S	Taiwan	China	SU	S	US ·	SN	SU	US	Country
SUBSTRATE HAVING A PLURALITY OF SOLDER CONNECTION SITES THEREON	PHOTOSENSITIVE DIELECTRIC FILM	CAPACITIVE SUBSTRATE AND METHOD OF MAKING SAME	CAPACITIVE SUBSTRATE	METHOD OF FORMING FIBROUS LAMINATE CHIP CARRIER STRUCTURES	ADJUSTABLE THICKNESS THERMAL INTERPOSER AND ELECTRONIC PACKAGE UTILIZING SAME	METHOD AND APPARATUS FOR DEPOSITING CONDUCTIVE PASTE IN CIRCUITIZED SUBSTRATE OPENINGS	METHOD OF IMPROVING ELECTRICAL CONNECTIONS IN CIRCUITIZED SUBSTRATES	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH RESISTOR INCLUDING MATERIAL WITH METAL COMPONENT AND ELECTRICAL ASSEMBLY AND INFORMATION HANDLING SYSTEM UTILIZING SAID CIRCUITIZED SUBSTRATE	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH A RESISTOR	RESISTOR MATERAL WITH METAL COMPONENT FOR USE IN CIRCUITIZED SUBSTRATES, CIRCUITIZED SUBSTRATE UTILIZING SAME, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND INFORMATION HANDLING SYSTEM UTILIZING SAID CIRCUITIZED SUBSTRATE	METHOD OF MAKING AN INTERNAL CAPACITIVE SUBSTRATE FOR USE IN A CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE	CAPACITOR MATERIAL WITH METAL COMPONENT FOR USE IN CIRCUITIZED SUBSTRATES, CIRCUITIZED SUBSTRATE, CIRCUITIZED SUBSTRATE UTILIZING SAME, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND INFORMATION HANDLING SYSTEM UTILIZING SAID CIRCUITIZED SUBSTRATE	CAPACITOR MATERIAL WITH METAL COMPONENT FOR USE IN CIRCUITIZED SUBSTRATES, CIRCUITIZED SUBSTRATE, CIRCUITIZED SUBSTRATE, UTILIZING SAME, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND INFORMATION HANDLING SYSTEM UTILIZING SAID CIRCUITIZED SUBSTRATE	METHOD OF MAKING CIRCUITIZED SUBSTRATE	METHOD OF MAKING CIRCUITIZED SUBSTRATE	METHOD OF MAKING CIRCUITIZED SUBSTRATE	METHOD FOR MAKING CIRCUITIZED SUBSTRAITES HAVING PHOTO-IMAGEABLE DIELECTRIC LAYERS IN A CONTINUOUS MANNER	APPARATUS FOR MAKING CIRCUITIZED SUBSTRATES HAVING PHOTO-IMAGEABLE DIELECTRIC LAYERS IN A CONTINUOUS MANNER	APPARATUS FOR MAKING CIRCUITIZED SUBSTRATES IN A CONTINUOUS MANNER	APPARATUS AND METHOD FOR MAKING CIRCUITIZED SUBSTRATES IN A CONTINUOUS MANNER	CIRCUITIZED SUBSTRATES UTILIZING THREE SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF AND ELECTRICAL ASSEMBLIES AND INFORMATION HANDLING SYSTEMS UTILIZING SAME	Title
	7/27/2009	3/2/2009	5/23/2006	7/16/2010	4/4/2006	9/1/2005	12/19/2005	11/3/2010	5/2/2007	7/5/2005	7/5/2005	1/4/2006	1/10/2005	12/21/2006	12/21/2006	1/4/2006	1/20/2010	4/21/2005	8/3/2007	4/21/2005	8/31/2005	Filing Date
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	2011-0017498	2009-0206051	2007-0275525	2012-0012553	2007-0230130	2007-0048897	2007-0139977	2011-0043987	2008-0151515	2006-0151202	2006-0154434	2006-0154501		95148292		2007-0166944	2011-0173809	2006-0240364	2007-0266555		2006-0180343	Publication No. Issued
		9/28/2010	3/1/2011		12/8/2009	5/1/2007	12/8/2009	8/21/2012	1/18/2011	7/13/2006	6/10/2008		4/11/2006		7/11/2007	6/3/2008	7/12/2011	11/9/2010	2/12/2008	11/13/2007		Issued
		7,803,688	7,897,877		7,629,684	7,211,470	7,629,559	8,247,703	7,870,664	7,235,745	7,384,856		7,025,607		1,996,562	7,381,587	7,977,034	7,827,682	7,328,502	7,293,355		Patent No.
Pending	Pending	issued	Issued	Pending	Issued	Issued	issued	Issued	issued	Issued	Issued	Pending	Issued	Pending	issued	issued	Issued	ssued	Issued	issued	Pending	Status

2-06-015	2-06-011	IN-2-07-001	HK-2-07-001	2-07-001	2-05-027	2-05-026	TW-2-06-002	IN-2-06-002	CN-2-06-002	2-06-002	JP-2-05-024	2-05-024	2-06-010	2-05-021	JP-2-05-019	IN-2-05-019	2-05-019	Docket No.
S	US	India	Hong Kong	S	US	US	Taiwan	India	China	SU	Japan	US	US	S	Japan	India	SN	Country
CRENELLATED ISOLATION BORDER STRUCTURE AND METHOD	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH SOLDER BALLS HAVING ROUGHENED SURFACES, METHOD OF MAKING ELECTRICAL ASSEMBLY INCLUDING SAID CIRCUITIZED SUBSTRATE, AND METHOD OF MAKING MULTIPLE CIRCUITIZED SUBSTRATE ASSEMBLY	METHOD OF PROVIDING A PRINTED CIRCUIT BOARD WITH AN EDGE CONNECTION PORTION AND/OR A PLURALITY OF CAVITIES THEREIN	METHOD OF PROVIDING A PRINTED CIRCUIT BOARD WITH AN EDGE CONNECTION PORTION AND/OR A PLURALITY OF CAVITIES THEREIN	METHOD OF PROVIDING A PRINTED CIRCUIT BOARD WITH AN EDGE CONNECTION PORTION AND/OR A PLURALITY OF CAVITIES THEREIN	METHOD OF MAKING A CAPACITIVE SUBSTRATE USING PHOTOIMAGEABLE DIELECTRIC FOR USE AS PART OF A LARGER CIRCUITIZED SUBSTRATE, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE AND METHOD OF MAKING AN INFORMATION HANDLING SYSTEM INCLUDING SAID CIRCUITIZED SUBSTRATE	METHOD OF MAKING A CAPACITIVE SUBSTRATE FOR USE AS PART OF A LARGER CIRCUITIZED SUBSTRATE, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE AND METHOD OF MAKING AN INFORMATION HANDLING SYSTEM INCLUDING SAID CIRCUITIZED SUBSTRATE	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH SOLDER PASTE CONNECTIONS	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH SOLDER PASTE CONNECTIONS	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH SOLDER PASTE CONNECTIONS	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH SOLDER PASTE CONNECTIONS	FLUOROPOLYMER DIELECTRIC COMPOSITION FOR USE IN CIRCUITIZED SUBSTRATES AND CIRCUITIZED SUBSTRATE INCLUDING SAME	FLUOROPOLYMER DIELECTRIC COMPOSITION FOR USE IN CIRCUITIZED SUBSTRATES AND CIRCUITIZED SUBSTRATE INCLUDING SAME	INTERPOSER AND TEST ASSEMBLY FOR TESTING ELECTRONIC DEVICES	CIRCUITIZED SUBSTRATE WITH SOLDER- COATED MICROPARTICLE PASTE CONNECTIONS, MULTILAVERED SUBSTRATE ASSEMBLY, ELECTRICAL ASSEMBLY AND INFORMATION HANDLING SYSTEM UTILIZIGN SAME AND METHOD OF MAKING SAID SUBSTRATE	DIELECTRIC COMPOSITION FOR USE IN CIRCUITIZED SUBSTRATES AND CIRCUITIZED SUBSTRATE INCLUDING SAME	DIELECTRIC COMPOSITION FOR USE IN CIRCUITIZED SUBSTRATES AND CIRCUITIZED SUBSTRATE INCLUDING SAME	DIELECTRIC COMPOSITION FOR USE IN CIRCUITIZED SUBSTRATES AND CIRCUITIZED SUBSTRATE INCLUDING SAME	THE
4/26/2012	1/8/2007			1/12/2007	2/13/2006	2/13/2006			11/5/2007	11/14/2006		3/28/2006	12/4/2006	10/6/2005			11/3/2005	Filing Date
13/456,535	11/650,520	2709/DEL/2007	9103246.7	11/652,633	11/352,276	11/352,279	96138518	2156/DEL/2007	200710165173.9	11/598,647	2007-081228	11/390,386	11/607,973	11/244,180	2006-288641	2164/DEL/2006	11/265,287	Appl. No.
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				10/6/2009	9/30/2008	11/11/2008				6/16/2009		9/30/2008	3/10/2009	10/28/2008			4/26/2011	Issued
				7,596,863	7,429,510	7,449,381				7,547,577		7,429,789	7,501,839	7,442,879			7,931,830	Patent No
Pending	Pending	Pending	Pending	Issued	Issued	Issued	Pending	Pending	Issued	Issued	Pending	Issued	Issued	ssued	Pending	Pending	issued	Status

2-07-006	2-06-013	JP-2-07-005	EP-2-07-005	IN-2-07-005	CN-2-07-005	2-07-005	TW-2-07-002	JP-2-07-002	IN-2-07-002	2-07-002	2-06-016	2-07-003	2-06-008D	IN-2-06-008	CN-2-06-008	2-06-008	2-06-014	2-06-007 2-06-007D	2-06-005	2-06-006D1	2-06-006	2-06-009
US	US	Japan	Europe	India	China	SU	Taiwan	Japan	India	US	US	SU	US	India	China	S	SU	Sn	US	US	SU	<b>Country</b> US
PRODUCT PRODUCED FROM SAME	NON-FLAKING CAPACITOR MATERIAL, CAPACITIVE SUBSTRATE HAVING AN INTERNAL CAPACITOR THEREIN INCLUDING SAID NON-FLAKING CAPACITOR MATERIAL, AND METHOD OF MAKING A CAPACITOR MEMBER FOR USE IN A CAPACITIVE SUBSTRATE	METHOD FOR MAKING A MULTILAYERED CIRCUITIZED SUBSTRATE	FLEXIBLE CIRCUIT ELECTRONIC PACKAGE WITH STANDOFFS	CAPACITOR MATERIAL, CIRCUITIZED SUBSTRATE HAVING INTERNAL CAPACITOR COMPRISED OF SAID MATERIAL THEREIN AND ELECTRICAL ASSEMBLY INCLUDING SAID CIRCUITIZED SUBSTRATE	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH SELECTED CONDUCTORS HAVING SOLDER THEREON	HALOGEN-FREE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, MULTILAYERED SUBSTRATE STRUCTURE UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	HALOGEN-FREE CIRCUTTIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, MULTILAYERED SUBSTRATE STRUCTURE UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	HALOGEN-FREE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, MULTILAYERED SUBSTRATE STRUCTURE UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	HALOGEN-FREE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, MULTILAYERED SUBSTRATE STRUCTURE UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	PRINTED CONDUCTIVE LINES WITH LOW RESISTIVITY	SOLDER MASK APPLICATION PROCESS CIRCUITIZED SUBSTRATE ASSEMBLY	ANTIBACTERIAL AGENT	HIGH SPEED INTERPOSER	HIGH SPEED INTERPOSER	TILLE  METHOD OF MAKING A CIRCUITIZED SUBSTRATE WITH ENHANCED CIRCUITRY AND ELECTRICAL ASSEMBLY UTILIZING SAID SUBSTRATE SUBSTRATE							
7/31/2007	4/4/2007				4/30/2008	5/2/2007				3/26/2007	7/3/2012	3/30/2007	3/2/2009			10/3/2006	7/18/2011	9/12/2012	7/25/2006	1/24/2008	6/19/2006	Filing Date 11/1/2006
11/882,149	11/730,761	2008-114868	8251545.3	887/DEL/2008	200810094487.9	11/797,232	97106659	2008-057976	422/DEL/2008	11/727,314	13/540,645	11/730,212	12/380,618	2044/DEL/2007	200710161542.7	11/541,776	13/184,699	11/500,328 13/610,976	11/492,029	12/010,335	11/454,896	Appl: No. 11/590,888
2009-0035455	2007-0177331				101299911	2007-0199195				2008-0237840		2008-0241359	2009-0175000			2008-0078570		2008-0038670	2008-0026316	2008-0142258	2007-0289773	Publication No. Issued 2008-0098595 9/29/2009
						12/8/2009				12/14/2010	· · · · · · · ·	3/22/2011				3/30/2010		10/16/2012	12/22/2009	1/25/2011	12/8/2009	
						7,627,947				7,851,906		7,910,156				7,687,722		8,288,266	7,635,552	/,8/5,811	7,629,541	7,595,454
Pending	Pending	Pending	Pending	Pending	Issued	Issued	Pending	Pending	Pending	Issued	Pending	Issued	Pending	Pending	Pending	Issued	Pending	Pending	Issued	ssued	Issued	Status Issued

2-07-007	2-07-040	2-07-010C	IN-2-07-004	НК-2-07-004	2-07-004	2-08-003	2-07-013	2-07-009	2-06-029	JP-2-07-008	IN-2-07-008	2-07-008D	2-07-008	2-06-026	TW-2-06-012	JP-2-06-012	EP-2-06-012	2-06-012	Docket No.
S	SN	US	India	Hong Kong	SN	Sn	SN	Sń	SN	Japan	India	SN	S	SN	Taiwan	Japan	Europe	S	Country
CIRCUITIZED SUBSTRATE WITH INTERNAL RESISTOR, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND ELECTRICAL ASSEMBLY UTILIZING SAID CIRCUITIZED SUBSTRATE	DEFECTIVE CONDUCTIVE SURFACE PAD REPAIR FOR MICROELECTRONIC CIRCUIT CARDS	SUBSTRATE HAVING INTERNAL CAPACITOR AND METHOD OF MAKING SAME	LED LIGHTING ASSEMBLY AND LAMP UTILIZING SAME	LED LIGHTING ASSEMBLY AND LAMP UTILIZING SAME	LED LIGHTING ASSEMBLY AND LAMP UTILIZING SAME	HIGH BANDWIDTH SEMICONDUCTOR BALL GRID ARRAY PACKAGE	POWER CORE FOR USE IN CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAME	METHOD OF PROVIDING A PRINTED CIRCUIT BOARD WITH AN EDGE CONNECTION PORTION	ELECTRICALLY CONDUCTIVE ADHESIVE (ECA) FOR MULTILAYER DEVICE INTERCONNECTS	CIRCUITIZED SUBSTRATE WITH INTERNAL RESISTOR, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE AND ELECTRICAL ASSEMBLY UTILIZING SAID CIRCUITIZED SUBSTRATE	CIRCUITIZED SUBSTRATE WITH INTERNAL RESISTOR, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE AND ELECTRICAL ASSEMBLY UTILIZING SAID CIRCUITIZED SUBSTRATE	CIRCUITIZED SUBSTRATE WITH CONDUCTIVE PASTE, ELECTRICAL ASSEMBLY INCLUDING SAID CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAID SUBSTRATE	CIRCUITIZED SUBSTRATE WITH CONDUCTIVE PASTE, ELECTRICAL ASSEMBLY INCLUDING SAID CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAID SUBSTRATE	SINTERED METAL MIXTURE FOR Z-AXIS ELECTRICAL INTERCONNECTION	CIRCUITIZED SUBSTRATE WITH INTERNAL STACKED SEMICONDUCTOR CHIPS, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME AND INFORMATION HANDLING SYSTEM UTILIZING SAME	CIRCUITIZED SUBSTRATE WITH INTERNAL STACKED SEMICONDUCTOR CHIPS, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME AND INFORMATION HANDLING SYSTEM UTILIZING SAME	CIRCUITIZED SUBSTRATE WITH INTERNAL STACKED SEMICONDUCTOR CHIPS, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME AND INFORMATION HANDLING SYSTEM UTILIZING SAME	CIRCUITIZED SUBSTRATE WITH INTERNAL STACKED SEMICONDUCTOR CHIPS, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME AND INFORMATION HANDLING SYSTEM UTILIZING SAME	Title
6/4/2007	3/7/2011	6/14/2012			4/2/2007	11/4/2010	5/18/2010	6/7/2007	8/5/2011			10/4/2011	5/23/2007	9/26/2012				4/9/2007	Filing Date
11/806,685	13/041,655	13/517,776	642/DEL/2008	9103287.7	11/730,404	12/939,659	12/782,187	11/808,140	13/198,756	2008-127348	912/DEL/2008	13/252,256	11/802,434	13/626,961	97111078	2008-098245	8251098.3	11/783,306	Appl. No.
2008-0087459	2012-0228013				2008-0238323	2012-0112345	2011-0284273	2008-0301933	2013-0033827			2012-0017437	2007-0221404					2008-0244902	Publication No.
3/30/2010					11/30/2010		6/12/2012	5/11/2010					11/22/2011					9/21/2010	Issued
7,687,724					7,841,741		8,198,551	7,712,210					8,063,315					7,800,916	Patent No.
Issued	Pending	Pending	Pending	Pending	Issued	Pending	issued	Issued	Pending	Pending	Pending	Pending	Issued	Pending	Pending	Pending	Pending	Pending	Status

2-09-002	2-08-021-3	2-08-021-2	2-08-021-1	2-08-025	2-08-016	2-08-012	2-08-024	2-08-008D	2-08-008	2-08-006	2-08-023	2-08-007D	2-08-007	2-07-028	2-08-002D	2-08-002	2-07-017D	2-07-017	2-07-023	2-08-010	2-08-001	2-07-015	EI-2-07-007D	TW-2-07-007	JP-2-07-007
S	US	US	SU	SU	SO	US	S	SU	SU	US	US	S	SU	SO	S	S	S	S	SU	S	US	US	US	Taiwan	Japan
CONDUCTIVE PASTE COMPOSITION AND METHOD OF MAKING CIRCUITIZED SUBSTRATE	CORELESS LAYER BUILDUP STRUCTURE WITH LGA AND JOINING LAYER	CORELESS LAYER BUILDUP STRUCTURE WITH	CORELESS LAYER BUILDUP STRUCTURE	NEW HIGH DENSITY PACKAGING-COMPUTING SYSTEM	SILICON INTERPOSER CONTAINING ACTIVE COMPONENTS AND AN INTEGRATED CONNECTOR	LIQUID CRYSTAL POLYMER LAYER FOR ENCAPSULATION AND IMPROVED HERMITICITY OF CIRCUITIZED SUBSTRATES	METHOD FOR VIA PLATING IN ELECTRONIC PACKAGES CONTAINING FLUOROPOLYMER DIELECTRIC LAYERS	MULTI-LAYER EMBEDDED CAPACITANCE AND RESISTANCE SUBSTRATE CORE	MULTI-LAYER EMBEDDED CAPACITANCE AND RESISTANCE SUBSTRATE CORE	A METHOD OF JOINING A SEMICONDUCTOR DEVICE/CHIP TO A PRINTED WIRING BOARD	CONDUCTIVE PASTE FOR DEVICE LEVEL INTERCONNECTS	METHOD OF APPLYING FORCE TO ELECTRICAL CONTACTS ON A PRINTED CIRCUIT BOARD	SPRING ACTUATED CLAMPING MECHANISM	CONDUCTIVE METAL NUB FOR ENHÂNCED ELECTRICAL INTERCONNECTION, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	MULTILAYERED CIRCUITIZED SUBSTRATE WITH P-ARAMID DIELECTRIC LAYERS AND METHOD OF MAKING SAME	MULTILAYERED CIRCUITIZED SUBSTRATE WITH P-ARAMID DIELECTRIC LAYERS AND METHOD OF MAKING SAME	METHOD OF MAKING A CIRCUITIZED SUBSTRATE WITH CONTINUOUS THERMOPLASTIC SUPPORT FILM DIELECTRIC LAYERS	CIRCUITIZED SUBSTRATE WITH P-ARAMID DIELECTRIC LAYERS AND METHOD OF MAKING SAME	METHOD FOR IMPREGNATING ORGANIC FIBER PAPERS, INCLUDING P-ARAMID PAPERS	METHOD OF FORMING MULTILAYER CAPACITORS IN A PRINTED CIRCUIT SUBSTRATE	CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAME	METHOD OF MAKING CIRCUITIZED ASSEMBLY INCLUDING A PLURALITY OF CIRCUITIZED SUBSTRATES	CIRCUITIZED SUBSTRATE WITH INTERNAL RESISTOR, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND ELECTRICAL ASSEMBLY UTILIZING SAID CIRCUITIZED SUBSTRATE	CIRCUITIZED SUBSTRATE WITH INTERNAL RESISTOR, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND ELECTRICAL ASSEMBLY UTILIZING SAID CIRCUITIZED SUBSTRATE	CIRCUITIZED SUBSTRATE WITH INTERNAL RESISTOR, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND ELECTRICAL ASSEMBLY UTILIZING SAID CIRCUITIZED SUBSTRATE
4/8/2011	4/22/2010	4/22/2010	4/22/2010	4/8/2011	1/31/2012	9/17/2010	4/22/2010	3/10/2010	9/9/2008	7/16/2010	9/17/2010	4/20/2011	6/25/2008	1/20/2011	3/2/2009	4/10/2008	3/2/2009	4/10/2008	7/7/2010	10/22/2010	3/28/2008	1/15/2008	10/20/2009		rung bate
13/082,502	12/764,997	12/764,994	12/764,993	13/082,599	13/362,135	12/884,392	12/765,110	12/720,849	12/283,146	12/837,640	12/884,657	13/090,676	12/215,079	13/009,922	12/380,617	12/081,042	12/380,637	12/081,051	12/831,411	12/909,983	12/078,206	12/007,704	12/589,239	97118394	2008-145499
2012-0257343	2012-0031649	2012-0160544	2012-0160547	2012-0260063		2012-0069288	2011-0260299	2010-0167210	2010-0060381	2012-0015532	2012-0069531	2011-0197430	2009-0320280	2012-0243155	2009-0173426	2008-0191353	2009-0258161	2008-0191354		2012-0223047	2009-0241332	2009-0178273	2011-0039212		Publication No. Issued
						3/27/2012		3/27/2012	9/7/2010	8/14/2012		6/12/2012	10/4/2011		7/3/2012	1/12/2010		12/27/2011							ssued
						8,143,530		8,144,480	7,791,897	8,240,031		8,196,281	8,028,390		8,211,790	7,646,098		8,084,863							Patent No.
Pending	Pending	Pending	Pending	Pending	Pending	Issued	Pending	Issued	Issued	issued	Pending	Issued	issued	Pending	Issued	Issued	Pending	Issued (CIP of EI-2-04-007)	Pending	Pending	Pending	Pending	Pending	Pending	Pending

2-10-021	2-10-018	2-10-017	2-10-016	2-10-015	2-10-014	2-10-013	2-10-012	2-10-011	2-10-010	2-10-009	2-10-008	2-10-007	2-10-006	2-10-005	2-10-004	2-10-003	2-10-002	2-10-001D	2-10-001	2-09-015	2-09-012	2-09-009	2-09-008	2-09-005A	2-09-005D	2-09-005	2-09-003
US	US	SO	US	SU	US	S	SU	SU	SU	S	US	SU	S	S	S	SU	S	SU	SU	US	US	Sn	SU	SU	US	SN	S
CIRCUITIZED SUBSTRATE WITH EMBEDDED CAPACITORS FOR SELF DESTRUCTIVE ANTI- TAMPER PACKAGIN	BUMPED CONNECTION FOR FLEX SUBSTRATES	METHOD OF MAKING A DIMENSIONALLY STABLE CIRCUITIZED SUBSTRATE	PROCEDURE 10 ROW FULLOW ON PROCESSES FOR PRODUCT THAT WAS RUN ON THE OPTICAL REGISTRATION SYSTEM AT LAYUPICAMINATIONS	RIGID-FLEX CIRCUIT BOARD	MINIATURIZED ELECTRONICS PACKAGE FOR CLANDESTINE USE AND METHOD OF MAKING SAME	FROCESS IO PURITY WAS IEWALEK GENERATED IN THE PROCESS OF HYDRO FRACTURING OF NON-CONVENTIONAL GEOLOGIC FORMATIONS	THERMAL SUBSTRATE	INTEGRATED CIRCUIT DIE COVER PLATE AND THERMAL ADHESIVE FOR ANTI-TAMPERING PACKAGING	ELECTRONIC PACKAGE AND METHOD OF MAKING SAME	ELECTRONIC PACKAGE WITH THERMAL INTERPOSER AND METHOD OF MAKING SAME	METAL BUMP CONTACT FOR FLEXIBLE SUBSTRATES, AND INFORMATION HANDLING SYSTEM UTILIZING SAME	POLYDIMETHYLSILOXANE (PPMS) RIGD-FLEX SUBSTRATE FOR ELECTRONICS, ELECTRICALLY CONOUCTIVE ADHESIVE (ECA), AND METHOD FOR MAKING SAME	CIRCUITIZED SUBSTRATE WITH INTERNAL THIN FILM CAPACITOR AND METHOD OF MAKING SAME	SOLDER AND ELECTRICALLY CONDUCTIVE ADHESIVE BASED INTERCONNECTS FOR CZT CRYSTAL ATTACH	CIRCUITIZED SUBSTRATE WITH LOW LOSS CAPACITIVE MATERIAL AND METHOD OF MAKING SAME	LAND GRID ARRAY (LGA) CONTACT CONNECTOR MODIFICATION	ANTI-TAMPER MICROCHIP PACKAGE BASED ON THERMAL NANOFLUIDS OR FLUIDS	CIRCUITIZED SUBSTRATE WITH DIELECTRIC INTERPOSER ASSEMBLY AND METHOD	CIRCUITIZED SUBSTRATE WITH DIELECTRIC INTERPOSER ASSEMBLY AND METHOD	METHOD OF SMALL CAVITY FORMATION ON BURIED RESISTOR LAYER USING FUSION BONDING	LIQUID CRYSTAL POLYMER (LCP) SURFACE LAYER ADHESION ENHANCEMENT	ELECTRONIC PACKAGE AND METHOD OF MAKING SAME	HIGH DENSITY CONNECTOR FOR INTERCONNECTING FINE PITCH CIRCUIT PACKAGING STRUCTURES	MÉTHÓD OF MAKING HIGH DENSITY INTERPOSER AND ELECTRONIC PACKAGE UTILIZING SAME	ELECTRONIC PACKAGE INCLUDING HIGH DENSITY INTERPOSER AND CIRCUITIZED SUBSTRATE ASSEMBLY UTILIZING SAME	ELECTRONIC PACKAGE INCLUDING HIGH DENSITY INTERPOSER AND CIRCUITIZED SUBSTRATE ASSEMBLY UTILIZING SAME	SEMI-CONDUCTOR CHIP WITH COMPRESSIBLE CONTACT STRUCTURE AND ELECTRONIC PACKAGE UTILIZING SAME
6/15/2012	9/22/2011	11/21/2012	4/16/2012	4/16/2012	1/30/2012	9/21/2011	7/25/2011	5/8/2012	4/17/2012	2/8/2011	7/19/2011	4/17/2012	3/8/2011	1/26/2012	10/10/2011	10/14/2010	9/17/2010	9/19/2012	12/20/2010	4/8/2011	8/4/2011	10/22/2010	5/28/2010	12/1/2009	2/26/2013	11/30/2009	7/15/2010
13/523,956	13/239,544	13/682,805	13/447,644	13/447,701	13/360,935	13/238,392	13/189,980	13/466,164	13/448,574	13/022,654	13/184,882	13/448,505	13/042,578	13/358,716	13/269,770	12/904,305	12/884,421	13/622,478	12/972,700	13/082,444	13/197,804	12/910,020	12/789,642	12/592,734	13/776,777	12/592,682	12/836,612
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																	10/16/2012		10/30/2012				7/5/2011	8/21/2012		3/26/2013	6/12/2012
																	8,288,857		8,299,371				7,972,178	8,245,392		8,405,229	8,198,739
Pending	Pending	Pending	Pending	Pending	Pending	Pending	Pending	Pending	Pending	Pending	Pending	Pending	Pending	Pending	Allowed	Pending	Issued	Pending	Issued	Pending	Pending	Pending	ssued	Issued	Pending	issued	Issued

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Docket No.	Country	Title	Filing Date	Appl. No.	Publication No. Issued F	Patent No. Status
2-10-022	SN	SELF DESTRUCTIVE INTEGRATED CIRCUIT DIE FOR ANTI-TAMPER PACKAGING	5/8/2012	13/466,181		Pending
2-11-006	S	CIRCUITIZED SUBSTRATE INCLUDING RFID TECHNOLOGY AND METHOD OF MAKING SAME	5/30/2012	13/483,600		Pending
2-11-007	US	THIN CORE ELECTRONIC PACKAGE AND METHOD OF MAKING SAME	8/31/2012	13/600,332		Pending
2-11-009	SU	METHOD OF VERIFYING PRODUCT AUTHENTICITY	4/17/2012	13/448,778		Pending
2-11-010	SU	HIGH PERFORMANCE COMPUTER WITH FIELD PROGRAMMABLE GATE ARRAY	6/28/2012	13/535,432	:	Pending
		ACCELERATION				