3/9/15

03/11/2015
103671543

FORM PTO-1595
(Rev. 08/05)
Office OMB No. 0651-0027 (exp. 06/30/2008)

U.S. DEPARTMENT OF COMMERCE
United States Patent and Trademark

To the Director of the U.S. Patent and Trademark Office: Please record the attached original documents or the new address(es) below.

1. Name of conveying party(ies):
Silicon Valley Bank
3003 Tasman Drive
Santa Clara, CA 95054
Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies):
Name: Ramtron International Corporation
Internal Address:
Street Address: 1850 Ramtron Drive
City: Colorado Springs
State: CO
Country: USA Zip: 80921
Additional name(s) & address(es) attached? ☐ Yes ☒ No

3. Nature of conveyance/Execution Date(s):
Execution Date: **09/15/2005**
☐ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☐ Joint Research Agreement
☐ Government Interest Assignment
☐ Executive Order 9424, Confirmatory License
☒ Other: **Release**

4. Application or patent number(s):
☐ This document is being filed together with a new application.

A. Patent Application No.(s)	B. Patent No.(s)				
	5024964	4910708	5580814	5475248	5525528
	5598366	4918654	5374578	5866926	5822237
	5214300	4914627	5495117	5371699	5438023
	5774392	5889428	5838605		
	4873664	4893272	5338951	5381364	5578867
	5969935				
	4809225	4888733	5369296	5530668	5592410
	5800683				
	4853893	5005102	5523595	5572459	5815430
	6008659				

Additional numbers attached? ☒ Yes ☐ No

5. Name and address of party to whom correspondence concerning document should be mailed:
Name: **UCC Direct**
Internal Address: **Attn: 14080632**
Street Address: **187 Wolf Road, Suite 101**
City: **Albany**
State: **NY** Zip: **12205**
Phone Number: **1-800-342-3676 X 4065**
Fax Number: **1-800-962-7049**
Email Address: **cls-udsalbany@wolterskluwer.com**

6. Total number of applications and patents involved: 94

7. Total fee (37 CFR 1.21 (h) & 3.41) **$ 3,760.00**
☒ Authorized to be charged by credit card
☐ Authorized to be charged to deposit account
☐ Enclosed
☐ None required (government interest not affecting title)

8. Payment Information
a. Credit Card Last 4 Numbers 0974
Expiration Date 3-17
03/17/2015 KNGUYEN1 00000027 5024964
b. Deposit Account Number
Authorized User Name
01 FC:8021 3760.00 OP

9. Signature:
Joseph D Borgman
Signature
3-9-15
Date
Joseph D Borgman
Name of Person Signing
Total number of pages including cover sheet, attachments, and documents:

Ramtron International Corporation Additional Patent Numbers:

6141237	5985713	6185123
6495413	5864932	6856573
6650158	5902131	6358755
6661695	5956266	5852376
6275425	6560137	6211542
6455326	6174735	6287637
6597028	5920453	5986919
6894549	5880989	5978251
6853535	5854568	6249014
6661696	5969980	5890199
6362675	6190926	5818771
6492673	6027947	6263398
6423592	6080499	6252793
6728093	6028783	5995406
6459609	5892728	
6682772	6201726	
6376259	6203608	
6430093	6242299	
6717839	6613586	
6535446	5999461	
6445608	6150184	
6538914	6090443	

RELEASE OF SECURITY AGREEMENT COVERING INTERESTS IN PATENTS

Silicon Valley Bank ("Secured Party"), hereby releases its security interest in the interests of **Ramtron International Corporation.** ("Assignor") in the **patented** works set forth in that certain **Intellectual Property Security Agreement** dated **09/15/2005**, executed by Assignor in favor of Secured Party recorded with the United States Department of Commerce, Patent and Trademark Office on **10/17/2005**, Reel **17105**, Frame **174**

Dated: **03/09/2015**

SILICON VALLEY BANK

By: _____
Name: **Romil Randhawa**
Title: **Senior Operations Manager**

INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement is entered into as of September 15, 2005, by and between SILICON VALLEY BANK ("Bank") and RAMTRON INTERNATIONAL CORPORATION, a Delaware corporation ("Grantor").

RECITALS

A. Bank has agreed to make certain advances of money and to extend certain financial accommodation to Grantor (the "Loans") in the amounts and manner set forth in that certain Amended and Restated Loan and Security Agreement by and between Bank and Grantor dated as of the date hereof (as the same may be amended, modified or supplemented from time to time, the "Loan Agreement"; capitalized terms used herein are used as defined in the Loan Agreement). Bank is willing to make the Loans to Grantor, but only upon the condition, among others, that Grantor shall grant to Bank a security interest in certain Copyrights, Trademarks, Patents, and Mask Works to secure the obligations of Grantor under the Loan Agreement.

B. Pursuant to the terms of the Loan Agreement, Grantor has granted to Bank a security interest in all of Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of its obligations under the Loan Agreement, Grantor hereby represents, warrants, covenants and agrees as follows:

AGREEMENT

To secure its obligations under the Loan Agreement, Grantor grants and pledges to Bank a security interest in all of Grantor's right, title and interest in, to and under its Intellectual Property Collateral (including without limitation those Copyrights, Patents, Trademarks and Mask Works listed on Schedules A, B, C, and D hereto), and including without limitation all proceeds thereof (such as, by way of example but not by way of limitation, license royalties and proceeds of infringement suits), the right to sue for past, present and future infringements, all rights corresponding thereto throughout the world and all re-issues, divisions continuations, renewals, extensions and continuations-in-part thereof.

This security interest is granted in conjunction with the security interest granted to Bank under the Loan Agreement. The rights and remedies of Bank with respect to the security interest granted hereby are in addition to those set forth in the Loan Agreement and the other Loan Documents, and those which are now or hereafter available to Bank as a matter of law or equity. Each right, power and remedy of Bank provided for herein or in the Loan Agreement or any of the Loan Documents, or now or hereafter existing at law or in equity shall be cumulative and concurrent and shall be in addition to every right, power or remedy provided for herein and the exercise by Bank of any one or more of the rights, powers or remedies provided for in this Intellectual Property Security Agreement, the Loan Agreement or any of the other Loan

Documents, or now or hereafter existing at law or in equity, shall not preclude the simultaneous or later exercise by any person, including Bank, of any or all other rights, powers or remedies.

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

Address of Grantor:

RAMTRON INTERNATIONAL CORPORATION

1850 Ramtron Drive
Colorado Springs, CO 80921

By: _____
Eric A. Balzer
Title: CFO

BANK:

Address of Bank:

SILICON VALLEY BANK

4410 Arapahoe Ave., Suite 200
Boulder, CO 80303
Attn: Cindy Schatz

By: _____

Title: Relationship Manager

EXHIBIT A

Copyrights

Description	Registration/ Application Number	Registration/ Application Date

{00180692.DOC}

EXHIBIT B

Patents

Description	Registration/ Application Number	Registration/ Application Date

Total Number of
Issued Patent Applications

RAM No. / Application:	Tech. / America USA	Short Title	Patent No.	Issued	Expires	Inventor
RAM 240	FRAM	Monolithic F.E. Integrated Circuit	5,024,964	6/18/1991	6/18/2008	Rohrer
RAM 240 DIV 2	FRAM	Monolithic F.E.I.C. Structures	5,214,300	5/25/1993	5/25/2010	Rohrer
RAM 302	FRAM	Self Restoring FE Memory	4,873,664	10/10/1989	2/12/2007	Eaton
RAM 303	FRAM	Shadow RAM	4,809,225	2/28/1989	7/2/2007	Dimmler
RAM 305	DRAM	Programmable Capacitance Divide	4,853,893	8/1/1989	7/2/2007	Eaton
RAM 305 DIV1	DRAM	SRAM with Programmable	4,918,654	4/17/1990	7/2/2007	Eaton
RAM 305 DIV2	DRAM	DRAM with Programmable	4,910,708	3/20/1990	7/2/2007	Eaton
RAM 305 DIV3	DRAM	Memory Cell with Programmable	4,914,627	4/3/1990	7/2/2007	Eaton
RAM 309	FRAM	Ferroelectric Retention	4,893,272	1/9/1990	4/22/2008	Eaton
RAM 311/312	FRAM	2T Cell and Read Method	4,888,733	12/19/1989	9/12/2008	Mobley
RAM 314	FRAM	Electrode Structures	5,005,102	4/2/1991	6/20/2009	Larson
RAM 329 FWC	FRAM	Ozone Gas Processing	5,374,578	12/20/1994	12/20/2011	Patel/Sheldon
RAM 332 DIV	FRAM	Stacked FE Memory Cell	5,580,814	12/3/1996	6/10/2014	Larson
RAM 332 FWC 2	FRAM	Stacked FE Memory Cell	5,495,117	2/27/1996	5/27/2013	Larson
RAM 339	FRAM	Fabrication of High Dielectric	5,336,951	8/16/1994	11/6/2011	Argos
RAM 348 FWC	FRAM	Ferroelectric Memory Device	5,389,296	11/29/1994	5/12/2012	Kato
RAM 352 FWC	FRAM	Semiconductor Device	5,523,595	6/4/1996	6/4/2013	Takenaka
RAM 357 FWC	FRAM	Semiconductor Device	5,866,926	2/2/1999	2/2/2016	Takenaka
RAM 358 FWC 2	FRAM	Semiconductor Device	5,475,248	12/12/1995	12/13/2013	Takenaka
RAM 360	FRAM	Non-Volatile Ferroelectric Memory	5,371,699	12/6/1994	11/17/2012	Larson
RAM 365	FRAM	FE-Based RAM Sensing Scheme	5,381,364	1/10/1995	6/24/2013	Chern
RAM 370	FRAM	High Speed Ferroelectric Based	6,530,668	8/25/1996	4/12/2015	Chern
RAM 371	FRAM	Voltage Reference for FE 1T/1C	5,572,459	11/5/1996	8/16/2014	Wilson
RAM 371 DIV	FRAM	Voltage Reference for FE 1T/1C	5,822,237	10/13/1998	9/16/2014	Wilson
RAM 374	FRAM	Rejuvenation Anneal	5,525,528	6/11/1996	2/23/2014	Perino
RAM 378	FRAM	Passivation Method/Structure Using	5,438,023	8/1/1995	3/11/2014	Argos
RAM 378 DIV	FRAM	Passivation Method/Structure Using	5,578,867	11/26/1996	3/11/2014	Argos
RAM 384	FRAM	Circuit Method for Reducing	5,592,410	1/7/1997	4/10/2016	Verhaeghe
RAM 384 DIV	FRAM	Circuit Method for Reducing	5,815,430	9/29/1998	4/10/2016	Verhaeghe
RAM 386	FRAM	Low Loss, Regulated Charge Pump	5,889,428	3/30/1999	3/30/2016	Young, D.
RAM 387	FRAM	Ferroelectric Nonvolatile Random	5,598,366	1/29/1997	8/16/2015	Kraus
RAM 388	FRAM	Bootstrapping Circuit Utilizing	5,774,392	6/30/1998	3/26/2016	Kraus
RAM 396	FRAM	The Use of Calcium and Strontium	5,989,935	10/19/1999	3/15/2016	Kammerdiner
RAM 396 DIV	FRAM	The Use of Calcium and Strontium	5,800,683	9/1/1998	3/15/2016	Kammerdiner
RAM 397	FRAM	A Method of Measuring Retention	6,009,659	12/28/1999	3/15/2016	Traynor
RAM 398	FRAM	Iridium Oxide Local Interconnect	5,838,605	11/17/1998	3/20/2016	Bailey
RAM 398 DIV	FRAM	Method of Forming Iridium Oxide	5,985,713	11/16/1999	3/20/2016	Bailey
RAM 399 DIV	FRAM	Yield Enhancement Technique	6,190,926	2/20/2001	2/20/2017	Mitra/Argos
RAM 400	FRAM/DRAM	Low Voltage Bootstrapping Circuit	5,999,461	12/7/1999	8/7/2016	Verhaeghe
RAM 405	FRAM	Bandgap Reference Based	5,852,376	12/22/1998	8/23/2016	Kraus
RAM 406	FRAM	Data Processor Inc A FE Memory	5,890,199	3/30/1999	3/30/2016	Downs
RAM 407	FRAM	Partially or Completely	5,820,453	7/6/1999	8/20/2016	Evans
RAM 407 CIP	FRAM	Partially or Completely	5,864,932	2/2/1999	8/20/2016	Evans
RAM 407CIP2	FRAM	Partially or Completely	6,027,947	2/22/2000	10/11/2016	Evans
RAM 407CIP2 DIV	FRAM	Method of Fabricating Partially	6,160,184	11/21/2000	11/21/2016	Evans
RAM 407CIP3	FRAM	Completely Encapsulated TE	6,211,542	4/3/2001	4/3/2017	Eastep/Evans
RAM 409 (Hitachi)	DRAM	Semiconductor Memory Device	5,818,771	10/6/1998	9/30/2016	Yasu
RAM 414	FRAM	Sensing Methodology for a 1T/1C	5,880,989	3/9/1999	11/14/2017	Wilson
RAM 415	FRAM	Dual-Level Metallization Method	5,902,131	5/11/1999	5/9/2017	Argos
RAM 421	FRAM	Multi-Layer Approach for Optimiz	6,080,499	6/27/2000	7/16/2017	Eastep
RAM 421 CIP	FRAM	Multi-Layer Approach for Optimiz	6,090,443	7/18/2000	7/18/2017	Eastep
RAM 421 CIP2	FRAM	Multi-Layer Approach for Optimiz	6,287,637	9/11/2001	9/11/2018	Chu/Fox/Eastep
RAM 422	EDRAM/FRAM	Integrated Circuit Memory Device	6,263,398	7/17/2001	7/17/2018	Alwais
RAM 424	FRAM	Voltage Boost Circuit and Operation	5,854,568	12/29/1998	9/20/2017	Moscaluk
RAM 433	FRAM	Reference Cell for a 1T/1C	5,956,266	9/21/1999	11/14/2017	Wilson
RAM 434	FRAM	Memory Cell Config for a 1T/1C	6,028,783	2/22/2000	11/14/2017	Allen/Kraus
RAM 434CON	FRAM	Memory Cell Config for a 1T/1C	6,185,123	2/6/2001	2/6/2018	Allen/Kraus
RAM 435	FRAM	Reference Cell Configuration for a	5,986,919	11/16/1999	11/14/2017	Allen
RAM 435CON	FRAM	Reference Cell Configuration for a	6,252,793	6/26/2001	6/26/2018	Allen/Kraus
RAM 436	FRAM	Sense Amplifier Configuration for a	5,969,980	10/19/1999	11/14/2017	Allen
RAM 436CON	FRAM	Sense Amplifier Configuration for a	6,560,137	5/6/2003	5/23/2018	Allen
RAM 437	FRAM	Column Decoder Configuration for	5,892,728	4/6/1999	11/14/2017	Allen
RAM 437CON	FRAM	Column Decoder Configuration for	6,856,573	2/15/2005	2/15/2018	Allen/Wilson/Perkelis
RAM 439	FRAM	Plate Line Driver Circuit for	5,978,251	11/2/1999	11/14/2017	Kraus
RAM 440	FRAM	Plate Line Driver Circuit for	5,995,405	11/30/1999	11/14/2017	Kraus
RAM 442	FRAM	FE Thin Films and Solutions	6,203,608	3/20/2001	3/20/2018	Sun/DH/TD
RAM 444	FRAM	Method of Manufacturing FE Mem	6,174,735	1/16/2001	1/16/2018	Evans
RAM 444 DIV	FRAM	FE Memory Device Structure Use	6,201,726	3/13/2001	10/23/2018	Evans
RAM 444 DIV 2	FRAM	FE Memory Device Structure Use	6,358,755	3/19/2002	3/19/2019	Evans
RAM 445	FRAM	Hydrogen Barrier Encapsulation	6,249,014	6/18/2001	6/18/2018	Bailey
RAM 446	FRAM	Hydrogen Barrier Encapsulation	6,613,586	9/2/2003	9/2/2020	Bailey
RAM 446 DIV	FRAM	Barrier Layer to Protect a FE	6,242,299	6/5/2001	6/5/2019	Hickert
RAM 454	FRAM	FE Non-Volatile Latch Circuit	6,141,237	10/31/2000	10/31/2018	Eliason/Kraus
RAM 456	FRAM	Enhanced Process Capability for	6,456,326	9/24/2002	9/24/2017	Brian Eastep
RAM 458	FRAM	Nonvolatile Octal Latch & D-Type	6,982,675	3/26/2002	3/26/2019	Alwais
RAM 462	FRAM/Ulvac	High Temperature Deposition of...	6,682,772	1/27/2004	1/27/2021	Fox
RAM 467	FRAM	Two Stage Low Voltage FE Boost	6,535,448	3/18/2003	6/28/2021	Moscaluk
RAM 477						

RAM 478	FRAM	FE Voltage Boost Circuits	6,275,425	8/14/2001	11/18/2020	Ellason
RAM 479	FRAM	Process and Structure for Masking	6,495,413	12/17/2002	12/17/2019	Sun, et al
RAM 480	FRAM	Capacitively Coupled FE Random	6,587,028	7/22/2003	7/22/2020	Glen Fox
RAM 482	FRAM	Charge Pump or Other Charge...	6,492,673	12/10/2002	12/10/2019	Glen Fox
RAM 483	FRAM	Method for Mfg a FE Mem Cell	6,376,259	4/23/2002	4/21/2021	Chu/Fox
RAM 485	FRAM	Ferroelectric Random Access	6,445,608	9/3/2002	9/10/2018	Schwartz/Alwais
RAM 485 CON	FRAM	Ferroelectric Random Access	6,661,696	12/9/2003	12/9/2020	Schwartz/Alwais
RAM 493	FRAM	Ferroelectric Non-Volatile Logic	6,650,158	11/18/2003	11/18/2020	Ellason
RAM 493DIV	FRAM	Ferroelectric Non-Volatile Logic	6,894,549	5/17/2005	5/17/2022	Ellason
RAM 494	FRAM	PZT Layer as a Temporary Encap	6,423,592	7/23/2002	7/23/2019	Shan Sun
RAM 495	FRAM	CMOS Boosting Circuit Utilizing	6,430,093	8/6/2002	8/6/2019	Ellason/Kraus
RAM 497	FRAM	FE Memory w/Bit-Plate Parallel	6,538,914	3/25/2003	3/25/2020	YB Chung
RAM 500	FRAM	Self Referencing 1T/1C FE	6,459,609	10/1/2002	12/13/2018	Xiao Hong DU
RAM 501	FRAM	Capacitance Sensing Technique	6,661,695	12/9/2003	12/9/2020	Dave Flach
RAM 502	FRAM	Method for Producing Crystall.	6,853,535	2/8/2005	10/26/2022	Glen Fox/Tom D.
RAM 503	FRAM	Method for Producing Crystall.	6,728,093	4/27/2004	4/27/2021	Glen Fox
RAM 507	FRAM	Bit-Line Shielding Method for FE	6,717,838	4/6/2004	4/6/2021	Xiao Hong DU
Application:	Germany					
RAM 302 EPO	FRAM	Self Restoring Ferroelectric Memor	P3781171.8-08	8/17/1994	12/31/2008	Eaton
RAM 414 EPO (To be Abandoned)	FRAM	Sensing Method for a 1T/1C FE	69811181.8-08	2/5/2003	10/6/2018	Wilson
RAM 414 EPO DIV (To be Aban.)	FRAM	Reference Cell for a 1T/1C FE	1265251	2/9/2005		Wilson
Application:	Italy					
RAM 414 EPO DIV (To be Aban.)	FRAM	Reference Cell for a 1T/1C FE	1265251	2/9/2005		
Application:	Japan					
RAM 302 JPN	FRAM	Self Restoring Ferroelectric Memor	2,674,775	5/30/1997	2/12/2008	Eaton
RAM 336 JPN	FRAM	Structure of High Dielectric	3,162,512	2/23/2001	2/23/2013	Argos
RAM 370 JPN (To be Abandoned)	FRAM	FE Memory Sensing Scheme	3,238,068	10/5/2001	4/12/2016	Wilson/Chern
RAM 371 JPN (To be Abandoned)	FRAM	Voltage Reference for a FE 1T1C	2,987,316	10/1/1999	10/1/2012	Meadows
RAM 415 JPN	FRAM	Dual-Level Metalization Method	2,962,475	8/6/1999	5/11/2018	Argos

EXHIBIT C

Trademarks

Description	Registration/ Application Number	Registration/ Application Date

EXHIBIT D

Mask Works

Description	Registration/ Application Number	Registration/ Application Date

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