PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT3330117

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
ATMEL CORPORATION	09/28/2012

RECEIVING PARTY DATA

Name:	ARTEMIS ACQUISITION
Street Address:	1250 BORREGAS AVE.
City:	SUNNYVALE
State/Country:	CALIFORNIA
Postal Code:	94089

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	14698205

CORRESPONDENCE DATA

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ATTORNEY DOCKET NUMBER:	37441-0021002
NAME OF SUBMITTER:	MI KYONG SHIN
SIGNATURE:	/Mi Kyong Shin/
DATE SIGNED:	04/28/2015

Total Attachments: 8
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PATENT ASSIGNMENT

This Patent Assignment (the "Assignment") is entered into as of September 28 , 2012 by and between Atmel Corporation, a Delaware corporation ("Assignor") and Artemis Acquisition LLC, a California Limited Liability Company ("Assignee").

RECITALS

WHEREAS, pursuant to that certain Purchase and Sale Agreement, dated as of July 12, 2012 by and between Assignor and Assignee, as amended to date, Assignor has assigned and/or agreed to assign to Assignee, all right, title and interest in and to those patents and patent applications listed in Schedule 1 to this Assignment;

WHEREAS, Assignor and Assignee desire to execute and record this Assignment, in order to effect and/or confirm the assignment of the Transferred Patents (as defined below).

NOW, THEREFORE, the parties hereby agree as follows:

1.   Assignor does hereby sell, assign, and transfer to Assignee, for itself and its successors, transferees, and assignees, the entire worldwide right, title, and interest in and to (a) the patents and patent applications listed in Schedule 1, (b) all patents and patent applications that claim priority to any of the foregoing, including all continuations, divisionals, reexaminations, reissues, extensions, and foreign counterparts of the foregoing; (c) all patents and patent applications from which any of the foregoing claims priority; (d) all patents that issue from any of the foregoing; and (e) the right to sue in its own name and to recover for past infringement of any applications or patents issuing therefrom together with all rights to recover damages for infringement of provisional rights (collectively, the "Transferred Patents").

2.   Assignor agrees to execute all oaths, assignments, powers of attorney, applications, and other papers necessary or desirable to fully secure to Assignee the legal rights, titles and interests herein conveyed, when requested, and without further consideration, in order to carry out the intent of this Assignment.

<u>Duly Authorized Representative of ASSIGNOR</u>

<u>Date of Signature</u>

Atmel Corporation

September 28, 2012

By: _____

Name: _STEPHEN SCHMIDT_

Title: _SVP_

State of _____

County of _____

On _____ before me, _____ personally
              [DATE]   [NOTARY PUBLIC]

appeared _____ personally known to me or proved to me on the
            [REPRESENTATIVE]

basis of satisfactory evidence to be the person whose name is subscribed to the within
instrument and acknowledged to me that [he/she] executed the same in [his/her] authorized
capacity, and that by [his/her] signature on the instrument the person, or the entity upon behalf
of which the person acted, executed the instrument.

_____
Notary

Notary Seal

See attached California All-Purpose Acknowledgment "

[ASSIGNOR SIGNATURE PAGE TO PATENT ASSIGNMENT]
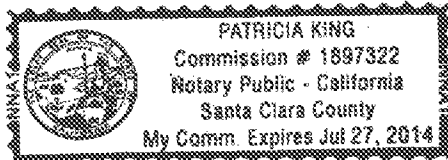
CALIFORNIA ALL-PURPOSE ACKNOWLEDGMENT

CIVIL CODE § 1189

State of California

County of Santa Clara

On September 28, 2012 before me, Patricia King, Notary Public
Date   Here Insert Name and Title of the Officer

personally appeared Stephen Skaggs
Name(s) of Signer(s)

PATRICIA KING
Commission # 1897322
Notary Public - California
Santa Clara County
My Comm. Expires Jul 27, 2014

who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/are subscribed to the within instrument and acknowledged to me that he/she/they executed the same in his/her/their authorized capacity(ies), and that by his/her/their signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

Signature: Patricia King
Signature of Notary Public

Place Notary Seal Above

─────────── OPTIONAL ───────────

Though the information below is not required by law, it may prove valuable to persons relying on the document and could prevent fraudulent removal and reattachment of this form to another document.

Description of Attached Document

Title or Type of Document: Patent Assignment

Document Date: September 28, 2012 _____ Number of Pages: _____

Signer(s) Other Than Named Above: _____

Capacity(ies) Claimed by Signer(s)

Signer's Name: _____	Signer's Name: _____
☐ Corporate Officer — Title(s): _____	☐ Corporate Officer — Title(s): _____
☐ Individual	☐ Individual
☐ Partner — ☐ Limited ☐ General	☐ Partner — ☐ Limited ☐ General
☐ Attorney in Fact	☐ Attorney in Fact
☐ Trustee	☐ Trustee
☐ Guardian or Conservator	☐ Guardian or Conservator
☐ Other: _____	☐ Other: _____
Signer Is Representing: _____	Signer Is Representing: _____

RIGHT THUMBPRINT OF SIGNER
Top of thumb here

RIGHT THUMBPRINT OF SIGNER
Top of thumb here

**PATENT
REEL: 035516 FRAME: 0991**

<u>Duly Authorized Representative of ASSIGNEE</u>   <u>Date of Signature</u>

(signature)

Name: NARBEH DERHACOBIAN   9/28 _____, 2012

Title: CEO

State of _____
County of _____

        On _____ before me, _____ personally
                      [DATE]   [NOTARY PUBLIC]
appeared _____ personally known to me or proved to me on the
              [REPRESENTATIVE]
basis of satisfactory evidence to be the person whose name is subscribed to the within
instrument and acknowledged to me that [he/she] executed the same in [his/her] authorized
capacity, and that by [his/her] signature on the instrument the person, or the entity upon behalf
of which the person acted, executed the instrument.

                                 See attached _____
                                Notary _____

Notary Seal

[SIGNATURE PAGE TO PATENT ASSIGNMENT]

CALIFORNIA ALL-PURPOSE
CERTIFICATE OF ACKNOWLEDGMENT

State of California

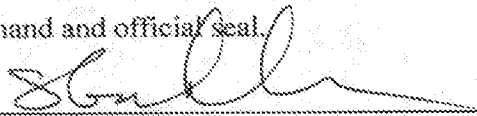County of _Santa Clara_

On _9/28/12_ before me, _Sharon L. Li_ ,
(Here insert name and title of the officer)

personally appeared _Narbeh Derhacobian_ ,

who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/are subscribed to the within instrument and acknowledged to me that he/she/they executed the same in his/her/their authorized capacity(ies), and that by his/her/their signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

_____ (Notary Seal)
Signature of Notary Public

> SHARON L. LI
> Comm. # 1955511
> NOTARY PUBLIC-CALIFORNIA
> SANTA CLARA COUNTY
> My Comm. Exp. Nov. 4, 2015

ADDITIONAL OPTIONAL INFORMATION

DESCRIPTION OF THE ATTACHED DOCUMENT

Patent assignment
(Title or description of attached document)

signature page
(Title or description of attached document continued)

Number of Pages _1_   Document Date _9/28/12_

_____
(Additional information)

CAPACITY CLAIMED BY THE SIGNER

☐ Individual (s)
☐ Corporate Officer
  _____
  (Title)
☐ Partner(s)
☐ Attorney-in-Fact
☐ Trustee(s)
☐ Other _____

SCHEDULE 1 to PATENT ASSIGNMENT

List of Patents and Patent Applications

Application Title	Country	Application Number	Filing Date	Patent Number	Issue Date	Inventors
Method and System to Access Memory	US	12/205,518	05-Sep-2008	7,929,356	19-Apr-2011	DeCaro, Richard; Manea, Danut
Method and System to Access Memory	TW	98129756	03-Sep-2009			DeCaro, Richard; Manea, Danut
Configurable Number for Dummy Bytes for a Sequential Access Memory Device	CN	2009-100087964	04-Sep-2009			DeCaro, Richard; Manea, Danut
Method and System to Access Memory	US	13/052,810	21-Mar-2011	8,208,315	26-Jun-2012	DeCaro, Richard; Manea, Danut
Method and System for Reducing Soft-Writing in a Multi-Level Flash Memory	US	11/144,174	02-Jun-2005	7,522,455	21-Apr-2009	Oddone, Giorgio; Bartoli, Simone; Caser, Fabio T.; Bedarida, Lorenzo
Reference Cell for High Speed Sensing in Non-Volatile Memories	US	09/602,108	21-Jun-2000	6,411,549	25-Jun-2002	Pathak, Jagdish; Payne, James E; Pathak (S), Saroj
Reference Cell for High Speed Sensing in Non-Volatile Memories	CN	01801049.0	14-May-2001	ZL 01801049.0	04-May-2005	Pathak, Jagdish; Payne, James E; Pathak (S), Saroj
Reference Cell for High Speed Sensing in Non-Volatile Memories	TW	90114695	18-Jun-2001	NI-167346	03-Apr-2003	Pathak, Jagdish; Payne, James E; Pathak (S), Saroj
Low Power Voltage Regulator Circuit for Use in an Integrated Circuit Device	US	09/586,664	01-Jun-2000	6,320,454	20-Nov-2001	Kuo, Harry H; Payne, James E; Pathak (S), Saroj
Low Power Voltage Regulator Circuit for Use in an Integrated Circuit Device	TW	90112073	21-May-2001	NI-166239	01-Nov-2002	Kuo, Harry H; Payne, James E; Pathak (S), Saroj
Low Power Voltage Regulator Circuit for Use in an Integrated Circuit Device	CN	01810120.8	20-Apr-2001	ZL 01810120.8	08-Jun-2005	Kuo, Harry H; Payne, James E; Pathak (S), Saroj
Low Power Voltage Regulator Circuit for Use in an Integrated Circuit Device	DE	01 928 713.5	20-Apr-2001	1 301 982	02-Aug-2006	Kuo, Harry H; Payne, James E; Pathak (S), Saroj
Row Decoder Circuit for Use in Programming a Memory Device	US	10/174,632	18-Jun-2002	6,621,745	16-Sep-2003	Manea, Danut
Row Decoder Circuit for Use in Programming a Memory Device	TW	92112834	12-May-2003	I-238417	21-Aug-2005	Manea, Danut

Row Decoder Circuit for Use in Programming a Memory Device	CN	03819561.5	14-Apr-2003	ZL 03819561.5	08-Oct-2008	Manea, Danut
Method of Programming a Multi-Level Memory Device	US	10/190,374	02-Jul-2002	6,714,448	30-Mar-2004	Manea, Danut
Method of Programming a Multi-Level Memory Device	TW	92113850	22-May-2003	I-238532	21-Aug-2005	Manea, Danut
Method of Programming a Multi-Level Memory Device	CN	03820720.6	30-Apr-2003	ZL 03820720.6	20-Apr-2011	Manea, Danut
Method of Establishing Reference Levels for Sensing Multilevel Memory Cell States	US	10/211,437	02-Aug-2002	6,618,297	09-Sep-2003	Manea, Danut
Method of Recovering Overerased Bits in a Memory Device	US	10/235,265	04-Sep-2002	6,724,662	20-Apr-2004	Manea, Danut
Dual Stage Voltage Regulation Circuit	US	10/666,324	17-Sep-2003	7,064,529	20-Jun-2006	Telecco, Nicola
Method for Identification of SPI	US	10/284,597	30-Oct-2002	7,032,039	18-Apr-2006	DeCaro, Richard
Method for Identification of SPI	TW	92128993	20-Oct-2003	I-289748	11-Nov-2007	DeCaro, Richard
Method for Identification of SPI	CN	03825730.0	25-Sep-2003	ZL 03825730.0	04-Apr-2007	DeCaro, Richard
Method and Apparatus of a Smart Decoding Scheme for Fast Synchronous Read in a Memory System	US	10/686,243	14-Oct-2003	7,143,257	28-Nov-2006	Schumann, Steven; Ching, Fai; Kowshik, Vikram
Functional Register Decoding System for Multiple Plane Operation	US	10/686,401	14-Oct-2003	7,099,226	29-Aug-2006	Yuan, Yolanda; Guo, Jason; Tsang, Sai; Kowshik, Vikram; Schumann, Steven
Approach for Zero Dummy Byte Flash Memory Read Operation	US	10/929,899	30-Aug-2004	6,879,535	12-Apr-2005	Perisetty, Srinivas
Redundant Column Read in a Memory Array	US	11/131,017	17-May-2005	7,296,196	13-Nov-2007	Perisetty, Srinivas
Channel Discharging After Erasing Flash Memory Devices	US	11/190,722	27-Jul-2005	7,397,699	08-Jul-2008	Trinh, Stephen P
Column/Sector Redundancy CAM Fast Programming Scheme Using Regular Memory Core Array in Mulit-Plane Flash Memory Device	US	11/295,878	07-Dec-2005	7,196,952	27-Mar-2007	Trinh, Stephen P

A Method For Preventing Over-Erasing of Unused Redundt Memory Cells in a Flash Memory Having Single-Transistor Memory Cells	US	11/553,393	26-Oct-2006	7,457,167	25-Nov-2008	Patrascu, Dinu; Ho, On-Pong R.; Kuo (W), Wei-Yen
Device and Method for Access Time Reduction by Speculatively Decoding Non-Memory Read Commands on a Serial Interface	US	11/566,555	04-Dec-2006	7,769,909	03-Aug-2010	Ho, On-Pong R.; Nguyen, Dixie; Patrascu, Dinu
A New Implementation of Column Redundancy for a Flash Memory With a High Write Parallelism	US	11/611,452	15-Dec-2006	7,551,498	23-Jun-2009	Bartoli, Simone; Surico, Stefano; Sacco, Andrea; Mostola, Maria
A New Implementation of Column Redundancy for a Flash Memory With a High Write Parallelism	TW	096143993	20-Nov-2007			Bartoli, Simone; Surico, Stefano; Sacco, Andrea; Mostola, Maria
A New Implementation of Column Redundancy for a Flash Memory With a High Write Parallelism	CN	2007-80046296.9	12-Nov-2007			Bartoli, Simone; Surico, Stefano; Sacco, Andrea; Mostola, Maria
Ultra-Deep Power-Down Mode for Memory Devices	US	13/559,320	26-Jul-2012			DeCaro, Richard, Manea, Danut, Wang, Bill, Trinh, Stephen; Hill, Paul