PATENT ASSIGNMENT COVER SHEET

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
STRATEGIC GLOBAL ADVISORS OF OREGON, INC.	04/22/2015

RECEIVING PARTY DATA

Name:	TESSERA ADVANCED TECHNOLOGIES, INC.
Street Address:	3025 ORCHARD PARKWAY
City:	SAN JOSE
State/Country:	CALIFORNIA
Postal Code:	95134

PROPERTY NUMBERS Total: 29

Property Type	Number
Patent Number:	7033932
Patent Number:	7186639
Patent Number:	7514793
Patent Number:	7247917
Patent Number:	7214581
Patent Number:	7521771
Patent Number:	7361583
Patent Number:	7071054
Patent Number:	7247533
Patent Number:	7326645
Patent Number:	7344992
Patent Number:	7071057
Patent Number:	7314831
Patent Number:	7575980
Patent Number:	7839006
Patent Number:	7482692
Patent Number:	7465629
Patent Number:	7952133
Patent Number:	7602236
Patent Number:	7642659

Property Type	Number
Patent Number:	7849436
Patent Number:	7869175
Patent Number:	8117582
Patent Number:	8008966
Patent Number:	7944195
Patent Number:	7940075
Patent Number:	8040118
Patent Number:	8441246
Patent Number:	7978010

CORRESPONDENCE DATA

Fax Number:

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ATTORNEY DOCKET NUMBER:	ACQ-DONGB2:STRATEGIC-TATI
NAME OF SUBMITTER:	JENNIFER KOSTIC
SIGNATURE:	/Jennifer Kostic/
DATE SIGNED:	05/12/2015

Total Attachments: 11
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DEED OF ASSIGNMENT

THIS DEED OF ASSIGNMENT ("**Assignment**"), EFFECTIVE AS OF April 1, 2015, IS MADE BY AND BETWEEN

Strategic Global Advisors of Oregon, Inc. (hereinafter "**ASSIGNOR**"), an Oregon corporation having a place of business at 15320 SE Baron Loop, Happy Valley, OR 97086; and

Tessera Advanced Technologies, Inc. (hereinafter "**BUYER**"), a Delaware corporation having a place of business at 3025 Orchard Parkway, San Jose, California 95134.

WHEREAS:

A **ASSIGNOR** is the sole owner in respect of the patents and patent applications listed in the attached Appendix (hereinafter "the **PATENTS**"); and

B **BUYER** is desirous of acquiring all of the worldwide right, title and interest in and to the **PATENTS** and the inventions disclosed therein.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, **ASSIGNOR** has sold, assigned and transferred, and does hereby sell, assign and transfer to **BUYER** all of the worldwide right, title and interest in (i) the **PATENTS** and the inventions and improvements disclosed therein; (ii) all reissues, divisionals, continuations, continuations-in-part, extensions, renewals, reexaminations and foreign counterparts thereof, and other patents, patent applications, certificates of invention other governmental grants resulting from the **PATENTS**; (iii) all patents and applications which claim priority to or have common disclosure or common priority with any such patents or patent applications, and (iv) all rights corresponding to any of the foregoing throughout the world (including the right to claim the priority date of any of the **PATENTS** and the right to sue for and recover damages for any past, present or future infringement of the Patents, and including all benefits, privileges and powers), the same to be held and enjoyed by **BUYER** for its own use and enjoyment, and for the use and enjoyment of its successors, assigns and other legal representatives, to the end of the term or terms of said **PATENTS** granted or reissued or reexamined as fully and entirely as the same would have been held and enjoyed by **ASSIGNOR**, if this assignment and sale had not been made.

IN WITNESS WHEREOF, **ASSIGNOR** has caused these presents to be signed by its duly appointed officer having full authority to convey its property.

And if the issue date and/or patent number of any of the **PATENTS** is unknown to **ASSIGNOR** and **BUYER** at the time this Assignment is executed, **ASSIGNOR** does hereby authorize its attorneys to insert on this Assignment the issue date and patent number of said any patent when known.

ASSIGNOR hereby declares that **BUYER** may take the steps for recordal of this assignment in the sole name of **BUYER**.

ASSIGNOR hereby undertakes that it shall, without further consideration, but at the expense of **BUYER**, execute all documents and do all such acts and things as **BUYER** may in its absolute discretion consider necessary or desirable to enable Letters Patent or any other form of protection to be issued in respect of any of said **PATENTS** and the inventions disclosed therein in any part of the world and to enable or to assist **BUYER** to defend oppositions thereto, to maintain the **PATENTS** and to prosecute for the infringement thereof.

SIGNED for and on behalf of **ASSIGNOR**

By _____ on April 22, 2015
(Signature) (Date)

Daniel P Morris, CEO
(Print Name and Title)

A notary public or other officer completing this certificate verifies only the identity of the individual who signed the document to which this certificate is attached, and not the truthfulness, accuracy, or validity of that document.

State of California)
County of Santa Clara)

On April 22, 2015 before me, Jennifer Kostic, Notary Public
(Name of Notary Public)

personally appeared Daniel Morris
who proved to me on the basis of satisfactory evidence to be the person(s)whose name(s) is/are subscribed to the within instrument and who acknowledged to me that he/she/they executed the same in his/her/their authorized capacity(ies),and that by his/her/their signature(s) on the instrument the person(s), or entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY of PERJURY under the laws of the state of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal

_____ (SEAL)

JENNIFER KOSTIC
Commission # 1934890
Notary Public - California
Santa Clara County
My Comm. Expires Jun 1, 2015

SIGNED for and on behalf of **BUYER**

By _____ on May 8, 2015
(Signature) (Date)

Paul Davis, SVP and General Counsel
(Print Name and Title)

A notary public or other officer completing this certificate verifies only the identity of the individual who signed the document to which this certificate is attached, and not the truthfulness, accuracy, or validity of that document.

State of California)
County of Santa Clara)

On May 8, 2015 before me, Karen A. Perricone, Notary Public
(Name of Notary Public)

personally appeared Paul Davis

who proved to me on the basis of satisfactory evidence to be the person(s)whose name(s) is/are subscribed to the within instrument and who acknowledged to me that he/she/they executed the same in his/her/their authorized capacity(ies),and that by his/her/their signature(s) on the instrument the person(s), or entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY of PERJURY under the laws of the state of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal

_____ (SEAL)

KAREN A. PERRICONE
Commission # 2065518
Notary Public - California
Santa Clara County
My Comm. Expires May 18, 2018

APPENDIX – LISTED PATENTS AND PATENT APPLICATIONS

Date Format (MM/DD/YYYY)

1. United States Listed Issued Patents

US Issued Patents

Patent Number	Filing Date	Application Number	Issue Date	Publication Number	Title
7033932	08/16/2004	10/919,954	04/25/2006	20050048750	Method for fabricating a semiconductor device having salicide
7071054	12/31/2004	11/027,524	07/04/2006	20050142737	Methods of fabricating MIM capacitors in semiconductor devices
7071057	12/30/2004	11/027,312	07/04/2006	20050170583	Methods of fabricating MIM capacitors of semiconductor devices
7186639	12/10/2004	11/009,723	03/06/2007	20050127510	Metal interconnection lines of semiconductor devices and methods of forming the same
7214581	12/23/2004	11/019,300	05/08/2007	20050142744	Method of fabricating flash memory device
7247533	12/30/2004	11/024,660	07/24/2007	20050142790	Method of fabricating semiconductor device using selective epitaxial growth
7247917	12/27/2004	11/023,314	07/24/2007	20050139896	Nonvolatile semiconductor memory devices and methods of manufacturing the same
7314831	08/11/2005	11/201,203	01/01/2008	20060035461	Copper line of semiconductor device and method for forming the same
7326645	12/30/2004	11/027,533	02/05/2008	20050142864	Methods for forming copper interconnect of semiconductor devices
7344992	12/30/2004	11/024,685	03/18/2008	20050158987	Method for forming via hole and trench for dual damascene interconnection
7361583	07/25/2003	10/627,057	04/22/2008	20040067610	RF semiconductor devices and methods for fabricating the same
7465629	11/09/2006	11/595,522	12/16/2008	20070105311	Flash memory and method for manufacturing the same
7482692	12/30/2005	11/320,698	01/27/2009	20070102824	Tungsten plug structure of semiconductor device and method for forming the same

Patent Number	Filing Date	Application Number	Issue Date	Publication Number	Title
7514793	12/04/2006	11/633,697	04/07/2009	20070075429	Metal interconnection lines of semiconductor devices and methods of forming the same
7521771	12/30/2004	11/024,748	04/21/2009	20050139865	Method for fabricating a semiconductor device
7575980	12/21/2005	11/312,595	08/18/2009	20060138673	Semiconductor device and method for manufacturing the same
7602236	12/27/2006	11/645,530	10/13/2009	20070146059	Band gap reference voltage generation circuit
7642659	09/11/2007	11/853,547	01/05/2010	20080073791	Wire pad of semiconductor device
7839006	07/20/2009	12/458,682	11/23/2010	20100019353	Semiconductor device and method for manufacturing the same
7849436	08/13/2007	11/889,384	12/07/2010	20080038847	Method of forming dummy pattern
7869175	10/11/2007	11/870,902	01/11/2011	20080157204	Device for protecting semiconductor IC
7940075	11/09/2009	12/614,835	05/10/2011	20100117688	Differential pre-emphasis driver
7944195	12/14/2008	12/334,498	05/17/2011	20090160419	Start-up circuit for reference voltage generation circuit
7952133	11/13/2008	12/270,803	05/31/2011	20090072293	Flash memory and method for manufacturing the same
7978010	12/17/2009	12/640,993	07/12/2011	20100164626	Boost operational amplifier
8008966	10/30/2008	12/262,057	08/30/2011	20090140714	Start-up circuit for generating bandgap reference voltage
8040118	12/10/2009	12/635,570	10/18/2011	20100156364	Low-dropout voltage regulator with level limiter limiting level of output voltage when level of load current changes and method of operating the same

Patent Number	Filing Date	Application Number	Issue Date	Publication Number	Title
8117582	07/30/2008	12/183,036	02/14/2012	20090044164	Method for placing dummy patterns in a semiconductor device layout
8441246	12/09/2009	12/634,218	05/14/2013	20100156387	Temperature independent reference current generator using positive and negative temperature coefficient currents

US Pending Applications
None.

2. Foreign Listed Issued Patents and Pending Patent Applications

Foreign Issued Patents

Patent Number	Country	Filing Date	Application Number	Issue Date	Publication Number	Title
ZL20081 0189406. 3	CN	12/24/2008	200810189406 .3	02/29/2012	101470456	Start-up circuit for reference voltage generation circuit
4878361	JP	12/08/2008	2008-311993	12/09/2011	2009-153120	Starting circuit for reference voltage generating circuit
559572	KR	09/01/2003	2003-60925	03/03/2006	2005023650	Method For Fabricating Semiconductor Device Having Salicide
562318	KR	12/26/2003	2003-97919	03/13/2006	2005066611	Nonvolatile Semiconductor Memory Device And Manufacturing Method Thereof
572829	KR	12/31/2003	2003-102046	04/14/2006	2005069705	Method Of Fabricating Semiconductor Device With Mim Capacitor
577308	KR	12/29/2004	2004-114798	04/28/2006		Semiconductor Device And Method For Manufacturing The Same
579846	KR	12/11/2003	2003-90328	05/08/2006	2005058079	A Metal Layer Of Semiconductor Device, And A Method Thereof
587655	KR	12/31/2003	2003-102072	06/01/2006	2005071153	Method For Manufacturing Semiconductor Device Using Selective Epitaxial Growth
598294	KR	12/31/2003	2003-101322	06/30/2006	2005069334	Method For Forming Copper Line Using Dual Damascene
602082	KR	12/27/2003	2003-98358	7/10/2006	2005066874	Method For Fabricating A Flash Memory Device
602085	KR	12/31/2003	2003-101929	07/10/2006	2005069651	Semiconductor Device And Manufacturing Method Thereof
613375	KR	08/13/2004	2004-64022	08/09/2006	2006015172	Cu Line Of Semiconductor Device And Formation Method Thereof

Patent Number	Country	Filing Date	Application Number	Issue Date	Publication Number	Title
698101	KR	10/05/2005	2005-93463	03/15/2007		Tungsten Plug Structure Of Semiconductor Device And Method For Forming The Same
769152	KR	09/25/2006	2006-92886	10/16/2007		Wire Pad Of Semiconductor Device
788346	KR	12/28/2005	2005-132609	12/17/2007	2007069936	Band Gap Reference Voltage Generation Circuit
789614	KR	08/11/2006	2006-76189	12/20/2007		Dummy Pattern And Method For Forming The Same
831269	KR	12/29/2006	2006-137353	05/15/2008		Device For Protecting Semiconductor ICs From Electrostatic Discharge
847844	KR	8/10/2007	2007-80570	7/16/2008		Method Of Designing A Dummy Pattern For A Semiconductor Device
907893	KR	12/24/2007	2007-136467	7/8/2009	2009068728	Starting Circuit For The Reference Voltage Generating Circuit, Which Can Generate The Voltage Having The Fixed Level
940150	KR	12/3/2007	2007-124439	1/26/2010	2009057733	A Strat-Up Circuit For Bandgap Reference Voltage Generation
1024817	KR	11/12/2008	2008-112040	3/17/2011	2010053069	Differential Pre-Emphasis Driver
1483941	KR	12/24/2008	2008-132840	1/13/2015	2010074420	Apparatus For Generating The Reference Current Independent Of Temperature

Foreign Pending Applications

Country	Filing Date	Application Number	Publication Number	Title
KR	12/24/2008	2008-132841	2010074421	Low-Dropout Voltage Regulator, And Operating Method Of The Regulator
KR	12/29/2008	2008-135851	2010077804	Boost Operational Amplifier

3. US and Foreign Listed Abandoned/Expired Patents and Applications

Patent Number	Country	Filing Date	Application Number	Issue Date	Publication Number	Title
	US	03/10/2008	12/075,338		20080157391	RF Semiconductor Devices And Methods For Fabricating The Same
	US	03/10/2009	12/401,373		20090174004	Semiconductor Device And Fabricating Method Thereof
	CN	08/10/2007	200710149468		101123203	Method Of Forming Dummy Pattern
	CN	12/06/2007	200710194795		101211910	Device For Protecting Semiconductor IC
	CN	08/07/2008	200810145360		101364595	Semiconductor Device Layout And Method For Placing Dummy Patterns Therein
	CN	11/12/2009	200910208380		101741360	Differential Pre-Emphasis Driver
	CN	12/28/2009	200910215547		101882916	Boost Operational Amplifier
	CN	12/22/2009	200910254355		101763131	Low-Dropout Voltage Regulator And Operating Method Of The Same
	CN	12/17/2009	200910260393		101763135	Temperature Independent Type Reference Current Generating Device
	KR	07/26/2002	2002-44084		2004011016	Method For Manufacturing RF Semiconductor Device
529637	KR	12/31/2003	2003-101800	11/11/2005	2005071024	Method For Fabricating The Via Hole And Trench For Dual Damascene Interconnection
545219	KR	12/31/2003	2003-101801	01/16/2006	2005069587	Method For Fabricating The Via Hole And Trench For Dual Damascene Interconnection

Patent Number	Country	Filing Date	Application Number	Issue Date	Publication Number	Title
	KR	11/09/2005	2005-106813		2007049731	Flash Memory And Manufacturing Method Thereof
I370535	TW	10/17/2007	96138908	8/11/2012	200828557	Device For Protecting Semiconductor IC
	TW	11/05/2008	97142762		200926593	Start-Up Circuit For Generating Bandgap Reference Voltage
I375873	TW	12/10/2008	97148103	11/1/2012	200928657	Start-Up Circuit For Reference Voltage Generation Circuit
	TW	11/11/2009	98138320		201019617	Differential Pre-Emphasis Driver
	TW	12/16/2009	98143203		201024954	Temperature Independent Type Reference Current Generating Device
	TW	12/16/2009	98143215		201024951	Low-Dropout Voltage Regulator And Operating Method Of The Same
	TW	12/16/2009	98143219		201025834	Boost Operational Amplifier