

<b>PATENT ASSIGNMENT COVER SHEET</b>
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Electronic Version v1.1  
 Stylesheet Version v1.2

EPAS ID: PAT3362849

<b>SUBMISSION TYPE:</b>	NEW ASSIGNMENT
<b>NATURE OF CONVEYANCE:</b>	RELEASE OF SECURITY INTEREST

**CONVEYING PARTY DATA**

Name	Execution Date
AMERICAN CAPITAL, LTD.	05/15/2015
STILL RIVER FUND III, LIMITED PARTNERSHIP	05/15/2015
SARAH G. KURZON 2001 REVOCABLE TRUST	05/15/2015
OVONYX, INC.	05/15/2015
DONALD PERRIN	05/15/2015
RUNNING DEER FOUNDATION	05/15/2015
RUNNING DEER TRUST	05/15/2015

**RECEIVING PARTY DATA**

<b>Name:</b>	CONTOUR SEMICONDUCTOR, INC.
<b>Street Address:</b>	85 RANGEWAY ROAD
<b>Internal Address:</b>	BLDG 1
<b>City:</b>	N. BILLERICA
<b>State/Country:</b>	MASSACHUSETTS
<b>Postal Code:</b>	01862

**PROPERTY NUMBERS Total: 47**

Property Type	Number
Patent Number:	5673218
Patent Number:	5889694
Patent Number:	RE41733
Patent Number:	RE42310
Patent Number:	6586327
Patent Number:	7183206
Patent Number:	7507663
Patent Number:	6598164
Patent Number:	6956757
Patent Number:	7460384
Patent Number:	7593246
Patent Number:	7826244
Patent Number:	8358525

PATENT

Property Type	Number
Patent Number:	7149934
Patent Number:	8108735
Patent Number:	7376008
Patent Number:	7652916
Patent Number:	7916530
Patent Number:	7548454
Patent Number:	7593256
Patent Number:	7548453
Patent Number:	7667996
Patent Number:	7813157
Patent Number:	7933133
Patent Number:	8116109
Patent Number:	8000129
Patent Number:	7682981
Patent Number:	8358526
Patent Number:	8351238
Patent Number:	8325556
Patent Number:	8325557
Patent Number:	8035416
Patent Number:	8526217
Patent Number:	8455298
Patent Number:	8773881
Patent Number:	8451024
Patent Number:	8635426
Patent Number:	8934293
Patent Number:	8537618
Patent Number:	8776227
Patent Number:	8786023
Application Number:	13714499
Application Number:	12924167
Application Number:	12930655
Application Number:	13199437
Application Number:	13385371
Application Number:	61725620

**CORRESPONDENCE DATA**

**Fax Number:**

*Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.*

**PATENT**

**REEL: 035749 FRAME: 0957**

**Email:** cthomas@pattersonsheridan.com,  
SVerSteeg@pattersonsheridan.com  
**Correspondent Name:** STEVEN H. VERSTEEG  
**Address Line 1:** 24 GREENWAY PLAZA  
**Address Line 2:** SUITE 1600  
**Address Line 4:** HOUSTON, TEXAS 77046

<b>ATTORNEY DOCKET NUMBER:</b>	PROJECT LION
<b>NAME OF SUBMITTER:</b>	STEVEN H. VERSTEEG
<b>SIGNATURE:</b>	/Steven H. VerSteeg/
<b>DATE SIGNED:</b>	05/20/2015

**Total Attachments: 9**

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**RELEASE OF SECURITY INTEREST IN PATENTS**

**THIS RELEASE OF SECURITY INTEREST IN PATENTS** (this “**Release**”) is made as of May 15, 2015 (“**Effective Date**”) by and among Contour Semiconductor, Inc., a Delaware corporation, with a principal office located at 85 Rangeway Road, Bldg. 1, N. Billerica, MA 01862 (the “**Grantor**”) and the undersigned grantees (“**Grantees**”).

**WHEREAS**, pursuant to the terms and conditions of those certain Security Agreements (the “**Security Agreements**”) dated January 18, 2013 and June 20, 2014, respectively (as the same may have been amended, modified, extended or restated from time to time) to which Grantor and Grantees were parties, Grantor and Grantees entered into those certain Grants of Security Interest in U.S. Patents, also executed on January 18, 2013 and June 20, 2014, respectively (the “**Patent Security Agreements**”) (it being acknowledged that only some, but not all, of the Grantees were parties to the Security Agreement dated January 18, 2013 and the related Patent Security Agreement);

**WHEREAS**, pursuant to the terms and conditions of the Patent Security Agreements, and the Security Agreements, Grantor granted to Grantees a continuing security interest in and to, and lien on, all of Grantor’s right, title and interest in, to and under certain Patents (as defined in the Patent Security Agreements), including, without limitation, the patents set forth on Schedule A attached hereto (the “**Patents**”);

**WHEREAS**, the Patent Security Agreements were recorded with the U.S. Patent and Trademark Office (“**USPTO**”) on January 18, 2013 at Reel/Frame 29659-615 and on June 20, 2014 at Reel/Frame 33204-428, respectively; and

**WHEREAS**, Section 11 of each Security Agreement provides that any provision of such Security Agreement may be amended or modified with the prior written consent of the Majority Holders (as defined in each Security Agreement, respectively);

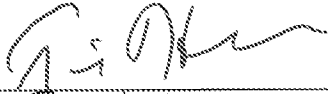
**WHEREAS**, the undersigned Grantees, constituting the Majority Holders under the Security Agreements, desire to, on behalf of all Grantees, terminate all the security interests granted pursuant to the Security Agreements and the Patent Security Agreements, and to execute and deliver to Grantor all deeds, assignments and other instruments as may be reasonably necessary to release the security interests relating to the Patents granted pursuant to the Security Agreements and the Patent Security Agreements.

**NOW, THEREFORE**, for and in consideration of the foregoing, and other good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, Grantees hereby confirm that they have terminated the Patent Security Agreements and the Security Agreements, and relinquish unto Grantor the continuing security interest in, and lien on, the Patents granted pursuant to the Security Agreements and the Patent Security Agreements and, in furtherance of (and for purposes of only) the foregoing, otherwise assign, grant and convey to Grantor, without recourse, any and all right, title and interest the Grantees may have in, to or under to the Patents in order to revest in Grantor full and unencumbered title to said Patents.

[Signature page follows.]

IN WITNESS WHEREOF, Grantees have caused this Release of Security Interest in Patents to be executed by their duly authorized signatories as of the date first written above.

AMERICAN CAPITAL, LTD.

By:   
Name: Tim Hudman  
Title: Vice President

*[Signatures continue on the next page.]*

[Signature Page to Release of Security Interest in Patents]

**IN WITNESS WHEREOF**, Grantees have caused this Release of Security Interest in Patents to be executed by their duly authorized signatories as of the date first written above.

**STILL RIVER FUND III, LIMITED PARTNERSHIP**

By: Still River Fund III GP, LP  
Its: General Partner

By: James Sealfield  
Name: TAMES SEALFIELD  
Title: mg. Gen. Ptn.

*[Signatures continue on the next page.]*

[Signature Page to Release of Security Interest in Patents]

IN WITNESS WHEREOF, Grantees have caused this Release of Security Interest in Patents to be executed by their duly authorized signatories as of the date first written above.

**SARAH G. KURZON 2001 REVOCABLE TRUST**

By: *Sarah G. Kurzon*  
Name: *SARAH G. KURZON*  
Title: *TRUSTEE*

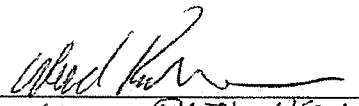
*[Signatures continue on the next page.]*

*[Signature Page to Release of Security Interest in Patents]*

**PATENT**  
**REEL: 035749 FRAME: 0962**

IN WITNESS WHEREOF, Grantees have caused this Release of Security Interest in Patents to be executed by their duly authorized signatories as of the date first written above.

OVONYX, INC.

By:   
Name: WARD PARKINSON  
Title: V.P.

[Signatures continue on the next page.]

[Signature Page to Release of Security Interest in Patents]



**IN WITNESS WHEREOF**, Grantees have caused this Release of Security Interest in Patents to be executed by their duly authorized signatories as of the date first written above.

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Donald Perrin

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[Signature Page to Release of Security Interest in Patents]

**PATENT**  
**REEL: 035749 FRAME: 0964**

**IN WITNESS WHEREOF**, Grantees have caused this Release of Security Interest in Patents to be executed by their duly authorized signatories as of the date first written above.

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**RUNNING DEER FOUNDATION**

By: \_\_\_\_\_  
Name: Edward Bedrosian  
Title: Trustee

**RUNNING DEER TRUST**

By: \_\_\_\_\_  
Name: Edward Bedrosian  
Title: Trustee

Schedule A

**ISSUED PATENTS**

<u>Patent No.</u>	<u>Issue Date</u>	<u>Title</u>
5,673,218	09/30/1997	Dual-Addressed Rectifier Storage Device
5,889,694	03/30/1999	Dual-Addressed Rectifier Storage Device
RE41,733	09/21/2010	Dual-Addressed Rectifier Storage Device
RE42,310	04/26/2011	Dual-Addressed Rectifier Storage Device
6,586,327	07/01/2003	Fabrication of Semiconductor Devices
7,183,206	02/27/2007	Fabrication of Semiconductor Devices
7,507,663	03/24/2009	Fabrication of Semiconductor Devices
ZL01819463X	01/01/1900	Fabrication of Semiconductor Devices
6,598,164	07/22/2003	Device & Method for Reducing Piracy of Digitized Information
6,956,757	10/18/2005	Low Cost High Density Rectifier Matrix Memory
7,460,384	12/02/2008	Low Cost High Density Rectifier Matrix Memory
7,593,246	09/22/2009	Low Cost High Density Rectifier Matrix Memory
7,826,244	11/02/2010	Low Cost High Density Rectifier Matrix Memory
8,358,525	01/22/2013	Low Cost High Density Rectifier Matrix Memory
7,149,934	12/12/2006	Error Correcting Memory Access Means and Method
8,108,735	01/31/2012	Error Correcting Memory Access Means and Method
7,376,008	05/20/2008	SCR Matrix Storage Device
7,652,916	01/26/2010	SCR Matrix Storage Device
7,916,530	03/29/2011	SCR Matrix Storage Device
7,548,454	06/16/2009	Memory Array with Readout Isolation
7,593,256	09/22/2009	Memory Array with Readout Isolation
7,548,453	06/16/2009	Memory Array with Readout Isolation
7,667,996	02/23/2010	Nano-Vacuum Tubes and their Application in Storage Devices
7,813,157	10/12/2010	Non-Linear Conductor Memory
7,933,133	04/26/2011	Low Cost, High-Density Rectifier Matrix Memory
8,116,109	02/14/2012	Low-Cost High Density Rectifier Matrix Memory
8,000,129	08/16/2011	Field-Emitter-Based Memory Array with Phase-Change Storage Devices
7,682,981	03/23/2010	Topography Transfer Method with Aspect Ratio Scaling
8,358,526	01/22/2013	Diagonal Connection Storage Array

8,351,238	01/08/2013	Low-Complexity Electronic Circuits & Methods for Forming the Same
8,325,556	12/04/2012	Sequencing Decoder Circuit
8,325,557	12/04/2012	Methods and Apparatus for Disabling a Memory-Array Portion
8,035,416	10/11/2011	Bipolar-MOS Driver Circuit
8,526,217	09/03/2013	Low-Complexity Electronic Circuits & Methods for Forming the Same
8,455,298	06/04/2013	Method for Forming Self-aligned Phase-Change Semiconductor Diode Memory
8,773,881	07/08/2014	Vertical Switch Three-Dimensional Memory Array
8,451,024	05/28/2013	Bipolar-MOS Driver Circuit
8,635,426	01/21/2014	Diagonally Accessed Memory Array Circuit
8,934,293	01/13/2015	Means and Method for Operating a Resistive Array
8,537,618	09/17/2013	RAM Memory Device with Nand Type Interface
8,766,227	07/01/2014	PINCHED CENTER RESISTIVE CHANGE MEMORY CELL (NUP-052US)
8,786,023	07/22/2014	EMBEDDED NON-VOLATILE MEMORY

#### **PENDING PATENTS**

<u>Applctn No.</u>	<u>Filing Date</u>	<u>Title</u>
13/714,499	12/14/2012	Bipolar-CMOS Driver Circuit
12/924,167	09/22/2010	Method of Phase Change Memory Programming
12/930,655	01/13/2011	Diode Polarity for Diode Array
13/199,437	08/30/2011	UNIFIED SWITCH ARRAY FOR MEMORY DEVICES
13/385,371	02/15/2012	CURRENT STEERING ELEMENT FORMATION FOR MEMORY CELLS (NUP-055US)
61/725,620	11/13/2012	Solid State Devices Having Fine Pitch Structures