PATENT ASSIGNMENT COVER SHEET

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
SPANSION LLC	07/31/2013

RECEIVING PARTY DATA

Name:	VALLEY DEVICE MANAGEMENT
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PROPERTY NUMBERS Total: 3

Property Type	Number
Patent Number:	5815438
Patent Number:	5995417
Patent Number:	6175522

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ATTORNEY DOCKET NUMBER:	SPANSION-VDM ASSIGNMENT
NAME OF SUBMITTER:	DANIEL G. HARRIS
SIGNATURE:	/Daniel G. Harris/
DATE SIGNED:	06/24/2015

Total Attachments: 7
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EXHIBIT A - ASSIGNMENT OF PATENT RIGHTS

This patent assignment (this "**Assignment**") is entered into as of the date set forth below by and between Spansion, Inc. a company organized under the laws of the United States with a principal place of business at 915 DeGuigne Sunnyvale, CA 94088-3453 ("**Assignor**"), and Valley Device Management, a Delaware corporation with principal place of business at Corporation Trust Center, 1209 Orange Street, Wilmington, DE 19801 ("**Assignee**").

Whereas, the Assignor and Assignee have entered into a certain Patent Purchase Agreement dated July 31, 2013 under which, among other things, Assignor assigns to Assignee all right, title and interest in and to the Patents (as defined below).

For good and valuable consideration, the receipt of which is hereby acknowledged, Assignor, does hereby irrevocably sell, assign, transfer, and convey unto Assignee, or Assignee's designees, all of Assignor's right title and interest in and to all of the following (collectively, the "**Assigned Patent Rights**"):

(a) all provisional patent applications, patent applications, and patents listed in the attached Appendix (the "**Patents**");

(b) all provisional patent applications, patent applications, patents or other similar governmental grants or issuances worldwide (i) from which any of the Patents directly or indirectly claims priority and/or (ii) for which any of the Patents directly or indirectly forms a basis for priority ;

(c) any reissues, reexaminations, extensions, continuations, continuations in part, continuing prosecution applications, requests for continuing examinations, and divisions, worldwide, of any provisional patent application, patent application, patent or other governmental grant or issuance set forth in clauses (a) and/or (b) (clauses (a) through (c), excluding any subject matter that is not disclosed in the Patents(collectively, the "**Assigned Patents**");

(d) foreign patents, patent applications, and counterparts relating to any item in the foregoing categories (a) through (c), including, without limitation, certificates of invention, utility models, industrial design protection, design patent protection, and other governmental grants or issuances;

(e) items in any of the foregoing in categories (a) through (d), whether or not expressly listed as Patents below, except with respect to claims in any of the foregoing that have been rejected, withdrawn, cancelled, or the like;

(f) rights to all inventions described in any item in the foregoing categories (a) through (e) and all other rights arising out of such inventions, to the extent disclosed in the Patents;

(g) rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections, or other governmental grants or issuances of any type related to any item in the foregoing categories (a) through (f), including, without limitation, under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement, or understanding;

(h) any causes of action (whether currently pending, filed or otherwise)and all other enforcement rights and rights to remedies under, on account of, or related to any of the Patents and/or any item in any of the foregoing categories (a) through (g), including, without limitation, all causes of action and other enforcement rights for (i) damages, (ii) injunctive relief, and (iii) other remedies of any kind for past, current and future infringement, misappropriation or violation of rights and all rights to sue for any of the foregoing;

(i) all rights to collect royalties and other payments under or on account of any of the Patents and/or any item in the foregoing categories (b) through (h); subject to covenants not to sue and licenses granted by Assignor or its Affillates to third parties prior to the Assignment Date and

(j) any and all other rights and interests worldwide, arising out of the Assigned Patents.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Assigned Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

The terms and conditions of this Assignment will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

In witness whereof, intending to be legally bound, the Parties have executed this Assignment as of the Assignment

Date.

ASSIGNOR

Spansion, LLC.

By: _____

Name: Scot Griffin

Title: SVP, General Counsel

Date:

Appendix to Assignment of Patent Rights

Family	Country	Patent #	Application #	Patent Title
1	US	5815438	08/810,170	OPTIMIZED BIASING SCHEME FOR NAND READ AND HOT-CARRIER WRITE OPERATIONS
2	DE	69904856.7	99950160.4	SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON -VOLATILE MEMORY ARRAY
2	EP	1125302		A SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON-VOLATILE MEMORY ARRAY
2	FR	1125302	99950160.4	SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON -VOLATILE MEMORY ARRAY
2	GB	1125302	99950160.4	SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON -VOLATILE MEMORY ARRAY
2	JP		2002-528841	Scheme for page erase and erase verify in a non-volatile memory array
2	KR	564378	7004996/2001	SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON -VOLATILE MEMORY ARRAY
2	TW	142628	88118017	SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON -VOLATILE MEMORY ARRAY
2	US	5995417	09/175,646	SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON -VOLATILE MEMORY ARRAY
2	WO	WO0024002		A SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON-VOLATILE MEMORY ARRAY
3	US	6181605	09/414,750	GLOBAL ERASE/PROGRAM VERIFICATION APPARATUS AND METHOD
4	US	6240020	09/427,406	METHOD OF BITLINE SHIELDING IN CONJUNCTION WITH A PRECHARGING SCHEME FOR NAND-BASED FLASH MEMORY DEVICES
5	US	6269025	09/500,699	Memory system having a program and erase voltage modifier
6	US	6295228	09/514,933	System for programming memory cells
7	US	6307783	09/794,485	Descending staircase read technique for a multilevel cell NAND flash memory device
8	US	6504757	09/922,415	DOUBLE BOOSTING SCHEME FOR NAND TO IMPROVE PROGRAM INHIBIT CHARACTERISTICS
9	US	7154769	11/052,689	MEMORY DEVICE INCLUDING BARRIER LAYER FOR IMPROVED SWWITCHING SPEED AND DATA RETENTION
9	WO	WO2006086248		MEMORY DEVICE INCLUDING BARRIER LAYER FOR IMPROVED SWITCHING SPEED AND DATA RETENTION
10	TW	I222071	90103881	INTERLACED MULTI-LEVEL MEMORY
10	US	6707713	09/516,478	INTERLACED MULTI-LEVEL MEMORY
10	WO	WO0167462		INTERLACED MULTI-LEVEL MEMORY
11	US	6728913	09/513,698	DATA RECYCLING IN MEMORY
12	US	6996004	10/700,414	MINIMIZATION OF FG-FG COUPLING IN FLASH MEMORY

PATENT
REEL: 035961 FRAME: 0488

13	EP	1239488		MEMORY DEVICE FOR CONTROLLING NONVOLATILE AND VOLATILE MEMORIES
13	JP	4017177	2002-4150	Memory Device
13	US	7266664	10/077,778	MEMORY DEVICE FOR CONTROLLING NONVOLATILE AND VOLATILE MEMORIES
14	JP	4672673	2006-546540	SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING SAID SEMICONDUCTOR DEVICE
14	US	7286398	11/290,002	SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING SAID SEMICONDUCTOR DEVICE
14	WO	2006059374		SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING SAID SEMICONDUCTOR DEVICE
15	US	7342830	11/332,263	PROGRAM AND PROGRAM VERIFY OPERATIONS FOR FLASH MEMORY
16	JP	4896011	2007-512381	SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME
16	US	7362620	11/394,491	SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME
16	WO	2006106577		SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME
17	TW	I342024	96124086	Nonvolatile storage and erase control method thereof
17	US	7564720	11/879,989	NONVOLATILE STORAGE AND ERASE CONTROL
17	WO	2008010258		NONVOLATILE STORAGE DEVICE AND ITS ERASE CONTROL METHOD
18	JP	4871280	2007-533065	Semiconductor device and fabrication method therefor
18	US	7626253	11/514,390	NONVOLATILE STORAGE AND ERASE CONTROL
18	US	7859096	12/624,117	SEMICONDUCTOR DEVICE
18	US	8329562	12/965,706	METHODS OF MAKING A SEMICONDUCTOR DEVICE
18	US	8330263	12/965,672	SEMICONDUCTOR DEVICE
18	US		13/711,443	SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFORE
18	WO	2007026392		SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING SAME
19	US	7675776	11/963,286	BIT MAP CONTROL OF ERASE BLOCK DEFECT LIST IN A MEMORY
20	JP		2008117505	SEMICONDUCTOR DEVICE AND ITS CONTROL METHOD
20	TW		200901197	SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREOF
20	US	7706186	11/982,864	CONTROLLING A SEMICONDUCTOR DEVICE
20	WO	2008057498		CONTROLLING A SEMICONDUCTOR DEVICE
21	US	7743203	11/747,608	MANAGING FLASH MEMORY BASED UPON USAGE HISTORY
22	US	7761740	11/955,934	POWER SAFE TRANSLATION TABLE OPERATION IN FLASH MEMORY

23	US	7602639	11/957,309	READING ELECTRONIC MEMORY UTILIZING RELATIONSHIPS BETWEEN CELL STATE DISTRIBUTIONS
23	US	7869281	12/550,642	READING ELECTRONIC MEMORY UTILIZING RELATIONSHIPS BETWEEN CELL STATE DISTRIBUTIONS
24	TW	200926201	97139850	TAMPER REACTIVE MEMORY DEVICE TO SECURE DATA FROM TAMPER ATTACKS
24	US	7945792	11/873,980	TAMPER REACTIVE MEMORY DEVICE TO SECURE DATA FROM TAMPER ATTACKS
24	WO	2009052385		TAMPER REACTIVE MEMORY DEVICE TO SECURE DATA FROM TAMPER ATTACKS
25	US	7949851	11/966,919	TRANSLATION MANAGEMENT OF LOGICAL BLOCK ADDRESSES AND PHYSICAL BLOCK ADDRESSES
26	US	7953919	11/963,306	PHYSICAL BLOCK ADDRESSING OF ELECTRONIC MEMORY DEVICES
26	US	8239875	11/962,918	COMMAND QUEUING FOR NEXT OPERATIONS OF MEMORY DEVICES
27	JP	5192825	2007-554752	SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME
27	US	7968990	11/654,704	SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME
27	WO	2007083351		SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME
28	US	7979667	11/953,501	MEMORY ARRAY SEARCH ENGINE
29	US	7995386	12/275,663	APPLYING NEGATIVE GATE VOLTAGE TO WORDLINES ADJACENT TO WORDLINE ASSOCIATED WITH READ OR VERIFY TO REDUCE ADJACENT WORDLINE DISTURB
30	US	8010776	11/957,793	ADAPTIVE SYSTEM BOOT ACCELERATOR FOR COMPUTING SYSTEMS
31	US	8041895	12/020,698	TRANSLATION TABLE COHERENCY MECAHANISM USING CACHE WAY AND SET INDEX WRITE BUFFERS
32	US	8085588	12/433,084	SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREOF
33	US	8117521	12/198,381	IMPLEMENTATION OF RECYCLING UNUSED ECC PARITY BITS DURING FLASH MEMORY PROGRAMMING
34	US	6175522	09/408,846	READ OPERATION SCHEME FOR A HIGH-DENSITY, LOW VOLTAGE, AND SUPERIOR RELIABILITY NAND FLASH MEMORY DEVICE
35	AT		248400	REDUNDANT DUAL BANK ARCHITECTURE FOR A SIMULTANEOUS OPERATION FLASH MEMORY
35	CN		1379878	Redundant dual bank architecture for simultaneous operation flash memory
35	EP	1224549		REDUNDANT DUAL BANK ARCHITECTURE FOR A SIMULTANEOUS OPERATION FLASH MEMORY
35	JP		2003512690	REDUNDANT DUAL BANK ARCHITECTURE FOR A SIMULTANEOUS OPERATION FLASH MEMORY

35	TW	484055	TW097139850	Redundant dual bank architecture for a simultaneous operation flash memory
35	US	6175523	09/433,187	PRECHARGING MECHANISM AND METHOD FOR NAND-BASED FLASH MEMORY DEVICES
35	WO	WO0129668		REDUNDANT DUAL BANK ARCHITECTURE FOR A SIMULTANEOUS OPERATION FLASH MEMORY
36	US	6397313	09/632,390	REDUNDANT DUAL BANK ARCHITECTURE FOR A SIMULTANEOUS OPERATION FLASH MEMORY
37	US	6219276	09/513,643	MULTILEVEL CELL PROGRAMMING
37	US	6424569	09/513,027	USER SELECTABLE CELL PROGRAMMING
37	WO	WO0163615		USER SELECTABLE CELL PROGRAMMING
38	US	6452869	09/794,478	ADDRESS BROADCASTING TO A PAGED MEMORY DEVICE TO ELIMINATE ACCESS LATENCY PENALTY
39	US	7042766	10/896,651	METHOD OF PROGRAMMING A FLASH MEMORY DEVICE USING MULTILEVEL CHARGE STORAGE
40	EP	1785998		SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE TESTING METHOD, AND DATA WRITING METHOD
40	US	7184338	11/215,253	SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE TESTING METHOD, AND PROGRAMMING METHOD
40	WO	2006025083		SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE TESTING METHOD, AND DATA WRITING METHOD
41	US	7630245	11/543,399	SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREFOR
41	WO	2007104016		SEMICONDUCTOR DEVICE AND METHOD FOR CONTROLLING SAME
42	JP		2008-165917	SEMICONDUCTOR DEVICE AND ITS CONTROL METHOD
42	TW	I359425	96149656	Semiconductor device and method of controlling the same
42	US	7643371	11/986,385	ADDRESS/DATA MULTIPLEXED DEVICE
42	WO	2008082606		SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME
43	JP	5014125	2007-518819	Semiconductor device and program data redundancy method therefor
43	US	7739559	11/444,251	SEMICONDUCTOR DEVICE AND PROGRAM DATA REDUNDANCY METHOD THEREFOR
43	WO	2006129345		SEMICONDUCTOR DEVICE AND PROGRAM DATA REDUNDANT METHOD
44	JP		2008-152549	MEMORY DEVICE, AND PASSWORD STORAGE METHOD FOR MEMORY DEVICE
44	TW	366832	96145085	Memory device and password storing method thereof
44	US	7895406	11/986,332	MEMORY DEVICE AND PASSWORD STORING METHOD THEREOF
44	WO	2008076999		MEMORY DEVICE AND PASSWORD STORING METHOD THEREOF

45	US	7894267	11/929,741	DETERMINISTIC PROGRAMMING ALGORITHM THAT PROVIDES TIGHTER CELL DISTRIBUTIONS WITH A REDUCED NUMBER OF PROGRAMMING PULSES