

## PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1  
Stylesheet Version v1.2

EPAS ID: PAT3418632

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| <b>SUBMISSION TYPE:</b>           | NEW ASSIGNMENT                    |
| <b>NATURE OF CONVEYANCE:</b>      | ASSIGNMENT                        |
| <b>CONVEYING PARTY DATA</b>       |                                   |
| <b>Name</b>                       | <b>Execution Date</b>             |
| SPANSION, LLC                     | 06/01/2015                        |
| <b>RECEIVING PARTY DATA</b>       |                                   |
| <b>Name:</b>                      | Cypress Semiconductor Corporation |
| <b>Street Address:</b>            | 198 Champion Court                |
| <b>City:</b>                      | San Jose                          |
| <b>State/Country:</b>             | CALIFORNIA                        |
| <b>Postal Code:</b>               | 95134                             |
| <b>PROPERTY NUMBERS Total: 50</b> |                                   |
| <b>Property Type</b>              | <b>Number</b>                     |
| Patent Number:                    | 6653190                           |
| Patent Number:                    | 6653191                           |
| Patent Number:                    | 6653871                           |
| Patent Number:                    | 6654283                           |
| Patent Number:                    | 6654285                           |
| Patent Number:                    | 6654848                           |
| Patent Number:                    | 6656763                           |
| Patent Number:                    | 6660588                           |
| Patent Number:                    | 6662262                           |
| Patent Number:                    | 6664191                           |
| Patent Number:                    | 6665214                           |
| Patent Number:                    | 6665777                           |
| Patent Number:                    | 6667212                           |
| Patent Number:                    | 6667511                           |
| Patent Number:                    | 6667552                           |
| Patent Number:                    | 6670227                           |
| Patent Number:                    | 6670241                           |
| Patent Number:                    | 6670669                           |
| Patent Number:                    | 6670691                           |
| Patent Number:                    | 6671207                           |

PATENT

| Property Type  | Number  |
|----------------|---------|
| Patent Number: | 6674138 |
| Patent Number: | 6674277 |
| Patent Number: | 6674657 |
| Patent Number: | 6675277 |
| Patent Number: | 6680507 |
| Patent Number: | 6680509 |
| Patent Number: | 6682978 |
| Patent Number: | 6684353 |
| Patent Number: | 6686263 |
| Patent Number: | 6689666 |
| Patent Number: | 6690225 |
| Patent Number: | 6690236 |
| Patent Number: | 6690602 |
| Patent Number: | 6693009 |
| Patent Number: | 6693321 |
| Patent Number: | 6696331 |
| Patent Number: | 6696821 |
| Patent Number: | 6700201 |
| Patent Number: | 6700815 |
| Patent Number: | 6706576 |
| Patent Number: | 6706595 |
| Patent Number: | 6707078 |
| Patent Number: | 6707718 |
| Patent Number: | 6709924 |
| Patent Number: | 6709927 |
| Patent Number: | 6713809 |
| Patent Number: | 6713842 |
| Patent Number: | 6714063 |
| Patent Number: | 6715059 |
| Patent Number: | 6716698 |

#### CORRESPONDENCE DATA

Fax Number: (408)545-6911

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Correspondent Name: CYPRESS SEMICONDUCTOR CORPORATION

Address Line 1: 198 CHAMPION COURT

Address Line 4: SAN JOSE, CALIFORNIA 95134

**PATENT**

**REEL: 036034 FRAME: 0416**

|                           |                    |
|---------------------------|--------------------|
| <b>NAME OF SUBMITTER:</b> | LARRY J JOHNSON    |
| <b>SIGNATURE:</b>         | /Larry J. Johnson/ |
| <b>DATE SIGNED:</b>       | 06/29/2015         |

**Total Attachments: 147**

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## **CORPORATE ASSIGNMENT**

**SPANSION LLC**, a corporation duly organized under and pursuant to the laws of **DELAWARE** and having its principal place of business at **915 DE GUIGNE DRIVE, SUNNYVALE, CALIFORNIA 94085-3836** (hereafter referred to as the “Assignor”), is the owner by respective assignment of the Issued Patents and Pending Patent Applications set forth in **SCHEDULE A**, attached hereto (hereafter referred to as the “Patents and Applications”).

**CYPRESS SEMICONDUCTOR CORPORATION**, a corporation duly organized under and pursuant to the laws of **DELAWARE** and having its principal place of business at **198 CHAMPION COURT, SAN JOSE, CALIFORNIA 95134-1709** (hereafter referred to as the “Assignee”), desires to acquire the entire right, title, and interest in and to the Patents and Applications.

THEREFORE, in consideration of the sum of One Dollar (\$1.00) and other good and sufficient consideration, the receipt of which is hereby acknowledged, the Assignor hereby sells, assigns, transfers, and sets over to the Assignee, its successors, legal representatives and assigns the entire right, title and interest in and to the Patents and Applications and all inventions described and claimed therein, the right to file any and all classes and types of applications on the inventions (including utility patents, design patents, inventor’s certificates, utility models, and similar rights) for Letters Patent of the United States or other countries, and the entire right, title and interest in and to any and all classes and types of applications for Letters Patent of the United States or other countries claiming priority to the Patents and Applications, including continuations, divisions, continuations-in-part, and continuing prosecution applications of the Patents and Applications, and reissues, renewals, revisions, substitutions, extensions, and all results of oppositions, reexaminations, supplemental examinations and other review procedures (including ex parte reexaminations, inter partes review, post grant review, and covered business method review) of the Patents or Letters Patents, and any and all Letters Patent or Patents of the United States of America and all foreign countries that may be granted therefor and thereon, and all rights under the International Convention for the Protection of Industrial Property, the same to be held and enjoyed by the Assignee, for its own use and behalf and the use and behalf of its successors, legal representatives, and assigns, to the full end of the term or terms for which the Patents and Applications have been granted, and for which Letters Patent or Patents may be

granted, as fully and entirely as the same would have been held and enjoyed by the Assignor had the present sale and assignment not been made.

By its undersigned representative, the Assignor agrees:

- a. to execute all papers necessary in connection with the Patents and Applications and any continuations, divisions, continuations-in-part, and continuing prosecution applications of the Patents and Applications, and reissues, renewals, revisions, substitutions, extensions, and all results of oppositions, reexaminations, supplemental examinations and other review procedures (including ex parte reexaminations, inter partes review, post grant review, and covered business method review) of the Patents and Applications in any country, and also to execute separate assignments in connection with such application as the Assignee may deem necessary or expedient;
- b. to execute all papers necessary in connection with any interference that may be declared concerning the Patents and Applications or any continuations, divisions, continuations-in-part, and continuing prosecution applications of the Patents and Applications, and reissues, renewals, revisions, substitutions, extensions, and all results of oppositions, reexaminations, supplemental examinations and other review procedures (including ex parte reexaminations, inter partes review, post grant review, and covered business method review) thereof, and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such interference; and
- c. to perform all affirmative acts and take all lawful oaths that may be necessary or required to obtain a grant of a valid patent to the Assignee on the Patents and Applications and on any continuations, divisions, continuations-in-part, and continuing prosecution applications of the Patents and Applications, and reissues, renewals, revisions, substitutions, extensions, and all results of oppositions, reexaminations, supplemental examinations and other review procedures (including ex parte reexaminations, inter partes review, post grant review, and covered business method review) of the Patents and Applications in any country, and for the procurement, maintenance, enforcement, and defense of Letters Patent or Patents for the inventions described and claimed therein, without charge to the Assignee, its successors, legal representatives, and assigns, but at the cost and expense of the Assignee, its successors, legal representatives, and assigns.

The Assignor hereby covenants that, at the time of execution and delivery of the present assignment, the Assignor is the sole and lawful owner of the entire right, title, and interest in and to the inventions set forth in the Patents and Applications identified above, and has the full and complete right, title, and interest to convey the entire interest herein assigned, and that it has not executed, and will not execute, any agreement in conflict therewith.

The undersigned has reviewed the documents in the Patents and Applications identified above, and, to the best of undersigned's knowledge and belief, title is in the Assignor identified

above.

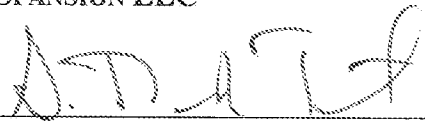
The undersigned is empowered to sign this assignment on behalf of the Assignor.

I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the Patents and Applications, corresponding applications or any patents issuing thereon.

IN WITNESS WHEREOF, executed by the Assignor's undersigned representative on the date following the undersigned's name.

**SPANSION LLC**

By:

  
Thad Trent

Title: Secretary

Date: June 1, 2015

## ACKNOWLEDGMENT

A notary public or other officer completing this certificate verifies only the identity of the individual who signed the document to which this certificate is attached, and not the truthfulness, accuracy, or validity of that document.

State of California

County of Santa Clara

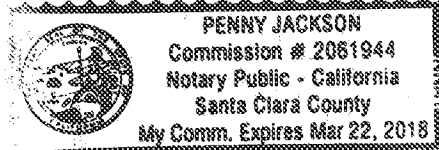
On June 1, 2015 before me, Penny Jackson, Notary  
(insert name and title of the officer)

personally appeared Thad Trent  
who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/are subscribed to the within instrument and acknowledged to me that he/~~she~~/they executed the same in his/~~her~~/their authorized capacity(ies), and that by his/~~her~~/their signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

Signature Penny Jackson (Seal)



PATENT

REEL: 036034 FRAME: 0424

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY   | FILING DATE | ISSUE DATE | TITLE                                                                                                                                           |
|-----------------------|--------------------------|-----------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 2001280952            | AF01073AU                | Australia | 07/31/2001  |            | WORD LINE DECODING ARCHITECTURE IN A FLASH MEMORY                                                                                               |
| 2001280932            | AF01081US                | Australia | 08/11/2000  | 05/08/2001 | BURST READ WORDLINE BOOSTING                                                                                                                    |
| 2001266701            | AF01085AU                | Australia | 06/04/2001  |            | METHOD TO REDUCE CAPACITIVE LOADING IN FLASH MEMORY X-<br>DECODER FOR ACCURATE VOLTAGE CONTROL AT WORDLINES AND<br>SELECT LINES                 |
| 2002239301            | AF01090AU                | Australia | 11/14/2001  |            | I/O PARTITIONING AND METHODOLOGY TO REDUCE BAND-TO-BAND<br>TUNNELING CURRENT DURING ERASE                                                       |
| 2002230944            | AF01096AU                | Australia | 12/12/2001  |            | SOFT PROGRAM AND SOFT PROGRAM VERIFY OF THE CORE CELLS<br>IN FLASH MEMORY ARRAY                                                                 |
| 2003228271            | AF01116WO                | Australia | 03/03/2003  | 10/17/2007 | METHOD FOR MULTI-BIT FLASH READS USING DUAL DYNAMIC<br>REFERENCES                                                                               |
| 26183/00              | AF02593AU                | Australia | 01/18/2000  |            | SHARED MEMORY APPARATUS AND METHOD FOR<br>MULTIPROCESSOR SYSTEMS                                                                                |
| 2002245464            | G0259AU                  | Australia | 02/19/2002  |            | FLASH MEMORY DEVICE WITH INCREASE OF EFFICIENCY DURING AN<br>APDE (AUTOMATIC PROGRAM DISTURB AFTER ERASE) PROCESS                               |
| 2003211090            | G0863US                  | Australia | 02/14/2003  |            | OVERERASE CORRECTION METHOD                                                                                                                     |
| 2003219707            | G1255AU                  | Australia | 02/05/2003  |            | PARTIAL PAGE PROGRAMMING OF MULTI LEVEL FLASH                                                                                                   |
| 56618/01              | P-2448WO                 | Australia | 05/03/2001  |            | PROGRAMMING OF NONVOLATILE MEMORY CELLS                                                                                                         |
| 2002363046            | P-4006AU                 | Australia | 10/24/2002  |            | METHOD FOR ERASING A MEMORY CELL                                                                                                                |
| 2003222282            | SE0002AU                 | Australia | 03/11/2003  |            | SYSTEM AND METHOD OF ERASE VOLTAGE CONTROL DURING<br>MULTIPLE SECTOR ERASE OF A FLASH MEMORY DEVICE                                             |
| 1297534               | AF01085AT                | Austria   | 06/04/2001  | 03/14/2007 | METHOD TO REDUCE CAPACITIVE LOADING IN FLASH MEMORY X-<br>DECODER FOR ACCURATE VOLTAGE CONTROL AT WORDLINES AND<br>SELECT LINES                 |
| 1226586               | AF01086AT                | Austria   | 09/29/2000  | 06/18/2003 | A WORD LINE TRACKING STRUCTURE FOR USE IN AN ARRAY OF<br>FLASH EEPROM MEMORY CELLS                                                              |
| 60043444.3            | D833AT                   | Austria   | 08/29/2000  | 10/15/2009 | 1 TRANSISTOR FOR EEPROM APPLICATION                                                                                                             |
| 01910464.5            | E0264                    | Austria   | 02/07/2001  |            | TRIMMING METHOD FOR WORDLINE BOOSTER TO MINIMIZE<br>PROCESS VARIATION OF BOOSTED WORDLINE VOLTAGE                                               |
| 09166120              | FMA13-0289AT             | Austria   | 08/21/2006  |            | PRESALER AND BUFFER                                                                                                                             |
| 01309289.5            | P-2448US CON             | Austria   | 11/01/2001  |            | PROGRAMMING AND ERASING METHODS FOR A REFERENCE CELL OF<br>AN NROM ARRAY                                                                        |
| 20010117103           | H1979BR                  | Brazil    | 08/13/2001  |            | MEMORY CELL                                                                                                                                     |
| 2,367,065             | AF02593CA                | Canada    | 01/18/2000  |            | SHARED MEMORY APPARATUS AND METHOD FOR<br>MULTIPROCESSOR SYSTEMS                                                                                |
| ZL00814522.9          | AF01002CN                | China     | 10/07/2000  | 04/20/2005 | LOW VOLTAGE READ CASCODE FOR 2V/3V AND DIFFERENT BANK<br>COMBINATIONS WITHOUT METAL OPTIONS FOR A SIMULTANEOUS<br>OPERATION FLASH MEMORY DEVICE |
| 00814408.7            | AF01006CN                | China     | 10/09/2000  |            | REDUNDANT DUAL BANK ARCHITECTURE FOR A SIMULTANEOUS<br>OPERATION FLASH MEMORY                                                                   |
| ZL01805509.5          | AF01036CN                | China     | 02/07/2001  | 11/30/2005 | WORDLINE DRIVER FOR FLASH MEMORY READ MODE                                                                                                      |
| 455629                | AF01054CN                | China     | 10/16/2000  | 10/16/2000 | HIGH TEMPERATURE OXIDE DEPOSITION PROCESS FOR<br>FABRICATING AN ONO FLOATING-GATE ELECTRODE IN A TWO BIT<br>EEPROM DEVICE                       |
| ZL01806877.4          | AF01064CN                | China     | 03/20/2001  | 04/20/2005 | METHOD FOR FORMING HIGH QUALITY MULTIPLE THICKNESS OXIDE<br>LAYERS USING HIGH TEMPERATURE DESCUM                                                |
| ZL01806969.X          | AF01066CN                | China     | 03/20/2001  | 02/01/2006 | METHOD FOR FORMING HIGHQUALITY MULTIPLE THICKNESS OXIDE<br>LAYERS BY REDUCING DESCUM INDUCED DEFECTS                                            |
| ZL01804591.X          | AF01072CN                | China     | 02/05/2001  | 10/18/2006 | VOLTAGE BOOST LEVEL CLAMPING CIRCUIT FOR A FLASH MEMORY                                                                                         |
| ZL01814914.6          | AF01073CN                | China     | 07/31/2001  | 03/14/2007 | WORD LINE DECODING ARCHITECTURE IN A FLASH MEMORY                                                                                               |
| ZL01806325.X          | AF01075CN                | China     | 03/12/2001  | 09/27/2006 | MULTIPLE BANK SIMULTANEOUS OPERATION FOR A FLASH MEMORY                                                                                         |
| 01810500.9            | AF01076CN                | China     | 05/21/2001  | 10/21/2009 | BURST ARCHITECTURE FOR A FLASH MEMORY                                                                                                           |
| 200810135828.2        | AF01076CN DIV            | China     | 07/15/2008  | 04/10/2013 | BURST ARCHITECTURE FOR A FLASH MEMORY                                                                                                           |
| ZL01813382.7          | AF01078CN                | China     | 07/17/2001  | 09/13/2006 | BURST READ INCORPORATING OUTPUT BASED REDUNDANCY                                                                                                |
| ZL01811070.3          | AF01085CN                | China     | 06/04/2001  | 07/12/2006 | METHOD TO REDUCE CAPACITIVE LOADING IN FLASH MEMORY X-<br>DECODER FOR ACCURATE VOLTAGE CONTROL AT WORDLINES AND<br>SELECT LINES                 |
| ZL00813967.9          | AF01086CN                | China     | 09/29/2000  | 07/27/2005 | A WORD LINE TRACKING STRUCTURE FOR USE IN AN ARRAY OF<br>FLASH EEPROM MEMORY CELLS                                                              |
| z01806239.3           | AF01088CN                | China     | 03/05/2001  | 04/20/2005 | SINGLE TUNNEL GATE OXIDATION PROCESS FOR FABRICATING NAND<br>FLASH MEMORY                                                                       |
| 366895                | AF01090CN                | China     | 11/14/2001  | 12/26/2007 | I/O PARTITIONING AND METHODOLOGY TO REDUCE BAND-TO-BAND<br>TUNNELING CURRENT DURING ERASE                                                       |
| 02814417.1            | AF01094CN                | China     | 03/14/2002  | 11/04/2009 | VOLTAGE BOOST CIRCUIT USING SUPPLY VOLTAGE DETECTION TO<br>COMPENSATE FOR SUPPLY VOLTAGE VARIATION IN READ MODE<br>VOLTAGES                     |
| 374910                | AF01096CN                | China     | 12/12/2001  | 01/30/2008 | SOFT PROGRAM AND SOFT PROGRAM VERIFY OF THE CORE CELLS<br>IN FLASH MEMORY ARRAY                                                                 |
| 01819608.X            | AF01102CN                | China     | 08/07/2001  | 08/19/2009 | SIMULTANEOUS FORMATION CHARGE STORAGE AND BITLINE TO<br>WORDLINE ISOLATION                                                                      |
| 03808311.6            | AF01116CN                | China     | 03/03/2003  | 10/28/2009 | SYSTEM AND METHOD FOR MULTI-BIT FLASH READS USING DUAL<br>DYNAMIC REFERENCES                                                                    |
| 320166                | AF01124CN                | China     | 12/11/2002  | 04/18/2007 | MONOS DEVICE HAVING BURIED METAL SILICIDE BIT LINE                                                                                              |
| 328863                | AF01132CN                | China     | 01/21/2003  | 06/06/2007 | HARD MASK PROCESS FOR MEMORY DEVICE WITHOUT BITLINE<br>SHORTS                                                                                   |
| 352780                | AF01134CN                | China     | 01/21/2003  | 10/17/2007 | METHOD OF MAKING MEMORY WORDLINE HARD MASK EXTENSION                                                                                            |
| 323601                | AF01137CN                | China     | 02/14/2003  | 05/09/2007 | MEMORY MANUFACTURING PROCESS WITH BITLINE ISOLATION                                                                                             |
| 03819817.7            | AF01165CN                | China     | 06/10/2003  |            | COLUMN-DECODING AND PRECHARGING IN A FLASH MEMORY<br>DEVICE                                                                                     |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                      |
|-----------------------|--------------------------|---------|-------------|------------|----------------------------------------------------------------------------------------------------------------------------|
| 200480017247.9        | AF01169CN                | China   | 05/21/2004  | 10/21/2009 | MEMORY WITH A CORE-BASED VIRTUAL GROUND AND DYNAMIC<br>REFERENCE SENSING SCHEME                                            |
| 674356                | AF01186CN                | China   | 01/08/2004  | 09/22/2010 | CHARGE-TRAPPING MEMORY ARRAYS RESISTANT TO DAMAGE FROM<br>CONTACT HOLE FORMATION                                           |
| 200480012016.9        | AF01209CN                | China   | 04/13/2004  | 11/12/2008 | METHOD FOR REDUCING SHORT CHANNEL EFFECTS IN MEMORY<br>CELLS AND RELATED STRUCTURE                                         |
| 200480040446.1        | AF01214CN                | China   | 12/17/2004  |            | EFFICIENT USE OF WAFER AREA WITH DEVICE UNDER THE PAD<br>APPROACH                                                          |
| 200480040892.2        | AF01220CN                | China   | 12/17/2004  | 02/13/2009 | STRUCTURE AND METHOD FOR LOW VSS RESISTANCE AND<br>REDUCED DIBL IN A FLOATING GATE MEMORY CELL                             |
| 200580022719.4        | AF01232CN                | China   | 04/29/2005  |            | BOND PAD STRUCTURE FOR COPPER METALLIZATION HAVING<br>INCREASED RELIABILITY AND METHOD FOR FABRICATING SAME                |
| 200480042988.2        | AF01240CN                | China   | 03/26/2004  | 04/28/2010 | ABORT CIRCUIT FOR MLC PROGRAMMING                                                                                          |
| 200480043296.X        | AF01241CN                | China   | 04/13/2004  |            | NEW COMMAND FOR SECTOR PROTECTION                                                                                          |
| 200480043290.2        | AF01248CN                | China   | 04/21/2004  | 05/05/2010 | NON-VOLATILE SEMICONDUCTOR DEVICE AND METHOD FOR<br>AUTOMATICALLY RECOVERING ERASE FAILURE IN THE DEVICE                   |
| 200680027637.3        | AF01285CN                | China   | 07/17/2006  |            | PROGRAM/ERASE WAVESHAPING CONTROL TO INCREASE DATA<br>RETENTION OF A MEMORY CELL                                           |
| 101023539             | AF01306CN                | China   | 06/30/2005  | 08/24/2011 | SWITCHABLE MEMORY DIODE- A NEW MEMORY DEVICE                                                                               |
| 200580027947.0        | AF01320CN                | China   | 08/08/2005  |            | SYSTEMS AND METHODS FOR ADJUSTING PROGRAMMING<br>THRESHOLDS OF POLYMER MEMORY CELLS                                        |
| 201310228388.6        | AF01320CN DIV            | China   | 08/08/2005  |            | SYSTEMS AND METHODS FOR ADJUSTING PROGRAMMING<br>THRESHOLDS OF POLYMER MEMORY CELLS                                        |
| 200580027937.7        | AF01321US                | China   | 08/08/2005  |            | POLYMER MEMORY DEVICE WITH VARIABLE PERIOD OF RETENTION<br>TIME                                                            |
| 744679                | AF01329CN                | China   | 08/30/2004  | 03/02/2011 | ERASING METHOD FOR NONVOLATILE STORAGE, AND NONVOLATILE<br>STORAGE                                                         |
| 200480044696.2        | AF01338CN                | China   | 10/26/2004  | 08/19/2009 | METHOD OF SETTING INFORMATION OF NON-VOLATILE MEMORY AND<br>NON-VOLATILE MEMORY                                            |
| 200580022786.6        | AF01361CN                | China   | 06/30/2005  |            | METHOD OF IMPROVING ERASE VOLTAGE DISTRIBUTION FOR A<br>FLASH MEMORY ARRAY HAVING DUMMY WORDLINES                          |
| 200580026253.5        | AF01365CN                | China   | 04/29/2005  |            | FLASH MEMORY UNIT AND METHOD OF PROGRAMMING A FLASH<br>MEMORY DEVICE                                                       |
| 200480042780.0        | AF01372CN                | China   | 02/19/2004  | 08/19/2009 | CURRENT-VOLTAGE CONVERTER CIRCUIT AND CONTROL METHOD<br>THEREOF                                                            |
| 200480042774.5        | AF01376CN                | China   | 02/20/2004  | 12/07/2011 | A SEMICONDUCTOR MEMORY STORAGE DEVICE AND ITS<br>REDUNDANT METHOD                                                          |
| ZL200480042775.X      | AF01377CN                | China   | 02/20/2004  | 11/06/2013 | A SEMICONDUCTOR MEMORY STORAGE DEVICE AND ITS<br>REDUNDANCY CONTROL METHOD                                                 |
| 200580026447.5        | AF01379CN                | China   | 04/29/2005  | 11/02/2011 | FLOATING GATE MEMORY CELL                                                                                                  |
| 200480042812.7        | AF01380CN                | China   | 02/20/2004  | 03/03/2010 | A SEMICONDUCTOR MEMORY STORAGE DEVICE AND ITS CONTROL<br>METHOD                                                            |
| 756499                | AF01383CN                | China   | 09/20/2005  | 04/06/2011 | READ APPROACH FOR MULTI-LEVEL VIRTUAL GROUND MEMORY                                                                        |
| 200580018934.7        | AF01386CN                | China   | 02/11/2005  |            | ERASE ALGORITHM FOR MULTI-LEVEL BIT FLASH MEMORY                                                                           |
| 841560                | AF01390CN                | China   | 12/20/2005  | 09/14/2011 | MULTI-LEVEL ONO FLASH PROGRAM ALGORITHM FOR THRESHOLD<br>WIDTH CONTROL                                                     |
| 200480044077.3        | AF01402CN                | China   | 07/30/2004  | 10/28/2009 | NEW CASCADE AND SENSE-AMPLIFIER                                                                                            |
| 200480044076.9        | AF01403CN                | China   | 07/30/2004  | 03/13/2009 | MLC WRITE BUFFER CIRCUITRY                                                                                                 |
| 200480043688.6        | AF01412CN                | China   | 07/29/2004  | 09/01/2010 | METHOD FOR SETTING INFORMATION IN NON-VOLATILE STORAGE<br>DEVICE, NON-VOLATILE STORAGE DEVICE AND SYSTEM USING THE<br>SAME |
| 200480043591.5        | AF01416CN                | China   | 05/12/2004  |            | IMPROVED NEGATIVE DECODING                                                                                                 |
| 200480043574.1        | AF01417CN                | China   | 05/11/2004  |            | HIGH SPEED BOOST OPERATION                                                                                                 |
| 757179                | AF01422CN                | China   | 05/11/2004  | 04/06/2011 | SEMICONDUCTOR DEVICE AND PROGRAM METHOD                                                                                    |
| 200480043332.2        | AF01423CN                | China   | 05/11/2004  | 05/11/2004 | MULTI BIT PROGRAMMING FOR VIRTUAL GROUND ARRAY                                                                             |
| 200480043511.6        | AF01425CN                | China   | 05/11/2004  |            | IMPROVED APPARATUS FOR ADVANCED SECTOR PROTECTION (1)                                                                      |
| 200480043544.0        | AF01427CN                | China   | 05/12/2004  | 04/14/2010 | IMPROVED SLATCH AND THE LAYOUT                                                                                             |
| 789501                | AF01438CN                | China   | 12/24/2004  | 06/08/2011 | METHOD AND APPARATUS FOR APPLYING BIAS TO A STORAGE<br>DEVICE                                                              |
| 200480044854.4        | AF01439CN                | China   | 11/30/2004  |            | NON-VOLATILE SELECT GATE IN NAND FLASH MEMORY                                                                              |
| 200480044104.7        | AF01441CN                | China   | 07/29/2004  |            | METHOD FOR INITIALIZING NON-VOLATILE STORAGE DEVICE, AND<br>NOT-VOLATILE STORAGE DEVICE                                    |
| 689912                | AF01443CN                | China   | 05/11/2004  | 10/13/2010 | CARRIER FOR MULTILAYER SEMICONDUCTOR DEVICE AND PROCESS<br>FOR MANUFACTURING MULTILAYER SEMICONDUCTOR DEVICE               |
| 200480044895.3        | AF01445CN                | China   | 12/28/2004  | 12/28/2004 | SONOS WITH USE OF SWITCH GATE, WITHOUT BURIED DIFFUSION<br>LAYER BITLINE                                                   |
| 642574                | AF01446CN                | China   | 05/20/2004  | 06/16/2010 | Process for Producing Semiconductor Device and Semiconductor Dvice                                                         |
| 637334                | AF01451CN                | China   | 04/24/2006  | 06/09/2011 | THE FORMATION METHOD OF AN ARRAY SOURCE LINE IN NAND<br>FLASH                                                              |
| 200580019314.5        | AF01453CN                | China   | 02/11/2005  |            | METHOD AND SYSTEMS FOR HIGH WRITE PERFORMANCE IN MULTI-<br>BIT FLASH MEMORY DEVICES                                        |
| 200480044857.8        | AF01454CN                | China   | 11/30/2004  | 06/27/2012 | NONVOLATILE STORAGE AND ITS MANUFACTURING METHOD                                                                           |
| 200480044770.0        | AF01455CN                | China   | 11/30/2004  |            | NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                   |
| 200680012958.6        | AF01459CN                | China   | 04/24/2006  | 06/13/2012 | SELF-ALIGNED STI SONOS                                                                                                     |
| 200480044407.9        | AF01463CN                | China   | 09/30/2004  |            | SEMICONDUCTOR DEVICE AND DATA WRITING METHOD                                                                               |
| 200680002239.6        | AF01467CN                | China   | 01/12/2006  | 03/30/2011 | MEMORY DEVICE HAVING TRAPEZOIDAL BITLINES AND METHOD OF<br>FABRICATING SAME                                                |
| 200480044750.3        | AF01468CN                | China   | 10/29/2004  | 08/19/2009 | SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME                                                                    |
| 200480044853.X        | AF01470CN                | China   | 11/30/2004  | 03/21/2012 | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREOF                                                                            |
| 200480044729.3        | AF01479CN                | China   | 12/28/2004  | 09/05/2012 | SEMICONDUCTOR DEVICE AND OPERATION CONTROL METHOD FOR<br>SAME                                                              |

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| PATENT OR APPL NO. | SPANSION REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                              |
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| 200680015533.0     | AF01482CN              | China   | 05/26/2006  |            | PAGE BUFFER ARCHITECTURE FOR PROGRAMMING, ERASING AND READING NANOSCALE RESISTIVE MEMORY DEVICES   |
| 201210105258.9     | AF01482CN DIV          | China   | 05/26/2006  |            | PAGE BUFFER ARCHITECTURE FOR PROGRAMMING, ERASING AND READING NANOSCALE RESISTIVE MEMORY DEVICES   |
| 200580043866.X     | AF01485CN              | China   | 12/20/2005  |            | METHOD OF PROGRAMMING, READING AND ERASING MEMORY-DIODE IN A MEMORY-DIODE ARRAY                    |
| 691427             | AF01491CN              | China   | 11/10/2005  | 10/27/2010 | DIODE ARRAYS ARCHITECTURE FOR ADDRESSING NANOSCALE RESISTIVE MEMORY ARRAYS                         |
| 200580038928.8     | AF01500CN              | China   | 11/10/2005  |            | PROTECTION OF ACTIVE LAYERS OF MEMORY CELLS DURING PROCESSING OF OTHER ELEMENTS                    |
| 101088126          | AF01523CN              | China   | 12/20/2005  | 01/18/2012 | SENSE AMPLIFIER WITH HIGH VOLTAGE SWING                                                            |
| 201110358517.4     | AF01523CN DIV          | China   | 12/20/2005  |            | SENSE AMPLIFIER WITH HIGH VOLTAGE SWING                                                            |
| 200680007399.X     | AF01524CN              | China   | 03/07/2006  | 07/04/2012 | DECODER FOR MEMORY DEVICE                                                                          |
| 200480044704.3     | AF01645CN              | China   | 10/26/2004  |            | NON-VOLATILE MEMORY DEVICE                                                                         |
| 200580046970.4     | AF01653CN              | China   | 01/24/2005  | 03/06/2009 | SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME                                            |
| 200680010627.9     | AF01665CN              | China   | 04/04/2006  |            | SPLIT GATE MULTI-BIT MEMORY CELL                                                                   |
| 200680033325.3     | AF01668CN              | China   | 09/08/2006  | 05/02/2012 | HIGH PERFORMANCE FLASH MEMORY DEVICE CAPABLE OF HIGH DENSITY DATA STORAGE                          |
| 847573             | AF01669CN              | China   | 09/07/2006  | 09/07/2011 | MULTI-BIT FLASH MEMORY DEVICE HAVING IMPROVED PROGRAM RATE                                         |
| 200480044666.1     | AF01688CN              | China   | 10/25/2004  |            | IMPROVEMENT METHOD OF DATA RETENTION OF SEMICONDUCTOR MEMORY                                       |
| 200480044889.8     | AF01691CN              | China   | 12/24/2004  | 12/19/2012 | SYNCHRONIZATION TYPE STORAGE DEVICE AND CONTROLLING METHOD THEREOF                                 |
| 101171683          | AF01695CN              | China   | 04/26/2006  | 02/12/2014 | MULTI-CHIP MODULE AND METHOD OF MANUFACTURE                                                        |
| 201310319901.2     | AF01695CN DIV          | China   | 04/26/2006  |            | MULTI-CHIP MODULE AND METHOD OF MANUFACTURE                                                        |
| 101138089          | AF01696CN              | China   | 01/31/2005  | 02/09/2011 | LAYERED SEMICONDUCTOR DEVICE AND LAYERED SEMICONDUCTOR DEVICE MANUFACTURING METHOD                 |
| 741645             | AF01698CN              | China   | 01/27/2005  | 02/16/2011 | SEMICONDUCTOR DEVICE, ADDRESS ASSIGNMENT METHOD, AND VERIFY METHOD                                 |
| 200580048775.5     | AF01707CN              | China   | 03/31/2005  |            | STACKED-TYPE SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME                             |
| 685418             | AF01709CN              | China   | 03/22/2006  | 10/06/2010 | VARIABLE BREAKDOWN CHARACTERISTIC DIODE                                                            |
| 200580049592.5     | AF01728CN              | China   | 04/27/2005  |            | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR                                             |
| 200580049950.2     | AF01729CN              | China   | 05/30/2005  |            | IMPROVEMENT OF DATE RETENTION CHARACTERISTICS OF SONOS FLASH MEMORY                                |
| 200680012623.4     | AF01730CN              | China   | 03/24/2006  |            | MULTI CHIP MODULE AND METHOD OF MANUFACTURE                                                        |
| 200680016641.X     | AF01741CN              | China   | 05/25/2006  |            | READ-ONLY MEMORY ARRAY WITH DIELECTRIC BREAKDOWN PROGRAMMABILITY                                   |
| 200680033453.8     | AF01746CN              | China   | 09/06/2006  |            | METHOD FOR FORMING SPACERS BETWEEN BITLINES IN A VIRTUAL GROUND MEMORY ARRAY AND REALTED STRUCTURE |
| 200680015957.7     | AF01775CN              | China   | 04/26/2006  |            | RESISTIVE MEMORY DEVICE WITH IMPROVED DATA RETENTION AND REDUCED POWER                             |
| 794220             | AF01777CN              | China   | 10/06/2006  | 06/15/2011 | METHOD FOR MANUFACTURING A SEMICONDUCTOR COMPONENT USING A SACRIFICIAL MASKING STRUCTURE           |
| 101203954          | AF01792CN              | China   | 06/28/2005  | 09/28/2011 | SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF                                                |
| 200580050283.X     | AF01802CN              | China   | 06/28/2005  | 02/02/2011 | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREOF                                                    |
| 815563             | AF01810CN              | China   | 03/16/2007  | 07/27/2011 | VERTICAL EEPROM DEVICE                                                                             |
| 845197             | AF01852CN              | China   | 07/07/2006  | 09/28/2011 | INTEGRATED CIRCUIT TEST SOCKET                                                                     |
| 200680040776.X     | AF01853CN              | China   | 10/06/2006  |            | MEMORY ARRAY ARRANGED IN BANKS AND SECTORS AND ASSOCIATED DECODERS                                 |
| 201410409924.7     | AF01853CN DIV          | China   | 10/06/2006  |            | MEMORY ARRAY ARRANGED IN BANKS AND SECTORS AND ASSOCIATED DECODERS                                 |
| 200780012951.9     | AF01907CN              | China   | 04/05/2007  | 02/01/2012 | MULTI MEDIA CARD WITH HIGH STORAGE CAPACITY                                                        |
| 200780018096.2     | AF01954CN              | China   | 04/05/2007  |            | MEMORY CELL ARRAY WITH LOW RESISTANCE COMMON SOURCE AND HIGH CURRENT DRIVABILITY                   |
| 101449370          | AF02071CN              | China   | 05/21/2007  | 06/26/2013 | MEMORY SYSTEM WITH SWITCH ELEMENT                                                                  |
| 1286359            | AF02136CN              | China   | 04/05/2007  | 10/16/2013 | REDUCTION OF LEAKAGE CURRENT AND PROGRAM DISTURBS IN FLASH MEMORY DEVICES                          |
| 201310403394.0     | AF02136CN DIV          | China   | 04/05/2007  |            | REDUCTION OF LEAKAGE CURRENT AND PROGRAM DISTURBS IN FLASH MEMORY DEVICES                          |
| 200780014867.0     | AF02137CN              | China   | 04/05/2007  | 11/28/2012 | METHODS FOR ERASING AND PROGRAMMING MEMORY DEVICES                                                 |
| 200780016294.5     | AF02138CN              | China   | 04/05/2007  |            | METHODS FOR ERASING MEMORY DEVICES AND MULTI-LEVEL PROGRAMMING MEMORY DEVICE                       |
| 1411492            | AF02146CN              | China   | 04/05/2007  | 06/04/2014 | FLASH MEMORY PROGRAMMING AND VERIFICATION WITH REDUCED LEAKAGE CURRENT                             |
| 201410172165.7     | AF02146CN DIV          | China   | 04/05/2007  |            | FLASH MEMORY PROGRAMMING AND VERIFICATION WITH REDUCED LEAKAGE CURRENT                             |
| 03109522.4         | AF02208CN              | China   | 04/08/2003  | 06/06/2007 | NONVOLATILE SEMICONDUCTOR MEMORY AND                                                               |
| ZL03136844.1       | AF02212CN              | China   | 05/21/2003  | 09/06/2006 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                            |
| ZL03107621.1       | AF02214CN              | China   | 03/21/2003  | 02/15/2006 | SEMICONDUCTOR MEMORY DEVICE                                                                        |
| 100358048          | AF02219CN              | China   | 09/12/2003  | 12/26/2007 | SEMICONDUCTOR MEMORY FOR FUNCTION WELL                                                             |
| ZL03153352.3       | AF02220CN              | China   | 08/11/2003  | 12/19/2007 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                   |
| ZL03156893.9       | AF02221CN              | China   | 09/11/2003  | 08/06/2008 | MEMORY CIRCUIT HAVING                                                                              |
| CN100351950C       | AF02222CN              | China   | 08/12/2003  | 11/28/2007 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                   |
| CN 1685444B        | AF02226CN              | China   | 02/27/2003  | 07/06/2011 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                   |
| 03824062.9         | AF02229CN              | China   | 02/28/2003  |            | FLASH MEMORY AND MEMORY CONTROL                                                                    |
| 200380100622.1     | AF02230CN              | China   | 12/17/2003  | 07/09/2008 | SEMICONDUCTOR DEVICE AND TEST METHOD                                                               |
| 03824185.4         | AF02232CN              | China   | 03/11/2003  |            | MEMORY DEVICE                                                                                      |
| 200380100721       | AF02233CN              | China   | 12/17/2003  | 01/21/2012 | NONVOLATILE MEMORY AND METHOD AND WRITE METHOD OF THE SAME                                         |

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|--------------------|------------------------|---------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| CN100442394C       | AF02234CN              | China   | 11/19/2003  | 12/10/2008 | SEMICONDUCTOR MEMORY DEVICE AND CONTROL                                                                                                          |
| 1558423            | AF02236CN              | China   | 01/21/2004  | 04/28/2010 | SEMICONDUCTOR MEMORY                                                                                                                             |
| 03826339.4         | AF02238CN              | China   | 04/24/2003  | 12/02/2009 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                                                                 |
| 100470676          | AF02241CN              | China   | 06/06/2003  | 03/18/2009 | SEMICONDUCTOR STORAGE DEVICE AND SEMICONDUCTOR STORAGE DEVICE BIT LINE SELECTION METHOD                                                          |
| 200880023742.9     | AF02453CN              | China   | 05/09/2008  |            | SELF ALIGNED NARROW STORAGE ELEMENTS FOR ADVANCED MEMORY DEVICE                                                                                  |
| 200880025232.5     | AF02465CN              | China   | 07/21/2008  | 03/13/2013 | SYNCHRONOUS MEMORY DEVICES AND CONTROL METHODS FOR PERFORMING BURST WRITE OPERATIONS                                                             |
| ZL200880016146.8   | AF02477CN              | China   | 03/14/2008  | 07/09/2014 | DIVISION-BASED SENSING AND PARTITIONING OF ELECTRONIC MEMORY                                                                                     |
| 201180049007.7     | AF03209CN              | China   | 04/10/2013  |            | STITCH BUMP STACKING DESIGN FOR OVERALL PACKAGE SIZE REDUCTION FOR MULTIPLE STACK                                                                |
| 201180041602.6     | AF03219CN              | China   | 06/29/2011  |            | METHOD AND SYSTEM FOR THIN MULTI CHIP STACK PACKAGE WITH FILM ON WIRE AND COPPER WIRE                                                            |
| 03820714.1         | AF04012US DIV          | China   | 08/29/2003  | 03/05/2008 | SEMICONDUCTOR MEMORY DEVICE                                                                                                                      |
| CN101048872B       | AF04020US              | China   | 10/19/2005  | 08/24/2011 | Non-volatile memory and pseudo-sram based on resonant tunneling concept                                                                          |
| 20081147128        | AF04022US              | China   | 08/20/2008  |            | CMOS LOGIC COMPATIBLE NON-VOLATILE MEMORY CELL STRUCTURE, OPERATION, AND ARRAY CONFIGURATION                                                     |
| 201280070114.2     | AF04035CN              | China   | 12/18/2012  |            | ACOUSTIC PROCESSING UNIT INTERFACE                                                                                                               |
| 201280070112.3     | AF04036CN              | China   | 12/18/2012  |            | ARITHMETIC LOGIC UNIT ARCHITECTURE                                                                                                               |
| ZL00813303.4       | C656497CN              | China   | 08/31/2000  | 03/09/2005 | TUNGSTEN GATE MOS TRANSISTOR AND MEMORY CELL AND METHOD OF MAKING SAME                                                                           |
| ZL 00811545.1      | C725497CN              | China   | 08/01/2000  | 11/03/2004 | CIRCUIT IMPLEMENTATION TO QUENCH BIT LINE LEAKAGE CURRENT IN PROGRAM AND AUTO PROGRAM DISTURB MODE IN FLASH EPROM USING RESISTOR SOURCE LOAD     |
| ZL00812395.0       | D833CN                 | China   | 08/29/2000  | 11/30/2005 | 1 TRANSISTOR FOR EEPROM APPLICATION                                                                                                              |
| ZL00815128.8       | D838CN                 | China   | 10/24/2000  | 12/01/2004 | SOLID-SOURCE DOPING FOR SOURCE/DRAIN OF FLASH MEMORY                                                                                             |
| ZL00811313.0       | D844CN                 | China   | 07/14/2000  | 12/29/2004 | RAMPED GATE TECHNIQUE FOR SOFT PROGRAMMING TO TIGHTEN THE VI DISTRIBUTION                                                                        |
| 00817240.4         | D853CN                 | China   | 12/05/2000  |            | METHOD TO PROVIDE A REDUCED CONSTANT E-FIELD DURING ERASE OF EEPROMS FOR RELIABILITY IMPROVEMENT                                                 |
| ZL00812201.6       | D877CN                 | China   | 07/17/2000  | 12/29/2004 | INTEGRATED CIRCUIT HAVING INCREASED GATE COUPLING CAPACITANCE                                                                                    |
| ZL00814181.9       | D894CN                 | China   | 09/29/2000  | 01/26/2005 | METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITH REDUCED ARC LOSS IN PERIPHERAL CIRCUITRY REGION                                              |
| ZL00818639.1       | D958CN                 | China   | 12/13/2000  | 04/06/2005 | NOVEL NITRIDATION BARRIERS FOR NITRIDATED TUNNEL OXIDE FOR CIRCUITRY FOR FLASH TECHNOLOGY AND FOR LOCOS/STI ISOLATION                            |
| ZL00811367.X       | DA01016CN              | China   | 07/14/2000  | 12/01/2004 | METHOD FOR PROVIDING A DOPANT LEVEL FOR POLYSILICON FOR FLASH MEMORY DEVICES                                                                     |
| 00811962.7         | E0251CN                | China   | 07/14/2000  | 10/21/2009 | FLASH MEMORY ARCHITECTURE EMPLOYING THREE LAYER METAL INTERCONNECT                                                                               |
| ZL01805426.9       | E0264CN                | China   | 02/07/2001  | 07/27/2005 | TRIMMING METHOD FOR WORDLINE BOOSTER TO MINIMIZE PROCESS VARIATION OF BOOSTED WORDLINE VOLTAGE                                                   |
| 01809611.5         | E0302CN                | China   | 05/01/2001  | 08/22/2008 | UNIFORM BITLINE STRAPPING OF NON-VOLATILE MEMORY CELL                                                                                            |
| ZL01806324.1       | E0370CN                | China   | 03/12/2001  | 04/06/2005 | A DUAL SPACER PROCESS NON-VOLATILE MEMORY DEVICES                                                                                                |
| ZL01810229.8       | E0462CN                | China   | 05/21/2001  | 06/01/2005 | DUAL PORTED CAMS FOR SIMULTANEOUS OPERATION FLASH MEMORY                                                                                         |
| 01805671.7         | E1030CN                | China   | 02/07/2001  | 08/05/2009 | TEMPERATURE COMPENSATED BIAS GENERATOR                                                                                                           |
| 01812247.7         | F0004CN                | China   | 06/08/2001  |            | AUTOMATED DETERMINATION AND DISPLAY OF THE PHYSICAL LOCATION OF A FAILED CELL IN AN ARRAY OF MEMORY CELLS                                        |
| 331606             | F0257CN                | China   | 08/07/2001  | 06/20/2007 | METHOD AND SYSTEM FOR EMBEDDED CHIP ERASE VERIFICATION                                                                                           |
| 02827260.9         | F0258CN                | China   | 12/17/2002  |            | METHOD AND APPARATUS FOR SOFT PROGRAM VERIFICATION IN A MEMORY DEVICE                                                                            |
| 455657             | F0260CN                | China   | 12/12/2001  | 12/31/2008 | METHOD AND APPARATUS FOR BOOSTING BITLINES FOR LOW VCC READ                                                                                      |
| 464256             | F0262CN                | China   | 12/17/2002  | 01/28/2009 | METHOD AND APPARATUS FOR SOFT PROGRAM VERIFICATION IN A MEMORY DEVICE                                                                            |
| 02827250.1         | F0272CN                | China   | 12/17/2002  | 11/12/2008 | CHARGE INJECTION                                                                                                                                 |
| 414908             | F0282CN                | China   | 09/30/2002  | 07/30/2008 | DOUBLE DENSED CORE GATES IN SONOS FLASH MEMORY                                                                                                   |
| 02819075.0         | F0283CN                | China   | 09/27/2002  | 12/26/2008 | SALICIDED GATE FOR VIRTUAL GROUND ARRAYS                                                                                                         |
| ZL01817852.9       | F0499CN                | China   | 08/06/2001  | 10/12/2005 | A SOURCE SIDE BORON IMPLANTING AND DIFFUSING DEVICE ARCHITECTURE FOR DEEP SUBSTANCE 0.18UM FLASH MEMORY TECHNOLOGIES                             |
| ZL01817027.7       | F0932CN                | China   | 08/06/2001  | 01/03/2007 | SOURCE SIDE BORON IMPLANT AND DRAIN SIDE MDD IMPLANT FOR DEEP SUB 0.18 MICRON FLASH MEMORY                                                       |
| 100571326          | FMA13-00305CN          | China   | 09/15/2006  | 12/16/2009 | IMAGE PROCESSING APPARATUS AND METHOD FOR IMAGE RESIZING MATCHING DATA SUPPLY SPEED                                                              |
| 100547554          | FMA13-00310CN          | China   | 08/20/2007  | 10/07/2009 | ERROR PROCESSING METHOD AND INFORMATION PROCESSING APPARATUS                                                                                     |
| 100550588          | FMA13-00312CN          | China   | 10/30/2007  | 10/14/2009 | POWER SUPPLY CIRCUIT, POWER SUPPLY CONTROL CIRCUIT, AND POWER SUPPLY CONTROL METHOD                                                              |
| 101071984          | FMA13-00313CN          | China   | 05/10/2007  | 01/19/2011 | CONTROLLER FOR DC-DC CONVERTER                                                                                                                   |
| 101656477          | FMA13-00313CN DIV      | China   | 05/10/2007  | 10/03/2012 | DC-DC CONVERTER AND CONTROLLER OF THE DC-DC CONVERTER                                                                                            |
| 101106326          | FMA13-00314CN          | China   | 07/13/2007  | 06/09/2010 | DC-DC CONVERTER                                                                                                                                  |
| 101154892          | FMA13-00315CN          | China   | 09/28/2007  | 06/23/2010 | CONTROL CIRCUIT OF SYNCHRONOUS RECTIFICATION TYPE POWER SUPPLY UNIT, SYNCHRONOUS RECTIFICATION TYPE POWER SUPPLY UNIT AND CONTROL METHOD THEREOF |
| 101087105          | FMA13-00317CN          | China   | 05/11/2007  | 03/14/2012 | DC-DC CONVERTER AND CONTROL FOR DC-DC CONVERTER                                                                                                  |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                 |
|-----------------------|---------------------------|---------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------------|
| 101145731             | FMA13-00319CN             | China   | 08/22/2007  | 07/06/2011 | CONTROL CIRCUIT OF POWER SUPPLY UNIT, POWER SUPPLY UNIT<br>AND CONTROL METHOD THEREOF                                                 |
| 101247078             | FMA13-00320CN             | China   | 02/15/2008  | 05/30/2012 | DC-DC CONVERSION CIRCUIT, DC-DC CONVERSION CONTROL<br>CIRCUIT, AND DC-DC CONVERSION CONTROL METHOD                                    |
| 101247075             | FMA13-00321CN             | China   | 02/13/2008  | 06/09/2010 | POWER SOURCE CIRCUIT, POWER SOURCE CONTROL CIRCUIT AND<br>POWER SOURCE CONTROL METHOD                                                 |
| 101252356             | FMA13-00322CN             | China   | 01/28/2008  | 10/12/2011 | FRACTIONAL FREQUENCY DIVIDER PLL DEVICE AND CONTROL<br>METHOD THEREOF                                                                 |
| 100585996             | FMA13-00323CN             | China   | 09/14/2007  | 01/27/2010 | METHOD AND CIRCUIT FOR CONTROLLING DC-DC CONVERTER                                                                                    |
| 101636906             | FMA13-00335CN             | China   | 03/14/2007  | 01/02/2013 | OUTPUT CIRCUIT                                                                                                                        |
| 1251411               | FMA13-00344US             | China   | 09/12/2003  | 04/12/2006 | PHASELOCKED LOOP CLOCK GENERATING CIRCUIT AND CLOCK<br>GENERATING METHOD                                                              |
| 101247081             | FMA13-00347CN             | China   | 01/24/2008  | 05/02/2012 | DETECTION CIRCUIT AND POWER SOURCE SYSTEM                                                                                             |
| 101247082             | FMA13-00350CN             | China   | 01/24/2008  | 05/02/2012 | DETECTION CIRCUIT                                                                                                                     |
| 201310537550.2        | FMA13-00357CN             | China   | 06/18/2007  |            | STEP-UP/STEP-DOWN TYPE DC-DC CONVERTER, AND CONTROL<br>CIRCUIT AND CONTROL METHOD OF THE SAME                                         |
| 101552556             | FMA13-00366CN             | China   | 12/12/2008  | 02/13/2013 | DC-DC CONVERTER, DC-DC CONVERTER CONTROL METHOD, AND<br>ELECTRONIC DEVICE                                                             |
| 1183740               | FMA13-0042CN              | China   | 06/28/1997  | 01/05/2005 | OSCILLATOR AND PHASELOCKED LOOP USING THE SAME                                                                                        |
| 1086892               | FMA13-0042US              | China   | 06/28/1997  | 06/26/2002 | OSCILLATOR AND PHASE-LOCKED LOOP EMPLOYING SAME                                                                                       |
| 101714819             | FMA13-00432US             | China   | 09/17/2009  | 12/04/2013 | OUTPUT-VOLTAGE CONTROL APPARATUS, OUTPUT-VOLTAGE<br>CONTROL METHOD, AND ELECTRONIC APPARATUS (AS AMENDED)                             |
| 101753020             | FMA13-00471US<br>CON      | China   | 11/16/2009  | 06/05/2013 | OUTPUT VOLTAGE CONTROLLER, ELECTRONIC DEVICE, AND OUTPUT<br>VOLTAGE CONTROL METHOD                                                    |
| 1584120               | FMA13-00472US             | China   | 11/11/2008  | 02/11/2015 | METHOD OF DETECTING AN OPERATING CONDITION OF AN ELECTRIC<br>STEPPER MOTOR                                                            |
| 200710109427.5        | FMA13-00491JP             | China   | 06/18/2007  |            | STEP-UP/STEP-DOWN TYPE DC-DC CONVERTER, AND CONTROL<br>CIRCUIT AND CONTROL METHOD OF THE SAME                                         |
| 201410645436.6        | FMA13-00503CN             | China   | 03/14/2011  |            | SEMICONDUCTOR MEMORY                                                                                                                  |
| 1546287               | FMA13-00503US             | China   | 01/24/2013  |            | SEMICONDUCTOR MEMORY                                                                                                                  |
| ZL201110174962.5      | FMA13-00511US DIV         | China   | 06/22/2011  | 09/17/2014 | OSCILLATION CIRCUIT                                                                                                                   |
| 201110180133.8        | FMA13-00514CN             | China   | 06/24/2011  |            | OUTPUT SWITCHING CIRCUIT                                                                                                              |
| 201110240124.3        | FMA13-00516US             | China   |             |            | SWITCHING REGULATOR                                                                                                                   |
| 201110220791.5        | FMA13-00517US             | China   | 07/27/2011  |            | SWITCHING REGULATOR                                                                                                                   |
| 201110461288.9        | FMA13-00518US             | China   | 12/30/2011  |            | SEMICONDUCTOR DEVICE                                                                                                                  |
| 201110261652.7        | FMA13-00519US             | China   | 08/29/2011  |            | LEVEL SHIFT CIRCUIT AND SEMICONDUCTOR DEVICE                                                                                          |
| 201210055671.9        | FMA13-00525CN             | China   | 02/28/2012  |            | MOTOR CONTROL DEVICE, CONTROL PROGRAM THEREFOR, AND<br>METHOD FOR THE CONTROL                                                         |
| 201110461257.3        | FMA13-00526CN             | China   | 12/26/2011  |            | CONTROL CIRCUIT, ELECTRONIC DEVICE, AND METHOD FOR<br>CONTROLLING POWER SUPPLY                                                        |
| 201210177950.2        | FMA13-00528US<br>CON      | China   | 05/29/2012  |            | POWER SUPPLY DEVICE, CONTROL CIRCUIT, ELECTRONIC DEVICE<br>AND CONTROL METHOD FOR POWER SUPPLY                                        |
| 201210275497.9        | FMA13-00529US             | China   | 07/31/2012  |            | A/D CONVERTER                                                                                                                         |
| 201210274218.7        | FMA13-00531US             | China   | 08/03/2012  |            | SEMICONDUCTOR DEVICE AND VOLTAGE DIVIDER                                                                                              |
| 201210310346.2        | FMA13-00532CN             | China   | 08/22/2012  |            | CLOCK DATA RECOVERY CIRCUIT AND CLOCK DATA RECOVERY<br>METHOD                                                                         |
| 101026334             | FMA13-00533US             | China   | 06/15/2006  | 05/22/2013 | POWER SOURCE CONTROL CIRCUIT, POWER SUPPLY DEVICE, AND<br>CONTROL METHOD FOR THE SAME                                                 |
| 100483914             | FMA13-00539US             | China   | 03/04/2002  | 04/29/2009 | OVERVOLTAGE PROTECTOR FOR ELECTRIC POWER SYSTEM, AC/DC<br>CONVERTER AND DC/DC CONVERTER COMPOSED OF THE SAME<br>ELECTRIC POWER SYSTEM |
| 1240035               | FMA13-00543CN             | China   | 11/28/2002  | 02/01/2006 | SEMICONDUCTOR DEVICE EQUIPPED WITH SERIES TRANSMISSION<br>CIRCUIT                                                                     |
| 100376082             | FMA13-00544CN             | China   | 03/26/2002  | 03/19/2008 | PLL CIRCUIT MODE SWITCHING METHOD AND PLL CIRCUIT MODE<br>CONTROL CIRCUIT                                                             |
| 1240178               | FMA13-00551US             | China   | 12/20/2000  | 02/01/2006 | BIPOLAR SUPPLY VOLTAGE GENERATOR AND ITS SEMICONDUCTOR<br>DEVICE                                                                      |
| 100574074             | FMA13-00556US             | China   | 06/19/2006  | 12/23/2009 | DC-DC CONVERTER, AND ITS CONTROL CIRCUIT AND METHOD                                                                                   |
| 101043151             | FMA13-00561US             | China   | 09/18/2006  | 07/20/2011 | CIRCUIT AND METHOD FOR CONTROLLING DC-DC CONVERTER                                                                                    |
| 101018013             | FMA13-00562US             | China   | 06/19/2006  | 08/10/2011 | CURRENT-CONTROLLED DC-DC CONVERTER, CONTROL CIRCUIT AND<br>CONTROL METHOD FOR THE SAME                                                |
| 100566162             | FMA13-00563CN             | China   | 08/30/2006  | 12/02/2009 | CONTROL CIRCUIT OF POWER SUPPLY AND CONTROL METHOD OF<br>THE POWER SUPPLY                                                             |
| 200610112382.2        | FMA13-00564US             | China   | 08/31/2006  |            | ELECTRONIC DEVICE INCORPORATING SYSTEM POWER SUPPLY UNIT<br>AND METHOD FOR SUPPLYING POWER SUPPLY VOLTAGE                             |
| 101145699             | FMA13-00565US             | China   | 09/14/2007  | 01/12/2011 | POWER SUPPLY SYSTEM AND METHOD FOR CONTROLLING OUTPUT<br>VOLTAGE                                                                      |
| 101034850             | FMA13-00566US             | China   | 10/11/2006  | 01/19/2011 | DC-DC CONVERTER, CONTROL CIRCUIT THEREOF, CONTROL<br>METHOD THEREOF, AND POWER SUPPLY UNIT                                            |
| 101039067             | FMA13-00569US             | China   | 09/27/2006  | 08/31/2011 | CONTROL CIRCUIT OF POWER SUPPLY, POWER SUPPLY AND<br>CONTROL METHOD THEREOF                                                           |
| 200610086904.6        | FMA13-00570US             | China   | 02/22/2006  |            | RECONFIGURABLE CIRCUIT                                                                                                                |
| 101247051             | FMA13-00573CN             | China   | 02/13/2008  | 08/22/2012 | POWER SUPPLY CIRCUIT, POWER SUPPLY CONTROL CIRCUIT, AND<br>POWER SUPPLY CONTROL METHOD                                                |
| 201310329567.9        | FMA13-00574CN             | China   | 07/31/2013  |            | ADJUSTING APPARATUS AND ADJUSTMENT METHOD                                                                                             |
| 1168212               | FMA13-0093US DIV          | China   | 08/18/2000  | 09/22/2004 | FREQUENCY MEASUREMENT CIRCUIT                                                                                                         |
| 1238951               | FMA13-0122US              | China   | 03/07/2002  | 01/25/2006 | DC-DC CONVERTER POWER SOURCE CIRCUIT, METHOD FOR<br>CONTROLLING DC-DC CONVERTER AND METHOD FOR CONTROLLING<br>POWER SOURCE CIRCUIT    |
| 1251400               | FMA13-0129US              | China   | 05/17/2002  | 04/12/2006 | OPERATION AMPLIFIER WITH DEVIATION OFFSET FUNCTION                                                                                    |
| 1197163               | FMA13-0132CN              | China   | 03/15/2002  | 04/13/2005 | NON-VOLATILE SEMICONDUCTOR STORAGE DEVICE                                                                                             |
| 100576351             | FMA13-0132CN DIV          | China   | 03/15/2002  | 12/30/2009 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICES                                                                                              |

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|--------------------|------------------------|---------|-------------|------------|------------------------------------------------------------------------------------------------------------------------|
| 1246951            | FMA13-0136US           | China   | 05/29/2002  | 03/22/2006 | DC/DC CONVERTER CONTROL CIRCUIT AND DC/DC CONVERTER SYSTEM                                                             |
| 405451             | FMA13-0147CN           | China   | 01/10/2003  | 07/23/2008 | LIQUID DISPLAY DEVICE AND SIGNAL TRANSMITTING SYSTEM                                                                   |
| 1235182            | FMA13-0147US           | China   | 01/10/2003  | 01/04/2006 | INTEGRATED CIRCUIT FOR ELIMINATING CUMULATION OF DUTY RATIO ERROR                                                      |
| 1278277            | FMA13-0158US           | China   | 02/25/2003  | 10/04/2006 | FINGER MOBILE DETECTION METHOD AND APPTS. THEREOF                                                                      |
| 100397441          | FMA13-0164US           | China   | 05/21/2003  | 06/25/2008 | SEMICONDUCTOR DEVICE, DISPLAY DEVICE AND SIGNAL TRANSMISSION SYSTEM                                                    |
| 1225840            | FMA13-0169US           | China   | 05/20/2003  | 11/02/2005 | CIRCUIT FOR FREQUENCY SYNTHESIZER                                                                                      |
| 100521542          | FMA13-0172CN           | China   | 12/26/2002  | 07/29/2009 | SIGNADELTA MODULATOR OF PLL CIRCUIT                                                                                    |
| 1266841            | FMA13-0177US DIV2      | China   | 12/24/2003  | 07/26/2006 | SPREAD SPECTRUM CLOCK GENERATING CIRCUIT                                                                               |
| 100334455          | FMA13-0185US           | China   | 04/10/2003  | 08/29/2007 | PULSE WIDTH MEASURING APPARATUS WITH AUTO-RANGE SETTING FUNCTION                                                       |
| 100571040          | FMA13-0197CN           | China   | 11/28/2003  | 12/16/2009 | SIGMA-DELTA MODULATOR OF PLL CIRCUIT                                                                                   |
| 101394131          | FMA13-0210CN           | China   | 03/29/2005  | 12/05/2012 | SWITCHING REGULATOR CONTROL CIRCUIT, SWITCHING REGULATOR AND SWITCHING REGULATOR CONTROL METHOD                        |
| 100440096          | FMA13-0210US           | China   | 03/29/2005  | 12/03/2008 | SWITCHING REGULATOR CONTROL CIRCUIT, SWITCHING REGULATOR AND SWITCHING REGULATOR CONTROL METHOD                        |
| 100374868          | FMA13-0211US           | China   | 04/22/2005  | 03/12/2008 | CAPACITANCE DIFFERENCE DETECTING CIRCUIT AND MEMS SENSOR                                                               |
| 101015124          | FMA13-0217US           | China   | 09/08/2004  | 04/20/2011 | PLL FREQUENCY SYNTHESIZER                                                                                              |
| 100530630          | FMA13-0224US           | China   | 02/25/2005  | 08/19/2009 | SEMICONDUCTOR DEVICE                                                                                                   |
| 200510002822.4     | FMA13-0225US           | China   | 01/25/2005  |            | SEMICONDUCTOR DEVICE                                                                                                   |
| 100397334          | FMA13-0227US           | China   | 03/16/2005  | 06/25/2008 | SEMICONDUCTOR DEVICE                                                                                                   |
| 101388239          | FMA13-0234CN           | China   | 05/25/2005  | 05/23/2012 | SEMICONDUCTOR MEMORY DEVICE                                                                                            |
| 100477007          | FMA13-0234US DIV CON   | China   | 05/25/2005  | 04/08/2009 | SEMICONDUCTOR MEMORY DEVICE                                                                                            |
| 100555872          | FMA13-0238CN           | China   | 06/13/2005  | 10/28/2009 | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT AND A METHOD OF CONTROLLING THEREOF                                           |
| 100423424          | FMA13-0240US           | China   | 06/17/2005  | 10/01/2008 | MULTIPHASE DC-DC CONVERTER                                                                                             |
| 100456199          | FMA13-0241US           | China   | 06/13/2005  | 01/28/2009 | EARLY EFFECT CANCELLING CIRCUIT, DIFFERENTIAL AMPLIFIER, LINEAR REGULATOR, AND EARLY EFFECT CANCELING METHOD           |
| 100530917          | FMA13-0257US           | China   | 02/24/2006  | 08/19/2009 | DC-DC CONVERTER AND ITS CONTROL METHOD, AND SWITCHING REGULATOR AND ITS CONTROL METHOD                                 |
| 1913363            | FMA13-0260US           | China   | 12/08/2005  | 07/18/2012 | SUCCESSIVE APPROXIMATION A/D CONVERTER                                                                                 |
| 100414535          | FMA13-0263CN           | China   | 02/17/2006  | 08/27/2008 | RECONFIGURABLE INTEGRATED CIRCUIT DEVICE                                                                               |
| 1940991            | FMA13-0264US           | China   | 02/16/2006  | 05/12/2010 | RECONFIGURABLE ADDRESS GENERATION CIRCUIT FOR IMAGE PROCESSING, AND RECONFIGURABLE LSI COMPRISING THE SAME             |
| 101075809          | FMA13-0265US           | China   | 12/21/2005  | 12/22/2010 | CLOCK GENERATION CIRCUIT AND METHOD                                                                                    |
| 1885720            | FMA13-0266US           | China   | 11/23/2005  | 05/12/2010 | CLOCK GENERATING CIRCUIT AND CLOCK GENERATING METHOD                                                                   |
| 100514813          | FMA13-0273US           | China   | 02/17/2006  | 07/15/2009 | DC-DC CONVERTER AND DC-DC CONVERTER CONTROL METHOD                                                                     |
| 1929274            | FMA13-0276US           | China   | 03/27/2006  | 05/18/2011 | CONTROLLER AND CONTROL METHOD FOR DC-DC CONVERTER                                                                      |
| 100530916          | FMA13-0278US           | China   | 03/17/2006  | 08/19/2009 | STEP-UP TYPE DC-DC CONVERTER AND METHOD FOR CONTROLLING STEP-UP TYPE DC-DC CONVERTER                                   |
| 100461595          | FMA13-0279US           | China   | 03/17/2006  | 02/11/2009 | CONTROL CIRCUIT AND CONTROL METHOD FOR DC-DC CONVERTER                                                                 |
| 100511941          | FMA13-0280US           | China   | 03/31/2006  | 07/08/2009 | CONTROL CIRCUIT AND CONTROL METHOD FOR DC-DC CONVERTER                                                                 |
| 100514815          | FMA13-0281US           | China   | 04/27/2006  | 07/15/2009 | CONTROL CIRCUIT FOR DC-DC CONVERTER AND CONTROL METHOD THEREFOR                                                        |
| 100520971          | FMA13-0282CN           | China   | 09/27/2006  | 07/29/2009 | NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE, ERASE METHOD FOR SAME, AND TEST METHOD FOR SAME                              |
| 101034387          | FMA13-0287US           | China   | 10/25/2006  | 12/14/2011 | RECONFIGURABLE CIRCUIT                                                                                                 |
| 101047372          | FMA13-0288CN           | China   | 08/30/2006  | 12/02/2009 | PULSE WIDTH MODULATION CIRCUIT                                                                                         |
| 101047380          | FMA13-0300CN           | China   | 08/07/2006  | 09/29/2010 | COMMON INPUT/OUTPUT TERMINAL CONTROL CIRCUIT                                                                           |
| 1992494            | FMA13-0302US DIV       | China   | 06/09/2006  | 07/13/2011 | DC-DC CONVERTER AND CONTROL CIRCUIT FOR DC-DC CONVERTER                                                                |
| 395811             | G0063CN                | China   | 11/14/2001  | 05/14/2008 | ACCURATE VERIFY APPARATUS AND METHOD FOR NOR FLASH MEMORY CELLS IN THE PRESENCE OF HIGH COLUMN LEAKAGE                 |
| 02810072.7         | G0259CN                | China   | 02/19/2002  |            | FLASH MEMORY DEVICE WITH INCREASE OF EFFICIENCY DURING AN APDE (AUTOMATIC PROGRAM DISTURB AFTER ERASE) PROCESS         |
| 03817695.5         | G0391CN                | China   | 06/10/2003  | 12/26/2008 | BUILT-IN-SELF-TEST (BIST) OF FLASH MEMORY CELLS AND IMPLEMENTATION OF BIST INTERFACE                                   |
| 357578             | G0689CN                | China   | 12/11/2002  | 11/14/2007 | SHALLOW TRENCH ISOLATION APPROACH FOR IMPROVED STI CORNER ROUNDING                                                     |
| 375132             | G0730CN                | China   | 09/24/2003  | 01/30/2008 | METHOD AND SYSTEM FOR REDUCING CONTACT DEFECTS USING NON CONVENTIONAL CONTACT FORMATION METHOD FOR SEMICONDUCTOR CELLS |
| 200480003688.3     | G0752CN                | China   | 01/08/2004  | 02/27/2009 | IMPROVED PERFORMANCE IN FLASH MEMORY DEVICES                                                                           |
| 03807746.9         | G0861CN                | China   | 02/14/2003  |            | IMPROVED ERASE METHOD FOR SINGLE SIDED MIRROR OPERATION                                                                |
| 03807744.2         | G0862CN                | China   | 02/14/2003  | 04/28/2010 | REFRESH SCHEME FOR DYNAMIC PAGE PROGRAMMING                                                                            |
| 03807742.6         | G0864CN                | China   | 02/14/2003  | 09/09/2009 | REFRESH SCHEME FOR DYNAMIC PAGE PROGRAMMING                                                                            |
| 03825406.9         | G0865CN                | China   | 07/10/2003  | 04/08/2009 | MOCVD FORMATION OF Cu <sub>2</sub> S                                                                                   |
| ZL03811863.7       | G0866CN                | China   | 04/22/2003  | 04/22/2003 | STEPPED PRE-ERASE VOLTAGE FOR MIRRORBIT ERASE                                                                          |
| 422711             | G0871CN                | China   | 07/10/2003  | 08/27/2008 | LATERAL DOPED CHANNEL                                                                                                  |
| 03825466.2         | G0878CN                | China   | 07/10/2003  |            | A METHOD AND SYSTEM FOR ERASING A NITRIDE MEMORY DEVICE                                                                |
| 03803612.6         | G1255CN                | China   | 02/05/2003  | 05/23/2012 | PARTIAL PAGE PROGRAMMING OF MULTI LEVEL FLASH                                                                          |
| 03824885.9         | H0297CN                | China   | 07/10/2003  | 03/21/2012 | CONTROL OF MEMORY ARRAYS UTILIZING ZENER DIODE-LIKE DEVICES                                                            |

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| 691233                | H0325CN                  | China   | 09/19/2005  | 10/27/2010 | CONTROL OF MEMORY DEVICES POSSESSING VARIABLE RESISTANCE CHARACTERISTICS                                                  |
| 03825408.5            | H0343CN                  | China   | 07/10/2003  | 03/03/2010 | MOCVD FORMATION OF Cu <sub>2</sub> S                                                                                      |
| 479416                | H0346CN                  | China   | 02/11/2005  | 10/31/2008 | IN-SITU SURFACE TREATMENT FOR MEMORY CELL FORMATION                                                                       |
| 200480006699.7        | H0354CN                  | China   | 03/01/2004  |            | SPIN ON POLYMERS FOR ORGANIC MEMORY DEVICES                                                                               |
| 200580017617.3        | H0368CN                  | China   | 02/11/2005  |            | POLYMER DIELECTRICS FOR ME ARRAY INTERN CONNECT                                                                           |
| 201410164564.9        | H0368CN DIV              | China   | 02/11/2005  |            | POLYMER DIELECTRICS FOR ME ARRAY INTERN CONNECT                                                                           |
| 652843                | H0385CN                  | China   | 09/08/2003  | 07/28/2010 | AN ORGANIC MEMORY DEVICE AND METHOD FOR FORMING A MEMORY CELL                                                             |
| 200480039780.5        | H0416CN                  | China   | 09/23/2004  | 04/17/2009 | SIDEWALL FORMATION FOR HIGH DENSITY POLYMER MEMORY ELEMENT ARRAY                                                          |
| 791975                | H0422CN                  | China   | 05/11/2004  | 06/08/2011 | METHOD AND SYSTEM FOR MANUFACTURING POLYMER MEMORY DEVICE IN VIA OPENING                                                  |
| 689908                | H0423CN                  | China   | 09/16/2004  | 10/13/2010 | SELF ASSEMBLY OF CONDUCTING POLYMER FOR FORMATION OF POLYMER MEMORY CELL                                                  |
| 03824963.4            | H0434CN                  | China   | 07/10/2003  | 09/09/2009 | STACKED ORGANIC MEMORY DEVICES AND METHODS OF OPERATING AND FABRICATING                                                   |
| 200480015312.4        | H0437CN                  | China   | 05/11/2004  | 08/08/2008 | PLANAR POLYMER MEMORY DEVICE                                                                                              |
| 200480025672.2        | H0442CN                  | China   | 05/21/2004  |            | ORGANIC MEMORY DEVICE AND METHODS OF USING AND MAKING THE DEVICE                                                          |
| 03824837.9            | H0514CN                  | China   | 06/10/2003  | 07/18/2008 | NITROGEN OXIDATION TO REDUCE ENCROACHMENT                                                                                 |
| 200480022338.1        | H0541CN                  | China   | 07/15/2004  | 08/08/2012 | LOW POWER CHARGE PUMP                                                                                                     |
| 03825526.X            | H0570CN                  | China   | 07/24/2003  |            | IMPROVED SYSTEM FOR PROGRAMMING A NON-VOLATILE MEMORY CELL                                                                |
| 03825514.6            | H0575CN                  | China   | 07/24/2003  | 08/19/2009 | IMPROVED PRE-CHARGE METHOD FOR READING A NON-VOLATILE MEMORY CELL ARRAY WITH STAGGERED LOCAL INTERCONNECT STRUCTURE       |
| 200480030197.8        | H0576CN                  | China   | 09/16/2004  | 04/28/2010 | RECESS CHANNEL FLASH ARCHITECTURE FOR REDUCED SHORT CHANNEL EFFECT                                                        |
| 200480029724.3        | H0577CN                  | China   | 09/16/2004  |            | METHOD OF PROGRAMMIN DUAL CELL MEMORY DEVICE TO STORE MULTIPLE DATA STATES PER CELL                                       |
| 200480010297.4        | H0587CN                  | China   | 03/08/2004  |            | METHOD OF DUAL CELL MEMORY DEVICE OPERATION FOR IMPROVED END-OF-LIFE READ MARGIN                                          |
| 204480011031.1        | H0588CN                  | China   | 03/08/2004  | 03/08/2004 | IMPROVED METHOD FOR READING A NON-VOLATILE MEMORY CELL ADJACENT TO AN INACTIVE REGION OF A NON-VOLATILE MEMORY CELL ARRAY |
| 844990                | H0625CN                  | China   | 01/08/2004  | 09/28/2011 | MEMORY DEVICE AND METHOD USING POSITIVE GATE STRESS TO RECOVER OVERERASED CELL                                            |
| 691340                | H0626CN                  | China   | 09/16/2004  | 10/27/2010 | IMPROVED PERFORMANCE IN FLASH MEMORY DEVICES                                                                              |
| 200480003682.6        | H0671CN                  | China   | 01/08/2004  | 08/26/2009 | CASCADE AMPLIFIER CIRCUIT FOR PRODUCING A FAST, STABLE AND ACCURATE BITLINE VOLTAGE                                       |
| 03825310.0            | H1203CN                  | China   | 07/10/2003  | 04/08/2009 | SELECTION CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS                                                                     |
| 200480003827.2        | H1204CN                  | China   | 01/08/2004  | 06/05/2009 | CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS                                                                               |
| 03825566.9            | H1205CN                  | China   | 07/24/2003  |            | PECVD SILICON-RICH OXIDE LAYER FOR REDUCED UV CHARGING                                                                    |
| 382619                | H1368CN                  | China   | 06/18/2004  | 03/05/2008 | NON-VOLATILE MEMORY DEVICE                                                                                                |
| 200480016228.4        | H1414CN                  | China   | 06/05/2004  |            | FLASH MEMORY DEVICE                                                                                                       |
| 839249                | H1415CN                  | China   | 10/26/2004  | 09/14/2011 | CIRCUIT FOR FAST AND ACCURATE MEMORY READ OPERATIONS                                                                      |
| 200480006883.1        | H1513CN                  | China   | 03/01/2004  | 03/01/2004 | MEMORY CELL STRUCTURE HAVING NITRIDE LAYER WITH REDUCED CHARGE LOSS AND METHOD FOR FABRICATING SAME                       |
| 2004800255363         | H1862CN                  | China   | 08/31/2004  | 12/26/2008 | FAST, ACCURATE AND LOW POWER SUPPLY VOLTAGE BOOSTER USING A/D CONVERTER                                                   |
| 200480009300.0        | H1892CN                  | China   | 03/08/2004  | 10/21/2009 | A MEMORY DEVICE WITH A SELF-ASSEMBLED POLYMER FILM AND METHOD OF MAKING THE SAME                                          |
| 02811337.3            | H1971CN                  | China   | 05/07/2002  |            | FLOATING GATE MEMORY DEVICE USING COMPOSITE MOLECULAR MATERIAL                                                            |
| ZL02812491.X          | H1973CN                  | China   | 05/07/2002  | 09/20/2006 | MEMORY SWITCH                                                                                                             |
| 02811743.3            | H1975CN                  | China   | 05/07/2002  |            | ORGANIC THIN FILM ZENER DIODES                                                                                            |
| 03821987.5            | H1978CN                  | China   | 09/08/2003  |            | MEMORY CELL                                                                                                               |
| 01823537.9            | H1979CN                  | China   | 08/13/2001  |            | METHODS AND APPARATUS FOR WORDLINE PROTECTION IN FLASH MEMORY DEVICES                                                     |
| 200580014381.8        | H1984CN                  | China   | 02/11/2005  | 12/26/2012 | POCKET IMPLANT FOR COMPLEMENTARY BIT DISTURB IMPROVEMENT AND CHARGING IMPROVEMENT OF SONOS MEMORY CELL                    |
| 200480040307.9        | H1985CN                  | China   | 12/17/2004  |            | POCKET IMPLANT FOR COMPLEMENTARY BIT DISTURB IMPROVEMENT AND CHARGING IMPROVEMENT OF SONOS MEMORY CELL                    |
| 201010126772.1        | H1985CN DIV              | China   | 02/22/2010  |            | METHOD OF FORMING NARROWLY SPACED FLASH MEMORY CONTACT OPENINGS                                                           |
| 635824                | H1990CN                  | China   | 04/29/2005  | 06/09/2010 | BITLINE IMPLANT UTILIZING DUAL POLY                                                                                       |
| 200580015098.7        | H1993CN                  | China   | 02/11/2005  | 04/15/2009 | NON-CRITICAL COMPLEMENTARY MASKING METHOD FOR POLY-1 DEFINITION IN FLASH MEMORY DEVICE FABRICATION                        |
| 200680010634.9        | H1998CN                  | China   | 04/04/2006  |            | USE OF SUPERCRITICAL FLUID TO DRY WAFER AND CLEAN LENS IN IMMERSION LITHOGRAPHY                                           |
| 101467102             | H2114CN                  | China   | 06/23/2006  | 01/11/2012 | METHOD FOR FORMING A SHALLOW TRENCH ISOLATION STRUCTURE WITH IMPROVED CORNER ROUNDING                                     |
| 357578                | P116WO-CN                | China   | 12/11/2002  | 11/14/2007 | METHOD SYSTEM AND CIRCUIT FOR PROGRAMMING A NON-VOLATILE MEMORY ARRAY                                                     |
| 200480039400.8        | P-5484US                 | China   | 10/27/2004  |            | METHOD CIRCUIT AND SYSTEM FOR DETERMINING A REFERENCE VOLTAGE                                                             |
| 200480038992.1        | P-5487-CN                | China   | 10/27/2004  |            | METHOD CIRCUIT AND SYSTEM FOR DETERMINING A REFERENCE VOLTAGE                                                             |
| 200480039234.1        | P-5487-CN                | China   | 10/27/2004  |            | THRESHOLD VOLTAGE SHIFT IN NROM CELLS                                                                                     |
| 200610091700.1        | P-7632EP                 | China   | 04/11/2006  |            |                                                                                                                           |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                     |
|-----------------------|---------------------------|---------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 455864                | SE0002CN                  | China   | 03/11/2003  | 03/11/2003 | A SYSTEM AND METHOD OF ERASE VOLTAGE CONTROL DURING MULTIPLE SECTOR ERASE OF A FLASH MEMORY DEVICE                                        |
| 201080029411.3        | SP09-0001CN               | China   | 12/29/2011  |            | ELECTRONIC DEVICE HAVING A MOLDING COMPOUND INCLUDING A COMPOSITE MATERIAL                                                                |
| 201380041113.X        | SP09-0030CN               | China   | 05/24/2013  |            | METHOD, APPARATUS, AND MANUFACTURE FOR FLASH MEMORY ADAPTIVE ALGORITHM                                                                    |
| 201280069204.X        | SP09-0056US               | China   | 12/07/2012  |            | HIGH SPEED SERIAL PERIPHERAL INTERFACE MEMORY SUBSYSTEM                                                                                   |
| 201380040574.5        | SP09-0058CN               | China   | 07/31/2013  |            | POWER SAVINGS APPARATUS AND METHOD FOR MEMORY DEVICE USING DELAY LOCKED LOOP                                                              |
| 201180067812.2        | SP10-0007CN               | China   | 12/17/2011  |            | SELF-ALIGNED NAND FLASH SELECT-GATE WORDLINES FOR SPACER DOUBLE PATTERNING                                                                |
| 201180067895.5        | SP10-0008CN               | China   | 12/19/2011  |            | EDGE ROUNDED FIELD EFFECT TRANSISTORS AND METHODS OF MANUFACTURING                                                                        |
| 201180067986.9        | SP10-0009CN               | China   | 12/19/2011  |            | PROCESS MARGIN ENGINEERING IN CHARGE TRAPPING FIELD EFFECT TRANSISTORS                                                                    |
| 201180068369.0        | SP10-0012CN               | China   | 12/29/2011  |            | MEMORY WITH EXTENDED CHARGE TRAPPING LAYER                                                                                                |
| 201380037766.0        | SP11-0015US               | China   | 05/14/2013  |            | SOFT ERROR RESISTANT CIRCUITRY                                                                                                            |
| 201310106856.2        | SP11-0021CN               | China   | 03/29/2013  |            | APPARATUS AND METHOD FOR A REDUCED PIN COUNT (PRC) MEMORY BUS INTERFACE INCLUDING A READ DATA STROBE SIGNAL                               |
| 201380020561.1        | SP11-0027CN               | China   | 02/08/2013  |            | IMPROVING REDUNDANCY LOADING EFFICIENCY                                                                                                   |
| 201310030270.2        | SP11-0034US               | China   | 01/25/2013  |            | CONTINUOUS READ BURST SUPPORT AT HIGH CLOCK RATES                                                                                         |
| 201380070070.3        | SP11-0042CN               | China   | 12/14/2012  |            | ACOUSTIC PROCESSING UNIT                                                                                                                  |
| 201380018825.X        | SP12-0013CN               | China   | 04/01/2013  |            | ADAPTIVELY PROGRAMMING OR ERASING FLASH MEMORY BLOCKS                                                                                     |
| 201380047005.3        | SP12-0017CN               | China   | 07/08/2013  |            | LEAKAGE REDUCING WRITELINE CHARGE PROTECTION CIRCUIT                                                                                      |
| 201380049319.7        | SP12-0021CN               | China   | 07/29/2013  |            | BITLENE VOLTAGE REGULATION IN NON-VOLATILE MEMORY                                                                                         |
| 201510087363.8        | SP13-0036CN               | China   | 02/25/2015  |            | MEMORY SUBSYSTEM WITH WRAPPED-TO-CONTINUOUS READ                                                                                          |
| 0656628               | A938EP                    | EPO     | 11/10/1994  | 04/09/2003 | PROGRAMMED REFERENCE                                                                                                                      |
| 1222663               | AF01002EP                 | EPO     | 10/07/2000  | 06/30/2004 | LOW VOLTAGE READ CASCODE FOR 2V/3V AND DIFFERENT BANK COMBINATIONS WITHOUT METAL OPTIONS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE |
| 01918843.2            | AF01064EP                 | EPO     | 03/20/2001  |            | METHOD FOR FORMING HIGH QUALITY MULTIPLE THICKNESS OXIDE LAYERS BY USING HIGH TEMPERATURE DESCUM                                          |
| 01959947.1            | AF01066EP                 | EPO     | 03/20/2001  |            | METHOD FOR FORMING HIGH QUALITY MULTIPLE THICKNESS OXIDE LAYERS BY REDUCING DESCUM INDUCED DEFECTS                                        |
| 1344221               | AF01073EP                 | EPO     | 07/31/2001  | 11/05/2008 | WORD LINE DECODING ARCHITECTURE IN A FLASH MEMORY                                                                                         |
| 1226586               | AF01086WO                 | EPO     | 09/29/2000  | 06/18/2003 | WORD LINE TRACKING IN WHOLE CHIP                                                                                                          |
| 01931109.1            | AF01088EP                 | EPO     | 03/05/2001  |            | SINGLE TUNNEL GATE OXIDATION PROCESS FOR FABRICATING NAND FLASH MEMORY                                                                    |
| 02721396.6            | AF01094EPC                | EPO     | 03/14/2002  |            | VOLTAGE BOOST CIRCUIT USING SUPPLY VOLTAGE DETECTION TO COMPENSATE FOR SUPPLY VOLTAGE VARIATIONS IN READ MODE VOLTAGES                    |
| 1415302               | AF01096EP                 | EPO     | 12/12/2001  | 12/07/2005 | SOFT PROGRAM AND SOFT PROGRAM VERIFY OF THE CORE CELLS IN FLASH MEMORY ARRAY                                                              |
| 1338034               | AF01102EP                 | EPO     | 08/07/2001  | 01/06/2010 | SIMULTANEOUS FORMATION CHARGE STORAGE AND BITLENE TO WORDLINE ISOLATION                                                                   |
| 1338037               | AF01112EP                 | EPO     | 11/15/2001  | 03/30/2011 | NON-VOLATILE SONOS SEMICONDUCTOR MEMORY DEVICE                                                                                            |
| 60316931.7            | AF01116WO                 | EPO     | 03/03/2003  |            | METHOD FOR MULTI-BIT FLASH READS USING DUAL DYNAMIC REFERENCES                                                                            |
| 02792367.1            | AF01124EP                 | EPO     | 12/11/2002  |            | MONOS DEVICE HAVING BURIED METAL SILICIDE BIT LINE                                                                                        |
| 1493185               | AF01137EP                 | EPO     | 02/14/2003  | 11/11/2009 | MEMORY MANUFACTURING PROCESS WITH BITLENE ISOLATION                                                                                       |
| 1665387               | AF01182                   | EPO     | 05/21/2004  | 08/13/2008 | MEMORY DEVICE HAVING HIGH WORK FUNCTION GATE AND METHOD OF ERASING SAME                                                                   |
| 04815008.0            | AF01214EP                 | EPO     | 12/17/2004  |            | EFFICIENT USE OF WAFER AREA WITH DEVICE UNDER THE PAD APPROACH                                                                            |
| 06786259.9            | AF01293EP                 | EPO     | 06/30/2006  |            | PREAMORPHIZATION TO MINIMIZE VOID FORMATION                                                                                               |
| 06803004.8            | AF01310EP                 | EPO     | 09/06/2006  |            | SEMICONDUCTOR MEMORY DEVICE COMPRISING ONE OR MORE INJECTING BILAYER ELECTRODES                                                           |
| 1788582               | AF01329EP                 | EPO     | 08/30/2004  | 04/28/2010 | ERASE METHOD OF A NON-VOLATILE MEMORY DEVICE AND A NON-VOLATILE MEMORY DEVICE                                                             |
| 1717816               | AF01372                   | EPO     | 02/19/2004  | 12/24/2008 | CURRENT-VOLTAGE CONVERTER CIRCUIT AND CONTROL METHOD THEREOF                                                                              |
| 04713227.9            | AF01376EP                 | EPO     | 02/20/2004  |            | SEMICONDUCTOR STORAGE DEVICE AND REDUNDANCY METHOD FOR SEMICONDUCTOR STORAGE DEVICE                                                       |
| 1720172               | AF01377EP                 | EPO     | 02/20/2004  | 06/06/2012 | A SEMICONDUCTOR MEMORY STORAGE DEVICE AND ITS REDUNDANCY CONTROL METHOD                                                                   |
| 1782460               | AF01379EP                 | EPO     | 04/29/2005  | 06/01/2011 | METHOD FOR FABRICATING A FLOATING GATE MEMORY CELL                                                                                        |
| 1717814               | AF01380EP                 | EPO     | 02/20/2004  | 09/19/2012 | SEMICONDUCTOR STORAGE DEVICE AND SEMICONDUCTOR STORAGE DEVICE CONTROL METHOD                                                              |
| 1788578               | AF01432EP                 | EPO     | 08/31/2004  | 05/11/2011 | THE SEMICONDUCTOR MEMORY STORAGE DEVICE WHICH CARRIED THE NEGATIVE VOLTAGE GENERATING CIRCUIT                                             |
| 1830366               | AF01438EP                 | EPO     | 12/24/2004  | 07/13/2011 | BIAS APPLICATION METHOD OF STORAGE AND STORAGE                                                                                            |
| 04808002.2            | AF01445EP                 | EPO     | 12/28/2004  |            | SONOS WITH USE OF SWITCH GATE, WITHOUT BURIED DIFFUSION LAYER BITLENE                                                                     |
| 18832929              | AF01482EP                 | EPO     | 05/26/2006  | 02/06/2008 | PAGE BUFFER ARCHITECTURE FOR PROGRAMMING, ERASING AND READING NANOSCALE RESISTIVE MEMORY DEVICES                                          |
| 1829048               | AF01485EP                 | EPO     | 12/20/2005  | 06/15/2011 | METHOD OF PROGRAMMING, READING AND ERASING MEMORY-DIODE IN A MEMORY-DIODE ARRAY                                                           |
| 1899977               | AF01586EP                 | EPO     | 06/30/2006  | 07/30/2014 | METHOD FOR PROGRAMMING A MEMORY DEVICE                                                                                                    |
| 06788225.8            | AF01638EP                 | EPO     | 07/21/2006  |            | MEMORY DEVICE WITH BARRIER LAYER                                                                                                          |
| 06749242.1            | AF01665EP                 | EPO     | 04/04/2006  |            | SPLIT GATE MULTI-BIT MEMORY CELL                                                                                                          |

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|-----------------------|---------------------------|---------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 06803199.6            | AF01668EP                 | EPO     | 09/08/2006  |            | HIGH PERFORMANCE FLASH MEMORY DEVICE USING A PROGRAMMING WINDOW FOR PREDETERMINATION OF BITS TO BE PROGRAMMED AND DC-TO-DC CONVERTER                   |
| 06814339.5            | AF01669EP                 | EPO     | 09/07/2006  |            | MULTI-BIT FLASH MEMORY DEVICE HAVING IMPROVED PROGRAM RATE                                                                                             |
| 06814331.2            | AF01673EP                 | EPO     | 09/07/2006  |            | FLASH MEMORY PROGRAMMING USING AN INDICATION BIT TO INTERPRET STATE                                                                                    |
| 1908077               | AF01676EP                 | EPO     | 07/17/2006  | 01/19/2009 | IMPROVED READ MODE FOR FLASH MEMORY                                                                                                                    |
| 05737365.6            | AF01728EP                 | EPO     | 04/27/2005  |            | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR                                                                                                 |
| 06739368.6            | AF01730EP                 | EPO     | 03/24/2006  |            | MULTI CHIP MODULE AND METHOD OF MANUFACTURE                                                                                                            |
| 06802940.4            | AF01746EP                 | EPO     | 09/06/2006  |            | SPACERS BETWEEN BITLINES IN VIRTUAL GROUND MEMORY                                                                                                      |
| 1898460               | AF01792EP                 | EPO     | 06/28/2005  | 01/04/2012 | MIRRORBIT DEVICE HAVING STI AND DUAL POLY FILMS                                                                                                        |
| 07753350.3            | AF01810EP                 | EPO     | 03/16/2007  |            | VERTICAL EEPROM DEVICE                                                                                                                                 |
| 06804173.0            | AF01828EP                 | EPO     | 09/26/2006  |            | DIGITAL DATA TRANSFER BETWEEN DIFFERENT CLOCK DOMAINS                                                                                                  |
| 07852715.7            | AF01836                   | EPO     | 10/12/2007  |            | SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME                                                                                                |
| 1907868               | AF01852EP                 | EPO     | 07/07/2006  | 07/29/2010 | INTEGRATED CIRCUIT TEST SOCKET                                                                                                                         |
| 06816539.8            | AF01853EP                 | EPO     | 10/06/2006  |            | MEMORY ARRAY ARRANGED IN BANKS AND SECTORS AND ASSOCIATED DECODERS                                                                                     |
| 07754965.7            | AF01907WO                 | EPO     | 04/05/2007  |            | MULTI MEDIA CARD WITH HIGH STORAGE CAPACITY                                                                                                            |
| 07754992.1            | AF01954                   | EPO     | 04/05/2007  |            | MEMORY CELL ARRAY WITH LOW RESISTANCE COMMON SOURCE AND HIGH CURRENT DRIVABILITY                                                                       |
| 07837325.5            | AF02067EP                 | EPO     | 08/23/2007  |            | MEMORY ERASE MANAGEMENT SYSTEM                                                                                                                         |
| 1310994               | AF02184EP                 | EPO     | 07/17/2000  | 02/13/2013 | NONVOLATILE MEMORY DEVICE AND                                                                                                                          |
| 01402621.5            | AF02192EP                 | EPO     | 10/10/2001  |            | SEMICONDUCTOR MEMORY AND MANUFACTURING                                                                                                                 |
| 01118675.6            | AF02198EP                 | EPO     | 08/03/2001  |            | SEMICONDUCTOR MEMORY DEVICE AND DRIVING                                                                                                                |
| 1286359               | AF02200                   | EPO     | 03/18/2002  | 01/17/2007 | MEMORY CONTROLLER FOR MULTI LEVEL                                                                                                                      |
| 03009892.5            | AF02212EP                 | EPO     | 05/15/2003  |            | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                                |
| 1574867               | AF02230EP                 | EPO     | 12/17/2003  | 08/08/2007 | SEMICONDUCTOR DEVICE AND TEST METHOD                                                                                                                   |
| 06811935.3            | AF02243EP                 | EPO     | 10/18/2006  |            | A VOLTAGE DETECTOR CIRCUIT                                                                                                                             |
| 07811531.8            | AF02282EP                 | EPO     | 08/23/2007  |            | MULTIPLE COMMUNICATION CHANNELS ON MMC OR SD CMD LINE                                                                                                  |
| 08780275.7            | AF02465EP                 | EPO     | 07/21/2008  |            | TERMINATE CYCLE FOR BURST WRITE OPERATION                                                                                                              |
| 08743943.6            | AF02477EP                 | EPO     | 03/14/2008  |            | DIVISION-BASED SENSING AND PARTITIONING OF ELECTRONIC MEMORY                                                                                           |
| 08755298.0            | AF02560EP                 | EPO     | 05/12/2008  |            | DIE ATTACHMENT, DIE STACKING, AND WIRE EMBEDDING USING FILM                                                                                            |
| 00904420.7            | AF02593EP                 | EPO     | 01/18/2000  |            | SHARED MEMORY APPARATUS AND METHOD FOR MULTIPROCESSOR SYSTEMS                                                                                          |
| 11816997.8            | AF03209EP                 | EPO     | 08/10/2011  |            | STITCH BUMP STACKING DESIGN FOR OVERALL PACKAGE SIZE REDUCTION FOR MULTIPLE STACK                                                                      |
| 11804189.6            | AF03219EP                 | EPO     | 06/29/2011  |            | METHOD AND SYSTEM FOR THIN MULTI CHIP STACK PACKAGE WITH FILM ON WIRE AND COPPER WIRE                                                                  |
| 12860893.2            | AF04035EP                 | EPO     | 12/18/2012  |            | ACOUSTIC PROCESSING UNIT INTERFACE                                                                                                                     |
| 12859642.6            | AF04036EP                 | EPO     | 12/18/2012  |            | ARITHMETIC LOGIC UNIT ARCHITECTURE                                                                                                                     |
| 0963587               | C144496EP                 | EPO     | 02/05/1998  | 01/16/2002 | HIGH VOLTAGE NMOS PASS GATE FOR INTEGRATED CIRCUIT WITH HIGH VOLTAGE GENERATOR AND FLASH NON-VOLATILE MEMORY DEVICE HAVING THE PASS GATE               |
| 0944907               | C196596EP                 | EPO     | 11/13/1997  | 10/17/2001 | BANK ARCHITECTURE FOR A NON-VOLATILE MEMORY ENABLING SIMULTANEOUS READING AND WRITING                                                                  |
| 1040486               | C369297EP                 | EPO     | 12/18/1998  | 02/27/2002 | BIASING METHOD AND STRUCTURE FOR REDUCING BAND-TO-BAND AND/OR AVALANCHE CURRENTS DURING THE ERASE OF FLASH MEMORY DEVICES                              |
| 1042810               | C627497EP                 | EPO     | 12/18/1998  | 05/20/2010 | METHODS AND ARRANGEMENTS FOR IMPROVED FORMATION OF CONTROL AND FLOATING GATES IN NON-VOLATILE MEMORY SEMICONDUCTOR DEVICES                             |
| 1247299               | C656497EP                 | EPO     | 08/31/2000  | 04/11/2007 | TUNGSTEN GATE MOS TRANSISTOR AND MEMORY CELL AND METHOD OF MAKING SAME                                                                                 |
| 1204989               | C695497EP                 | EPO     | 06/29/2000  | 04/02/2014 | THIN FLOATING GATE AND CONDUCTIVE SELECT GATE IN SITU                                                                                                  |
| 1116240               | C715497                   | EPO     | 09/21/1999  | 11/13/2002 | WORDLINE DRIVER FOR FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EEPROM)                                                                 |
| 1125302               | D138                      | EPO     | 10/05/1999  | 01/08/2003 | SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON-VOLATILE MEMORY ARRAY                                                                                  |
| 1116238               | D139                      | EPO     | 08/16/1999  | 02/26/2003 | BANK SELECTOR CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITETURE                                      |
| 1116239               | D168                      | EPO     | 08/16/1999  | 05/15/2002 | SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                                          |
| 1116236               | D169                      | EPO     | 08/16/1999  | 05/15/2002 | METHOD OF MAKING FLEXIBLY PARTITIONED METAL LINE SEGMENTS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE |
| 1125301               | D170                      | EPO     | 08/16/1999  | 10/16/2002 | MEMORY ADDRESS DECODING CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                           |
| 1175680               | D832EP                    | EPO     | 05/05/2000  | 02/26/2003 | RAMPED OR STEPPED GATE CHANNEL ERASE FOR FLASH MEMORY APPLICATION                                                                                      |
| 1214715               | D833EP                    | EPO     | 08/29/2000  | 10/15/2009 | 1 TRANSISTOR FOR EEPROM APPLICATION                                                                                                                    |
| 00983940.8            | D853                      | EPO     | 12/05/2000  |            | METHOD TO PROVIDE A REDUCED CONSTANT E-FIELD DURING ERASE OF EEPROMS FOR RELIABILITY IMPROVEMENT                                                       |
| 1218941               | D877EP                    | EPO     | 07/17/2000  | 04/02/2014 | NON-VOLATILE MEMORY HAVING HIGH GATE COUPLING CAPACITANCE                                                                                              |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                 |
|-----------------------|---------------------------|---------|-------------|------------|-----------------------------------------------------------------------------------------------------------------------|
| 1222690               | D894EP                    | EPO     | 09/29/2000  | 01/23/2008 | METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITH REDUCED ARC LOSS IN PERIPHERAL CIRCUITRY REGION                   |
| 00984473.9            | D958EP                    | EPO     | 12/13/2000  |            | NOVEL NITRIDATION BARRIERS FOR NITRIDATED TUNNEL OXIDE FOR CIRCUITRY FOR FLASH TECHNOLOGY AND FOR LOCOS/STI ISOLATION |
| 1218938               | DA01016EP                 | EPO     | 07/14/2000  | 12/19/2007 | METHOD FOR PROVIDING A DOPANT LEVEL FOR POLYSILICON FOR FLASH MEMORY DEVICES                                          |
| 00943282.4            | E0197EP                   | EPO     | 06/29/2000  |            | NEW METHOD OF FORMING SELECT GATE TO IMPROVE RELIABILITY AND PERFORMANCE FOR NAND-TYPE FLASH MEMORY DEVICES           |
| 1256116               | E0251                     | EPO     | 07/14/2000  | 09/03/2003 | FLASH MEMORY ARCHITECTURE EMPLOYING THREE LAYER METAL INTERCONNECT                                                    |
| 01916283.3            | E0255EP                   | EPO     | 02/27/2001  |            | CHARGE SHARING TO HELP BOOST THE WORDLINES DURING APDE VERIFY                                                         |
| 1266382               | E0264                     | EPO     | 02/07/2001  | 01/02/2004 | TRIMMING METHOD FOR WORDLINE BOOSTER TO MINIMIZE PROCESS VARIATION OF BOOSTED WORDLINE VOLTAGE                        |
| 1282915               | E0302EP                   | EPO     | 05/01/2001  | 11/05/2014 | UNIFORM BITLINE STRAPPING OF NON-VOLATILE MEMORY CELL                                                                 |
| 01916603.2            | E0370EP                   | EPO     | 03/12/2001  |            | A DUAL SPACER PROCESS NON-VOLATILE MEMORY DEVICES                                                                     |
| 1350253               | F0257EP                   | EPO     | 08/07/2001  | 09/22/2010 | METHOD AND SYSTEM FOR EMBEDDED CHIP ERASE VERIFICATION                                                                |
| 01990221.2            | F0260EP                   | EPO     | 12/12/2001  |            | METHOD AND APPARATUS FOR BOOSTING BITLINES FOR LOW VCC READ                                                           |
| 1366497               | F0274EP                   | EPO     | 11/01/2001  | 06/04/2014 | HIGHER PROGRAM VT AND FASTER PROGRAMMING RATES BASED ON IMPROVED ERASE METHODS                                        |
| 02800870.4            | F0282EP                   | EPO     | 09/30/2002  |            | DOUBLE DENSED CORE GATES IN SONOS FLASH MEMORY                                                                        |
| 1435114               | F0283EP                   | EPO     | 09/27/2002  | 12/08/2010 | SALICIDED GATE FOR VIRTUAL GROUND ARRAYS                                                                              |
| 01959586.7            | F0499EP                   | EPO     | 08/06/2001  |            | A SOURCE SIDE BORON IMPLANTING AND DIFFUSING DEVICE ARCHITECTURE FOR DEEP SUBSTANCE 0.18UM FLASH MEMORY TECHNOLOGIES  |
| 01957475.5            | F0932EP                   | EPO     | 08/06/2001  |            | SOURCE SIDE BORON IMPLANT AND DRAIN SIDE MDD IMPLANT FOR DEEP SUB 0.18 MICRON FLASH MEMORY                            |
| 1386323               | F1067EP                   | EPO     | 02/19/2002  | 06/17/2009 | THRESHOLD VOLTAGE COMPACTING FOR NON-VOLATILE SEMICONDUCTOR MEMORY DESIGNS                                            |
| 92307223.5            | FMA13-0002US CON          | EPO     | 08/07/1992  |            | PLL SYNTHESIZER CIRCUITRY                                                                                             |
| 0664604               | FMA13-0011DE              | EPO     | 12/13/1994  | 03/26/2003 | TRANSIMPEDANCE AMPLIFIER                                                                                              |
| 0627807               | FMA13-0015US CON          | EPO     | 05/26/1994  | 08/12/1998 | POWER LINE CONNECTION CIRCUIT AND POWER LINES SWITCH IC FOR THE SAME                                                  |
| 06254768.2            | FMA13-00305EP             | EPO     | 09/13/2006  |            | IMAGE PROCESSING APPARATUS AND RESIZING                                                                               |
| 06798412.0            | FMA13-00309EP             | EPO     | 09/28/2006  |            | SIGNAL RECEIVER APPARATUS AND WAVEFORM SHAPING METHOD                                                                 |
| 03019668.7            | FMA13-00344CN             | EPO     | 09/08/2003  |            | PLL CLOCK GENERATOR CIRCUIT AND CLOCK GENERATION METHOD                                                               |
| 08158811.3            | FMA13-00346US             | EPO     | 06/23/2008  |            | SIMULATION OF PROGRAM EXECUTION TO DETECT PROBLEM SUCH AS DEADLOCK                                                    |
| 07117198.7            | FMA13-00348US             | EPO     | 09/25/2007  |            | CIRCUIT FOR CORRECTING SENSOR TEMPERATURE CHARACTERISTICS                                                             |
| 07831164.4            | FMA13-00353US CON         | EPO     | 11/02/2007  |            | SIGNAL PROCESSOR AND COMMUNICATION DEVICE                                                                             |
| 07101756.0            | FMA13-0043EP              | EPO     | 11/18/1996  |            | SEMICONDUCTOR INTEGRATED CIRCUIT OPERABLE AS A PHASE-LOCKED LOOP                                                      |
| 07101761.0            | FMA13-0043EP DIV          | EPO     | 11/18/1996  |            | SEMICONDUCTOR INTEGRATED CIRCUIT OPERABLE AS A PHASE-LOCKED LOOP                                                      |
| 96308327.4            | FMA13-0043US              | EPO     | 11/18/1996  |            | SEMICONDUCTOR INTEGRATED CIRCUIT OPERABLE AS A PHASE-LOCKED LOOP                                                      |
| 0990987               | FMA13-00448DE             | EPO     | 04/22/1999  | 03/22/2006 | ELECTRONIC DEVICE WITH FLASH MEMORY BUILT-IN                                                                          |
| 2345148               | FMA13-00472DE             | EPO     | 11/11/2008  | 09/03/2014 | METHOD OF DETECTING AN OPERATING CONDITION OF AN ELECTRIC STEPPER MOTOR                                               |
| 2381450               | FMA13-00503DE             | EPO     | 02/03/2011  | 07/16/2014 | SEMICONDUCTOR MEMORY                                                                                                  |
| 12158984.0            | FMA13-00503EP             | EPO     | 02/03/2011  |            | SEMICONDUCTOR MEMORY                                                                                                  |
| 12159036.8            | FMA13-00503EP DIV         | EPO     | 02/03/2011  |            | SEMICONDUCTOR MEMORY                                                                                                  |
| 11179428.5            | FMA13-00508US CON         | EPO     | 08/30/2011  |            | NODE SYSTEM AND SUPERVISORY NODE                                                                                      |
| 0845864               | FMA13-0051DE              | EPO     | 07/11/1997  | 02/09/2005 | LEVEL CONVERTER AND SEMICONDUCTOR DEVICE                                                                              |
| 12180833.1            | FMA13-00532EP             | EPO     | 08/17/2012  |            | PROCESSOR USING INTERRUPT SIGNAL TO DEFINE INSTRUCTION DECODING                                                       |
| 1239573               | FMA13-00539DE             | EPO     | 01/07/2002  | 05/26/2010 | OVERVOLTAGE PROTECTOR FOR ELECTRIC POWER SYSTEM, AC/DC CONVERTER AND DC/DC CONVERTER CONSTITUTING THE POWER SYSTEM    |
| 1246369               | FMA13-00544EP             | EPO     | 03/18/2002  | 08/17/2005 | MODE SWITCHING METHOD FOR PLL CIRCUIT AND MODE CONTROL CIRCUIT FOR PLL CIRCUIT                                        |
| 1324477               | FMA13-00551DE             | EPO     | 12/06/2002  | 08/09/2006 | BIPOLAR SUPPLY VOLTAGE GENERATOR AND SEMICONDUCTOR DEVICE FOR THE SAME                                                |
| 06007107.3            | FMA13-00552US             | EPO     | 04/04/2006  |            | ANALOG MULTISTAGE AMPLIFICATION CIRCUIT IN THE FIELD OF SENSOR                                                        |
| 06252787.4            | FMA13-00570CN             | EPO     | 05/30/2006  |            | RECONFIGURABLE CIRCUIT                                                                                                |
| 0878910               | FMA13-0063DE              | EPO     | 11/10/1997  | 05/23/2007 | SKEW-REDUCTION CIRCUIT                                                                                                |
| 1016969               | FMA13-0076DE              | EPO     | 12/22/1999  | 03/24/2004 | MICROCONTROLLER PROVIDED WITH SUPPORT FOR DEBUGGING                                                                   |
| 1058385               | FMA13-0089DE-1            | EPO     | 03/29/2000  | 06/01/2005 | COMPARATOR CIRCUIT                                                                                                    |
| 1530293               | FMA13-0089EP              | EPO     | 03/29/2000  | 01/24/2007 | VOLTAGE CONTROLLED OSCILLATOR CIRCUIT                                                                                 |
| 1227591               | FMA13-0093DE              | EPO     | 08/18/2000  | 01/25/2006 | FREQUENCY MEASUREMENT CIRCUIT??                                                                                       |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                |
|-----------------------|---------------------------|---------|-------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 00400579.9            | FMA13-0096EP              | EPO     | 03/03/2000  |            | DEVICE AND METHOD OF SUPPLYING POWER TO PLURALITY OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICES                                                        |
| 01101163.2            | FMA13-0101US              | EPO     | 01/23/2001  |            | INTERFACE APPARATUS                                                                                                                                  |
| 1202245               | FMA13-0110DE              | EPO     | 05/02/2002  | 10/05/2011 | DOT-INVERSION DATA DRIVER FOR LIQUID CRYSTAL DISPLAY DEVICE WITH REDUCED POWER CONSUMPTION                                                           |
| 1164701               | FMA13-0115DE              | EPO     | 05/09/2001  | 09/13/2006 | FRACTIONAL-N-PLL FREQUENCY SYNTHESIZER AND PHASE ERROR CANCELING METHOD THEREFOR                                                                     |
| 1239574               | FMA13-0122DE              | EPO     | 03/05/2002  | 05/16/2007 | DC-DC CONVERTER, POWER SUPPLY CIRCUIT AND METHOD FOR CONTROLLING THE SAME                                                                            |
| 02250636.4            | FMA13-0132EP              | EPO     | 01/30/2002  |            | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                              |
| 1826775               | FMA13-0132EP DIV          | EPO     | 01/30/2002  | 09/07/2011 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                              |
| 1826776               | FMA13-0132EP DIV1         | EPO     | 01/30/2002  | 04/27/2011 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                              |
| 1830364               | FMA13-0132EP DIV2         | EPO     | 01/30/2002  | 12/10/2008 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                              |
| 07109299.3            | FMA13-0132EP DIV3         | EPO     | 01/30/2002  |            | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                              |
| 1349106               | FMA13-0158DE              | EPO     | 01/31/2003  | 12/14/2005 | FINGER MOVEMENT DETECTION METHOD AND APPARATUS                                                                                                       |
| 1435694               | FMA13-0177DE2             | EPO     | 12/23/2003  | 08/30/2006 | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT JITTER GENERATION CIRCUIT AND SEMICONDUCTOR DEVICE                                                          |
| 1641124               | FMA13-0177EP              | EPO     | 12/23/2003  | 08/30/2006 | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT                                                                                                             |
| 1672800               | FMA13-0177EP DIV          | EPO     | 12/23/2003  | 08/19/2009 | JITTER GENERATION CIRCUIT                                                                                                                            |
| 1553636               | FMA13-0178DE              | EPO     | 03/03/2003  | 05/01/2013 | MOS TYPE VARIABLE CAPACITANCE DEVICE                                                                                                                 |
| 1657821               | FMA13-0197EP              | EPO     | 11/28/2003  | 05/23/2007 | SD MODULATOR OF PLL CIRCUIT                                                                                                                          |
| 1557682               | FMA13-0200DE              | EPO     | 06/16/2004  | 08/04/2010 | TEST MODE ACTIVATION BY PHASE COMPARISON                                                                                                             |
| 1830196               | FMA13-0200EP              | EPO     | 06/16/2004  | 08/04/2010 | TEST MODE ACTIVATION BY PHASE COMPARISON                                                                                                             |
| 1596208               | FMA13-0211DE              | EPO     | 04/04/2005  | 08/07/2013 | CAPACITANCE DIFFERENCE DETECTING CIRCUIT AND MEMS SENSOR                                                                                             |
| 1857826               | FMA13-0211EP              | EPO     | 04/04/2005  | 08/07/2013 | CAPACITANCE DIFFERENCE DETECTING CIRCUIT AND MEMS SENSOR                                                                                             |
| 04258184.3            | FMA13-0225CN              | EPO     | 12/30/2004  |            | SEMICONDUCTOR DEVICE HAVING AN ARITHMETIC UNIT OF A RECONFIGURABLE CIRCUIT                                                                           |
| 1612682               | FMA13-0227DE              | EPO     | 01/26/2005  | 07/25/2012 | DYNAMIC MEMORY RECONFIGURATION                                                                                                                       |
| 1906312               | FMA13-0227EP              | EPO     | 01/26/2005  | 07/25/2012 | DYNAMIC MEMORY CONFIGURATION                                                                                                                         |
| 05009065.3            | FMA13-0236US CON          | EPO     | 04/26/2005  |            | ANALOG FILTER CIRCUIT AND ADJUSTMENT METHOD THEREOF                                                                                                  |
| 05009782.3            | FMA13-0237US              | EPO     | 05/04/2005  |            | SIGNAL DETECTION DEVICE, FREQUENCY DETECTION DEVICE, POWER CONSUMPTION CONTROL DEVICE, CORRESPONDING METHODS AND ELECTRONIC APPARATUS USING THE SAME |
| 1689088               | FMA13-0238EP              | EPO     | 05/17/2005  | 09/02/2009 | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT AND A METHOD OF CONTROLLING THEREOF                                                                         |
| 1708359               | FMA13-0248DE              | EPO     | 08/08/2005  | 03/14/2012 | AMPLIFICATION CIRCUIT AND CONTROL METHOD OF AMPLIFICATION                                                                                            |
| 1748562               | FMA13-0266DE              | EPO     | 11/01/2005  | 05/07/2008 | CLOCK GENERATING CIRCUIT AND CLOCK GENERATING METHOD                                                                                                 |
| 1764922               | FMA13-0269DE              | EPO     | 12/13/2005  | 10/29/2008 | CLOCK GENERATION CIRCUIT AND CLOCK GENERATION METHOD                                                                                                 |
| 06124192.3            | FMA13-0284US              | EPO     | 11/16/2006  |            | METHOD AND CIRCUIT FOR CORRECTING SENSOR TEMPERATURE DEPENDENCY CHARACTERISTIC                                                                       |
| 1832985               | FMA13-0287DE              | EPO     | 09/26/2006  | 07/04/2012 | RECONFIGURABLE CIRCUIT                                                                                                                               |
| 06119080.7            | FMA13-0288EP              | EPO     | 08/17/2006  |            | PULSE WIDTH MODULATION CIRCUIT                                                                                                                       |
| 06119268.8            | FMA13-0289EP              | EPO     | 08/21/2006  |            | PRESALER CIRCUIT AND BUFFER CIRCUIT                                                                                                                  |
| 2107681               | FMA13-0289EP DIV          | EPO     | 08/21/2006  | 07/19/2007 | PRESALER CIRCUIT AND BUFFER CIRCUIT                                                                                                                  |
| 06251768.5            | FMA13-0295US              | EPO     | 03/30/2006  |            | COMPARATOR CIRCUIT AND CONTROL METHOD THEREOF                                                                                                        |
| 01274195.5            | G0063EP                   | EPO     | 11/14/2001  |            | ACCURATE VERIFY APPARATUS AND METHOD FOR NOR FLASH MEMORY CELLS IN THE PRESENCE OF HIGH COLUMN LEAKAGE                                               |
| 1399965               | G0074EP                   | EPO     | 12/14/2001  | 01/12/2011 | SOURCE DRAIN IMPLANT DURING ONO FORMATION FOR IMPROVED ISOLATION OF SONOS DEVICES                                                                    |
| 02713624.1            | G0259EP                   | EPO     | 02/19/2002  |            | FLASH MEMORY DEVICE WITH INCREASE OF EFFICIENCY DURING AN APDE (AUTOMATIC PROGRAM DISTURB AFTER ERASE) PROCESS                                       |
| 1529293               | G0391EP                   | EPO     | 06/10/2003  | 11/23/2005 | BUILT-IN-SELF-TEST OF FLASH MEMORY CELLS                                                                                                             |
| 1459374               | G0689EP                   | EPO     | 12/11/2002  | 03/17/2010 | SHALLOW TRENCH ISOLATION APPROACH FOR IMPROVED STI CORNER ROUNDING                                                                                   |
| 1497833               | G0861EP                   | EPO     | 02/14/2003  | 12/17/2008 | IMPROVED ERASE METHOD FOR SINGLE SIDED MIRROR OPERATION                                                                                              |
| 1493159               | G0862EP                   | EPO     | 02/14/2003  | 10/01/2009 | REFRESH SCHEME FOR DYNAMIC PAGE PROGRAMMING                                                                                                          |
| 1568045               | G0865EP                   | EPO     | 07/10/2003  | 12/09/2009 | MOCVD FORMATION OF Cu <sub>2</sub> S                                                                                                                 |
| 03812414.5            | G0878EP                   | EPO     | 07/10/2003  |            | A METHOD AND SYSTEM FOR ERASING A NITRIDE MEMORY DEVICE                                                                                              |
| 1559110               | H0297EP                   | EPO     | 07/10/2003  | 01/20/2010 | CONTROL OF MEMORY ARRAYS UTILIZING ZENER DIODE-LIKE DEVICES                                                                                          |
| 03811994.7            | H0343EP                   | EPO     | 07/10/2003  |            | MOCVD FORMATION OF Cu <sub>2</sub> S                                                                                                                 |
| 03786509.4            | H0385EP                   | EPO     | 09/08/2003  |            | AN ORGANIC MEMORY DEVICE AND METHOD FOR FORMING A MEMORY CELL                                                                                        |
| 04784925.2            | H0416EP                   | EPO     | 09/23/2004  |            | SIDEWELL FORMATION FOR HIGH DENSITY POLYMER MEMORY ELEMENT ARRAY                                                                                     |
| 1559109               | H0434EP                   | EPO     | 12/03/2008  | 02/24/2010 | STACKED ORGANIC MEMORY DEVICES AND METHODS OF OPERATING AND FABRICATING                                                                              |
| 1629535               | H0437                     | EPO     | 05/11/2004  | 03/14/2007 | PLANAR POLYMER MEMORY DEVICE                                                                                                                         |
| 04752883.1            | H0442                     | EPO     | 05/21/2004  |            | ORGANIC MEMORY DEVICE AND METHODS OF USING AND MAKING THE DEVICE                                                                                     |
| 1556887               | H0514                     | EPO     | 06/10/2003  | 04/16/2008 | NITROGEN OXIDATION TO REDUCE ENCROACHMENT                                                                                                            |
| 1568043               | H0570                     | EPO     | 12/02/2002  | 09/21/2004 | IMPROVED SYSTEM FOR PROGRAMMING A NON-VOLATILE MEMORY CELL                                                                                           |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                        |
|-----------------------|---------------------------|---------|-------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 1590810               | H0625EP                   | EPO     | 01/08/2004  | 07/27/2011 | IMPROVED METHOD FOR READING A NON-VOLATILE MEMORY CELL ADJACENT TO AN INACTIVE REGION OF A NON-VOLATILE MEMORY CELL ARRAY                    |
| 1573746               | H1205EP                   | EPO     | 07/24/2003  | 12/24/2008 | CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS                                                                                                  |
| 1644974               | H1368EP                   | EPO     | 06/18/2004  | 06/15/2011 | METHOD OF FORMING PECVD SILICON-RICH OXIDE LAYER FOR REDUCED UV CHARGING IN AN EEPROM                                                        |
| 1602109               | H1513                     | EPO     | 03/01/2004  | 10/15/2008 | CIRCUIT FOR FAST AND ACCURATE MEMORY READ OPERATIONS                                                                                         |
| 1434232               | H1979EP                   | EPO     | 08/13/2001  | 09/19/2007 | MEMORY CELL                                                                                                                                  |
| 04814984.3            | H1985EP                   | EPO     | 12/17/2004  |            | POCKET IMPLANT FOR COMPLEMENTARY BIT DISTURB IMPROVEMENT AND CHARGING IMPROVEMENT OF SONOS MEMORY CELL                                       |
| 1745511               | H1993EP                   | EPO     | 02/11/2005  | 03/31/2010 | BITLINE IMPLANT UTILIZING DUAL POLY                                                                                                          |
| 1872399               | H1998EP                   | EPO     | 04/04/2006  | 06/18/2014 | NON-CRITICAL COMPLEMENTARY MASKING METHOD FOR POLY-1 DEFINITION IN FLASH MEMORY DEVICE FABRICATION                                           |
| 99965057.5            | JC684497EP                | EPO     | 11/29/1999  |            | HIGH YIELD, HIGH PERFORMANCE SEMICONDUCTOR PROCESS FLOW FOR NAND FLASH MEMORY PRODUCTS                                                       |
| 1074046               | JC688497EP                | EPO     | 02/11/1999  | 08/20/2008 | ELIMINATION OF POLY-CAP FOR EASY POLY1 CONTACT FOR NAND PRODUCT                                                                              |
| 00305940.9            | P-1164EP                  | EPO     | 07/13/2000  |            | AN NROM FABRICATION METHOD                                                                                                                   |
| 1459374               | P116WO-EP                 | EPO     | 12/11/2002  | 03/17/2010 | SHALLOW TRENCH ISOLATION APPROACH FOR IMPROVED STI CORNER ROUNDING                                                                           |
| 01309289.5            | P-2448US CON              | EPO     | 04/03/2002  |            | PROGRAMMING AND ERASING METHODS FOR A REFERENCE CELL OF AN NROM ARRAY                                                                        |
| 01309290.3            | P-2448US CON              | EPO     | 11/01/2001  |            | PROGRAMMING AND ERASING METHODS FOR A REFERENCE CELL OF AN NROM ARRAY                                                                        |
| 02252406.0            | P-2448US CON              | EPO     | 04/01/2002  |            | PROGRAMMING AND ERASING METHODS FOR A REFERENCE CELL OF AN NROM ARRAY                                                                        |
| 02252406.0            | P-2448US CON              | EPO     | 04/03/2002  |            | PROGRAMMING AND ERASING METHODS FOR A REFERENCE CELL OF AN NROM ARRAY                                                                        |
| 20010929943           | P-2448WO                  | EPO     | 11/02/2001  |            | ARCHITECTURE AND SCHEME FOR A NON-STROBED READ SEQUENCE                                                                                      |
| 02257381.0            | P-4006EP                  | EPO     | 10/24/2002  |            | METHOD FOR ERASING A MEMORY CELL                                                                                                             |
| 02257954.4            | P-4007EP                  | EPO     | 11/18/2002  |            | PROTECTIVE LAYER IN MEMORY DEVICE AND METHOD THEREFOR                                                                                        |
| 03254386.0            | P-4629EP                  | EPO     | 07/10/2003  |            | A MULTIPLE USE MEMORY CHIP                                                                                                                   |
| 03001943.4            | P-4676EP1                 | EPO     | 01/30/2003  |            | METHOD FOR OPERATING A MEMORY DEVICE                                                                                                         |
| 06100056.8            | P-4676EP3                 | EPO     | 01/04/2006  |            | METHOD FOR OPERATING A MEMORY DEVICE                                                                                                         |
| 04791843.8            | P-5484US                  | EPO     | 10/29/2003  | 11/14/2006 | METHOD SYSTEM AND CIRCUIT FOR PROGRAMMING A NON-VOLATILE MEMORY ARRAY                                                                        |
| 2004791844            | P-5487-CN                 | EPO     | 10/27/2004  |            | METHOD CIRCUIT AND SYSTEM FOR DETERMINING A REFERENCE VOLTAGE                                                                                |
| 2004791845.3          | P-5487-CN                 | EPO     | 10/27/2004  |            | METHOD CIRCUIT AND SYSTEM FOR DETERMINING A REFERENCE VOLTAGE                                                                                |
| 05111880.0            | P-6628US                  | EPO     | 12/09/2004  | 08/14/2007 | MEMORY FOR READING NON-VOLATILE MEMORY CELLS                                                                                                 |
| 06118948.6            | P-6628US CIP              | EPO     | 06/13/2008  |            | METHOD FOR READING NON-VOLATILE MEMORY CELLS                                                                                                 |
| 06112462.4            | P-7632EP                  | EPO     | 04/11/2006  |            | THRESHOLD VOLTAGE SHIFT IN NROM CELLS                                                                                                        |
| 60318714.5            | SE0002EP                  | EPO     | 03/11/2003  | 01/08/2009 | SYSTEM AND METHOD OF ERASE VOLTAGE CONTROL DURING MULTIPLE SECTOR ERASE OF A FLASH MEMORY DEVICE                                             |
| 10730637.5            | SP09-0001EP               | EPO     | 06/23/2010  |            | ELECTRONIC DEVICE HAVING A MOLDING COMPOUND INCLUDING A COMPOSITE MATERIAL                                                                   |
| 12854967.2            | SP09-0056CN               | EPO     | 12/07/2012  |            | HIGH SPEED SERIAL PERIPHERAL INTERFACE MEMORY SUBSYSTEM                                                                                      |
| 11848968.1            | SP10-0007EP               | EPO     | 12/16/2011  |            | SELF-ALIGNED NAND FLASH SELECT-GATE WORDLINES FOR SPACER DOUBLE PATTERNING                                                                   |
| 11850857.1            | SP10-0008EP               | EPO     | 12/19/2011  |            | EDGE ROUNDED FIELD EFFECT TRANSISTORS AND METHODS OF MANUFACTURING                                                                           |
| 11852012.1            | SP10-0009EP               | EPO     | 12/19/2011  |            | PROCESS MARGIN ENGINEERING IN CHARGE TRAPPING FIELD EFFECT TRANSISTORS                                                                       |
| 11853037.7            | SP10-0012EP               | EPO     | 12/29/2011  |            | MEMORY WITH EXTENDED CHARGE TRAPPING LAYER                                                                                                   |
| 13790045.2            | SP11-0015CN               | EPO     | 05/14/2013  |            | SOFT ERROR RESISTANT CIRCUITRY                                                                                                               |
| 12859602.0            | SP11-0042EP               | EPO     | 12/14/2012  |            | ACOUSTIC PROCESSING UNIT                                                                                                                     |
| 0657927               | TT0347DE                  | EPO     | 12/12/1994  | 02/27/2002 | FLASH EPROM DEVICES                                                                                                                          |
| 0729187               | TT0497DE                  | EPO     | 01/30/1996  | 04/03/2002 | A NON-VOLATILE MEMORY DEVICES HAVING A FLOATING GATE WITH ENHANCED CHANGE RETENTION                                                          |
| 96302994.7            | TT0607US                  | EPO     | 04/29/1996  |            | READING A NON-VOLATILE MEMORY ARRAY                                                                                                          |
| 1203378               | C725497                   | Finland | 08/01/2000  | 03/05/2003 | CIRCUIT IMPLEMENTATION TO QUENCH BIT LINE LEAKAGE CURRENT IN PROGRAM AND AUTO PROGRAM DISTURB MODE IN FLASH EPROM USING RESISTOR SOURCE LOAD |
| 0656628               | A938FR                    | France  | 11/10/1994  | 04/09/2003 | PROGRAMMED REFERENCE                                                                                                                         |
| 0690508               | A976/2067FR               | France  | 06/20/1995  | 09/11/2002 | HIGH ENERGY BURIED LAYER IMPLANT TO PROVIDE A LOW RESISTANCE P-WELL IN A FLASH EPROM ARRAY                                                   |
| 1234324               | AF01054FR                 | France  | 10/16/2000  | 10/04/2006 | HIGH TEMPERATURE OXIDE DEPOSITION PROCESS FOR FABRICATING AN ONO FLOATING-GATE ELECTRODE IN A TWO BIT EEPROM DEVICE                          |
| 1295294               | AF01076FR                 | France  | 05/21/2001  | 01/25/2005 | BURST ARCHITECTURE FOR A FLASH MEMORY                                                                                                        |
| 1327193               | AF01078FR                 | France  | 07/17/2001  | 02/21/2007 | BURST READ INCORPORATING OUTPUT BASED REDUNDANCY                                                                                             |
| 1297534               | AF01085FR                 | France  | 06/04/2001  | 03/14/2007 | METHOD TO REDUCE CAPACITIVE LOADING IN FLASH MEMORY X-DECODER FOR ACCURATE VOLTAGE CONTROL AT WORDLINES AND SELECT LINES                     |
| 1338037               | AF01112FR                 | France  | 11/15/2001  | 03/30/2011 | NON-VOLATILE SONOS SEMICONDUCTOR MEMORY DEVICE                                                                                               |
| 03746534.1            | AF01137FR                 | France  | 02/14/2003  |            | MEMORY MANUFACTURING PROCESS WITH BITLINE ISOLATION                                                                                          |
| 1636801               | AF01169FR                 | France  | 05/21/2004  | 11/02/2006 | MEMORY WITH A CORE-BASED VIRTUAL GROUND AND DYNAMIC REFERENCE SENSING SCHEME                                                                 |

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| 1665387               | AF01182FR                 | France  | 05/21/2004  | 08/13/2008 | MEMORY DEVICE HAVING HIGH WORK FUNCTION GATE AND METHOD OF ERASING SAME                                                                                |
| 1774530               | AF01365FR                 | France  | 04/29/2005  | 01/23/2008 | FLASH MEMORY UNIT AND METHOD OF PROGRAMMING A FLASH MEMORY DEVICE                                                                                      |
| 1782460               | AF01379FR                 | France  | 04/29/2005  | 06/01/2011 | METHOD FOR FABRICATING A FLOATING GATE MEMORY CELL                                                                                                     |
| 1830366               | AF01438FR                 | France  | 12/24/2004  | 07/13/2011 | BIAS APPLICATION METHOD OF STORAGE AND STORAGE                                                                                                         |
| 1829048               | AF01485FR                 | France  | 12/20/2005  | 06/15/2011 | METHOD OF PROGRAMMING, READING AND ERASING MEMORY-DIODE IN A MEMORY-DIODE ARRAY                                                                        |
| 1898460               | AF01792FR                 | France  | 06/28/2005  | 01/04/2012 | MIRRORBIT DEVICE HAVING STI AND DUAL POLY FILMS                                                                                                        |
| 1103980               | AF02178FR                 | France  | 11/24/2000  | 01/16/2008 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                                |
| E1223586              | AF02182FR                 | France  | 08/18/2000  | 08/03/2005 | NONVOLATILE MEMORY CIRCUIT STORAGE MULTI-                                                                                                              |
| 1310994               | AF02184FR                 | France  | 07/17/2000  | 02/13/2013 | NONVOLATILE MEMORY DEVICE AND                                                                                                                          |
| 1310963               | AF02186FR                 | France  | 06/29/2000  | 12/27/2006 | SEMICONDUCTOR MEMORY DEVICE                                                                                                                            |
| 1286359               | AF02200FR                 | France  | 03/18/2002  | 01/17/2007 | MEMORY CONTROLLER FOR MULTI LEVEL                                                                                                                      |
| 1574867               | AF02230FR                 | France  | 12/17/2003  | 08/08/2007 | SEMICONDUCTOR DEVICE AND TEST METHOD                                                                                                                   |
| 1575056               | AF02233FR                 | France  | 12/17/2003  | 06/06/2007 | NONVOLATILE MEMORY AND METHOD AND WRITE METHOD OF THE SAME                                                                                             |
| 700097                | B001FR                    | France  | 06/30/1995  | 05/31/2000 | A SELF-ALIGNED BURIED CHANNEL/JUNCTION STACKED GATE FLASH MEMORY CELL                                                                                  |
| 0792516               | B011/2097FR               | France  | 11/08/1995  | 03/10/1999 | NITRIDE ETCH PROCESS WITH CRITICAL DIMENSION (CD) GAIN                                                                                                 |
| 0799497               | B047FR                    | France  | 11/22/1995  | 01/19/2000 | NOVEL PROCESSING TECHNIQUES FOR ACHIEVING PRODUCTION WORTHY LOW DIELECTRIC LOW INTERCONNECT RESISTANCE AND HIGH PERFORMANCE                            |
| 0784867               | B100FR                    | France  | 07/31/1996  | 12/05/2007 | THREE-DIMENSIONAL NON-VOLATILE MEMORY                                                                                                                  |
| 0780023               | B111FR                    | France  | 06/21/1996  | 04/10/2002 | PROCESS FOR SELF-ALIGNED SOURCE FOR HIGH DENSITY MEMORY                                                                                                |
| 0856188               | B128FR                    | France  | 08/30/1996  | 10/27/1999 | A FLASH EEPROM MEMORY WITH SEPARATE REFERENCE ARRAY                                                                                                    |
| 0880783               | B257FR                    | France  | 08/15/1996  | 10/13/1999 | LOW SUPPLY VOLTAGE NEGATIVE CHARGE PUMP                                                                                                                |
| 0858661               | B260FR                    | France  | 07/19/1996  | 12/15/1999 | A NEW PROGRAM ALGORITHM FOR LOW VOLTAGE (3V) SINGLE POWER SUPPLY FLASH MEMORIES                                                                        |
| 0928497               | B277FR                    | France  | 03/25/1997  | 07/09/2008 | A NOVEL PROCESS FOR RELIABLE ULTRATHIN OXYNITRIDE FORMATION                                                                                            |
| 1019914               | C141496FR                 | France  | 04/10/1998  | 03/06/2002 | A DUAL SOURCE SIDE POLYSILICON SELECT GATE STRUCTURE AND PROGRAMMING METHOD UTILIZING SINGLE TUNNEL OXIDE FOR NAND ARRAY FLASH MEMORY                  |
| 0944907               | C196596FR                 | France  | 11/13/1997  | 10/17/2001 | BANK ARCHITECTURE FOR A NON-VOLATILE MEMORY ENABLING SIMULTANEOUS READING AND WRITING                                                                  |
| 1040486               | C369297FR                 | France  | 12/18/1998  | 02/27/2002 | BIASING METHOD AND STRUCTURE FOR REDUCING BAND-TO-BAND AND/OR AVALANCHE CURRENTS DURING THE ERASE OF FLASH MEMORY DEVICE                               |
| 1012878               | C526397FR                 | France  | 08/25/1998  | 07/28/2004 | REDUCTION OF CHARGE LOSS IN NONVOLATILE MEMORY CELLS BY PHOSPHOROUS IMPLANTATION INTO PECVD NITRIDE/OXYNITRIDE FILMS                                   |
| 1247299               | C656497FR                 | France  | 08/31/2000  | 04/11/2007 | TUNGSTEN GATE MOS TRANSISTOR AND MEMORY CELL AND METHOD OF MAKING SAME                                                                                 |
| 1116240               | C715497FR                 | France  | 09/21/1999  | 11/13/2002 | WORDLINE DRIVER FOR FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EEPROM)                                                                 |
| 1203378               | C725497FR                 | France  | 08/01/2000  | 03/05/2003 | CIRCUIT IMPLEMENTATION TO QUENCH BIT LINE LEAKAGE CURRENT IN PROGRAM AND AUTO PROGRAM DISTURB MODE IN FLASH EPROM USING RESISTOR SOURCE LOAD           |
| 1123547               | D016FR                    | France  | 10/05/1999  | 08/06/2003 | BIT LINE BIASING METHOD TO ELIMINATE PROGRAM DISTURBANCE IN A NON-VOLATILE MEMORY DEVICE AND MEMORY DEVICE EMPLOYING THE SAME                          |
| 1125302               | D138FR                    | France  | 10/05/1999  | 01/08/2003 | SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON-VOLATILE MEMORY ARRAY                                                                                  |
| 1116238               | D139FR                    | France  | 08/16/1999  | 02/26/2003 | BANK SELECTOR CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITETURE                                      |
| 1116239               | D168FR                    | France  | 08/16/1999  | 05/15/2002 | SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                                          |
| 1116236               | D169FR                    | France  | 08/16/1999  | 05/15/2002 | METHOD OF MAKING FLEXIBLY PARTITIONED METAL LINE SEGMENTS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE |
| 1125301               | D170FR                    | France  | 08/16/1999  | 10/16/2002 | MEMORY ADDRESS DECODING CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                           |
| 1142014               | D802FR                    | France  | 10/24/1999  | 09/03/2008 | METHOD FOR IMPROVING ELECTROSTATIC DISCHARGE (ESD) ROBUSTNESS                                                                                          |
| 1175680               | D832FR                    | France  | 05/05/2000  | 02/26/2003 | RAMPED OR STEPPED GATE CHANNEL ERASE FOR FLASH MEMORY APPLICATION                                                                                      |
| 1224696               | D838FR                    | France  | 10/24/2000  | 08/30/2006 | SOLID-SOURCE DOPING FOR SOURCE/DRAIN OF FLASH MEMORY                                                                                                   |
| 1218941               | D877FR                    | France  | 07/17/2000  | 04/02/2014 | NON-VOLATILE MEMORY HAVING HIGH GATE COUPLING CAPACITANCE                                                                                              |
| 1222690               | D894FR                    | France  | 09/29/2000  | 01/23/2008 | METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITH REDUCED ARC LOSS IN PERIPHERAL CIRCUITRY REGION                                                    |
| 1218938               | DA01016FR                 | France  | 07/14/2000  | 12/19/2007 | METHOD FOR PROVIDING A DOPANT LEVEL FOR POLYSILICON FOR FLASH MEMORY DEVICES                                                                           |
| 69412360              | FMA13-0015DE              | France  | 05/26/1994  | 08/12/1998 | POWER LINE CONNECTION CIRCUIT AND POWER LINES SWITCH IC FOR THE SAME                                                                                   |
| 2752114               | FMA13-0042CN DIV          | France  | 06/26/1997  | 03/15/2002 | OSCILLATOR HAVING SWITCHING CAPACITORS AND PHASE-LOCKED LOOP ...                                                                                       |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                     |
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| 2759217               | FMA13-0042FR              | France  | 06/26/1997  | 11/02/2001 | OSCILLATOR HAVING SWITCHING CAPACITORS AND PHASE-LOCKED LOOP ...                                                                          |
| 2345148               | FMA13-00472EP             | France  | 11/11/2008  | 09/03/2014 | METHOD OF DETECTING AN OPERATING CONDITION OF AN ELECTRIC STEPPER MOTOR                                                                   |
| 2381450               | FMA13-00503EP<br>DIV2     | France  | 02/03/2011  | 07/16/2014 | SEMICONDUCTOR MEMORY                                                                                                                      |
| 2773925               | FMA13-0066US              | France  | 07/22/1998  | 06/08/2001 | PLL FREQUENCY SYNTHESIZER WITH LOCK DETECTION CIRCUIT                                                                                     |
| 2774234               | FMA13-0069US              | France  | 08/20/1998  | 12/03/2004 | SEMICONDUCTOR DEVICE INCLUDING A BOOST CIRCUIT                                                                                            |
| 2779293               | FMA13-0070US              | France  | 12/29/1998  | 05/17/2002 | CIRCUIT DE SORTIE A TRANSISTORS                                                                                                           |
| 1435694               | FMA13-0177EP              | France  | 12/23/2003  | 06/03/2009 | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT JITTER GENERATION CIRCUIT AND SEMICONDUCTOR DEVICE                                               |
| 1641124               | FMA13-0177FR              | France  | 12/23/2003  | 06/03/2009 | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT                                                                                                  |
| 1672800               | FMA13-0177FR-1            | France  | 12/23/2003  | 08/19/2009 | JITTERY GENERATION CIRCUIT                                                                                                                |
| 1553636               | FMA13-0178EP              | France  | 03/03/2003  | 05/01/2013 | MOS TYPE VARIABLE CAPACITANCE DEVICE                                                                                                      |
| 1906312               | FMA13-0227EP DIV          | France  | 01/26/2005  | 07/25/2012 | DYNAMIC MEMORY CONFIGURATION                                                                                                              |
| 1748562               | FMA13-0266EP              | France  | 11/01/2005  | 05/07/2008 | CLOCK GENERATING CIRCUIT AND CLOCK GENERATING METHOD                                                                                      |
| 1529293               | G0391FR                   | France  | 06/10/2003  | 11/23/2005 | BUILT-IN-SELF-TEST OF FLASH MEMORY CELLS                                                                                                  |
| 1497833               | G0861FR                   | France  | 02/14/2003  | 12/08/2008 | IMPROVED ERASE METHOD FOR SINGLE SIDED MIRROR OPERATION                                                                                   |
| 03716045.4            | G0862FR                   | France  | 02/14/2003  |            | REFRESH SCHEME FOR DYNAMIC PAGE PROGRAMMING                                                                                               |
| 1518247               | G0866FR                   | France  | 04/22/2003  | 02/08/2006 | STEPPED PRE-ERASE VOLTAGE FOR MIRRORBIT ERASE                                                                                             |
| 1629535               | H0437FR                   | France  | 05/11/2004  | 03/14/2007 | PLANAR POLYMER MEMORY DEVICE                                                                                                              |
| 1556887               | H0514FR                   | France  | 06/10/2003  | 04/16/2008 | NITROGEN OXIDATION TO REDUCE ENCROACHMENT                                                                                                 |
| 1568043               | H0570FR                   | France  | 07/24/2003  | 12/05/2007 | IMPROVED SYSTEM FOR PROGRAMMING A NON-VOLATILE MEMORY CELL                                                                                |
| 1568037               | H0575FR                   | France  | 07/24/2003  | 06/18/2008 | IMPROVED PRE-CHARGE METHOD FOR READING A NON-VOLATILE MEMORY CELL ARRAY WITH STAGGERED LOCAL INTERCONNECT STRUCTURE                       |
| 1673781               | H0576FR                   | France  | 09/16/2004  | 07/25/2007 | IMPROVED METHOD FOR READING A NON-VOLATILE MEMORY CELL ADJACENT TO AN INACTIVE REGION OF A NON-VOLATILE MEMORY CELL ARRAY                 |
| 1590810               | H0625FR                   | France  | 01/08/2004  | 07/27/2011 | CASCADE AMPLIFIER CIRCUIT FOR PRODUCING A FAST, STABLE AND ACCURATE BITLINE VOLTAGE                                                       |
| 1563507               | H1203FR                   | France  | 07/10/2003  | 04/15/2009 | CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS                                                                                               |
| 1573746               | H1205FR                   | France  | 07/24/2003  | 12/24/2008 | PECVD SILICON-RICH OXIDE LAYER FOR REDUCED UV CHARGING                                                                                    |
| 1644974               | H1368FR                   | France  | 06/18/2004  | 06/15/2011 | CIRCUIT FOR FAST AND ACCURATE MEMORY READ OPERATIONS                                                                                      |
| 1602109               | H1513FR                   | France  | 03/01/2004  | 10/15/2008 | A NON-CRITICAL COMPLEMENTARY MASKING METHOD FOR POLY-1 DEFINITION IN FLASH MEMORY DEVICE FABRICATION                                      |
| 1872399               | H1998FR                   | France  | 04/04/2006  | 06/18/2014 | FLASH EPROM DEVICES                                                                                                                       |
| 0657927               | TT0347EP                  | France  | 12/12/1994  | 02/27/2002 | A NON-VOLATILE MEMORY DEVICES HAVING A FLOATING GATE WITH ENHANCED CHANGE RETENTION                                                       |
| 0729187               | TT0497EP                  | France  | 01/30/1996  | 04/03/2002 | MEMORY BLOCK SELECT USING MULTIPLE WORD LINES TO ADDRESS A SINGLE MEMORY CELL ROW                                                         |
| 0929898               | TT1997FR                  | France  | 09/29/1997  | 11/28/2001 | CHARGE PUMP APPARATUS                                                                                                                     |
| 69111499.4            | A768/1837DE               | Germany | 03/20/1991  | 07/26/1995 | METHOD OF PROGRAMMING FLASH EEPROM CELL ARRAYS                                                                                            |
| 69226546.5            | A808/1864DE               | Germany | 01/27/1992  | 08/12/1998 | PROGRAMMED REFERENCE                                                                                                                      |
| 69432452.3            | A938DE                    | Germany | 11/10/1994  | 04/09/2003 | METHOD AND APPARATUS FOR PROGRAMMING MEMORY DEVICES                                                                                       |
| 69520853.5            | A960/2054DE               | Germany | 03/23/1995  | 05/09/2001 | HIGH ENERGY BURIED LAYER IMPLANT TO PROVIDE A LOW RESISTANCE P-WELL IN A FLASH EPROM ARRAY                                                |
| 69528118              | A976/2067DE               | Germany | 06/20/1995  | 09/11/2002 | LOW VOLTAGE READ CASCODE FOR 2V/3V AND DIFFERENT BANK COMBINATIONS WITHOUT METAL OPTIONS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE |
| 60011921.1            | AF01002DE                 | Germany | 10/07/2000  | 06/30/2004 | WORDLINE DRIVER FOR FLASH MEMORY READ MODE                                                                                                |
| 60101047.7            | AF01036DE                 | Germany | 02/07/2001  | 10/22/2003 | HIGH TEMPERATURE OXIDE DEPOSITION PROCESS FOR FABRICATING AN ONO FLOATING-GATE ELECTRODE IN A TWO BIT EEPROM DEVICE                       |
| 60031155.4            | AF01054DE                 | Germany | 10/16/2000  | 10/14/2006 | VOLTAGE BOOST LEVEL CLAMPING CIRCUIT FOR A FLASH MEMORY                                                                                   |
| 60100741.7            | AF01072DE                 | Germany | 02/05/2001  | 10/09/2003 | WORD LINE DECODING ARCHITECTURE IN A FLASH MEMORY                                                                                         |
| 60136482.1            | AF01073DE                 | Germany | 07/31/2001  | 11/05/2008 | MULTIPLE BANK SIMULTANEOUS OPERATION FOR A FLASH MEMORY                                                                                   |
| 60130437.3            | AF01075DE                 | Germany | 03/12/2001  | 09/12/2007 | BURST ARCHITECTURE FOR A FLASH MEMORY                                                                                                     |
| 60108388.1-08         | AF01076DE                 | Germany | 05/21/2001  | 01/25/2005 | BURST READ INCORPORATING OUTPUT BASED REDUNDANCY                                                                                          |
| 60126800.8            | AF01078DE                 | Germany | 07/17/2001  | 02/21/2007 | METHOD TO REDUCE CAPACITIVE LOADING IN FLASH MEMORY X-DECODER FOR ACCURATE VOLTAGE CONTROL AT WORDLINES AND SELECT LINES                  |
| 60127260.9            | AF01085DE                 | Germany | 06/04/2001  | 03/14/2007 | A WORD LINE TRACKING STRUCTURE FOR USE IN AN ARRAY OF FLASH EEPROM MEMORY CELLS                                                           |
| 60003451.8            | AF01086DE                 | Germany | 09/29/2000  | 06/18/2003 | I/O PARTITIONING AND METHODOLOGY TO REDUCE BAND-TO-BAND TUNNELING CURRENT DURING ERASE                                                    |
| 10197225              | AF01090DE                 | Germany | 11/14/2001  | 10/11/2007 | VOLTAGE BOOST CIRCUIT USING SUPPLY VOLTAGE DETECTION TO COMPENSATE FOR SUPPLY VOLTAGE VARIATION IN READ MODE VOLTAGES                     |
| 60202077.8            | AF01094DE                 | Germany | 03/14/2002  | 11/24/2004 | SOFT PROGRAM AND SOFT PROGRAM VERIFY OF THE CORE CELLS IN FLASH MEMORY ARRAY                                                              |
| 60115716.8            | AF01096DE                 | Germany | 12/12/2001  | 12/07/2005 | SIMULTANEOUS FORMATION CHARGE STORAGE AND BITLINE TO WORDLINE ISOLATION                                                                   |
| 60141035.1            | AF01102DE                 | Germany | 08/07/2001  | 01/06/2010 | NON-VOLATILE SONOS SEMICONDUCTOR MEMORY DEVICE                                                                                            |
| 60144340.3            | AF01112DE                 | Germany | 11/15/2001  | 03/30/2011 | SYSTEM AND METHOD FOR MULTI-BIT FLASH READS USING DUAL DYNAMIC REFERENCES                                                                 |
| 60316931.7            | AF01116DE                 | Germany | 03/03/2003  | 10/17/2007 | HARD MASK PROCESS FOR MEMORY DEVICE WITHOUT BITLINE SHORTS                                                                                |
| 10392392.6            | AF01132DE                 | Germany | 01/21/2003  | 02/21/2008 |                                                                                                                                           |

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|-----------------------|---------------------------|---------|-------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10392314.4            | AF01134DE                 | Germany | 01/21/2003  |            | METHOD OF MAKING MEMORY WORDLINE HARD MASK EXTENSION                                                                                                       |
| 60329993.8            | AF01137DE                 | Germany | 02/14/2003  | 11/11/2009 | MEMORY MANUFACTURING PROCESS WITH BITLINE ISOLATION                                                                                                        |
| 602004003062.7        | AF01169DE                 | Germany | 05/21/2004  | 11/02/2006 | MEMORY WITH A CORE-BASED VIRTUAL GROUND AND DYNAMIC<br>REFERENCE SENSING SCHEME                                                                            |
| 602004015813.5        | AF01182DE                 | Germany | 05/21/2004  | 08/13/2008 | MEMORY DEVICE HAVING HIGH WORK FUNCTION GATE AND METHOD<br>OF ERASING SAME                                                                                 |
| 112004000380.6        | AF01186DE                 | Germany | 01/08/2004  |            | CHARGE-TRAPPING MEMORY ARRAYS RESISTANT TO DAMAGE FROM<br>CONTACT HOLE FORMATION                                                                           |
| 112004000753.4        | AF01209DE                 | Germany | 04/13/2004  | 06/26/2008 | METHOD FOR REDUCING SHORT CHANNEL EFFECTS IN MEMORY<br>CELLS AND RELATED STRUCTURE                                                                         |
| 112005001578.5        | AF01232DE                 | Germany | 04/29/2005  | 05/24/2007 | BOND PAD STRUCTURE FOR COPPER METALLIZATION HAVING<br>INCREASED RELIABILITY AND METHOD FOR FABRICATING SAME                                                |
| 112004002832.9        | AF01241DE                 | Germany | 04/13/2004  | 11/29/2012 | SECTOR PROTECTION CIRCUIT AND SECTOR PROTECTION METHOD<br>FOR NON-VOLATILE SEMICONDUCTOR STORAGE DEVICE, AND NON-<br>VOLATILE SEMICONDUCTOR STORAGE DEVICE |
| 112004002836.1        | AF01248DE                 | Germany | 04/21/2004  |            | NON-VOLATILE SEMICONDUCTOR DEVICE AND METHOD FOR<br>AUTOMATICALLY RECOVERING ERASE FAILURE IN THE DEVICE                                                   |
| 112005001526.2        | AF01306DE                 | Germany | 06/30/2005  |            | SWITCHABLE MEMORY DIODE- A NEW MEMORY DEVICE                                                                                                               |
| 112005001983.7        | AF01320DE                 | Germany | 08/08/2005  |            | SYSTEMS AND METHODS FOR ADJUSTING PROGRAMMING<br>THRESHOLDS OF POLYMER MEMORY CELLS                                                                        |
| 112005002011.8        | AF01321CN                 | Germany | 08/08/2005  |            | POLYMER MEMORY DEVICE WITH VARIABLE PERIOD OF RETENTION<br>TIME                                                                                            |
| 602004026934.4        | AF01329DE                 | Germany | 08/30/2004  | 04/28/2010 | ERASE METHOD OF A NON-VOLATILE MEMORY DEVICE AND A NON-<br>VOLATILE MEMORY DEVICE                                                                          |
| 112004003009          | AF01338DE                 | Germany | 10/26/2004  | 12/01/2011 | METHOD OF SETTING INFORMATION OF NON-VOLATILE MEMORY AND<br>NON-VOLATILE MEMORY                                                                            |
| 112005001595.5        | AF01361DE                 | Germany | 06/30/2005  |            | METHOD OF IMPROVING ERASE VOLTAGE DISTRIBUTION FOR A<br>FLASH MEMORY ARRAY HAVING DUMMY WORDLINES                                                          |
| 602005004553.8        | AF01365DE                 | Germany | 04/29/2005  | 01/29/2009 | FLASH MEMORY UNIT AND METHOD OF PROGRAMMING A FLASH<br>MEMORY DEVICE                                                                                       |
| 602004018687.2        | AF01372DE                 | Germany | 02/19/2004  | 01/05/2009 | CURRENT-VOLTAGE CONVERTER CIRCUIT AND CONTROL METHOD<br>THEREOF                                                                                            |
| 1720172               | AF01377DE                 | Germany | 02/20/2004  | 06/06/2012 | A SEMICONDUCTOR MEMORY STORAGE DEVICE AND ITS<br>REDUNDANCY CONTROL METHOD                                                                                 |
| 602005028333          | AF01379DE                 | Germany | 04/29/2005  | 06/01/2011 | METHOD FOR FABRICATING A FLOATING GATE MEMORY CELL                                                                                                         |
| 602004039357.6        | AF01380DE                 | Germany | 02/20/2004  | 09/19/2012 | SEMICONDUCTOR STORAGE DEVICE AND SEMICONDUCTOR<br>STORAGE DEVICE CONTROL METHOD                                                                            |
| 112005002275.7        | AF01383DE                 | Germany | 09/20/2005  | 07/04/2013 | TECHNIK ZUM LESEN VON MEHRPEGELSPEICHERN MIT VIRTUELLER<br>MASSE                                                                                           |
| 112005001325.1        | AF01386DE                 | Germany | 02/11/2005  | 10/17/2013 | ERASE ALGORITHM FOR MULTI-LEVEL BIT FLASH MEMORY                                                                                                           |
| 112005003380.5        | AF01390DE                 | Germany | 12/20/2005  |            | MULTI-LEVEL ONO FLASH PROGRAM ALGORITHM FOR THRESHOLD<br>WIDTH CONTROL                                                                                     |
| 112004002930.9        | AF01402DE                 | Germany | 07/30/2004  | 06/01/2011 | SEMICONDUCTOR DEVICE AND METHOD OF GENERATING SENSE                                                                                                        |
| 112004002927.9        | AF01403DE                 | Germany | 07/30/2004  | 03/02/2011 | MLC WRITE BUFFER CIRCUITRY                                                                                                                                 |
| 112004002859.0        | AF01416DE                 | Germany | 05/12/2004  | 07/14/2011 | IMPROVED NEGATIVE DECODING                                                                                                                                 |
| 112004002852          | AF01417DE                 | Germany | 05/11/2004  | 04/19/2012 | HIGH SPEED BOOST OPERATION                                                                                                                                 |
| 112004002856.6        | AF01422DE                 | Germany | 05/11/2004  | 08/19/2010 | DUMMY CELL ARRAY BETWEEN CORE AND REFERENCE ARRAYS                                                                                                         |
| 112004002851.5        | AF01423DE                 | Germany | 05/11/2004  |            | MULTI BIT PROGRAMMING FOR VIRTUAL GROUND ARRAY                                                                                                             |
| 112004002857.4        | AF01425DE                 | Germany | 05/11/2004  | 04/26/2007 | IMPROVED APPARATUS FOR ADVANCED SECTOR PROTECTION (1)                                                                                                      |
| 112004002860.4        | AF01427DE                 | Germany | 05/12/2004  |            | IMPROVED SLATCH AND THE LAYOUT                                                                                                                             |
| 602004032680.1        | AF01432DE                 | Germany | 08/31/2004  | 05/11/2011 | THE SEMICONDUCTOR MEMORY STORAGE DEVICE WHICH CARRIED<br>THE NEGATIVE VOLTAGE GENERATING CIRCUIT                                                           |
| 602004033496.0        | AF01438DE                 | Germany | 12/24/2004  | 07/13/2011 | BIAS APPLICATION METHOD OF STORAGE AND STORAGE                                                                                                             |
| 112004003023.4        | AF01439DE                 | Germany | 11/30/2004  |            | NON-VOLATILE SELECT GATE IN NAND FLASH MEMORY                                                                                                              |
| 112004002928.7        | AF01441DE                 | Germany | 07/29/2004  |            | A NON-VOLATILE MEMORY APPARATUS AND ITS CONTROL METHOD                                                                                                     |
| 112004002858.2        | AF01443DE                 | Germany | 05/11/2004  |            | CARRIER FOR SEMICONDUCTOR DEVICES TO BE STACKED AND<br>FABRICATION METHOD OF THE DEVICE                                                                    |
| 112004002862.0        | AF01446DE                 | Germany | 05/20/2004  |            | SEMICONDUCTOR CHIP ASSEMBLY AND FABRICATION METHOD OF<br>THE SAME                                                                                          |
| 1105000866.5          | AF01453DE                 | Germany | 02/11/2005  |            | METHOD AND SYSTEMS FOR HIGH WRITE PERFORMANCE IN MULTI-<br>BIT FLASH MEMORY DEVICES                                                                        |
| 112004003019.6        | AF01454DE                 | Germany | 11/30/2004  |            | NEW MEMORY CELL STRUCTURE IN WHICH HIGH-SPEED WRITING IS<br>POSSIBLE                                                                                       |
| 112004003021.8        | AF01455DE                 | Germany | 11/30/2004  |            | NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                                   |
| 112004002973.2        | AF01463DE                 | Germany | 09/30/2004  | 06/01/2011 | FAST PROGRAM MODE IN SO ARCHITECTURE                                                                                                                       |
| 11200600208.2         | AF01467DE                 | Germany | 01/12/2006  | 04/03/2014 | MEMORY DEVICE HAVING TRAPEZOIDAL BITLINES AND METHOD OF<br>FABRICATING SAME                                                                                |
| 112004003022.6        | AF01470DE                 | Germany | 11/30/2004  | 04/05/2012 | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREOF                                                                                                            |
| 602005028587.3        | AF01485DE                 | Germany | 12/20/2005  | 06/15/2011 | METHOD OF PROGRAMMING, READING AND ERASING MEMORY-<br>DIODE IN A MEMORY-DIODE ARRAY                                                                        |
| 112005002818          | AF01491DE                 | Germany | 11/10/2005  | 07/19/2012 | DIODE ARRAYS ARCHITECTURE FOR ADDRESSING NANOSCALE<br>RESISTIVE MEMORY ARRAYS                                                                              |
| 112005003277          | AF01523DE                 | Germany | 12/20/2005  | 10/30/2014 | LESEVERSTARKER MIT GROBEM SPANNUNGSHUB                                                                                                                     |
| 602006042508.2        | AF01586DE                 | Germany | 06/30/2006  | 07/30/2014 | METHOD FOR PROGRAMMING A MEMORY DEVICE                                                                                                                     |
| 112004003005          | AF01645DE                 | Germany | 10/26/2004  | 12/01/2011 | NON-VOLATILE MEMORY DEVICE                                                                                                                                 |
| 112005003421.6        | AF01653DE                 | Germany | 01/24/2005  |            | SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME                                                                                                    |
| 602006005080.1        | AF01676DE                 | Germany | 07/17/2006  | 11/05/2008 | IMPROVED READ MODE FOR FLASH MEMORY                                                                                                                        |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                                            |
|-----------------------|---------------------------|---------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 112005003436.4        | AF01698DE                 | Germany | 01/27/2005  |            | A NON-VOLATILE MEMORY STORAGE DEVICE AND ITS CONTROL METHOD (PLACEMENT FORMATION (STRUCTURE) OF "AN INFORMATION MEMORY CELL OF OPERATION", AND ITS READ/WRITE APPARATUS, AND ITS CONTROL METHOD) |
| 112006000661.4        | AF01709DE                 | Germany | 03/22/2006  | 02/21/2013 | VARIABLE BREAKDOWN CHARACTERISTIC DIODE                                                                                                                                                          |
| 102005011368.0        | AF01759DE                 | Germany | 03/11/2005  |            | AUTOMATIC RESOURCE ASSIGNMENT IN DEVICES HAVING STACKED MODULES                                                                                                                                  |
| 602005031987.5        | AF01792DE                 | Germany | 06/28/2005  | 01/04/2012 | MIRRORBIT DEVICE HAVING STI AND DUAL POLY FILMS                                                                                                                                                  |
| 602006016445.9        | AF01852DE                 | Germany | 07/07/2006  | 08/25/2010 | INTEGRATED CIRCUIT TEST SOCKET                                                                                                                                                                   |
| 60037786.5            | AF02178DE                 | Germany | 11/24/2000  | 01/22/2009 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                          |
| 60021746.9            | AF02182DE                 | Germany | 08/18/2000  | 08/03/2005 | NONVOLATILE MEMORY CIRCUIT STORAGE MULTI-                                                                                                                                                        |
| 1310994               | AF02184DE                 | Germany | 07/17/2000  | 02/13/2013 | NONVOLATILE MEMORY DEVICE AND                                                                                                                                                                    |
| 60032644.6            | AF02186DE                 | Germany | 06/29/2000  | 12/27/2006 | SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                                      |
| 60216010.3            | AF02194DE                 | Germany | 04/25/2002  | 11/15/2006 | READ METHOD FOR DUAL BIT MEMORY CELL                                                                                                                                                             |
| 10146013.9            | AF02195DE                 | Germany | 09/18/2001  | 01/29/2009 | SEMICONDUCTOR DEVICE AND MANUFACTURING                                                                                                                                                           |
| 60217591.7            | AF02200DE                 | Germany | 03/18/2002  | 01/17/2007 | MEMORY CONTROLLER FOR MULTI LEVEL                                                                                                                                                                |
| 60315508.1            | AF02230DE                 | Germany | 12/17/2003  | 08/08/2007 | SEMICONDUCTOR DEVICE AND TEST METHOD                                                                                                                                                             |
| 60314287.7            | AF02233DE                 | Germany | 12/17/2003  | 06/06/2007 | NONVOLATILE MEMORY AND METHOD AND WRITE METHOD OF THE SAME                                                                                                                                       |
| 10100939              | AF02649DE                 | Germany | 01/10/2001  | 01/10/2001 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                          |
| 112009002426.2        | AF04025DE                 | Germany | 10/07/2009  |            | REAL-TIME DATA PATTERN ANALYSIS SYSTEM AND METHOD OF OPERATION THEREOF                                                                                                                           |
| 112004000257.5        | AF04043JP                 | Germany | 02/05/2004  |            | RADIATION-SENSITIVE RESIN COMPOSITION, PROCESS FOR PRODUCING THE SAME AND PROCESS FOR PRODUCING SEMICONDUCTOR DEVICE THEREWITH                                                                   |
| 69517268.9            | B001DE                    | Germany | 06/30/1995  | 05/31/2000 | A SELF-ALIGNED BURIED CHANNEL/JUNCTION STACKED GATE FLASH MEMORY CELL                                                                                                                            |
| 69508273.6            | B011/2097DE               | Germany | 11/08/1995  | 03/10/1999 | NITRIDE ETCH PROCESS WITH CRITICAL DIMENSION (CD) GAIN                                                                                                                                           |
| 69637352.1            | B100DE                    | Germany | 07/31/1996  | 12/05/2007 | THREE-DIMENSIONAL NON-VOLATILE MEMORY                                                                                                                                                            |
| 69620559.9            | B111DE                    | Germany | 06/21/1996  | 04/10/2002 | PROCESS FOR SELF-ALIGNED SOURCE FOR HIGH DENSITY MEMORY                                                                                                                                          |
| 69702195.5            | B247ADE                   | Germany | 01/31/1997  | 05/31/2000 | A MULTI-LEVEL FLASH SHIFT REGISTER PAGE BUFFER                                                                                                                                                   |
| 69702256.0            | B247DE                    | Germany | 01/31/1997  | 06/07/2000 | A METHOD FOR DOUBLE DENSITY FLASH EPROM WITH PAGE MODE PROGRAM AND READ                                                                                                                          |
| 69603742.4-08         | B261DE                    | Germany | 06/21/1996  | 08/11/1999 | A PROGRAM ERASE ALGORITHM THAT GREATLY REDUCES UNDER ERASE IN FLASH MEMORIES                                                                                                                     |
| 69738821.2            | B277DE                    | Germany | 03/25/1997  | 07/09/2008 | A NOVEL PROCESS FOR RELIABLE ULTRATHIN OXYNITRIDE FORMATION                                                                                                                                      |
| 69727071.8            | B287DE                    | Germany | 02/28/1997  | 01/02/2004 | A METHOD AND SYSTEM FOR PROVIDING A DOUBLE DIFFUSE IMPLANT JUNCTION IN A VERY SHORT CHANNEL FLASH DEVICE                                                                                         |
| 69702196.3            | C072296DE                 | Germany | 03/28/1997  | 05/31/2000 | USING FLOATING GATE DEVICES AS SELECT GATE DEVICES FOR NAND FLASH MEMORY AND ITS BIAS SCHEME                                                                                                     |
| 69804122.4            | C141496DE                 | Germany | 04/10/1998  | 03/06/2002 | A DUAL SOURCE SIDE POLYSILICON SELECT GATE STRUCTURE AND PROGRAMMING METHOD UTILIZING SINGLE TUNNEL OXIDE FOR NAND ARRAY FLASH MEMORY                                                            |
| 0963587               | C144496DE                 | Germany | 02/05/1998  | 01/16/2002 | HIGH VOLTAGE NMOS PASS GATE FOR INTEGRATED CIRCUIT WITH HIGH VOLTAGE GENERATOR AND FLASH NON-VOLATILE MEMORY DEVICE HAVING THE PASS GATE                                                         |
| 69707502.8            | C196596DE                 | Germany | 11/13/1997  | 10/17/2001 | BANK ARCHITECTURE FOR A NON-VOLATILE MEMORY ENABLING SIMULTANEOUS READING AND WRITING                                                                                                            |
| 69804013.9            | C369297DE                 | Germany | 12/18/1998  | 02/27/2002 | BIASING METHOD AND STRUCTURE FOR REDUCING BAND-TO-BAND AND/OR AVALANCHE CURRENTS DURING THE ERASE OF FLASH MEMORY DEVICE                                                                         |
| 69825296.9            | C526397DE                 | Germany | 08/25/1998  | 07/28/2004 | REDUCTION OF CHARGE LOSS IN NONVOLATILE MEMORY CELLS BY PHOSPHOROUS IMPLANTATION INTO PECVD NITRIDE/OXYNITRIDE FILMS                                                                             |
| 69841724.0            | C627497DE                 | Germany | 12/18/1998  | 05/20/2010 | METHODS AND ARRANGEMENTS FOR IMPROVED FORMATION OF CONTROL AND FLOATING GATES IN NON-VOLATILE MEMORY SEMICONDUCTOR DEVICES                                                                       |
| 60034369.3            | C656497DE                 | Germany | 08/31/2000  | 04/11/2007 | TUNGSTEN GATE MOS TRANSISTOR AND MEMORY CELL AND METHOD OF MAKING SAME                                                                                                                           |
| 1204989               | C695497DE                 | Germany | 06/29/2000  | 04/02/2014 | THIN FLOATING GATE AND CONDUCTIVE SELECT GATE IN SITU                                                                                                                                            |
| 69903966.5            | C715497DE                 | Germany | 09/21/1999  | 11/13/2002 | WORDLINE DRIVER FOR FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EEPROM)                                                                                                           |
| 60001587.4            | C725497DE                 | Germany | 08/01/2000  | 03/05/2003 | CIRCUIT IMPLEMENTATION TO QUENCH BIT LINE LEAKAGE CURRENT IN PROGRAM AND AUTO PROGRAM DISTURB MODE IN FLASH EPROM USING RESISTOR SOURCE LOAD                                                     |
| 69910236.7-08         | D016DE                    | Germany | 10/05/1999  | 08/06/2003 | BIT LINE BIASING METHOD TO ELIMINATE PROGRAM DISTURBANCE IN A NON-VOLATILE MEMORY DEVICE AND MEMORY DEVICE EMPLOYING THE SAME                                                                    |
| 60101319.0            | D1030DE                   | Germany | 02/07/2001  | 11/26/2003 | TEMPERATURE COMPENSATED BIAS GENERATOR                                                                                                                                                           |
| 69904856.7            | D138                      | Germany | 10/05/1999  | 01/08/2003 | SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON-VOLATILE MEMORY ARRAY                                                                                                                            |
| 69905595.4            | D139DE                    | Germany | 08/16/1999  | 02/26/2003 | BANK SELECTOR CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITETURE                                                                                |
| 69901513.8            | D168DE                    | Germany | 08/16/1999  | 05/15/2002 | SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                                                                                    |
| 1116236               | D169DE                    | Germany | 08/16/1999  | 05/15/2002 | METHOD OF MAKING FLEXIBLY PARTITIONED METAL LINE SEGMENTS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                                           |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                        |
|-----------------------|---------------------------|---------|-------------|------------|------------------------------------------------------------------------------------------------------------------------------|
| 69903576.7            | D170DE                    | Germany | 08/16/1999  | 10/16/2002 | MEMORY ADDRESS DECODING CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE |
| 69939491.0            | D802DE                    | Germany | 10/27/1999  | 09/03/2008 | METHOD FOR IMPROVING ELECTROSTATIC DISCHARGE (ESD) ROBUSTNESS                                                                |
| 60001437.5            | D832DE                    | Germany | 05/05/2000  | 02/26/2003 | RAMPED OR STEPPED GATE CHANNEL ERASE FOR FLASH MEMORY APPLICATION                                                            |
| 60043444.3            | D833DE                    | Germany | 08/29/2000  | 10/15/2009 | 1 TRANSISTOR FOR EEPROM APPLICATION                                                                                          |
| 60030461.2            | D838DE                    | Germany | 10/24/2000  | 08/30/2006 | SOLID-SOURCE DOPING FOR SOURCE/DRAIN OF FLASH MEMORY                                                                         |
| 60128896.3            | D862DE                    | Germany | 02/27/2001  | 06/13/2007 | NEW METHOD TO FABRICATE A HIGH COUPLING FLASH CELL WITH LESS SILICIDE SEAM PROBLEM                                           |
| 1218941               | D877DE                    | Germany | 07/17/2000  | 04/02/2014 | NON-VOLATILE MEMORY HAVING HIGH GATE COUPLING CAPACITANCE                                                                    |
| 60037901.9            | D894DE                    | Germany | 09/29/2000  | 01/29/2009 | METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITH REDUCED ARC LOSS IN PERIPHERAL CIRCUITRY REGION                          |
| 60037528.5            | DA01016DE                 | Germany | 07/14/2000  | 12/19/2007 | METHOD FOR PROVIDING A DOPANT LEVEL FOR POLYSILICON FOR FLASH MEMORY DEVICES                                                 |
| 10196140.5            | DA01025                   | Germany | 04/03/2001  |            | FLASH MEMORY ARRAY AND A METHOD AND SYSTEM OF FABRICATION THEREOF                                                            |
| 60005064.5            | E0251DE                   | Germany | 07/14/2000  | 09/03/2003 | FLASH MEMORY ARCHITECTURE EMPLOYING THREE LAYER METAL INTERCONNECT                                                           |
| 60101677.7            | E0264DE                   | Germany | 02/07/2001  | 01/02/2004 | TRIMMING METHOD FOR WORDLINE BOOSTER TO MINIMIZE PROCESS VARIATION OF BOOSTED WORDLINE VOLTAGE                               |
| 1282915               | E0302EP                   | Germany | 05/01/2001  | 11/05/2014 | UNIFORM BITLINE STRAPPING OF NON-VOLATILE MEMORY CELL                                                                        |
| 60102466.4            | E0462DE                   | Germany | 05/21/2001  | 03/24/2004 | DUAL PORTED CAMS FOR SIMULTANEOUS OPERATION FLASH MEMORY                                                                     |
| 60143125.1.           | F0257DE                   | Germany | 08/07/2001  | 09/22/2010 | METHOD AND SYSTEM FOR EMBEDDED CHIP ERASE VERIFICATION                                                                       |
| 10297640.6            | F0258DE                   | Germany | 12/17/2002  |            | METHOD AND APPARATUS FOR SOFT PROGRAM VERIFICATION IN A MEMORY DEVICE                                                        |
| 60204600.9-08         | F0262DE                   | Germany | 12/17/2002  | 06/08/2005 | METHOD AND APPARATUS FOR SOFT PROGRAM VERIFICATION IN A MEMORY DEVICE                                                        |
| 10297641.4            | F0272DE                   | Germany | 12/17/2002  |            | CHARGE INJECTION                                                                                                             |
| 1366497               | F0274DE                   | Germany | 11/01/2001  | 06/04/2014 | HIGHER PROGRAM VT AND FASTER PROGRAMMING RATES BASED ON IMPROVED ERASE METHODS                                               |
| 60238549.0            | F0283DE                   | Germany | 09/27/2002  | 12/08/2010 | SALICIDED GATE FOR VIRTUAL GROUND ARRAYS                                                                                     |
| 60232651.6            | F1067DE                   | Germany | 02/19/2002  | 06/17/2009 | THRESHOLD VOLTAGE COMPACTING FOR NON-VOLATILE SEMICONDUCTOR MEMORY DESIGNS                                                   |
| 0664604               | FMA13-0011US CON          | Germany | 12/13/1994  | 03/26/2003 | TRANSIMPEDANCE AMPLIFIER                                                                                                     |
| 69412360              | FMA13-0015EP              | Germany | 05/26/1994  | 08/12/1998 | POWER LINE CONNECTION CIRCUIT AND POWER LINES SWITCH IC FOR THE SAME                                                         |
| 102008006648.6        | FMA13-00311DE             | Germany | 01/29/2008  |            | SIMULATOR ENGINE DEVELOPMENT SYSTEM AND ...                                                                                  |
| 102009018928.9        | FMA13-00375DE             | Germany | 04/28/2009  |            | LINE PLOTTING METHOD                                                                                                         |
| 0990987               | FMA13-00448US             | Germany | 04/22/1999  | 03/22/2006 | ELECTRONIC DEVICE WITH FLASH MEMORY BUILT-IN                                                                                 |
| 2345148               | FMA13-00472CN             | Germany | 11/11/2008  | 09/03/2014 | METHOD OF DETECTING AN OPERATING CONDITION OF AN ELECTRIC STEPPER MOTOR                                                      |
| 2381450               | FMA13-00503CN DIV         | Germany | 02/03/2011  | 07/16/2014 | SEMICONDUCTOR MEMORY                                                                                                         |
| 0845864               | FMA13-0051US              | Germany | 07/11/1997  | 02/09/2005 | LEVEL CONVERTER AND SEMICONDUCTOR DEVICE                                                                                     |
| 1239573               | FMA13-00539CN             | Germany | 01/07/2002  | 05/26/2010 | OVERVOLTAGE PROTECTOR FOR ELECTRIC POWER SYSTEM, AC/DC CONVERTER AND DC/DC CONVERTER CONSTITUTING THE POWER SYSTEM           |
| 10150472.1            | FMA13-00540US             | Germany | 10/16/2001  |            | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE WITH VARIABLE GAIN AMPLIFIER                                                         |
| 60205518              | FMA13-00544DE             | Germany | 03/18/2002  | 08/17/2005 | MODE SWITCHING METHOD FOR PLL CIRCUIT AND MODE CONTROL CIRCUIT FOR PLL CIRCUIT                                               |
| 1324477               | FMA13-00551CN             | Germany | 12/06/2002  | 08/09/2006 | BIPOLAR SUPPLY VOLTAGE GENERATOR AND SEMICONDUCTOR DEVICE FOR THE SAME                                                       |
| 0878910               | FMA13-0063US              | Germany | 11/10/1997  | 05/23/2007 | SKEW-REDUCTION CIRCUIT                                                                                                       |
| 1016969               | FMA13-0076US              | Germany | 12/22/1999  | 03/24/2004 | MICROCONTROLLER PROVIDED WITH SUPPORT FOR DEBUGGING                                                                          |
| 19950255              | FMA13-0083US              | Germany | 10/18/1999  | 05/13/2004 | MIKROPROZESSOR                                                                                                               |
| 1530293               | FMA13-0089DE              | Germany | 03/29/2000  | 01/24/2007 | VOLTAGE CONTROLLED OSCILLATOR CIRCUIT                                                                                        |
| 1058385               | FMA13-0089US              | Germany | 03/29/2000  | 06/01/2005 | COMPARATOR CIRCUIT                                                                                                           |
| 10012079              | FMA13-0092US              | Germany | 03/14/2000  | 02/17/2005 | TAKTSTEUERSCHALTUNG UND- VERFAHREN                                                                                           |
| 1227591               | FMA13-0093CN              | Germany | 08/18/2000  | 01/25/2006 | FREQUENCY MEASUREMENT CIRCUIT??                                                                                              |
| 1202245               | FMA13-0110US              | Germany | 05/02/2002  | 10/05/2011 | DOT-INVERSION DATA DRIVER FOR LIQUID CRYSTAL DISPLAY DEVICE WITH REDUCED POWER CONSUMPTION                                   |
| 1164701               | FMA13-0115US              | Germany | 05/09/2001  | 09/13/2006 | FRACTIONAL-N-PLL FREQUENCY SYNTHESIZER AND PHASE ERROR CANCELING METHOD THEREFOR                                             |
| 1239574               | FMA13-0122CN              | Germany | 03/05/2002  | 05/16/2007 | DC-DC CONVERTER, POWER SUPPLY CIRCUIT, AND METHOD FOR CONTROLLING THE SAME                                                   |
| 1826775               | FMA13-0132DE DIV          | Germany | 01/30/2002  | 09/07/2011 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                      |
| 1826776               | FMA13-0132DE DIV1         | Germany | 01/30/2002  | 04/27/2011 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                      |
| 1830364               | FMA13-0132DE DIV2         | Germany | 01/30/2002  | 12/10/2008 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                      |
| 10253333.4            | FMA13-0143US              | Germany | 11/14/2002  |            | RECEIVING CIRCUIT                                                                                                            |
| 1349106               | FMA13-0158CN              | Germany | 01/31/2003  | 12/14/2005 | FINGER MOVEMENT DETECTION METHOD AND APPARATUS                                                                               |
| 1435694               | FMA13-0177CN              | Germany | 12/23/2003  | 08/30/2006 | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT JITTER GENERATION CIRCUIT AND SEMICONDUCTOR DEVICE                                  |
| 1641124               | FMA13-0177DE              | Germany | 12/23/2003  | 06/03/2009 | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT                                                                                     |
| 1672800               | FMA13-0177DE1             | Germany | 12/23/2003  | 08/19/2009 | JITTERY GENERATION CIRCUIT                                                                                                   |

# **ASSIGNMENT SCHEDULE A**

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|-----------------------|---------------------------|---------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------|
| 60343962.4            | FMA13-0178US              | Germany | 03/03/2003  | 05/01/2013 | VARIABLES MOS-KAPAZITÄTSBAUELEMENT                                                                                              |
| 1657821               | FMA13-0197DE              | Germany | 11/28/2003  | 05/23/2007 | SD MODULATOR OF PLL CIRCUIT                                                                                                     |
| 1830196               | FMA13-0200DE              | Germany | 06/16/2004  | 09/19/2007 | TEST MODE ACTIVATION BY PHASE COMPARISON                                                                                        |
| 1557682               | FMA13-0200US DIV          | Germany | 06/16/2004  | 09/19/2007 | TEST MODE ACTIVATION BY PHASE COMPARISON                                                                                        |
| 1596208               | FMA13-0211CN              | Germany | 04/04/2005  | 07/29/2009 | CAPACITANCE DIFFERENCE DETECTING CIRCUIT AND MEMS SENSOR                                                                        |
| 1857826               | FMA13-0211DE              | Germany | 04/04/2005  | 07/29/2009 | CAPACITANCE DIFFERENCE DETECTING CIRCUIT AND MEMS SENSOR                                                                        |
| 1612682               | FMA13-0227CN              | Germany | 01/26/2005  | 08/20/2008 | DYNAMIC MEMORY RECONFIGURATION                                                                                                  |
| 1906312               | FMA13-0227DE              | Germany | 01/26/2005  | 08/20/2008 | DYNAMIC MEMORY CONFIGURATION                                                                                                    |
| 1689088               | FMA13-0238DE              | Germany | 05/17/2005  | 09/02/2009 | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT AND A METHOD<br>OF CONTROLLING THEREOF                                                 |
| 1708359               | FMA13-0248US              | Germany | 08/08/2005  | 03/14/2012 | AMPLIFICATION CIRCUIT AND CONTROL METHOD OF AMPLIFICATION                                                                       |
| 102006010284.3        | FMA13-0256US              | Germany | 03/02/2006  |            | SEMICONDUCTOR DEVICE WITH OPERATION MODE SET BY<br>EXTERNAL RESISTOR                                                            |
| 1748562               | FMA13-0266CN              | Germany | 11/01/2005  | 05/07/2008 | CLOCK GENERATING CIRCUIT AND CLOCK GENERATING METHOD                                                                            |
| 1764922               | FMA13-0269CN              | Germany | 12/13/2005  | 10/29/2008 | CLOCK GENERATION CIRCUIT AND CLOCK GENERATION METHOD                                                                            |
| 1832985               | FMA13-0287CN              | Germany | 09/26/2006  | 07/04/2012 | RECONFIGURABLE CIRCUIT                                                                                                          |
| 2107681               | FMA13-0289DE              | Germany | 08/21/2006  | 07/19/2007 | PRESCALER CIRCUIT AND BUFFER CIRCUIT                                                                                            |
| 60143856.6            | G0074DE                   | Germany | 12/14/2001  | 01/12/2011 | SOURCE DRAIN IMPLANT DURING ONO FORMATION FOR IMPROVED<br>ISOLATION OF SONOS DEVICES                                            |
| 60302473.4            | G0391DE                   | Germany | 06/10/2003  | 11/23/2005 | BUILT-IN-SELF-TEST (BIST) OF FLASH MEMORY CELLS AND<br>IMPLEMENTATION OF BIST INTERFACE                                         |
| 60235721.7            | G0689DE                   | Germany | 12/11/2002  | 03/10/2010 | SHALLOW TRENCH ISOLATION APPROACH FOR IMPROVED STI<br>CORNER ROUNDING                                                           |
| 10393870.2            | G0730DE                   | Germany | 09/24/2003  | 05/16/2012 | METHOD AND SYSTEM FOR REDUCING CONTACT DEFECTS USING<br>NON CONVENTIONAL CONTACT FORMATION METHOD FOR<br>SEMICONDUCTOR CELLS    |
| 112004000254          | G0752DE                   | Germany | 01/08/2004  | 02/16/2012 | IMPROVED PERFORMANCE IN FLASH MEMORY DEVICES                                                                                    |
| 1497833               | G0861DE                   | Germany | 02/14/2003  | 12/08/2008 | IMPROVED ERASE METHOD FOR SINGLE SIDED MIRROR OPERATION                                                                         |
| 60329834.6            | G0862DE                   | Germany | 02/14/2003  | 10/01/2009 | REFRESH SCHEME FOR DYNAMIC PAGE PROGRAMMING                                                                                     |
| 10392492.2            | G0864DE                   | Germany | 02/14/2003  |            | REFRESH SCHEME FOR DYNAMIC PAGE PROGRAMMING                                                                                     |
| 60330499.0            | G0865DE                   | Germany | 07/10/2003  | 12/02/2009 | METHOD AND SYSTEM FOR DEFINING A REDUNDANCY WINDOW<br>AROUND A PARTICULAR COLUMN IN A MEMORY ARRAY                              |
| 60303511.6            | G0866DE                   | Germany | 04/22/2003  | 02/08/2006 | STEPPED PRE-ERASE VOLTAGE FOR MIRRORBIT ERASE                                                                                   |
| 10392271.7            | G1255DE                   | Germany | 02/05/2003  |            | PARTIAL PAGE PROGRAMMING OF MULTI LEVEL FLASH                                                                                   |
| 60331097.4            | H0297DE                   | Germany | 07/10/2003  | 02/09/2010 | CONTROL OF MEMORY ARRAYS UTILIZING ZENER DIODE-LIKE<br>DEVICES                                                                  |
| 112005002286.2        | H0325DE                   | Germany | 09/19/2005  |            | CONTROL OF MEMORY DEVICES POSSESSING VARIABLE<br>RESISTANCE CHARACTERISTICS                                                     |
| 112005000724.3        | H0346DE                   | Germany | 02/11/2005  |            | IN-SITU SURFACE TREATMENT FOR MEMORY CELL FORMATION                                                                             |
| 112004000423.3        | H0354DE                   | Germany | 03/01/2004  |            | SPIN ON POLYMERS FOR ORGANIC MEMORY DEVICES                                                                                     |
| 112005000747.2        | H0368DE                   | Germany | 02/11/2005  |            | POLYMER DIELECTRICS FOR ME ARRAY INTERN CONNECT                                                                                 |
| 112004001234.1        | H0422DE                   | Germany | 05/11/2004  |            | METHOD AND SYSTEM FOR MANUFACTURING POLYMER MEMORY<br>DEVICE IN VIA OPENING                                                     |
| 112004001855.2        | H0423DE                   | Germany | 09/16/2004  |            | SELF ASSEMBLY OF CONDUCTING POLYMER FOR FORMATION OF<br>POLYMER MEMORY CELL                                                     |
| 60331462.7            | H0434DE                   | Germany | 07/10/2003  | 02/24/2010 | STACKED ORGANIC MEMORY DEVICES AND METHODS OF<br>OPERATING AND FABRICATING                                                      |
| 602004005333.3        | H0437DE                   | Germany | 05/11/2004  | 03/14/2007 | PLANAR POLYMER MEMORY DEVICE                                                                                                    |
| 1556887               | H0514DE                   | Germany | 06/10/2003  | 06/18/2009 | NITROGEN OXIDATION TO REDUCE ENCROACHMENT                                                                                       |
| 112004001628          | H0541DE                   | Germany | 07/15/2004  | 11/27/2014 | LOW POWER CHARGE PUMP                                                                                                           |
| 60317930.4            | H0570DE                   | Germany | 07/24/2003  | 12/05/2007 | IMPROVED SYSTEM FOR PROGRAMMING A NON-VOLATILE MEMORY<br>CELL                                                                   |
| 60321716.8            | H0575DE                   | Germany | 07/24/2003  | 06/18/2008 | IMPROVED PRE-CHARGE METHOD FOR READING A NON-VOLATILE<br>MEMORY CELL ARRAY WITH STAGGERED LOCAL INTERCONNECT<br>STRUCTURE       |
| 602004007815.8        | H0576DE                   | Germany | 09/16/2004  | 07/25/2007 | RECESS CHANNEL FLASH ARCHITECTURE FOR REDUCED SHORT<br>CHANNEL EFFECT                                                           |
| 112004001922          | H0577DE                   | Germany | 09/16/2004  | 01/22/2009 | METHOD OF PROGRAMMING DUAL CELL MEMORY DEVICE TO STORE<br>MULTIPLE DATA STATES PER CELL                                         |
| 112004000658          | H0587DE                   | Germany | 03/08/2004  | 12/31/2014 | METHOD OF DUAL CELL MEMORY DEVICE OPERATION FOR<br>IMPROVED END-OF-LIFE READ MARGIN                                             |
| 112004000703.8        | H0588DE                   | Germany | 03/08/2004  |            | IMPROVED METHOD FOR READING A NON-VOLATILE MEMORY CELL<br>ADJACENT TO AN INACTIVE REGION OF A NON-VOLATILE MEMORY<br>CELL ARRAY |
| 602004033624.6        | H0625DE                   | Germany | 01/08/2004  | 07/27/2011 | MEMORY DEVICE AND METHOD USING POSITIVE GATE STRESS TO<br>RECOVER OVERERASED CELL                                               |
| 112004001862.5        | H0626DE                   | Germany | 09/16/2004  |            | IMPROVED PERFORMANCE IN FLASH MEMORY DEVICES                                                                                    |
| 112004000248.6        | H0671DE                   | Germany | 01/08/2004  |            | CASCADE AMPLIFIER CIRCUIT FOR PRODUCING A FAST, STABLE AND<br>ACCURATE BITLINE VOLTAGE                                          |
| 60327239.8            | H1203DE                   | Germany | 07/10/2003  | 04/15/2009 | SELECTION CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS                                                                           |
| 112004000268.0        | H1204DE                   | Germany | 01/08/2004  |            | CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS                                                                                     |
| 60325509.4            | H1205DE                   | Germany | 07/24/2003  | 01/05/2009 | PECVD SILICON-RICH OXIDE LAYER FOR REDUCED UV CHARGING                                                                          |
| 602004033102.3        | H1368DE                   | Germany | 06/18/2004  | 06/15/2011 | NON-VOLATILE MEMORY DEVICE                                                                                                      |
| 112004001049          | H1414DE                   | Germany | 06/05/2004  | 02/24/2011 | FLASH MEMORY DEVICE                                                                                                             |
| 112004002399.8        | H1415DE                   | Germany | 10/26/2004  |            | CIRCUIT FOR FAST AND ACCURATE MEMORY READ OPERATIONS                                                                            |
| 1602109               | H1513DE                   | Germany | 03/01/2004  | 10/15/2008 | MEMORY CELL STRUCTURE HAVING NITRIDE LAYER WITH REDUCED<br>CHARGE LOSS AND METHOD FOR FABRICATING SAME                          |
| 112004001510.3        | H1862DE                   | Germany | 08/31/2004  |            | FAST, ACCURATE AND LOW POWER SUPPLY VOLTAGE BOOSTER<br>USING A/D CONVERTER                                                      |
| 112004000588.4        | H1892DE                   | Germany | 03/08/2004  |            |                                                                                                                                 |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL NO. | SPANSION REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                        |
|--------------------|------------------------|---------|-------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 1434232            | H1979DE                | Germany | 08/13/2001  | 09/19/2007 | MEMORY CELL                                                                                                                                  |
| 112005001008.2     | H1984DE                | Germany | 02/11/2005  |            | METHODS AND APPARATUS FOR WORDLINE PROTECTION IN FLASH MEMORY DEVICES                                                                        |
| 602005020270.6     | H1993DE                | Germany | 02/11/2005  | 04/16/2010 | BITLINE IMPLANT UTILIZING DUAL POLY                                                                                                          |
| 602006041959.7     | H1998DE                | Germany | 04/04/2006  | 06/18/2014 | A NON-CRITICAL COMPLEMENTARY MASKING METHOD FOR POLY-1 DEFINITION IN FLASH MEMORY DEVICE FABRICATION                                         |
| 69939375.2         | JC688497DE             | Germany | 02/11/1999  |            | ELIMINATION OF POLY-CAP FOR EASY POLY1 CONTACT FOR NAND PRODUCT                                                                              |
| 10 2005 020062.1   | JDE0584DE              | Germany | 04/29/2005  |            | PORTABLE WIRELESS DATA STORAGE DEVICE                                                                                                        |
| 60235721           | P116WO-DE              | Germany | 12/11/2002  | 03/17/2010 | A SHALLOW TRENCH ISOLATION APPROACH FOR IMPROVED STI CORNER ROUNDING                                                                         |
| 60122059.5         | P-2505DE               | Germany | 06/15/2001  | 03/08/2007 | Transfer In Progress - Incomplete Record                                                                                                     |
| 20051037072        | P-6415US               | Germany | 08/12/2004  | 08/22/2006 | DYNAMIC MATCHING OF SIGNAL PATH AND REFERENCE PATH FOR SENSING                                                                               |
| 60318714.5         | SE0002DE               | Germany | 03/11/2003  | 01/08/2009 | A SYSTEM AND METHOD OF ERASE VOLTAGE CONTROL DURING MULTIPLE SECTOR ERASE OF A FLASH MEMORY DEVICE                                           |
| 112013003845.5     | SP09-0058DE            | Germany | 07/31/2013  |            | POWER SAVINGS APPARATUS AND METHOD FOR MEMORY DEVICE USING DELAY LOCKED LOOP                                                                 |
| 112013003828.5     | SP12-0021DE            | Germany | 07/29/2013  |            | BITLINE VOLTAGE REGULATION IN NON-VOLATILE MEMORY                                                                                            |
| 10 2015 203 202.7  | SP13-0036DE            | Germany | 02/23/2015  |            | MEMORY SUBSYSTEM WITH WRAPPED-TO-CONTINUOUS READ                                                                                             |
| 69429973.1         | TT0381US               | Germany | 12/12/1994  | 02/27/2002 | FLASH EPROM DEVICES                                                                                                                          |
| 69620283.2         | TT0497US DIV           | Germany | 01/30/1996  | 04/03/2002 | A NON-VOLATILE MEMORY DEVICES HAVING A FLOATING GATE WITH ENHANCED CHANGE RETENTION                                                          |
| 69708669.0         | TT1997DE               | Germany | 09/29/1997  | 11/28/2001 | MEMORY BLOCK SELECT USING MULTIPLE WORD LINES TO ADDRESS A SINGLE MEMORY CELL ROW                                                            |
| 1218938            | DA01016IE              | Ireland | 07/14/2000  | 12/19/2007 | METHOD FOR PROVIDING A DOPANT LEVEL FOR POLYSILICON FOR FLASH MEMORY DEVICES                                                                 |
| 145531             | AF02593IL              | Israel  | 01/18/2000  |            | SHARED MEMORY APPARATUS AND METHOD FOR MULTIPROCESSOR SYSTEMS                                                                                |
| 134304             | P-1025IL               | Israel  | 08/02/1998  | 12/09/2004 | TWO BIT NON-VOLATILE ELECTRICALLY ERASABLE AND PROGRAMMABLE SEMICONDUCTOR MEMORY CELL UTILIZING ASYMMETRICAL CHARGE TRAPPING                 |
| 19980124846        | P-1164IL               | Israel  | 06/10/1998  |            | AN NROM FABRICATION METHOD                                                                                                                   |
| 125604             | P-1326IL               | Israel  | 07/30/1998  | 06/29/2004 | NON-VOLATILE ELECTRICALLY ERASABLE AND PROGRAMMABLE SEMICONDUCTOR MEMORY CELL UTILIZING ASYMMETRICAL CHARGE TRAPPING                         |
| 144680             | P-1907IL               | Israel  | 08/01/2001  | 10/26/2005 | METHOD FOR INITIATING A RETRIEVAL PROCEDURE IN VIRTUAL GROUND ARRAYS                                                                         |
| 148959             | P-2448US CON           | Israel  | 04/05/2001  | 12/03/2002 | ARCHITECTURE AND SCHEME FOR A NON-STROBED READ SEQUENCE                                                                                      |
| 148960             | P-2448US CON           | Israel  | 11/21/2002  |            | PROGRAMMING AND ERASING METHODS FOR A REFERENCE CELL OF AN NROM ARRAY                                                                        |
| 152465             | P-4006IL               | Israel  | 10/24/2002  | 11/02/2006 | METHOD FOR ERASING A MEMORY CELL                                                                                                             |
| 152913             | P-4007IL               | Israel  | 11/18/2002  |            | PROTECTIVE LAYER IN MEMORY DEVICE AND METHOD THEREFOR                                                                                        |
| 154205             | P-4676IL               | Israel  | 01/30/2003  | 11/21/2006 | METHOD FOR OPERATING A MEMORY DEVICE                                                                                                         |
| 0677850            | A960/2054IT            | Italy   | 03/23/1995  | 05/09/2001 | METHOD AND APPARATUS FOR PROGRAMMING MEMORY DEVICES                                                                                          |
| 1116240            | C715497                | Italy   | 09/21/1999  | 11/13/2002 | WORDLINE DRIVER FOR FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EEPROM)                                                       |
| 1203378            | C725497                | Italy   | 08/01/2000  | 03/05/2003 | CIRCUIT IMPLEMENTATION TO QUENCH BIT LINE LEAKAGE CURRENT IN PROGRAM AND AUTO PROGRAM DISTURB MODE IN FLASH EPROM USING RESISTOR SOURCE LOAD |
| 1125302            | D138                   | Italy   | 10/20/1998  | 11/30/1999 | SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON-VOLATILE MEMORY ARRAY                                                                        |
| 1125301            | D170                   | Italy   | 08/16/1999  | 10/16/2002 | MEMORY ADDRESS DECODING CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                 |
| 1830364            | FMA13-0132IT DIV2      | Italy   | 01/30/2002  | 12/10/2008 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                      |
| 1349106            | FMA13-0158EP           | Italy   | 01/31/2003  | 12/14/2005 | FINGER MOVEMENT DETECTION METHOD AND APPARATUS                                                                                               |
| 1553636            | FMA13-0178GB           | Italy   | 03/03/2003  | 05/01/2013 | MOS TYPE VARIABLE CAPACITANCE DEVICE                                                                                                         |
| 124.627/86         | A342/1324              | Japan   | 05/28/1986  |            | HIGH VOLTAGE ISOLATION ON CMOS NETWORKS                                                                                                      |
| 2648749            | A413/1408JP            | Japan   | 12/15/1986  | 05/16/1997 | AN IMPROVED MOS-TYPE INTEGRATED CIRCUIT STRUCTURE AND METHOD OF CONSTRUCTING SAME                                                            |
| 49766/1989         | A628C/1701JP           | Japan   | 03/01/1989  |            | EPROM ELEMENT EMPLOYING SELF-ALIGNING PROCESS                                                                                                |
| 2911476            | A629/1703JP            | Japan   | 04/20/1989  | 04/09/1999 | TWO-STEP 80A TUNNEL OXIDATION WITH PASSIVATION                                                                                               |
| 241654/1989        | A674/1751JP            | Japan   | 09/18/1989  |            | ONE TRANSISTOR FLASH EPROM CELL                                                                                                              |
| 132411/1990        | A719/1812JP            | Japan   | 05/22/1990  |            | METHOD OF FORMING AND REMOVING POLYSILICON LIGHTLY DOPED DRAIN SPACERS                                                                       |
| 341158/1990        | A738/1820JP            | Japan   | 11/29/1990  |            | PROCESS FOR FABRICATING A CONTROL GATE FOR A FLOATING GATE FET                                                                               |
| 236909/1990        | A747/1841US            | Japan   | 09/05/1990  |            | ASYNCHRONOUS/SYNCHRONOUS PIPELINE DUAL MODE MEMORY ACCESS CIRCUIT                                                                            |
| 213576/1990        | A750/1853JP            | Japan   | 08/09/1990  |            | SEMICONDUCTOR ANTIFUSE STRUCTURE AND METHOD                                                                                                  |
| 3183672            | A767/1836JP            | Japan   | 04/04/1991  | 04/27/2001 | CHARGE PUMP APPARATUS                                                                                                                        |
| 3260144            | A768/1837JP            | Japan   | 04/02/1991  | 12/14/2001 | CHARGE PUMP APPARATUS                                                                                                                        |
| 192406/1991        | A807/1897JP            | Japan   | 08/01/1991  |            | POWER CONTROL CIRCUIT                                                                                                                        |
| 53656/1992         | A808/1864JP            | Japan   | 03/13/1992  |            | METHOD OF PAGE-MODE PROGRAMMING FLASH EEPROM CELL ARRAYS                                                                                     |
| 3763590            | A887JP                 | Japan   | 10/20/1993  | 01/27/2006 | VPP POWER SUPPLY                                                                                                                             |
| 3604166            | A888/1987JP            | Japan   | 10/21/1993  | 10/08/2004 | DRAIN POWER SUPPLY                                                                                                                           |
| 3638623            | A889/1988JP            | Japan   | 10/20/1993  | 01/21/2005 | NEGATIVE POWER SUPPLY                                                                                                                        |
| 134310/1994        | A900/1996JP            | Japan   | 06/16/1994  |            | OUTPUT BUFFER CIRCUIT FOR LOW VOLTAGE EPROM                                                                                                  |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                     |
|-----------------------|---------------------------|---------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 119954/1994           | A901/1997JP               | Japan   | 06/01/1994  |            | A SYSTEM FOR ALLOWING A CONTENT ADDRESSABLE MEMORY TO OPERATE WITH MULTIPLE POWER VOLTAGE LEVELS                                          |
| 194124/1994           | A927/2024JP               | Japan   | 08/18/1994  |            | DISTRIBUTED NEGATIVE GATE POWER SUPPLY                                                                                                    |
| 3768251               | A928/2025JP               | Japan   | 08/22/1994  | 02/10/2006 | INDEPENDENT ARRAY GROUNDS FOR FLASH EEPROM WITH PAGED ERASE ARCHITECTURE                                                                  |
| 3657290               | A931/2028JP               | Japan   | 08/24/1994  | 03/18/2005 | SECTOR-BASED REDUNDANCY ARCHITECTURE                                                                                                      |
| 3813640               | A938/2033JP               | Japan   | 11/29/1994  | 06/09/2006 | PROGRAMMED REFERENCE                                                                                                                      |
| 114736/2006           | A938/2033JP DIV           | Japan   | 11/29/1994  |            | PROGRAMMED REFERENCE                                                                                                                      |
| 294652/1994           | A939/2034JP               | Japan   | 11/29/1994  |            | BOOSTED AND REGULATED GATE POWER SUPPLY WITH REFERENCE TRACKING FOR MULTI-DENSITY AND LOW VOLTAGE SUPPLY MEMORIES                         |
| 98394/1995            | A956JP                    | Japan   | 04/24/1995  |            | METHOD AND SYSTEM FOR PROTECTING STACKED GATE EDGE                                                                                        |
| 160563/1995           | A959/2050                 | Japan   | 06/27/1995  |            | FLASH EEPROM ARRAY WITH FLOATING SUBSTRATE ERASE OPERATION                                                                                |
| 3741744               | A960/2054JP               | Japan   | 04/12/1995  | 11/18/2005 | METHOD AND APPARATUS FOR PROGRAMMING MEMORY DEVICES                                                                                       |
| 165526/1995           | A975/2066                 | Japan   | 06/30/1995  |            | MULTISTEPPED TRESHOLD CONVERGENCE FOR A FLASH MEMORY ARRAY                                                                                |
| 163415/1995           | A976/2067                 | Japan   | 06/29/1995  |            | HIGH ENERGY BURIED LAYER IMPLANT TO PROVIDE A LOW RESISTANCE P-WELL IN A FLASH EPROM ARRAY                                                |
| 5185710               | A976/2067JP DIV           | Japan   | 06/30/2008  | 01/25/2013 | ELECTRICAL PATH AND METHOD OF ERASING CHARGE FROM FLOATING GATES OF MEMORY CELLS                                                          |
| 4557482               | AF01002JP                 | Japan   | 10/07/2000  | 07/30/2010 | LOW VOLTAGE READ CASCODE FOR 2V/3V AND DIFFERENT BANK COMBINATIONS WITHOUT METAL OPTIONS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE |
| 2001-532396           | AF01006JP                 | Japan   | 10/09/2000  |            | REDUNDANT DUAL BANK ARCHITECTURE FOR A SIMULTANEOUS OPERATION FLASH MEMORY                                                                |
| 2001-562498           | AF01036JP                 | Japan   | 02/07/2001  |            | WORDLINE DRIVER FOR FLASH MEMORY READ MODE                                                                                                |
| 4907815               | AF01054JP                 | Japan   | 10/16/2000  | 01/20/2012 | PROCESS FOR FABRICATING ONO FLOATING-GATE ELECTRODE IN TWO-BIT EEPROM DEVICE                                                              |
| 2001-569874           | AF01064JP                 | Japan   | 03/20/2001  |            | METHOD FOR FORMING HIGH QUALITY MULTIPLE THICKNESS OXIDE LAYERS USING HIGH TEMPERATURE DESCUM                                             |
| 4755380               | AF01066JP                 | Japan   | 03/20/2001  | 08/24/2011 | METHOD FOR FORMING HIGHQUALITY MULTIPLE THICKNESS OXIDE LAYERS BY REDUCING DESCUM INDUCED DEFECTS                                         |
| 4744761               | AF01072JP                 | Japan   | 02/05/2001  | 05/20/2011 | VOLTAGE BOOST LEVEL CLAMPING CIRCUIT FOR A FLASH MEMORY                                                                                   |
| 4916084               | AF01073JP                 | Japan   | 07/31/2001  | 02/03/2012 | WORD LINE DECODING ARCHITECTURE IN A FLASH MEMORY                                                                                         |
| 5059199               | AF01073JP DIV             | Japan   | 07/31/2001  | 08/10/2012 | CMOS DECODING CIRCUIT                                                                                                                     |
| 4744765               | AF01075JP                 | Japan   | 03/12/2001  | 05/20/2011 | MULTIPLE BANK SIMULTANEOUS OPERATION FOR A FLASH MEMORY                                                                                   |
| 4737917               | AF01076JP                 | Japan   | 05/21/2001  | 05/13/2011 | BURST ARCHITECTURE FOR A FLASH MEMORY                                                                                                     |
| 5406420               | AF01078JP                 | Japan   | 07/17/2001  | 11/08/2013 | BURST READ INCORPORATING OUPUT BASED REDUNDANCY                                                                                           |
| 2012-118740           | AF01078JP DIV             | Japan   | 07/17/2001  |            | BURST READ INCORPORATING OUPUT BASED REDUNDANCY                                                                                           |
| 4737918               | AF01085JP                 | Japan   | 06/04/2001  | 05/13/2011 | METHOD TO REDUCE CAPACITIVE LOADING IN FLASH MEMORY X-DECODER FOR ACCURATE VOLTAGE CONTROL AT WORDLINES AND SELECT LINES                  |
| 4757422               | AF01086JP                 | Japan   | 09/29/2000  | 06/10/2011 | A WORD LINE TRACKING STRUCTURE FOR USE IN AN ARRAY OF FLASH EEPROM MEMORY CELLS                                                           |
| 2001-566166           | AF01088JP                 | Japan   | 03/05/2001  |            | NAND FLASH MEMORY                                                                                                                         |
| 2007-229585           | AF01088JP DIV             | Japan   | 09/04/2007  |            | METHOD FOR MANUFACTURING NAND FLASH MEMORY                                                                                                |
| 2010-224726           | AF01088JP DIV2            | Japan   | 03/05/2001  |            | SINGLE TUNNEL GATE OXIDATION PROCESS FOR FABRICATING AND FLASH MEMORY                                                                     |
| 2002-578508           | AF01090JP                 | Japan   | 11/14/2001  |            | I/O PARTITIONING AND METHODOLOGY TO REDUCE BAND-TO-BAND TUNNELING CURRENT DURING ERASE                                                    |
| 2003-517883           | AF01094JP                 | Japan   | 03/14/2002  |            | VOLTAGE BOOST CIRCUIT USING SUPPLY VOLTAGE DETECTION TO COMPENSATE FOR SUPPLY VOLTAGE VARIATION IN READ MODE VOLTAGES                     |
| 4068464               | AF01096JP                 | Japan   | 12/12/2001  | 01/18/2008 | THE SOFT PROGRAM AND SOFT PROGRAM CERTIFICATION OF A CORE CELL IN A FLASH                                                                 |
| 5132024               | AF01102JP                 | Japan   | 08/07/2001  | 11/16/2012 | METHOD OF FORMING NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                |
| JP2003-585104         | AF01116JP                 | Japan   | 03/03/2003  |            | SYSTEM AND METHOD FOR MULTI-BIT FLASH READS USING DUAL DYNAMIC REFERENCES                                                                 |
| 4681227               | AF01124JP                 | Japan   | 12/11/2002  | 02/10/2011 | MONOS DEVICE HAVING BURIED METAL SILICIDE BIT LINE                                                                                        |
| JP2003-577341         | AF01132JP                 | Japan   | 01/21/2003  |            | HARD MASK PROCESS FOR MEMORY DEVICE WITHOUT BITLINE SHORTS                                                                                |
| JP2003-581243         | AF01134JP                 | Japan   | 01/21/2003  |            | METHOD OF MAKING MEMORY WORDLINE HARD MASK EXTENSION                                                                                      |
| JP2003-585178         | AF01137JP                 | Japan   | 02/14/2003  |            | MEMORY MANUFACTURING PROCESS WITH BITLINE ISOLATION                                                                                       |
| JP2004-530795         | AF01165JP                 | Japan   | 06/10/2003  |            | COLUMN-DECODING AND PRECHARGING IN A FLASH MEMORY DEVICE                                                                                  |
| 4601614               | AF01169JP                 | Japan   | 05/21/2004  | 10/08/2010 | MEMORY WITH A CORE-BASED VIRTUAL GROUND AND DYNAMIC REFERENCE SENSING SCHEME                                                              |
| 5255207               | AF01186JP                 | Japan   | 01/08/2004  | 04/26/2013 | MEMORY ARRAY AND ITS MANUFACTURING METHOD                                                                                                 |
| 5258193               | AF01209JP                 | Japan   | 04/13/2004  | 05/02/2013 | THE MANUFACTURING METHOD FOR FLOATING GATE TAPE                                                                                           |
| 2006-549303           | AF01214JP                 | Japan   | 12/17/2004  |            | EFFICIENT USE OF WAFER AREA WITH DEVICE UNDER THE PAD APPROACH                                                                            |
| 2006-551082           | AF01220JP                 | Japan   | 12/17/2004  |            | STRUCTURE AND METHOD FOR LOW VSS RESISTANCE AND REDUCED DIBL IN A FLOATING GATE MEMORY CELL                                               |
| 520299/2007           | AF01232JP                 | Japan   | 04/29/2005  |            | BOND PAD STRUCTURE FOR COPPER METALLIZATION HAVING INCREASED RELIABILITY AND METHOD FOR FABRICATING SAME                                  |
| 2006-511368           | AF01240JP                 | Japan   | 03/26/2004  |            | ABORT CIRCUIT FOR MLC PROGRAMMING                                                                                                         |
| 5270627               | AF01240JP DIV             | Japan   | 09/01/2010  | 05/17/2013 | SEMICONDUCTOR DEVICE                                                                                                                      |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                               |
|-----------------------|---------------------------|---------|-------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 4642017               | AF01241JP                 | Japan   | 04/13/2004  | 12/10/2010 | SECTOR PROTECTION CIRCUIT AND SECTOR PROTECTION METHOD FOR NON-VOLATILE SEMICONDUCTOR STORAGE DEVICE, AND NON-VOLATILE SEMICONDUCTOR STORAGE DEVICE |
| 4642018               | AF01248JP                 | Japan   | 04/21/2004  | 12/10/2010 | NON-VOLATILE SEMICONDUCTOR DEVICE AND METHOD FOR AUTOMATICALLY RECOVERING ERASE FAILURE IN THE DEVICE                                               |
| 4757196               | AF01273JP                 | Japan   | 07/02/2004  | 06/10/2011 | MEMORY SYSTEM AND TEST METHOD THEREOF                                                                                                               |
| 4139421               | AF01274JP                 | Japan   | 08/30/2004  | 06/13/2008 | IMPROVEMENT OF THE REDUNDANT EFFICIENCY FOR THE SEMICONDUCTOR MEMORY                                                                                |
| 2006-537605           | AF01276JP                 | Japan   | 09/29/2004  |            | SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE MANUFACTURING METHOD                                                                                  |
| 5529216               | AF01276JP DIV             | Japan   | 09/29/2004  | 04/25/2014 | SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE MANUFACTURING METHOD                                                                                  |
| 4642895               | AF01278JP                 | Japan   | 03/22/2006  | 12/10/2010 | TEMPERATURE COMPENSATION OF THIN FILM DIODE VOLTAGE THRESHOLD IN MEMORY SENSING CIRCUIT                                                             |
| 523957/2008           | AF01285                   | Japan   | 07/17/2006  |            | PROGRAM/ERASE WAVESHAPING CONTROL TO INCREASE DATA RETENTION OF A MEMORY CELL                                                                       |
| 5085530               | AF01286JP                 | Japan   | 03/22/2006  | 09/14/2012 | VARIABLE BREAKDOWN CHARACTERISTIC DIODE                                                                                                             |
| 4927727               | AF01306JP                 | Japan   | 06/30/2005  | 02/17/2012 | SWITCHABLE MEMORY DIODE- A NEW MEMORY DEVICE                                                                                                        |
| 4750119               | AF01320JP                 | Japan   | 08/08/2005  | 08/17/2011 | SYSTEMS AND METHODS FOR ADJUSTING PROGRAMMING THRESHOLDS OF POLYMER MEMORY CELLS                                                                    |
| 5255276               | AF01321GB                 | Japan   | 08/08/2005  | 04/26/2013 | POLYMER MEMORY WITH VARIABLE DATA RETENTION TIME                                                                                                    |
| 5162129               | AF01327JP                 | Japan   | 06/14/2004  | 12/21/2012 | SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE MANUFACTURING METHOD                                                                                  |
| 5552521               | AF01327JP DIV             | Japan   | 06/14/2004  | 05/30/2014 | SEMICONDUCTOR DEVICE MANUFACTURING METHOD                                                                                                           |
| 4668199               | AF01329JP                 | Japan   | 08/30/2004  | 01/21/2011 | ERASE METHOD OF A NON-VOLATILE MEMORY DEVICE AND A NON-VOLATILE MEMORY DEVICE                                                                       |
| 4499111               | AF01338JP                 | Japan   | 10/26/2004  | 04/23/2010 | METHOD OF SETTING INFORMATION OF NON-VOLATILE MEMORY AND NON-VOLATILE MEMORY                                                                        |
| 4895815               | AF01342JP CIP             | Japan   | 08/12/2005  | 01/06/2012 | SEMICONDUCTOR DEVICE AND WORD LINE BOOSTING METHOD                                                                                                  |
| 4698592               | AF01343JP                 | Japan   | 06/25/2004  | 03/11/2011 | VOLTAGE CONTROL CIRCUIT AND SEMICONDUCTOR DEVICE                                                                                                    |
| 5255609               | AF01343JP DIV             | Japan   | 08/12/2010  | 04/26/2013 | VOLTAGE CONTROL CIRCUIT AND VOLTAGE CONTROL METHOD                                                                                                  |
| 4642030               | AF01346JP                 | Japan   | 09/30/2004  | 12/10/2010 | SEMICONDUCTOR DEVICE AND METHOD FOR CONTROLLING THE SAME                                                                                            |
| 4653747               | AF01349JP                 | Japan   | 07/23/2004  | 12/24/2010 | FILE MANAGEMENT FOR RECOVERING FROM SUDDEN POWER OFF                                                                                                |
| 2006-542176           | AF01351JP                 | Japan   | 10/29/2004  |            | MULTICHIP PACKAGE AND MANUFACTURING METHOD THEREOF                                                                                                  |
| 2007-520416           | AF01361JP                 | Japan   | 06/30/2005  |            | METHOD OF IMPROVING ERASE VOLTAGE DISTRIBUTION FOR A FLASH MEMORY ARRAY HAVING DUMMY WORDLINES                                                      |
| 2007-524789           | AF01365JP                 | Japan   | 04/29/2005  |            | FLASH MEMORY UNIT AND METHOD OF PROGRAMMING A FLASH MEMORY DEVICE                                                                                   |
| 2006-537604           | AF01370JP                 | Japan   | 09/29/2004  |            | BL SHIELD                                                                                                                                           |
| 4680195               | AF01371JP                 | Japan   | 06/25/2004  | 02/10/2011 | SEMICONDUCTOR DEVICE AND SOURCE VOLTAGE CONTROL METHOD                                                                                              |
| 4541355               | AF01372JP                 | Japan   | 02/19/2004  | 07/02/2010 | CURRENT-VOLTAGE CONVERTER CIRCUIT AND CONTROL METHOD THEREOF                                                                                        |
| 4642077               | AF01379JP                 | Japan   | 04/29/2005  | 12/10/2010 | FLOATING GATE MEMORY CELL                                                                                                                           |
| 5452441               | AF01379JP DIV             | Japan   | 10/07/2010  | 01/10/2014 | METHOD FOR FABRICATING FLOATING GATE MEMORY CELL AND FLOATING GATE MEMORY CELL                                                                      |
| 4467565               | AF01380JP                 | Japan   | 02/20/2004  | 03/05/2010 | A SEMICONDUCTOR MEMORY STORAGE DEVICE AND ITS CONTROL METHOD                                                                                        |
| 4465009               | AF01383JP                 | Japan   | 09/20/2005  | 02/26/2010 | READ APPROACH FOR MULTI-LEVEL VIRTUAL GROUND MEMORY                                                                                                 |
| 4630902               | AF01386JP                 | Japan   | 02/11/2005  | 11/19/2010 | ERASE ALGORITHM FOR MULTI-LEVEL BIT FLASH MEMORY                                                                                                    |
| 4674239               | AF01390JP                 | Japan   | 12/20/2005  | 01/28/2011 | MULTI-LEVEL ONO FLASH PROGRAM ALGORITHM FOR THRESHOLD WIDTH CONTROL                                                                                 |
| 4618688               | AF01402JP                 | Japan   | 12/05/2006  | 11/05/2010 | NEW CASCADE AND SENSE-AMPLIFIER                                                                                                                     |
| 4750034               | AF01403JP                 | Japan   | 07/30/2004  | 05/27/2011 | SEMICONDUCTOR DEVICE AND WRITING METHOD                                                                                                             |
| 2006-531191           | AF01404JP                 | Japan   | 08/30/2004  |            | APPARATUS FOR ADJUSTING RAMP GATE PGM CONDITION IN MANUAL PGM                                                                                       |
| 4472701               | AF01412JP                 | Japan   | 07/29/2004  | 03/12/2010 | A NON-VOLATILITY MEMORY DEVICE AND ITS CONTROL METHOD                                                                                               |
| 4554613               | AF01413JP                 | Japan   | 07/30/2004  | 07/23/2010 | SEMICONDUCTOR DEVICE AND METHOD FOR WRITING DATA INTO SEMICONDUCTOR DEVICE                                                                          |
| 4698583               | AF01416JP                 | Japan   | 05/12/2004  | 03/11/2011 | SEMICONDUCTOR DEVICE AND ITS CONTROL METHOD                                                                                                         |
| 4642019               | AF01417JP                 | Japan   | 05/11/2004  | 12/10/2010 | NONVOLATILE SEMICONDUCTOR MEMORY, SEMICONDUCTOR DEVICE AND CHARGE PUMP CIRCUIT                                                                      |
| 4613353               | AF01422JP                 | Japan   | 10/26/2006  | 10/29/2010 | SEMICONDUCTOR DEVICE AND PROGRAM METHOD                                                                                                             |
| 4614115               | AF01423JP                 | Japan   | 05/11/2004  | 10/29/2010 | SEMICONDUCTOR DEVICE AND WRITING METHOD                                                                                                             |
| 4577849               | AF01425JP                 | Japan   | 05/11/2004  | 09/03/2010 | SEMICONDUCTOR DEVICE AND CONTROL METHOD FOR SEMICONDUCTOR DEVICE                                                                                    |
| 4623669               | AF01427JP                 | Japan   | 10/26/2006  | 11/12/2010 | SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE CONTROL METHOD                                                                                        |
| 2006-531207           | AF01432JP                 | Japan   | 08/31/2004  |            | THE SEMICONDUCTOR MEMORY STORAGE DEVICE WHICH CARRIED THE NEGATIVE VOLTAGE GENERATING CIRCUIT                                                       |
| 2006-546543           | AF01434                   | Japan   | 11/30/2004  |            | SEMICONDUCTOR DEVICE, FABRICATING METHOD THEREOF, AND PHOTOMASK                                                                                     |
| 2008-309489           | AF01434JP DIV             | Japan   | 12/04/2008  |            | METHOD FOR THE MONITORING OF THE BEST FOCUSING POSITION AND INLINE WAFER WITH THE BEST FOCUS MONITORING MARK                                        |
| 4421615               | AF01438JP                 | Japan   | 12/24/2004  | 12/11/2009 | METHOD AND APPARATUS FOR APPLYING BIAS TO A STORAGE DEVICE                                                                                          |
| 4698605               | AF01439JP                 | Japan   | 11/30/2004  | 03/11/2011 | SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE CONTROL METHOD                                                                                        |
| 2010-249631           | AF01439JP DIV             | Japan   | 11/08/2010  |            | SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE CONTROL METHOD                                                                                        |

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| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                          |
|-----------------------|--------------------------|---------|-------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 4499103               | AF01441JP                | Japan   | 07/29/2004  | 04/23/2010 | A NON-VOLATILE MEMORY APPARATUS AND ITS CONTROL METHOD                                                                                         |
| 5270598               | AF01441JP DIV            | Japan   | 03/10/2010  | 05/17/2013 | NON-VOLATILE MEMORY DEVICE                                                                                                                     |
| 5390006               | AF01441JP DIV2           | Japan   | 07/29/2004  | 10/18/2013 | A NON-VOLATILE MEMORY APPARATUS AND ITS CONTROL METHOD                                                                                         |
| 4547377               | AF01443JP                | Japan   | 05/11/2004  | 07/09/2010 | CARRIER FOR SEMICONDUCTOR DEVICES TO BE STACKED AND<br>FABRICATION METHOD OF THE DEVICE                                                        |
| 4895823               | AF01445JP                | Japan   | 12/28/2004  | 01/06/2012 | SEMICONDUCTOR DEVICE                                                                                                                           |
| 2006-513655           | AF01446JP                | Japan   | 05/20/2004  |            | SEMICONDUCTOR CHIP ASSEMBLY AND FABRICATION METHOD OF<br>THE SAME                                                                              |
| 4989630               | AF01451JP                | Japan   | 04/24/2006  | 05/11/2012 | THE ARRAY SOURCE LINE IN A NAND FLASH MEMORY                                                                                                   |
| 4674234               | AF01453JP                | Japan   | 02/11/2005  | 01/28/2011 | METHOD AND SYSTEMS FOR HIGH WRITE PERFORMANCE IN MULTI-<br>BIT FLASH MEMORY DEVICES                                                            |
| 4794462               | AF01454JP                | Japan   | 11/30/2004  | 08/05/2011 | NEW MEMORY CELL STRUCTURE IN WHICH HIGH-SPEED WRITING IS<br>POSSIBLE                                                                           |
| 5014802               | AF01455JP                | Japan   | 11/30/2004  | 06/15/2012 | SEMICONDUCTOR MEMORY AND MANUFACTURING METHOD<br>THEREOF                                                                                       |
| 2012-032938           | AF01455JP DIV            | Japan   | 11/30/2004  |            | SEMICONDUCTOR MEMORY AND MANUFACTURING METHOD<br>THEREOF                                                                                       |
| 2008-509068           | AF01459JP                | Japan   | 04/24/2006  |            | METHOD OF FABRICATING A SEMICONDUCTOR DEVICE                                                                                                   |
| 4672673               | AF01462                  | Japan   | 11/30/2004  | 01/28/2011 | SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE CONTROL<br>METHOD                                                                                |
| 4582551               | AF01463JP                | Japan   | 09/30/2004  | 09/10/2010 | SEMICONDUCTOR DEVICE AND DATA WRITING METHOD                                                                                                   |
| 5096929               | AF01467JP                | Japan   | 01/12/2006  | 09/28/2012 | MEMORY DEVICE HAVING TRAPEZOIDAL BITLINES AND METHOD OF<br>FABRICATING SAME                                                                    |
| 4777899               | AF01468JP                | Japan   | 10/29/2004  | 07/08/2011 | SEMICONDUCTOR DEVICE                                                                                                                           |
| 4738347               | AF01470JP                | Japan   | 11/30/2004  | 05/13/2011 | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREOF                                                                                                |
| 4804359               | AF01472JP                | Japan   | 10/29/2004  | 08/19/2011 | DRAIN VOLTAGE REGULATION                                                                                                                       |
| 4896011               | AF01475JP                | Japan   | 03/31/2005  | 01/06/2012 | SRAM STRUCTURE FOR NAND I/F BASED ON MIRROR BIT MEMORY<br>ARRAY                                                                                |
| 5237554               | AF01477JP                | Japan   | 10/29/2004  | 04/05/2013 | SEMICONDUCTOR DEVICE MANUFACTURING METHOD                                                                                                      |
| 5392985               | AF01479JP                | Japan   | 12/28/2004  | 10/25/2013 | SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING<br>OPERATION THEREOF                                                                            |
| 4704460               | AF01482JP                | Japan   | 05/26/2006  | 03/18/2011 | PAGE BUFFER ARCHITECTURE FOR PROGRAMMING, ERASING AND<br>READING NANOSCALE RESISTIVE MEMORY DEVICES                                            |
| 4616355               | AF01485JP                | Japan   | 06/22/2007  | 10/29/2010 | METHOD OF PROGRAMMING, READING AND ERASING MEMORY-<br>DIODE IN A MEMORY-DIODE ARRAY                                                            |
| 4854729               | AF01490JP                | Japan   | 03/24/2006  | 11/04/2011 | WRITE-ONCE READ-MANY TIMES MEMORY                                                                                                              |
| 4547008               | AF01491JP                | Japan   | 11/10/2005  | 07/09/2010 | DIODE ARRAYS ARCHITECTURE FOR ADDRESSING NANOSCALE<br>RESISTIVE MEMORY ARRAYS                                                                  |
| 5032330               | AF01500JP                | Japan   | 11/10/2005  | 07/06/2012 | METHOD OF FABRICATING ELECTRONIC DEVICE                                                                                                        |
| 5363536               | AF01500JP DIV            | Japan   | 11/10/2005  | 09/13/2013 | PROTECTION OF ACTIVE LAYERS OF MEMORY CELLS DURING<br>PROCESSING OF OTHER ELEMENTS                                                             |
| 4601672               | AF01523JP                | Japan   | 12/20/2005  | 10/08/2010 | SENSE AMPLIFIER WITH HIGH VOLTAGE SWING                                                                                                        |
| 2007-558345           | AF01524JP                | Japan   | 03/07/2006  |            | DECODER FOR MEMORY DEVICE                                                                                                                      |
| 4890435               | AF01530JP                | Japan   | 01/28/2005  | 12/22/2011 | NON-VOLATILE MEMORY AND CONTROL METHOD THEREOF                                                                                                 |
| 503121/2008           | AF01625JP                | Japan   | 03/22/2006  |            | NON-VOLATILE MEMORY SEMICONDUCTOR DEVICE AND METHOD OF<br>FORMING THE SAME                                                                     |
| 5014118               | AF01642JP                | Japan   | 02/23/2005  | 06/15/2012 | METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE INCLUDING<br>FLASH MEMORY AND SEMICONDUCTOR DEVICE INCLUDING FLASH<br>MEMORY                      |
| 4903687               | AF01643JP                | Japan   | 02/24/2005  | 01/13/2012 | SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR                                                                                           |
| 4613367               | AF01644JP                | Japan   | 08/30/2004  | 10/29/2010 | CARRIER ARRANGEMENT FOR STACKED SEMICONDUCTOR DEVICE,<br>PROCESS FOR PRODUCING SAME, AND PROCESS FOR PRODUCING<br>STACKED SEMICONDUCTOR DEVICE |
| 4619367               | AF01645JP                | Japan   | 10/26/2004  | 11/05/2010 | NON-VOLATILE MEMORY DEVICE                                                                                                                     |
| 4950037               | AF01650JP                | Japan   | 04/27/2005  | 03/16/2012 | SEMICONDUCTOR DEVICE, DATA READ OUT METHOD AND<br>SEMICONDUCTOR DEVICE MANUFACTURING METHOD                                                    |
| 4918367               | AF01653JP                | Japan   | 01/24/2005  | 02/03/2012 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE<br>SAME                                                                                  |
| 4974880               | AF01654JP                | Japan   | 01/27/2005  | 04/20/2012 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING<br>SAME                                                                                      |
| 5166870               | AF01657JP                | Japan   | 05/30/2005  | 12/28/2012 | SEMICONDUCTOR DEVICE MANUFACTURING APPARATUS AND<br>SEMICONDUCTOR DEVICE MANUFACTURING METHOD                                                  |
| 4927708               | AF01661JP                | Japan   | 02/28/2005  | 02/17/2012 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING<br>SAME                                                                                      |
| 4944766               | AF01662JP                | Japan   | 02/25/2005  | 03/09/2012 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING<br>SAME                                                                                      |
| 4675955               | AF01663JP                | Japan   | 01/28/2005  | 02/04/2011 | LAYERED SEMICONDUCTOR DEVICE CARRIER AND LAYERED<br>SEMICONDUCTOR DEVICE MANUFACTURING METHOD                                                  |
| 505450/2008           | AF01665JP                | Japan   | 04/04/2006  |            | SPLIT GATE MULTI-BIT MEMORY CELL                                                                                                               |
| 4916437               | AF01666JP                | Japan   | 03/31/2005  | 02/03/2012 | SEMICONDUCTOR DEVICE                                                                                                                           |
| 4763793               | AF01668JP                | Japan   | 09/08/2006  | 06/17/2011 | HIGH PERFORMANCE FLASH MEMORY DEVICE CAPABLE OF HIGH<br>DENSITY DATA STORAGE                                                                   |
| 2010-243038           | AF01668JP DIV            | Japan   | 09/08/2006  |            | HIGH PERFORMANCE FLASH MEMORY DEVICE CAPABLE OF HIGH<br>DENSITY DATA STORAGE                                                                   |
| 4908512               | AF01669JP                | Japan   | 09/07/2006  | 01/20/2012 | MULTI-BIT FLASH MEMORY DEVICE HAVING IMPROVED PROGRAM<br>RATE                                                                                  |
| 5047625               | AF01688JP                | Japan   | 10/25/2004  | 07/27/2012 | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF                                                                                          |
| 2006-550540           | AF01689JP                | Japan   | 12/28/2004  |            | PROCESS FOR PRODUCING SEMICONDUCTOR                                                                                                            |
| 2007-500378           | AF01690                  | Japan   | 01/27/2005  |            | A MEMORY DEVICE AND ITS CONTROL METHOD                                                                                                         |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                        |
|-----------------------|---------------------------|---------|-------------|------------|--------------------------------------------------------------------------------------------------------------|
| 4771961               | AF01691JP                 | Japan   | 12/24/2004  | 07/21/2011 | SYNCHRONOUS STORAGE DEVICE AND CONTROLLING METHOD THEREOF                                                    |
| 4927716               | AF01694JP                 | Japan   | 04/27/2005  | 02/17/2012 | SEMICONDUCTOR DEVICE                                                                                         |
| 4785917               | AF01695JP                 | Japan   | 04/26/2006  | 10/05/2011 | MULTI-CHIP MODULE AND METHOD OF MANUFACTURE                                                                  |
| 5518789               | AF01695JP DIV             | Japan   | 05/25/2011  | 04/11/2014 | MULTI-CHIP MODULE                                                                                            |
| 4991518               | AF01696JP                 | Japan   | 01/31/2005  | 05/11/2012 | LAYERED SEMICONDUCTOR DEVICE AND LAYERED SEMICONDUCTOR DEVICE MANUFACTURING METHOD                           |
| 2012-065366           | AF01696JP DIV             | Japan   | 01/31/2005  |            | PACKAGE ON PACKAGE USING CONNECTION FILM                                                                     |
| 4944763               | AF01698JP                 | Japan   | 01/27/2005  | 03/09/2012 | SEMICONDUCTOR DEVICE, ADDRESS ASSIGNMENT METHOD, AND VERIFY METHOD                                           |
| 5607581               | AF01698JP DIV             | Japan   | 01/27/2005  | 09/05/2014 | A SEMICONDUCTOR DEVICE AND A VERIFY METHOD                                                                   |
| 5099691               | AF01706JP                 | Japan   | 03/31/2005  | 10/05/2012 | SEMICONDUCTOR DEVICE                                                                                         |
| 4896010               | AF01707JP                 | Japan   | 03/31/2005  | 01/06/2012 | STACKED-TYPE SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME                                       |
| 4672767               | AF01709JP                 | Japan   | 03/22/2006  | 01/28/2011 | VARIABLE BREAKDOWN CHARACTERISTIC DIODE                                                                      |
| 4763689               | AF01713JP                 | Japan   | 03/31/2005  | 06/17/2011 | IMPROVED HYBRID READ                                                                                         |
| 4828520               | AF01721JP                 | Japan   | 08/02/2007  | 09/22/2011 | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREFOR                                                             |
| 4722123               | AF01723JP                 | Japan   | 02/23/2005  | 04/05/2011 | A MEMORY DEVICE AND ITS REDUNDANCY SETTING METHOD                                                            |
| 4738405               | AF01724JP                 | Japan   | 02/23/2005  | 05/13/2011 | A MEMORY DEVICE AND ITS TEST METHOD                                                                          |
| 4510073               | AF01725JP                 | Japan   | 01/31/2005  | 05/14/2010 | REFERENCE CELL TRIMMING IN BIST                                                                              |
| 5047786               | AF01728JP                 | Japan   | 04/27/2005  | 07/27/2012 | METHOD OF FABRICATING SEMICONDUCTOR DEVICE                                                                   |
| 5330687               | AF01729JP                 | Japan   | 05/30/2005  | 08/02/2013 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING SAME                                                       |
| 2008-508850           | AF01730JP                 | Japan   | 03/24/2006  |            | MULTI CHIP MODULE AND METHOD OF MANUFACTURE                                                                  |
| 2011-013674           | AF01730JP DIV             | Japan   | 03/24/2006  |            | MULTI CHIP MODULE AND METHOD OF MANUFACTURE                                                                  |
| 4804462               | AF01733JP                 | Japan   | 07/27/2005  | 08/19/2011 | NEW PROGRAMMING ALGORITHM FOR XTREME MODE                                                                    |
| 4950036               | AF01735JP                 | Japan   | 04/27/2005  | 03/16/2012 | METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE                                                                |
| 5014125               | AF01739JP                 | Japan   | 05/30/2005  | 06/15/2012 | SEMICONDUCTOR DEVICE AND PROGRAM DATA REDUNDANT METHOD                                                       |
| 512615/2008           | AF01741JP                 | Japan   | 05/25/2006  |            | READ-ONLY MEMORY ARRAY WITH DIELECTRIC BREAKDOWN PROGRAMMABILITY                                             |
| 2007-523280           | AF01742JP                 | Japan   | 06/30/2005  |            | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME                                                    |
| 2007-507983           | AF01743                   | Japan   | 03/16/2005  |            | MEMORY DEVICE AND ITS CONTROL METHOD                                                                         |
| 5053084               | AF01744JP                 | Japan   | 05/30/2005  | 08/03/2012 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING SAME                                                       |
| 4804459               | AF01745JP                 | Japan   | 05/30/2005  | 08/19/2011 | A IMPROVED REFERENCE CELL STRUCTURE OPTIMIZING THE PROGRAM/READ FUNCTION                                     |
| 2011-046554           | AF01745JP DIV             | Japan   | 03/03/2011  |            | A IMPROVED REFERENCE CELL STRUCTURE OPTIMIZING THE PROGRAM/READ FUNCTION                                     |
| 2008-531173           | AF01746JP                 | Japan   | 09/06/2006  |            | SPACERS BETWEEN BITLINES IN VIRTUAL GROUND MEMORY ARRAY                                                      |
| 2007-539720           | AF01757US CIP             | Japan   | 09/30/2005  |            | STORAGE DEVICE AND CONTROL METHOD THEREOF                                                                    |
| 2007-518814           | AF01758JP                 | Japan   | 05/30/2005  |            | DC-DC CONVERTER FOR PROGRAM-MOUNTED MEMORY DEVICE                                                            |
| 4672024               | AF01770                   | Japan   | 12/15/2005  | 01/18/2011 | A NON VOLATILE MEMORY DEVICE AND ITS CONTROL METHOD                                                          |
| 4731601               | AF01775JP                 | Japan   | 04/26/2006  | 04/28/2011 | RESISTIVE MEMORY DEVICE WITH IMPROVED DATA RETENTION AND REDUCED POWER                                       |
| 5313679               | AF01777JP                 | Japan   | 10/06/2006  | 07/12/2013 | METHOD FOR MANUFACTURING A SEMICONDUCTOR COMPONENT USING A SACRIFICIAL MASKING STRUCTURE                     |
| 2006-340280           | AF01780                   | Japan   | 12/18/2006  |            | PROGRAM ALGORITHM FOR MIRRORBIT                                                                              |
| 4980914               | AF01781JP                 | Japan   | 08/30/2005  | 04/27/2012 | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREOF                                                              |
| 4965443               | AF01783JP                 | Japan   | 06/30/2005  | 04/06/2012 | METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE                                                                |
| 2007-531988           | AF01784JP                 | Japan   | 08/25/2005  |            | STORAGE DEVICE, CONTROL METHOD OF STORAGE DEVICE, AND CONTROL METHOD OF STORAGE CONTROL DEVICE               |
| 4652409               | AF01785JP                 | Japan   | 08/25/2005  | 12/24/2010 | MEMORY DEVICE AND CONTROL METHOD OF MEMORY DEVICE                                                            |
| 4762986               | AF01789JP                 | Japan   | 06/30/2005  | 06/17/2011 | NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD OF NON-VOLATILE MEMORY DEVICE                                  |
| 2007-523257           | AF01792JP                 | Japan   | 06/28/2005  |            | SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF                                                          |
| 5657612               | AF01792JP DIV             | Japan   | 06/28/2005  | 12/05/2014 | SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF                                                          |
| 5069109               | AF01793JP                 | Japan   | 06/29/2005  | 08/24/2012 | SEMICONDUCTOR DEVICE AND PRODUCTION METHOD THEREFOR                                                          |
| 4922932               | AF01802JP                 | Japan   | 06/28/2005  | 02/10/2012 | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREOF                                                              |
| 4950049               | AF01803JP                 | Japan   | 07/25/2005  | 03/16/2012 | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREOF                                                              |
| 2007-539725           | AF01812JP                 | Japan   | 09/30/2005  |            | FABRICATION METHOD OF SEMICONDUCTOR DEVICE                                                                   |
| 2007-526761           | AF01813                   | Japan   | 07/24/2006  |            | MULTI-LEVEL MEMORY CELL ON SOI SUBSTRATE                                                                     |
| 4965445               | AF01818JP                 | Japan   | 07/27/2005  | 04/06/2012 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING SAME                                                       |
| 4792034               | AF01819JP                 | Japan   | 08/08/2005  | 07/29/2011 | FVREF circuit                                                                                                |
| 5123664               | AF01829JP                 | Japan   | 09/28/2005  | 11/02/2012 | PACKAGE USING AC INTERPOSERS                                                                                 |
| 4871280               | AF01833JP                 | Japan   | 08/30/2005  | 11/25/2011 | IMPROVED CoP and PiP                                                                                         |
| 2006-279418           | AF01836                   | Japan   | 10/13/2006  |            | NORNAND                                                                                                      |
| 2006-353410           | AF01839JP                 | Japan   | 12/27/2006  |            | STRUCTURE AND PROGRAMMING/ERASING OPERATIONS OF MIRROR BIT MEMORY DEVICE HAVING THE SHORTENED CHANNEL LENGTH |
| 2007-539754           | AF01840JP                 | Japan   | 10/04/2005  |            | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREFOR                                                             |
| 5379366               | AF01843JP                 | Japan   | 09/20/2007  | 10/04/2013 | SONOS DEVICE WITH INSULATING STORAGE LAYER AND P-N JUNCTION ISOLATION, AND THE FABRICATION METHOD THEREOF    |
| 521484/2008           | AF01852JP                 | Japan   | 07/07/2006  |            | INTEGRATED CIRCUIT TEST SOCKET                                                                               |
| 537735/2008           | AF01853JP                 | Japan   | 10/06/2006  |            | MEMORY ARRAY ARRANGED IN BANKS AND SECTORS AND ASSOCIATED DECODERS                                           |
| 2008-513037           | AF01854JP                 | Japan   | 04/28/2006  |            | SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD                                                                  |
| 2006-340294           | AF01860JP                 | Japan   | 12/18/2006  |            | LOW POWER CONSUMPTION AND HIGH-SPEED CASCODE CIRCUIT AND ITS SYSTEM                                          |
| 5015008               | AF01862JP                 | Japan   | 12/15/2005  | 06/15/2012 | SEMICONDUCTOR DEVICE AND ITS CONTROL METHOD                                                                  |

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| 2006-353415           | AF01869                   | Japan   | 12/27/2006  |            | CONVEX SHAPED THIN-FILM-TRANSISTOR DEVICE                                                              |
| 4918498               | AF01870JP                 | Japan   | 12/08/2005  | 02/03/2012 | SEMICONDUCTOR MANUFACTURING DEVICE, ITS CONTROLLING SYSTEM AND ITS CONTROLLING METHOD                  |
| 2006-353413           | AF01872                   | Japan   | 12/27/2006  |            | PoP HAVING HEAT RELEASE STRUCTURE                                                                      |
| 2006-353414           | AF01873                   | Japan   | 12/27/2006  |            | SEMICONDUCTOR DEVICE HAVING A PREVENTIVE CIRCUIT FOR PLASMA DAMAGE                                     |
| 2006-353416           | AF01879JP                 | Japan   | 12/27/2006  |            | MIRRORBIT DEVICE WITHOUT NITRIDE LAYER BETWEEN THE WORDLINE                                            |
| 2007-118845           | AF01882JP                 | Japan   | 04/27/2007  |            | COLUMN LEAK EFFECTIVELY CONTROLLED FOR 3D MEMORY                                                       |
| 2007-533144           | AF01884                   | Japan   | 07/31/2006  |            | MULTI-BIT DEVICE HAVING A BURIED BIT LINE AND A BURIED WORDLINE                                        |
| 2006-355027           | AF01887                   | Japan   | 12/28/2006  |            | THE IMPROVEMENT PROCESS USING SION LAYER                                                               |
| 2006-340143           | AF01889JP                 | Japan   | 12/18/2006  |            | THE METHOD OF STORING A PASSWORD DATA AND ADDRESS CHANGE FOR READ                                      |
| 2006-355025           | AF01890JP                 | Japan   | 12/28/2006  |            | THIN PoP                                                                                               |
| 2006-353411           | AF01891                   | Japan   | 12/27/2006  |            | THIN PiP                                                                                               |
| 4288376               | AF01894JP                 | Japan   | 04/24/2007  | 04/10/2009 | SERIAL CONNNECTED MIM+TFT TYPE FOR 3D MEMORY                                                           |
| 5036563               | AF01895JP                 | Japan   | 01/17/2006  | 07/13/2012 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING SAME                                                 |
| 2006-355023           | AF01897                   | Japan   | 12/24/2007  | 03/01/2012 | ADDRESS/DATA MUX.X32 DEVICE USING 2-CHIPS                                                              |
| 2006-353412           | AF01898                   | Japan   | 12/27/2006  |            | PoP USING STUD BUMP                                                                                    |
| 2007-025336           | AF01903                   | Japan   | 02/05/2007  |            | THREE-D TFT SONOS DEVICE                                                                               |
| 2006-355026           | AF01906                   | Japan   | 12/28/2006  |            | IMPROVED U-SHAPED SONOS DEVICE                                                                         |
| 2009-505396           | AF01907JP                 | Japan   | 04/05/2007  |            | MULTI MEDIA CARD WITH HIGH STORAGE CAPACITY                                                            |
| 4934053               | AF01908JP                 | Japan   | 12/09/2005  | 02/24/2012 | SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD                                                      |
| 4804479               | AF01949JP                 | Japan   | 12/13/2005  | 08/19/2011 | WRITE/READ LATCH FOR ORNAND                                                                            |
| 5192825               | AF01953JP                 | Japan   | 01/17/2006  | 02/08/2013 | LOWER PACKAGE WITH DIMPLES IN THE RESIN FOR PoP                                                        |
| 5348785               | AF01954JP                 | Japan   | 04/27/2006  | 08/30/2013 | MEMORY CELL ARRAY WITH LOW RESISTANCE COMMON SOURCE AND HIGH CURRENT DRIVABILITY                       |
| 5331683               | AF02071JP                 | Japan   | 05/21/2007  | 08/02/2013 | THE MEMORY SYSTEM WITH SWITCH ELEMENT                                                                  |
| 5705247               | AF02071JP DIV             | Japan   | 05/21/2007  | 03/06/2015 | MEMORY SYSTEM WITH SWITCH ELEMENT                                                                      |
| 2006-355024           | AF02075                   | Japan   | 12/28/2006  |            | IMPROVED FABRICATION METHOD OF STI FORMATION                                                           |
| 2007-025337           | AF02076                   | Japan   | 02/05/2007  |            | REFERENCE CIRCUIT HAVING A CALIBRATION CELL                                                            |
| 5301123               | AF02077JP                 | Japan   | 07/25/2007  | 06/28/2013 | SEMICONDUCTOR APPARATUS AND ITS MANUFACTURING METHOD                                                   |
| 2007-025334           | AF02078                   | Japan   | 02/05/2007  |            | IMPROVEMENT OF HIGH DENSITY PLASMA CVD MACHINE FROM NOVELLUS                                           |
| 2007-048693           | AF02080                   | Japan   | 02/28/2007  |            | WAFER LEVEL CSP WITH FRAME                                                                             |
| 2007-025335           | AF02081                   | Japan   | 02/05/2007  |            | UMEM DEVICE HAVING THE POCKET IMPLANTATION REGION                                                      |
| 5243237               | AF02083JP                 | Japan   | 02/28/2006  | 04/12/2013 | SEMICONDUCTOR DEVICE AND PROCESS FOR PRODUCING THE SAME                                                |
| 5313474               | AF02084JP                 | Japan   | 09/28/2007  | 07/12/2013 | METAL VOID MONITOR IN DAMASCENE PROCESS                                                                |
| 5443676               | AF02085JP                 | Japan   | 08/17/2007  | 12/27/2013 | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR                                                 |
| 2007-022714           | AF02086                   | Japan   | 02/01/2007  |            | THE CHARGE PUMP STYLE THAT SUPPLY VOLTAGE BAND IS WIDE AND SEMICONDUCTOR DEVICE BASED ON THEM.         |
| 5400279               | AF02087JP                 | Japan   | 06/07/2007  | 11/01/2013 | PROGRAMMING METHOD THEREOF, AND SEMICONDUCTOR MANUFACTURING DEVICE                                     |
| 2007-214096           | AF02093JP                 | Japan   | 08/20/2007  |            | FABRICATION METHOD OF SILICIDED SURFACE                                                                |
| 2007-023913           | AF02096                   | Japan   | 02/01/2007  |            | FLIP-CHIP PACKAGE COVERED WITH TAPE                                                                    |
| 2007-034742           | AF02097JP                 | Japan   | 02/15/2007  |            | DEVICE BUILT-IN SUBSTRATE BY USING VDM                                                                 |
| 2007-067151           | AF02102JP                 | Japan   | 03/15/2007  |            | METHOD OF SEPARATION OF ONO FILMS OVER CHANNEL REGION BY PLASMA OXIDATION PROCESSING                   |
| 2007-213001           | AF02103JP                 | Japan   | 08/17/2007  |            | FABRICATING METHOD OF SONOS FLASH MEMORY                                                               |
| 2009-504313           | AF02136JP                 | Japan   | 04/05/2007  |            | REDUCTION OF LEAKAGE CURRENT AND PROGRAM DISTURBS IN FLASH MEMORY DEVICES                              |
| 2009-504339           | AF02137JP                 | Japan   | 04/05/2007  |            | METHODS FOR ERASING AND PROGRAMMING MEMORY DEVICES                                                     |
| 2009-504316           | AF02138JP                 | Japan   | 04/05/2007  |            | METHODS FOR ERASING MEMORY DEVICES AND MULTI-LEVEL PROGRAMMING MEMORY DEVICE                           |
| 2009-504320           | AF02146JP                 | Japan   | 04/05/2007  |            | FLASH MEMORY PROGRAMMING AND VERIFICATION WIHT REDUCED LEAKAGE CURRENT                                 |
| 5280027               | AF02148JP                 | Japan   | 09/18/2007  | 05/31/2013 | SEMICONDUCTOR DEVICE AND ITS CONTROLLING METHOD                                                        |
| 2007-158750           | AF02150JP                 | Japan   | 06/15/2007  |            | ECC COMMAND                                                                                            |
| 4696227               | AF02153JP                 | Japan   | 12/28/2007  | 03/11/2011 | FLIP CHIP PACKAGE WITH STEP                                                                            |
| 5144964               | AF02155JP                 | Japan   | 06/05/2007  | 11/30/2012 | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF                                                  |
| 5508505               | AF02155JP DIV             | Japan   | 06/05/2007  | 03/28/2014 | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF                                                  |
| 2007-333154           | AF02156JP                 | Japan   | 12/25/2007  |            | METHOD OF INHIBITING FRINGE CURRENT IN MIRROR BITMEMORY DEVICE                                         |
| 5367235               | AF02159JP                 | Japan   | 06/07/2007  | 09/20/2013 | THE IMPROVEMENT OF THE HARD MASK PROCESS                                                               |
| 2007-149794           | AF02161JP                 | Japan   | 06/05/2007  |            | SEMICONDUCTOR DEVICE HAVING UV-BLOCKING LAYER CONTAINING GRANULAR MATERIAL WITH HIGH EXTINCTION EFFECT |
| 5260901               | AF02162JP                 | Japan   | 07/02/2007  | 05/02/2013 | SEMICONDUCTOR DEVICE AND ITS CONTROL METHOD                                                            |
| 5276824               | AF02170JP                 | Japan   | 10/17/2007  | 05/24/2013 | METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE                                                           |
| 3783240               | AF02171JP                 | Japan   | 09/19/1994  | 03/24/2006 | MANUFACTURING OF FLASH MEMORY                                                                          |
| 3780057               | AF02172JP                 | Japan   | 03/19/1997  | 03/10/2006 | SEMICONDUCTOR DEVICE AND MANUFACTURING                                                                 |
| 3442596               | AF02173JP                 | Japan   | 11/28/1996  | 06/20/2003 | MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE                                                           |
| H9-184773             | AF02174JP                 | Japan   | 07/10/1997  |            | NONVOLATILE SEMICONDUCTOR DEVICE AND                                                                   |
| 3892994               | AF02175JP                 | Japan   | 07/23/1999  | 12/15/2006 | NONVOLATILE MEMORY ALLOW ENCRYPTED                                                                     |
| 3430084               | AF02176JP                 | Japan   | 10/22/1999  | 05/16/2003 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                |
| 3912937               | AF02177JP                 | Japan   | 08/10/1999  | 02/09/2007 | MULTI-LEVEL NONVOLATILE MEMORY USING                                                                   |
| 4697993               | AF02178JP                 | Japan   | 11/25/1999  | 03/11/2011 | MANUFACTURING METHOD OF NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE                                       |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                |
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| 3762584               | AF02179JP                 | Japan   | 09/20/1999  | 01/20/2006 | SEMICONDUCTOR DEVICE AND MANUFACTURING                                                               |
| 3958899               | AF02180JP                 | Japan   | 09/03/1999  | 05/18/2007 | SEMICONDUCTOR MEMORY DEVICE AND                                                                      |
| 4623782               | AF02181JP                 | Japan   | 10/15/1999  | 11/12/2010 | SEMICONDUCTOR MEMORY AND USAGE METHOD THEREFOR                                                       |
| 3829161               | AF02182JP                 | Japan   | 10/14/1999  | 07/21/2006 | NONVOLATILE MEMORY CIRCUIT STORAGE MULTI-                                                            |
| 2001-560823           | AF02183JP                 | Japan   | 02/16/2000  |            | NONVOLATILE MEMORY                                                                                   |
| 4837230               | AF02184JP                 | Japan   | 07/17/2000  | 10/07/2011 | NONVOLATILE MEMORY DEVICE AND                                                                        |
| 4579493               | AF02185JP                 | Japan   | 08/03/2000  | 09/03/2010 | NONVOLATILE SEMICONDUCTOR MEMORY AND METHOD OF<br>READING DATA                                       |
| 2002-505627           | AF02186                   | Japan   | 06/29/2000  |            | SEMICONDUCTOR OR MEMORY DEVICE                                                                       |
| 4907758               | AF02187JP                 | Japan   | 09/12/2000  | 01/20/2012 | SEMICONDUCTOR STORAGE DEVICE AND ITS CONTROL METHOD                                                  |
| 2002-551860           | AF02188JP                 | Japan   | 12/21/2000  |            | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                              |
| 4730999               | AF02189JP                 | Japan   | 08/14/2000  | 04/28/2011 | MANUFACTURING METHOD OF NONVOLATILE                                                                  |
| 2001-123180           | AF02190JP                 | Japan   | 04/20/2001  |            | NONVOLATILE SEMICONDUCTOR MEMORY                                                                     |
| 4051175               | AF02191JP                 | Japan   | 11/17/2000  | 12/07/2007 | NONVOLATILE SEMICONDUCTOR DEVICE AND                                                                 |
| 3930256               | AF02192JP                 | Japan   | 02/07/2001  | 03/16/2007 | SEMICONDUCTOR MEMORY AND MANUFACTURING                                                               |
| 4674042               | AF02193JP                 | Japan   | 05/25/2001  | 01/28/2011 | NONVOLATILE SEMICONDUCTOR STORAGE DEVICE                                                             |
| 4142354               | AF02194JP                 | Japan   | 06/18/2002  | 06/20/2008 | READ METHOD FOR DUAL BIT MEMORY CELL                                                                 |
| 4152598               | AF02195JP                 | Japan   | 03/16/2001  | 07/11/2008 | SEMICONDUCTOR DEVICE AND MANUFACTURING                                                               |
| 2003-114392           | AF02196                   | Japan   | 04/18/2003  |            | PROGRAMMING METHOD FOR THRESHOLD                                                                     |
| 2007-109895           | AF02196JP DIV             | Japan   | 04/18/2007  |            | PROGRAMMING METHOD FOR THRESHOLD                                                                     |
| 5285674               | AF02196JP DIV2            | Japan   | 04/18/2003  | 06/07/2013 | SEMICONDUCTOR STORAGE DEVICE AND CONTROL METHOD<br>THEREOF                                           |
| 2010-213936           | AF02196JP DIV3            | Japan   | 04/18/2003  |            | PROGRAMMING METHOD FOR THRESHOLD                                                                     |
| 3930454               | AF02197JP                 | Japan   | 05/09/2003  | 03/16/2007 | READ METHOD FOR TWO BIT MEMORY CELL A                                                                |
| 2001-94582            | AF02198                   | Japan   | 03/29/2001  |            | SEMICONDUCTOR MEMORY DEVICE AND DRIVING                                                              |
| 3980874               | AF02199JP                 | Japan   | 11/30/2001  | 07/06/2007 | SEMICONDUCTOR MEMORY DEVICE AND DRIVING                                                              |
| 4437519               | AF02200JP                 | Japan   | 08/23/2001  | 01/15/2010 | MEMORY CONTROLLER FOR MULTI LEVEL                                                                    |
| 2002-012985           | AF02201JP                 | Japan   | 01/22/2002  |            | NONVOLATILE SEMICONDUCTOR MEMORY WITH A FUNCTION FOR<br>PREVENTING UNAUTHORIZED READING              |
| 2002-45116            | AF02202                   | Japan   | 02/21/2002  |            | METHOD OF MISSING READ DETECT AND CORRECT OF                                                         |
| 4138291               | AF02203JP                 | Japan   | 10/19/2001  | 06/13/2008 | NONVOLATILE SEMICONDUCTOR MEMORY AND                                                                 |
| 2003-51449            | AF02204JP                 | Japan   | 02/27/2003  |            | SETTING SYSTEM FOR THRESHOLD VOLTAGE OF                                                              |
| 3901570               | AF02205                   | Japan   | 04/23/2002  | 01/12/2007 | EQUIPMENT FOR LOW TEMPERATURE                                                                        |
| 4274870               | AF02206JP                 | Japan   | 07/14/2003  | 03/13/2009 | SYSTEM USING DYNAMIC REFERENCE BY                                                                    |
| 4017177               | AF02207JP                 | Japan   | 02/28/2001  | 09/28/2007 | MEMORY DEVICE                                                                                        |
| 2007-166979           | AF02207JP DIV             | Japan   | 06/25/2007  |            | MEMORY DEVICE                                                                                        |
| 2011-047578           | AF02207JP DIV2            | Japan   | 02/28/2001  |            | MEMORY DEVICE                                                                                        |
| 2002-114145           | AF02208JP                 | Japan   | 04/17/2002  |            | NONVOLATILE SEMICONDUCTOR MEMORY AND                                                                 |
| 3796457               | AF02209JP                 | Japan   | 02/28/2002  | 04/21/2006 | NONVOLATILE SEMICONDUCTOR DEVICE                                                                     |
| 2002-135688           | AF02210JP                 | Japan   | 05/10/2002  |            | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                              |
| 4105976               | AF02211JP                 | Japan   | 04/25/2003  | 04/04/2008 | CONTROL SYSTEM FOR PRECHARGE LEVEL ON                                                                |
| 3967193               | AF02212JP                 | Japan   | 05/21/2002  | 06/08/2007 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                              |
| 4030839               | AF02213JP                 | Japan   | 08/30/2002  | 10/26/2007 | MEMORY INTEGRATED CIRCUIT DEVICE                                                                     |
| 2002-80554            | AF02214JP                 | Japan   | 03/22/2002  |            | SEMICONDUCTOR MEMORY DEVICE                                                                          |
| 4607166               | AF02214JP DIV             | Japan   | 11/23/2007  | 10/15/2010 | SEMICONDUCTOR MEMORY DEVICE                                                                          |
| 2002-234463           | AF02215                   | Japan   | 08/12/2002  |            | NONVOLATILE MEMORY HAVING TRAN LAYER                                                                 |
| 3943526               | AF02216JP                 | Japan   | 06/04/2003  | 04/13/2007 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                     |
| 4067908               | AF02217JP                 | Japan   | 08/08/2002  | 01/18/2008 | SEMICONDUCTOR MEMORY DEVICE THE                                                                      |
| 2003-380841           | AF02218JP                 | Japan   | 11/11/2002  |            | NONVOLATILE SEMICONDUCTOR MEMORY                                                                     |
| 4175852               | AF02219JP                 | Japan   | 09/13/2002  | 08/29/2008 | SEMICONDUCTOR MEMORY FOR FUNCTION WELL                                                               |
| 2002-268315           | AF02220JP                 | Japan   | 09/13/2002  |            | NONVOLATILE SEMICONDUCTOR MEMORY                                                                     |
| 2002-265065           | AF02221JP                 | Japan   | 09/11/2002  |            | MEMORY CIRCUIT HAVING                                                                                |
| 4163473               | AF02222JP                 | Japan   | 09/13/2002  | 08/01/2008 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                     |
| 3987856               | AF02223JP                 | Japan   | 02/24/2003  | 07/20/2007 | VOLTAGE DETECTION CIRCUIT, SEMICONDUCTOR DEVICE, METHOD<br>FOR CONTROLLING VOLTAGE DETECTION CIRCUIT |
| 2004-568463           | AF02224JP                 | Japan   | 02/18/2003  |            | SEMICONDUCTOR MEMORY DEVICE AND DATA RESD                                                            |
| 2003-27514            | AF02225JP                 | Japan   | 02/04/2003  |            | SEMICONDUCTOR MEMORY DEVICE AND                                                                      |
| 4101809               | AF02226JP                 | Japan   | 02/27/2003  | 03/28/2008 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                     |
| 3831758               | AF02227JP                 | Japan   | 02/17/2003  | 07/28/2006 | VOLTAGE BOOSTER CIRCUIT USING SMALL                                                                  |
| 3857241               | AF02228JP                 | Japan   | 02/17/2003  | 09/22/2006 | CHARGE PUMP CIRCUIT REDUCE A SWING LEVEL OF                                                          |
| 4017178               | AF02229JP                 | Japan   | 02/28/2003  | 09/28/2007 | FLASH MEMORY AND MEMORY CONTROL                                                                      |
| 2002-370274           | AF02230JP                 | Japan   | 12/20/2002  |            | SEMICONDUCTOR DEVICE AND TEST METHOD                                                                 |
| 2004-571303           | AF02231                   | Japan   | 04/30/2003  |            | FLASH MEMORY WITH SPARE SECTOR QUICKEN                                                               |
| 2004-569330           | AF02232JP                 | Japan   | 03/11/2003  |            | MEMORY DEVICE                                                                                        |
| 3914869               | AF02233JP                 | Japan   | 12/20/2002  | 02/09/2007 | NONVOLATILE MEMORY AND METHOD FOR                                                                    |
| 4005909               | AF02234JP                 | Japan   | 12/26/2002  | 08/31/2007 | SEMICONDUCTOR MEMORY DEVICE AND CONTROL                                                              |
| 4175881               | AF02235JP                 | Japan   | 12/25/2002  | 08/29/2008 | METHOD FOR STORING IN NONVOLATILE MEMORY AND STORAGE<br>UNIT                                         |
| 2003-50264            | AF02236JP                 | Japan   | 02/27/2003  |            | SEMICONDUCTOR MEMORY DEVICE                                                                          |
| 2008-108127           | AF02236JP DIV             | Japan   | 04/17/2008  |            | SEMICONDUCTOR MEMORY DEVICE                                                                          |
| 4104151               | AF02237JP                 | Japan   | 04/28/2003  | 04/04/2008 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                              |
| 4002275               | AF02238JP                 | Japan   | 04/24/2003  | 08/24/2007 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                     |
| 4698638               | AF02238JP DIV             | Japan   | 06/04/2007  | 03/11/2011 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                     |
| 5318054               | AF02238JP DIV2            | Japan   | 04/24/2003  | 07/19/2013 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                     |
| 4010513               | AF02239JP                 | Japan   | 04/17/2003  | 09/14/2007 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                     |
| 4177167               | AF02240JP                 | Japan   | 05/14/2003  | 08/29/2008 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                              |
| 4060330               | AF02241JP                 | Japan   | 06/06/2003  | 12/28/2007 | SEMICONDUCTOR MEMORY DEVICE AND SELECT                                                               |
| 06811935.3            | AF02243JP                 | Japan   | 10/18/2006  |            | A VOLTAGE DETECTOR CIRCUIT                                                                           |
| 5601751               | AF02253JP                 | Japan   | 04/26/2007  | 08/29/2014 | SEMICONDUCTOR DEVICE, AND MANUFACTURING METHOD THEREOF                                               |
| 5411981               | AF02253JP DIV             | Japan   | 04/26/2007  | 11/15/2013 | MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE                                                         |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                             |
|-----------------------|---------------------------|---------|-------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2007-194277           | AF02254JP                 | Japan   | 07/26/2007  |            | HIGH-SPEED NONVOLATILE MEMORY COMPRISING SIMULTANEOUS OPERATION FUNCTION (AS FOR IT, PROGRAM/ERASE-POWER LINE COMPRISING NOISE SOURCE AND SENSITIVE READ-POWER LINE SEPARATED IN) |
| 5281770               | AF02256JP                 | Japan   | 08/17/2007  | 05/31/2013 | MIRROR BIT MEMEORY DEVICE APPLYING A GATE VOLTAGE ALTERNATELY TO GATE                                                                                                             |
| 5486152               | AF02257JP                 | Japan   | 07/30/2007  | 02/28/2014 | SEMICONDUCTOR DEVICE AND THE METHOD OF FABRICATING THE SAME                                                                                                                       |
| 2007-023570           | AF02259                   | Japan   | 02/01/2007  |            | PROGRAM/ERASE DISABLING CONTROL OF WPCAM BY DOUBLE CONTROLS                                                                                                                       |
| 2007-097578           | AF02261                   | Japan   | 04/03/2007  |            | BOOST DRIVE METHOD FOR PASS-GATE-TRANSISTOR CONTROLLED BY AN ADDRESS DECODER                                                                                                      |
| 2007-214097           | AF02262JP                 | Japan   | 08/20/2007  |            | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME                                                                                                                        |
| 2013-257563           | AF02262JP DIV             | Japan   | 08/20/2007  |            | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME                                                                                                                        |
| 2007-123298           | AF02263JP                 | Japan   | 05/08/2007  |            | SEMICONDUCTOR DEVICE AND ITS MANUFACTURING PROCESS                                                                                                                                |
| 5037241               | AF02266JP                 | Japan   | 07/04/2007  | 07/13/2012 | METHOD AND APPARATUS FOR MANUFACTURING SEMICONDUCTOR APPARATUS                                                                                                                    |
| 5425378               | AF02274JP                 | Japan   | 07/30/2007  | 12/06/2013 | FABRICATING METHOD OF SPLIT NITRIDE OF SONOS DEVICE                                                                                                                               |
| 2007-057828           | AF02287JP                 | Japan   | 03/07/2007  |            | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD                                                                                                                                     |
| 2007-070016           | AF02288JP                 | Japan   | 03/19/2007  |            | THIN COC PACKAGE                                                                                                                                                                  |
| 5388422               | AF02289JP                 | Japan   | 05/11/2007  | 10/18/2013 | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD                                                                                                                                     |
| 5350604               | AF02291JP                 | Japan   | 05/16/2007  | 08/30/2013 | SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD                                                                                                                                 |
| 2007-098763           | AF02293JP                 | Japan   | 04/04/2007  |            | LOW COST TROUGH HOLE PACKAGE                                                                                                                                                      |
| 5300248               | AF02298JP                 | Japan   | 11/20/2007  | 06/28/2013 | SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD                                                                                                                                 |
| 2007-290103           | AF02310JP                 | Japan   | 11/07/2007  |            | NON-VOLATILE SWITCHING DEVICE                                                                                                                                                     |
| 2014-233157           | AF02310JP DIV             | Japan   | 11/07/2007  |            | VARIABLE RESISTOR FOR NONVOLATILE MEMORY AND ITS MANUFACTURING METHOD, AND NONVOLATILE MEMORY                                                                                     |
| 2007-136396           | AF02312JP                 | Japan   | 05/23/2007  |            | FLASH MEMORY ENABLED OVER-PROGRAMMING OF SPARE MEMORY REGION                                                                                                                      |
| 4588060               | AF02313JP                 | Japan   | 09/19/2007  | 09/17/2010 | THIN LEAD FLAME PACKAGE                                                                                                                                                           |
| 5341337               | AF02314JP                 | Japan   | 10/25/2007  | 08/16/2013 | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR                                                                                                                            |
| 2007-055322           | AF02315JP                 | Japan   | 03/06/2007  |            | ERASURE SUSPENSION FEATURE                                                                                                                                                        |
| 5273956               | AF02316JP                 | Japan   | 07/02/2007  | 08/28/2013 | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD                                                                                                                                     |
| 2013-042131           | AF02316JP DIV             | Japan   | 07/02/2007  |            | SEMICONDUCTOR DEVICE AND MANUFACTURING THE SAME                                                                                                                                   |
| 4550102               | AF02320JP                 | Japan   | 10/25/2007  | 07/16/2010 | ONE CHIP TESTABLE FBGA FOR POP OR MCP                                                                                                                                             |
| 2007-238877           | AF02326JP                 | Japan   | 09/14/2007  |            | THE JUNCTION STRUCTURE OF STACKING PACKAGES ON THE WAFER                                                                                                                          |
| 5358077               | AF02340JP                 | Japan   | 09/28/2007  | 09/06/2013 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME                                                                                                                         |
| 5058714               | AF02455JP                 | Japan   | 08/21/2007  | 08/10/2012 | SEMICONDUCTOR DEVICE, AND ITS MANUFACTURING METHOD                                                                                                                                |
| 4937856               | AF02457JP                 | Japan   | 08/03/2007  | 03/02/2012 | SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD                                                                                                                                 |
| 5681761               | AF02460JP                 | Japan   | 12/20/2007  | 01/16/2015 | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF                                                                                                                             |
| 5319107               | AF02460US DIV             | Japan   | 12/20/2007  | 07/19/2013 | FABRICATING METHOD OF U-SHAPED NAND TYPE MEMORY DEVICE                                                                                                                            |
| 5352084               | AF02463JP                 | Japan   | 12/20/2007  | 08/30/2013 | MEMORY DEVICE HAVING LARGE POSITIONAL DEVIATION MARGIN OF BIT LINE CONTACT                                                                                                        |
| 4547490               | AF02464JP                 | Japan   | 11/02/2007  | 07/16/2010 | LENS REGULATION MECHANISM                                                                                                                                                         |
| 2007-187763           | AF02465JP                 | Japan   | 07/19/2007  |            | TERMINATE CYCLE FOR BURST WRITE OPERATION                                                                                                                                         |
| 2007-328337           | AF02466JP                 | Japan   | 12/20/2007  |            | TIME REDUCTION OF ADDRESS SETUP_HOLD TIME FOR SEMICONDUCTOR MEMORY                                                                                                                |
| 4635173               | AF02468JP                 | Japan   | 04/25/2008  | 12/03/2010 | A RESET CIRCUIT OF DATA RAM DIVIDED TO A SECTOR UNIT AND ITS METHOD                                                                                                               |
| 2008-027335           | AF02469JP                 | Japan   | 02/07/2008  |            | OUTPUT BUFFER CIRCUIT                                                                                                                                                             |
| 5566003               | AF02488JP                 | Japan   | 11/08/2007  | 06/27/2014 | A SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD                                                                                                                               |
| 5105417               | AF02535JP                 | Japan   | 11/20/2007  | 10/12/2012 | SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD                                                                                                                                 |
| 2007-273655           | AF02536JP                 | Japan   | 10/22/2007  |            | SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD                                                                                                                                 |
| 5621021               | AF02536JP DIV2            | Japan   | 10/22/2007  | 09/26/2014 | SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD THEREOF                                                                                                                         |
| 2007-154630           | AF02539JP                 | Japan   | 06/12/2007  |            | A WRITE COMMAND ENTRY METHOD OF SYNC. NVROM WHICH IS INTERFACE COMMAND ARCHITECTURE FOR SYNCHRONOUS FLASH MEMORY                                                                  |
| 5133147               | AF02540JP                 | Japan   | 06/24/2008  | 11/16/2012 | RECOGNITION DEVICE, RECOGNITION METHOD AND COMPUTER PROGRAM                                                                                                                       |
| 2007-154452           | AF02541                   | Japan   | 06/11/2007  |            | NEW FUNCTION OF "A NONVOLATILE MEMORY CONNECTED TO SDRAM CONTROLLER"                                                                                                              |
| 5405737               | AF02545JP                 | Japan   | 12/20/2007  | 11/08/2013 | SPLITTING METHOD OF ONO FILM IN U-SHAPED MEMORY                                                                                                                                   |
| 5308112               | AF02552JP                 | Japan   | 09/22/2008  | 07/05/2013 | SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME                                                                                                                           |
| 5098085               | AF02554JP                 | Japan   | 12/18/2007  | 10/05/2012 | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF                                                                                                                             |
| 2008-008456           | AF02555JP                 | Japan   | 01/17/2008  |            | FABRICATING METHOD OF REDUCING THE CONTACT RESISTANCE BY REMOVING THE DAMAGED REGION IN THE BIT LINE CONTACT                                                                      |
| 2014-065111           | AF02555JP DIV             | Japan   | 01/17/2008  |            | METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE                                                                                                                                      |
| 2007-318745           | AF02556JP                 | Japan   | 12/10/2007  |            | MANUFACTURING METHOD FOR ONE SIDE MOLDING PACKAGE                                                                                                                                 |
| 2013-231805           | AF02556JP DIV             | Japan   | 12/10/2007  |            | METHOD OF MANUFACTURING SEMICONDUCTOR APPARATUS                                                                                                                                   |
| 5301126               | AF02557JP                 | Japan   | 08/21/2007  | 06/28/2013 | SEMICONDUCTOR DEVICE AND ITS PRODUCTION PROCESS                                                                                                                                   |
| 5302522               | AF02559JP                 | Japan   | 08/10/2007  | 06/28/2013 | SEMICONDUCTOR DEVICE, AND MANUFACTURING METHOD THEREOF                                                                                                                            |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                               |
|-----------------------|---------------------------|---------|-------------|------------|-----------------------------------------------------------------------------------------------------|
| 5451971               | AF02582JP                 | Japan   | 11/09/2007  | 01/10/2014 | SEMICONDUCTOR DEVICE AND ITS CONTROL METHOD (AS AMENDED)                                            |
| 5057517               | AF02584JP                 | Japan   | 12/06/2007  | 08/10/2012 | SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME                                             |
| 5241148               | AF02585JP                 | Japan   | 06/08/2007  | 04/12/2013 | SEMICONDUCTOR DEVICE, AND CONTROL METHOD THEREOF                                                    |
| 5255234               | AF02586JP                 | Japan   | 05/29/2007  | 04/26/2013 | SEMICONDUCTOR DEVICE AND ITS CONTROL METHOD                                                         |
| 5072446               | AF02587JP                 | Japan   | 06/15/2007  | 08/31/2012 | SEMICONDUCTOR DEVICE AND ITS CONTROLLING METHOD                                                     |
| 5143655               | AF02596JP                 | Japan   | 07/22/2008  | 11/30/2012 | IMPROVEMENT OF CHARGE LOSS OF REDUCED FLOATING GATE TYPE NOR-FLASH MEMORY                           |
| 2007-300687           | AF02605JP                 | Japan   | 11/20/2007  |            | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD                                                       |
| 2639202               | AF02606                   | Japan   | 10/18/1990  | 04/25/1997 | MANUFACTURE OF SEMICONDUCTOR DEVICE                                                                 |
| 2720645               | AF02607                   | Japan   | 08/12/1991  | 11/21/1997 | MANUFACTURE OF SEMICONDUCTOR DEVICE                                                                 |
| 2900941               | AF02608                   | Japan   | 03/09/1989  | 03/19/1999 | SEMICONDUCTOR DEVICE                                                                                |
| 3409404               | AF02609JP                 | Japan   | 12/27/1993  | 03/20/2003 | FLASH MEMORY                                                                                        |
| 3414496               | AF02610JP                 | Japan   | 05/27/1994  | 04/04/2003 | SEMICONDUCTOR DEVICE                                                                                |
| 3414852               | AF02611JP                 | Japan   | 07/20/1994  | 04/04/2003 | SEMICONDUCTOR MEMORY                                                                                |
| 3418435               | AF02612                   | Japan   | 11/16/1993  | 04/11/2003 | CURRENT MIRROR TYPE OSCILLATOR CIRCUIT                                                              |
| 3444902               | AF02613JP                 | Japan   | 10/24/1991  | 06/27/2003 | TEST METHOD FOR SEMICONDUCTOR DEVICE                                                                |
| 3465416               | AF02614JP                 | Japan   | 06/22/1995  | 08/29/2003 | DATA OUTPUT CIRCUIT AND SEMICONDUCTOR MEMORY DEVICE                                                 |
| 3476479               | AF02615JP                 | Japan   | 09/19/1991  | 09/26/2003 | SEMICONDUCTOR MEMORY                                                                                |
| 3500564               | AF02616JP                 | Japan   | 12/19/1997  | 12/12/2003 | MANUFACTURE OF SEMICONDUCTOR DEVICE                                                                 |
| 3513056               | AF02617JP                 | Japan   | 09/20/1999  | 01/16/2004 | NONVOLATILE SEMICONDUCTOR STORAGE                                                                   |
| 3534815               | AF02618JP                 | Japan   | 03/18/1994  | 03/19/2004 | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                                                             |
| 3541427               | AF02619JP                 | Japan   | 05/27/1994  | 04/09/2004 | SEMICONDUCTOR MEMORY                                                                                |
| 3541503               | AF02620JP                 | Japan   | 07/10/1995  | 04/09/2004 | SEMICONDUCTOR MEMORY                                                                                |
| 3544222               | AF02621JP                 | Japan   | 03/18/1994  | 04/16/2004 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND DATA READING METHOD THEREOF                             |
| 3544731               | AF02622JP                 | Japan   | 01/11/1995  | 04/16/2004 | NONVOLATILE SEMICONDUCTOR STORAGE DEVICE                                                            |
| 3545010               | AF02623JP                 | Japan   | 06/23/1993  | 04/16/2004 | SEMICONDUCTOR STORAGE DEVICE                                                                        |
| 3558746               | AF02624JP                 | Japan   | 07/26/1995  | 05/28/2004 | METHOD AND EQUIPMENT FOR TESTING NONVOLATILE MEMORY                                                 |
| 3568265               | AF02625JP                 | Japan   | 02/20/1995  | 06/25/2004 | SEMICONDUCTOR MEMORY DEVICE                                                                         |
| 3573477               | AF02626JP                 | Japan   | 12/10/1993  | 07/09/2004 | ELECTRICALLY ERASABLE NON-VOLATILE SEMICONDUCTOR MEMORY                                             |
| 3578478               | AF02627JP                 | Japan   | 12/14/1993  | 07/23/2004 | NON-VOLTAGE SEMICONDUCTOR MEMORY                                                                    |
| 3599793               | AF02628JP                 | Japan   | 09/14/1994  | 09/24/2004 | SEMICONDUCTOR MEMORY DEVICE                                                                         |
| 3613312               | AF02629JP                 | Japan   | 08/06/1997  | 11/05/2004 | MANUFACTURE OF SEMICONDUCTOR DEVICE                                                                 |
| 3693181               | AF02630JP                 | Japan   | 10/25/1991  | 07/01/2005 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURE THEREOF                                     |
| 3728577               | AF02631JP                 | Japan   | 10/29/1998  | 10/14/2005 | MANUFACTURE OF SEMICONDUCTOR STORAGE DEVICE                                                         |
| 3881295               | AF02632JP                 | Japan   | 09/17/2002  | 11/17/2006 | NONVOLATILE SEMICONDUCTOR STORAGE DEVICE                                                            |
| 3882916               | AF02633JP                 | Japan   | 03/27/2003  | 11/24/2006 | CHARGING PUMP CIRCUIT                                                                               |
| 5421549               | AF02634JP                 | Japan   | 05/23/2008  | 11/29/2013 | METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE                               |
| 5308024               | AF02636JP                 | Japan   | 12/28/2007  | 07/05/2013 | SONOS-NAND DEVICE HAVING THE STORAGE REGION SEPARATED BETWEEN CELLS                                 |
| 5300291               | AF02642JP                 | Japan   | 03/13/2008  | 06/28/2013 | SEMICONDUCTOR SYSTEM AND ITS ACTIVATION METHOD                                                      |
| 4555956               | AF02646JP                 | Japan   | 01/09/2008  | 07/30/2010 | SYSTEM CONTROL METHOD OF MODE REGISTER SET OF DRAM IN MCP                                           |
| 4910117               | AF02647 JP                | Japan   | 04/04/2008  | 01/27/2012 | ORDER RELATION OF LOCATION MODEL IN MCP INCLUDING MB-DDR CHIP DIE AND DRAM CHIP DIE                 |
| 4765084               | AF02648JP                 | Japan   | 04/22/2008  | 06/24/2011 | THE DRAM CHIP DIE WHICH IT IS REFRESHED, AND IS CONTROLLED BY AN OPERATION RECOGNITION OF NV-MEMORY |
| 4002712               | AF02649JP                 | Japan   | 05/15/2000  | 08/24/2007 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                             |
| 2007-120247           | AF02649JP DIV             | Japan   | 04/27/2007  |            | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                             |
| 2003-104841           | AF02650JP                 | Japan   | 04/09/2003  |            | SEMICONDUCTOR MEMORY DEVICE                                                                         |
| 4005522               | AF02689JP                 | Japan   | 03/18/2003  | 08/31/2007 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                             |
| 2002-268643           | AF02692JP                 | Japan   | 09/13/2002  |            | NONVOLATILE MEMORY CIRCUIT                                                                          |
| 2007-148661           | AF02692JP DIV             | Japan   | 06/04/2007  |            | NONVOLATILE MEMORY CIRCUIT                                                                          |
| 5367256               | AF02767JP                 | Japan   | 12/17/2007  | 09/20/2013 | SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD                                                   |
| 5214208               | AF02770JP                 | Japan   | 10/01/2007  | 03/08/2013 | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREOF                                                     |
| 4698001               | AF02771JP                 | Japan   | 07/11/2000  | 03/11/2011 | SEMICONDUCTOR STORAGE DEVICE                                                                        |
| 2000-159102           | AF02772JP                 | Japan   | 05/29/2000  |            | SEMICONDUCTOR OR MEMORY DEVICE                                                                      |
| 4889889               | AF02773JP                 | Japan   | 08/30/2001  | 12/22/2011 | STATIC RANDOM ACCESS MEMORY WITH NO-VOLATILE DATA HOLDING FUNCTION AND ITS OPERATING METHOD         |
| 3963259               | AF02774JP                 | Japan   | 03/15/2002  | 06/01/2007 | SEMICONDUCTOR OR DEVICE                                                                             |
| 2002-319913           | AF02775JP                 | Japan   | 11/01/2002  |            | NONVOLATILE SEMICONDUCTOR OR DEVICE                                                                 |
| 4181363               | AF02776JP                 | Japan   | 08/29/2002  | 09/05/2008 | NONVOLATILE SEMICONDUCTOR OR MEMORY                                                                 |
| 4071572               | AF02777JP                 | Japan   | 08/12/2002  | 01/25/2008 | VOLTAGE CONTROL CIRCUIT                                                                             |
| 2002-319914           | AF02778                   | Japan   | 11/01/2002  |            | NONVOLATILE SEMICONDUCTOR OR MEMORY                                                                 |
| 2002-266995           | AF02779JP                 | Japan   | 09/12/2002  |            | SEMICONDUCTOR OR DEVICE                                                                             |
| 4197923               | AF02780JP                 | Japan   | 10/29/2002  | 10/10/2008 | SEMICONDUCTOR OR INTEGRATED                                                                         |
| 4667719               | AF02781JP                 | Japan   | 01/17/2003  | 01/21/2011 | NONVOLATILE MULTI-LEVEL SEMICONDUCTOR                                                               |
| 4073330               | AF02782JP                 | Japan   | 02/18/2003  | 02/01/2008 | NONVOLATILE SEMICONDUCTOR OR MEMORY                                                                 |
| 4271450               | AF02783JP                 | Japan   | 01/27/2003  | 03/06/2009 | SEMICONDUCTOR OR MEMORY DEVICE                                                                      |
| 4195266               | AF02784JP                 | Japan   | 09/13/2002  | 10/03/2008 | SEMICONDUCTOR MEMORY DEVICE                                                                         |
| 2002-268316           | AF02785JP                 | Japan   | 09/13/2002  |            | DESIGN METHOD FOR SEMICONDUCTOR                                                                     |
| 2002-267097           | AF02786JP                 | Japan   | 09/12/2002  |            | NONVOLATILE MEMORY WITH IMPROVED                                                                    |
| 2003-30977            | AF02787                   | Japan   | 02/07/2003  |            | NONVOLATILE SEMICONDUCTOR OR MEMORY                                                                 |
| 4875284               | AF02788JP                 | Japan   | 03/06/2003  | 12/02/2011 | SEMICONDUCTOR OR MEMORY DEVICE AND                                                                  |
| 2002-354049           | AF02789JP                 | Japan   | 12/05/2002  |            | NONVOLATILE SEMICONDUCTOR OR MEMORY                                                                 |
| 2002-370272           | AF02790JP                 | Japan   | 12/20/2002  |            | OPERATING METHOD FOR NONVOLATILE                                                                    |
| 2002-370273           | AF02791JP                 | Japan   | 12/20/2002  |            | CONTROL METHOD FOR SEMICONDUCTOR                                                                    |
| 2002-370275           | AF02792JP                 | Japan   | 12/20/2002  |            | SEMICONDUCTOR OR DEVICE SEMICONDUCTOR                                                               |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                       |
|-----------------------|---------------------------|---------|-------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3890014               | AF02793JP                 | Japan   | 12/20/2002  | 12/08/2006 | SEMICONDUCTOR MEMORY DEVICE AND                                                                                                                                             |
| 2005-500549           | AF02794JP                 | Japan   | 06/05/2003  |            | VIRTUAL GROUND NONVOLATILE                                                                                                                                                  |
| 4142685               | AF02795JP                 | Japan   | 06/05/2003  | 06/20/2008 | SEMICONDUCTOR OR MEMORY WITH                                                                                                                                                |
| 2002-348485           | AF02796                   | Japan   | 11/29/2002  |            | NONVOLATILE SEMICONDUCTOR OR MEMORY                                                                                                                                         |
| 2002-342677           | AF02797JP                 | Japan   | 11/26/2002  |            | SEMICONDUCTOR DEVICE AND TEST                                                                                                                                               |
| 4136646               | AF02798JP                 | Japan   | 12/20/2002  | 06/13/2008 | SEMICONDUCTOR OR MEMORY DEVICE AND                                                                                                                                          |
| 4067956               | AF02799JP                 | Japan   | 12/20/2002  | 01/18/2008 | CONTROL METHOD FOR NONVOLATILE                                                                                                                                              |
| 3999151               | AF02800JP                 | Japan   | 03/20/2003  | 08/17/2007 | SEMICONDUCTOR OR MEMORY DEVICE                                                                                                                                              |
| 4104133               | AF02801JP                 | Japan   | 05/09/2003  | 04/04/2008 | NONVOLATILE SEMICONDUCTOR OR DEVICE                                                                                                                                         |
| 4035573               | AF02802JP                 | Japan   | 12/20/2002  | 11/09/2007 | SEMICONDUCTOR OR MEMORY DEVICE AND                                                                                                                                          |
| 2002-230062           | AF02803JP                 | Japan   | 08/07/2002  |            | SEMICONDUCTOR OR MEMORY DEVICE AND                                                                                                                                          |
| 2005-096274           | AF02804JP                 | Japan   | 03/29/2005  |            | SEMICONDUCTOR DEVICE                                                                                                                                                        |
| H10-66888             | AF02805JP                 | Japan   | 03/17/1998  |            | MANUFACTURING METHOD OF                                                                                                                                                     |
| H10-66898             | AF02806JP                 | Japan   | 03/17/1998  |            | SEMICONDUCTOR OR DEVICE AND                                                                                                                                                 |
| H10-128682            | AF02807                   | Japan   | 05/12/1998  |            | MANUFACTURING METHOD OF                                                                                                                                                     |
| H10-345307            | AF02808                   | Japan   | 12/04/1998  |            | MANUFACTURING METHOD OF                                                                                                                                                     |
| H10-349028            | AF02809JP                 | Japan   | 12/08/1998  |            | SEMICONDUCTOR OR MEMORY DEVICE AND                                                                                                                                          |
| 2005-352897           | AF02810JP DIV             | Japan   | 12/07/2005  |            | PORTABLE ELECTRONIC EQUIPMENT USED WITH LID OPENED,<br>CONTROL METHOD OF ELECTRONIC EQUIPMENT, AND PROGRAM<br>INFORMATION RECORDING APPARATUS AND CONTROL METHOD<br>THEREOF |
| 2005-352898           | AF02811JP DIV             | Japan   | 12/07/2005  |            | STACKING TECHNOLOGY OF RERAM                                                                                                                                                |
| 5557419               | AF02812JP                 | Japan   | 10/17/2007  | 06/13/2014 | A SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD                                                                                                                         |
| 5319092               | AF02813JP                 | Japan   | 09/03/2007  | 07/19/2013 | The manufacturing method of a semiconductor device                                                                                                                          |
| 5313486               | AF02815JP                 | Japan   | 11/15/2007  | 07/12/2013 | SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD (AS<br>AMENDED)                                                                                                           |
| 5553960               | AF02822JP                 | Japan   | 10/25/2007  | 06/06/2014 | SEMICONDUCTOR DEVICE                                                                                                                                                        |
| 5395344               | AF02827JP                 | Japan   | 09/28/2007  | 10/25/2013 | MEMORY SYSTEM HAVING A SWITCHING ELEMENT                                                                                                                                    |
| 2013-046514           | AF02827JP DIV             | Japan   | 09/28/2007  |            | PROGRAMMING METHOD FOR MIM TYPE MEMORY                                                                                                                                      |
| 2008-123560           | AF02828JP                 | Japan   | 05/09/2008  |            | SEMICONDUCTOR DEVICE                                                                                                                                                        |
| 5435857               | AF02829JP                 | Japan   | 11/07/2007  | 12/20/2013 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE<br>SAME                                                                                                               |
| 5294611               | AF02830JP                 | Japan   | 11/14/2007  | 06/21/2013 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE<br>SAME                                                                                                               |
| 5686838               | AF02830JP DIV             | Japan   | 04/02/2013  | 01/30/2015 | MANUFACTURING METHOD FOR SEMICONDUCTOR DEVICE                                                                                                                               |
| 5264139               | AF02832JP                 | Japan   | 10/09/2007  | 05/10/2013 | ASYNCHRONOUS READ FUNCTION OF SYNCHRONOUS MB-DDR                                                                                                                            |
| 4759717               | AF02837JP                 | Japan   | 02/18/2008  | 06/17/2011 | MEMORY CONTROLLER                                                                                                                                                           |
| 5107776               | AF02838JP                 | Japan   | 04/07/2008  | 10/12/2012 | CONTROL METHOD OF GBL AND LBL IN A READ                                                                                                                                     |
| 2007-319147           | AF02839JP                 | Japan   | 12/11/2007  |            | MEMORY ARRAY STRUCTURE AND SENSE AMPLIFIER CIRCUIT AND<br>THE CONTROL METHOD FOR USE IN NONVOLATILE MEMORY                                                                  |
| 2008-167151           | AF02840JP                 | Japan   | 06/26/2008  |            | NONVOLATILE MEMORY AND METHOD OF READING DATA FROM<br>NONVOLATILE MEMORY (AS AMENDED)                                                                                       |
| 5289860               | AF02841JP                 | Japan   | 08/25/2008  | 06/14/2013 | METHOD AND VERIFY OF INTERNAL STEP-DOWN VOLTAGE CONTROL                                                                                                                     |
| 2008-178653           | AF02842JP                 | Japan   | 07/09/2008  |            | SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE<br>SAME                                                                                                                  |
| 2009-012221           | AF02843JP                 | Japan   | 01/22/2009  |            | SEMICONDUCTOR DEVICE, SEMICONDUCTOR SYSTEM                                                                                                                                  |
| 5161667               | AF02845JP                 | Japan   | 06/23/2008  | 12/21/2012 | SEMICONDUCTOR DEVICE AND DATA READ-OUT METHOD                                                                                                                               |
| 5314943               | AF02846JP                 | Japan   | 06/20/2008  | 07/12/2013 | THE ECC FUNCTION THAT IT IS EMBEDDED IN PROGRAM / ERASE -1-                                                                                                                 |
| 2008-066346           | AF02847                   | Japan   | 03/14/2008  |            | SENSE AMPLIFIER AND OPERATION METHOD FOR MIRRORBIT DDR                                                                                                                      |
| 2008-108886           | AF02852JP                 | Japan   | 04/18/2008  |            | The manufacturing method of a semiconductor device                                                                                                                          |
| 5363004               | AF02860JP                 | Japan   | 02/18/2008  | 09/13/2013 | ELECTRONIC CIRCUIT                                                                                                                                                          |
| 5301147               | AF02869JP                 | Japan   | 12/13/2007  | 06/28/2013 | SIMPLE CHAINED MEMORY SYSTEM PROTOCOL                                                                                                                                       |
| 2010-534979           | AF02873JP                 | Japan   | 11/25/2008  |            | A SYSTEM AND METHOD FOR ACCESSING MEMORY                                                                                                                                    |
| 5566899               | AF02874JP                 | Japan   | 11/25/2008  | 06/27/2014 | A METHOD FOR SETTING PARAMETERS AND DETERMINING LATENCY<br>IN A CHAINED DEVICE SYSTEM                                                                                       |
| 5429572               | AF02875JP                 | Japan   | 11/25/2008  | 12/13/2013 | A CONTROL SCHEME FOR LOWERING LATENCY AND IMPROVING<br>BANDWIDTH IN A DAISY CHAINED DEVICE SYSTEM                                                                           |
| 2010-534980           | AF02876JP                 | Japan   | 05/24/2010  |            | VOLTAGE COMPARATOR AND ELECTRONIC SYSTEM                                                                                                                                    |
| 5322457               | AF02878JP                 | Japan   | 02/19/2008  | 07/26/2013 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE<br>SAME                                                                                                                |
| 5358089               | AF02888JP                 | Japan   | 12/21/2007  | 09/06/2013 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE<br>SAME                                                                                                                |
| 5290592               | AF02891JP                 | Japan   | 02/18/2008  | 06/14/2013 | COMPONENTS CAPABLE OF DETECTING PREDETERMINED TIME BY<br>UTILIZING ReRAM                                                                                                    |
| 5174561               | AF02904JP                 | Japan   | 07/08/2008  | 01/11/2013 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE<br>SAME                                                                                                                |
| 5491694               | AF02908JP                 | Japan   | 11/28/2007  | 03/07/2014 | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF                                                                                                                       |
| 5237648               | AF02909JP                 | Japan   | 02/05/2008  | 04/05/2013 | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF                                                                                                                       |
| 5149694               | AF02910JP                 | Japan   | 05/15/2008  | 12/07/2012 | SYSTEM FOR SOURCE SIDE SENSING                                                                                                                                              |
| 2002-214179           | AF02911JP                 | Japan   | 07/23/2002  |            | SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD                                                                                                                           |
| 5270178               | AF02917JP                 | Japan   | 01/16/2008  | 05/17/2013 | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREOF                                                                                                                             |
| 5259279               | AF02919JP                 | Japan   | 07/04/2008  | 05/02/2013 | SEMICONDUCTOR DEVICE AND ITS CONTROL METHOD                                                                                                                                 |
| 5236343               | AF02920JP                 | Japan   | 04/16/2008  | 04/05/2013 | SEMICONDUCTOR DEVICE AND ITS CONTROL METHOD                                                                                                                                 |
| 5542222               | AF02920JP DIV             | Japan   | 04/16/2008  | 05/16/2014 | SEMICONDUCTOR DEVICE                                                                                                                                                        |
| 4995156               | AF02924JP                 | Japan   | 08/06/2008  | 05/18/2012 | A semiconductor device and its control method                                                                                                                               |
| 5420215               | AF02925JP                 | Japan   | 08/28/2008  | 11/29/2013 | HIGH-DENSITY CHIP STACK STRUCTURE UTILIZING SIDE WIRE IN<br>WAFER LEVEL PROCESS                                                                                             |
| 5174518               | AF02927JP                 | Japan   | 04/17/2008  | 01/11/2013 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE<br>SAME                                                                                                                |
| 5317548               | AF02928JP                 | Japan   | 06/23/2008  | 07/19/2013 |                                                                                                                                                                             |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                             |
|-----------------------|---------------------------|---------|-------------|------------|-----------------------------------------------------------------------------------------------------------------------------------|
| 5215032               | AF02929JP                 | Japan   | 05/09/2008  | 03/08/2013 | METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE                                                                                     |
| 5237731               | AF02935JP                 | Japan   | 09/10/2008  | 04/05/2013 | MEMORY SYSTEM, MEMORY DEVICE, AND MEMORY ACCESS METHOD                                                                            |
| 5489427               | AF02938JP                 | Japan   | 06/27/2008  | 03/07/2014 | MEMORY CONTROLLER, MEMORY SYSTEM AND CONTROL METHOD<br>FOR MEMORY DEVICE                                                          |
| 5566013               | AF02939JP                 | Japan   | 07/28/2008  | 06/27/2014 | A semiconductor device and its manufacturing method                                                                               |
| 5390822               | AF02940JP                 | Japan   | 10/02/2008  | 10/18/2013 | The manufacturing method of a semiconductor device, and a semiconductor<br>device                                                 |
| 5546114               | AF02941JP                 | Japan   | 08/27/2008  | 05/23/2014 | The manufacturing method of a semiconductor device, and a semiconductor<br>device                                                 |
| 5405066               | AF02942JP                 | Japan   | 07/28/2008  | 11/08/2013 | The manufacturing method of a semiconductor device                                                                                |
| 4967110               | AF02943JP                 | Japan   | 04/24/2008  | 04/13/2012 | METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE                                                                                     |
| 5511168               | AF02947JP                 | Japan   | 09/19/2008  | 04/04/2014 | The manufacturing method of a semiconductor device                                                                                |
| 2008-167044           | AF02950JP                 | Japan   | 06/26/2008  |            | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE<br>SAME                                                                      |
| 2014-116618           | AF02950JP DIV             | Japan   | 06/26/2008  |            | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE<br>SAME                                                                      |
| 4876231               | AF02952JP                 | Japan   | 04/11/2008  | 12/09/2011 | BIT LINE CONTACT FORMATION BY USING AMORPHOUS CARBON<br>MASK                                                                      |
| 2008-241259           | AF02954JP                 | Japan   | 09/19/2008  |            | SEMICONDUCTOR MEMORY AND METHOD OF READING THE SAME                                                                               |
| 4882055               | AF02955JP                 | Japan   | 04/11/2008  | 12/16/2011 | FABRICATING METHOD OF BIT LINE CONTACT USING TWO-LAYERS<br>AMORPHOUS CARBON LAYER AS ETCHING STOPPER LAYER                        |
| 2011-190423           | AF02955JP DIV             | Japan   | 04/11/2008  |            | FABRICATING METHOD OF BIT LINE CONTACT USING TWO-LAYERS<br>AMORPHOUS CARBON LAYER AS ETCHING STOPPER LAYER                        |
| 2013-234717           | AF02955JP DIV2            | Japan   | 04/11/2008  |            | FABRICATING METHOD OF BIT LINE CONTACT USING TWO-LAYERS<br>AMORPHOUS CARBON LAYER AS ETCHING STOPPER LAYER                        |
| 5264465               | AF02959JP                 | Japan   | 12/19/2008  | 05/10/2013 | The address designation method of a non-volatile memory apparatus and a<br>non-volatile memory apparatus                          |
| 5153474               | AF02961JP                 | Japan   | 06/23/2008  | 12/14/2012 | SEMICONDUCTOR DEVICE AND ITS CONTROL METHOD (AS<br>AMENDED)                                                                       |
| 2008-036605           | AF02971JP                 | Japan   | 02/18/2008  |            | METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE                                                                                      |
| 5475975               | AF02973JP                 | Japan   | 09/19/2008  | 02/14/2014 | A semiconductor device and its adjustment method                                                                                  |
| 2008-241281           | AF02977JP                 | Japan   | 09/19/2008  |            | GATE VOLTAGE CONTROL METHOD FOR READ OF MULTI-LEVEL CELL                                                                          |
| 5595644               | AF03007JP                 | Japan   | 06/26/2008  | 08/15/2014 | A semiconductor device and its manufacturing method                                                                               |
| 2013-524213           | AF03209JP                 | Japan   | 08/10/2011  |            | STITCH BUMP STACKING DESIGN FOR OVERALL PACKAGE SIZE<br>REDUCTION FOR MULTIPLE STACK                                              |
| 2013-518658           | AF03219JP                 | Japan   | 06/29/2011  |            | METHOD AND SYSTEM FOR THIN MULTI CHIP STACK PACKAGE WITH<br>FILM ON WIRE AND COPPER WIRE                                          |
| 4085147               | AF04002JP                 | Japan   | 10/11/2002  | 02/29/2008 | METHOD AND APPARATUS FOR MANUFACTURING SEMICONDUCTOR<br>DEVICE                                                                    |
| 5019685               | AF04008JP                 | Japan   | 09/20/2001  | 06/22/2012 | MANUFACTURING METHOD FOR SEMICONDUCTOR DEVICE                                                                                     |
| 5179692               | AF04011JP                 | Japan   | 08/30/2002  | 01/18/2013 | SEMICONDUCTOR MEMORY DEVICE AND ITS MANUFACTURING<br>METHOD                                                                       |
| 4171322               | AF04013JP                 | Japan   | 02/17/2003  | 08/15/2008 | ACCESS CONTROL SYSTEM AND ACCESS CONTROL PROGRAM                                                                                  |
| 4210107               | AF04014JP                 | Japan   | 12/06/2002  | 10/31/2008 | TESTING APPARATUS AND TESTING METHOD FOR SEMICONDUCTOR<br>STORAGE DEVICE                                                          |
| 4256185               | AF04015JP                 | Japan   | 03/24/2003  | 02/06/2009 | AIR CURRENT CONTROL STRUCTURE IN CLEAN ROOM                                                                                       |
| 5714495               | AF04026JP                 | Japan   | 10/07/2009  | 03/20/2015 | REAL-TIME DATA PATTERN ANALYSIS SYSTEM AND METHOD OF<br>OPERATION THEREOF                                                         |
| 4928691               | AF04034US                 | Japan   | 09/13/2001  | 02/17/2012 | ULTRAVIOLET-RAY IRRADIATION APPARATUS                                                                                             |
| 2014-547556           | AF04035JP                 | Japan   | 12/18/2012  |            | ACOUSTIC PROCESSING UNIT INTERFACE                                                                                                |
| 2014-547557           | AF04036JP                 | Japan   | 12/18/2012  |            | ARITHMETIC LOGIC UNIT ARCHITECTURE                                                                                                |
| 5513285               | AF04039JP                 | Japan   | 07/06/2010  | 04/04/2014 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                           |
| 2014-066682           | AF04040JP                 | Japan   | 07/06/2010  |            | CONTROL METHOD OF NONVOLATILE SEMICONDUCTOR MEMORY<br>DEVICE                                                                      |
| 5661353               | AF04040JP DIV             | Japan   | 07/06/2010  | 12/12/2014 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                           |
| 4340416               | AF04044JP                 | Japan   | 02/26/2002  | 10/07/2009 | METHOD OF FABRICATING SEMICONDUCTOR MEMORY DEVICE, AND<br>THE SEMICONDUCTOR MEMORY DEVICE                                         |
| 4139266               | AF04060JP                 | Japan   | 05/13/2003  | 06/13/2008 | METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE                                                                                      |
| 223235/1995           | B001JP                    | Japan   | 08/31/1995  |            | ONE-TRANSISTOR MEMORY CELL STRUCTURE AND METHOD FOR<br>FORMING SELF-ALIGNED ONE-TRANSISTOR MEMORY CELL<br>STRUCTURE               |
| 223234/1995           | B002JP                    | Japan   | 08/31/1995  |            | A SELF-ALIGNED BURIED CHANNEL/JUNCTION STACKED GATE FLASH<br>MEMORY CELL                                                          |
| 514582/1996           | B015/2104JP               | Japan   | 09/29/1995  |            | LAYERED LOW DIELECTRIC CONSTANT TECHNOLOGY                                                                                        |
| 1975164               | B047JP                    | Japan   | 06/19/1997  |            | NOVEL PROCESSING TECHNIQUES FOR ACHIEVING PRODUCTION<br>WORTHY LOW DIELECTRIC LOW INTERCONNECT RESISTANCE AND<br>HIGH PERFORMANCE |
| 3821848               | B100JP                    | Japan   | 07/31/1996  | 06/30/2006 | THREE-DIMENSIONAL NON-VOLATILE MEMORY                                                                                             |
| 3968107               | B100JP DIV                | Japan   | 09/21/2005  | 06/08/2007 | 3-D NONVOLATILE MEMORY                                                                                                            |
| 3941882               | B111JP                    | Japan   | 06/21/1996  | 04/13/2007 | THE PROCESS FOR THE SELF-ADJUSTMENT-IZED SOURCE FOR HIGH-<br>DENSITY MEMORY                                                       |
| 3928022               | B128JP                    | Japan   | 08/30/1996  | 03/16/2007 | A FLASH EEPROM MEMORY WITH SEPARATE REFERENCE ARRAY                                                                               |
| 3903142               | B132JP                    | Japan   | 06/18/1996  | 01/19/2007 | CHANNEL HOT CARRIER PAGE WRITE                                                                                                    |
| 521236/1997           | B255JP                    | Japan   | 08/08/1996  |            | POWER SUPPLY INDEPENDENT CURRENT SOURCE FOR FLASH<br>EPROM ERASE                                                                  |
| 3947781               | B260JP                    | Japan   | 07/19/1996  | 04/27/2007 | A NEW PROGRAM ALGORITHM FOR LOW VOLTAGE (3V) SINGLE<br>POWER SUPPLY FLASH MEMORIES                                                |
| 3976282               | B277JP                    | Japan   | 03/25/1997  | 06/29/2007 | THE NOVEL PROCESS FOR RELIABLE ULTR-THIN OXYNITRIDE<br>FORMATION                                                                  |
| 107348/2007           | B277JP DIV                | Japan   | 04/16/2007  |            | A NOVEL PROCESS FOR RELIABLE ULTRATHIN OXYNITRIDE<br>FORMATION                                                                    |

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| PATENT OR APPL<br>NO. | SPANION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                  |
|-----------------------|--------------------------|---------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 3429008               | C061296JP                | Japan   | 01/23/1998  | 05/16/2003 | HIGH VOLTAGE CMOS LEVEL SHIFTER                                                                                                                        |
| 2000-514272           | C141496JP                | Japan   | 04/10/1998  |            | A DUAL SOURCE SIDE POLYSILICON SELECT GATE STRUCTURE AND PROGRAMMING METHOD UTILIZING SINGLE TUNNEL OXIDE FOR NAND ARRAY FLASH MEMORY                  |
| 3283531               | C144496JP                | Japan   | 02/05/1998  | 03/01/2002 | HIGH VOLTAGE NMOS PASS GATE FOR INTEGRATED CIRCUIT WITH HIGH VOLTAGE GENERATOR AND FLASH NON-VOLATILE MEMORY DEVICE HAVING THE PASS GATE               |
| 3327337               | C196596JP                | Japan   | 11/13/1997  | 07/12/2002 | BANK ARCHITECTURE FOR A NON-VOLATILE MEMORY ENABLING SIMULTANEOUS READING AND WRITING                                                                  |
| 4197843               | C369297JP                | Japan   | 12/18/1998  | 10/10/2008 | BIASING METHOD AND STRUCTURE FOR REDUCING BAND-TO-BAND AND/OR AVALANCHE CURRENTS DURING THE ERASE OF FLASH MEMORY DEVICE                               |
| 4546641               | C526397JP                | Japan   | 08/25/1998  | 09/15/2010 | REDUCTION OF CHARGE LOSS IN NONVOLATILE MEMORY CELLS BY PHOSPHOROUS IMPLANTATION INTO PECVD NITRIDE/OXYNITRIDE FILMS                                   |
| 3703069               | C608497JP                | Japan   | 05/20/1999  | 07/29/2005 | SHALLOW TRENCH ISOLATION FILLED WITH THERMAL OXIDE                                                                                                     |
| 2000-537261           | C614497JP                | Japan   | 03/02/1999  |            | STEPPER ALIGNMENT MARK FORMATION WITH DUAL FIELD OXIDE PROCESS                                                                                         |
| 4606580               | C627497JP                | Japan   | 12/18/1998  | 01/05/2011 | METHODS AND ARRANGEMENTS FOR IMPROVED FORMATION OF CONTROL AND FLOATING GATES IN NON-VOLATILE MEMORY SEMICONDUCTOR DEVICES                             |
| 2001-520468           | C656497JP                | Japan   | 08/31/2000  |            | TUNGSTEN GATE MOS TRANSISTOR AND MEMORY CELL AND METHOD OF MAKING SAME                                                                                 |
| 2001-509081           | C695497JP                | Japan   | 06/29/2000  |            | THIN FLOATING GATE AND CONDUCTIVE SELECT GATE IN SITU                                                                                                  |
| 2000-575132           | C715497JP                | Japan   | 09/21/1999  |            | WORDLINE DRIVER FOR FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EEPROM)                                                                 |
| 3761815               | C725497JP                | Japan   | 08/01/2000  | 01/20/2006 | CIRCUIT IMPLEMENTATION TO QUENCH BIT LINE LEAKAGE CURRENT IN PROGRAM AND AUTO PROGRAM DISTURB MODE IN FLASH EPROM USING RESISTOR SOURCE LOAD           |
| 4044443               | C732497US                | Japan   | 04/26/2002  | 11/22/2007 | REMOTE MAINTENANCE SYSTEM AND REMOTE MAINTENANCE METHOD FOR SEMICONDUCTOR MANUFACTURING APPARATUS                                                      |
| 2000-577665           | D016                     | Japan   | 10/05/1999  |            | BIT LINE BIASING METHOD TO ELIMINATE PROGRAM DISTURBANCE IN A NON-VOLATILE MEMORY DEVICE AND MEMORY DEVICE EMPLOYING THE SAME                          |
| 2000-577666           | D138JP                   | Japan   | 04/19/2001  |            | SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON-VOLATILE MEMORY ARRAY                                                                                  |
| 4279469               | D139                     | Japan   | 08/16/1999  | 02/05/2010 | BANK SELECTOR CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITETURE                                      |
| 3197535               | D140JP                   | Japan   | 07/14/1999  | 06/08/2001 | VT REFERENCE VOLTAGE FOR EXTREMELY LOW POWER-SUPPLY                                                                                                    |
| 2000-571459           | D168JP                   | Japan   | 08/16/1999  |            | SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                                          |
| 4642234               | D169JP                   | Japan   | 08/16/1999  | 12/10/2010 | METHOD OF MAKING FLEXIBLY PARTITIONED METAL LINE SEGMENTS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE |
| 4279468               | D170                     | Japan   | 08/16/1999  | 03/19/2009 | MEMORY ADDRESS DECODING CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                           |
| 2000-584526           | D802JP                   | Japan   | 10/27/1999  |            | METHOD FOR IMPROVING ELECTROSTATIC DISCHARGE (ESD) ROBUSTNESS                                                                                          |
| 3811760               | D832JP                   | Japan   | 05/05/2000  | 06/09/2006 | RAMPED OR STEPPED GATE CHANNEL ERASE FOR FLASH MEMORY APPLICATION                                                                                      |
| 520419/2001           | D833JP                   | Japan   | 08/29/2000  |            | 1 TRANSISTOR FOR EEPROM APPLICATION                                                                                                                    |
| 4895452               | D838JP                   | Japan   | 10/24/2000  | 01/06/2012 | SOLID-SOURCE DOPING FOR SOURCE/DRAIN OF FLASH MEMORY                                                                                                   |
| 516197/2001           | D844JP                   | Japan   | 07/14/2000  |            | RAMPED GATE TECHNIQUE FOR SOFT PROGRAMMING TO TIGHTEN THE V <sub>t</sub> DISTRIBUTION                                                                  |
| 4641697               | D853JP                   | Japan   | 12/05/2000  | 12/10/2010 | METHOD TO PROVIDE A REDUCED CONSTANT E-FIELD DURING ERASE OF EEPROMS FOR RELIABILITY IMPROVEMENT                                                       |
| 4955880               | D877JP                   | Japan   | 07/17/2000  | 03/23/2012 | PROCESS FOR FABRICATING INTEGRATED CIRCUIT FORMING TRENCH IN SUBSTRATE (AS AMENDED)                                                                    |
| 4944328               | D894JP                   | Japan   | 09/29/2000  | 03/09/2012 | METHOD OF MANUFACTURING A SEMICONDUCTOR MEMORY DEVICE WITH ANTI-REFLECTIVE COATING                                                                     |
| 2001-555131           | D958JP                   | Japan   | 12/13/2000  |            | NITRIDATION BARRIERS FOR NITRIDATED TUNNEL OXIDE FOR CIRCUITRY FOR FLASH MEMORY TECHNOLOGY AND...                                                      |
| 203354/2010           | D958JP DIV               | Japan   | 12/13/2000  |            | NOVEL NITRIDATION BARRIERS FOR NITRIDATED TUNNEL OXIDE FOR CIRCUITRY FOR FLASH TECHNOLOGY AND FOR LOCOS/STI ISOLATION                                  |
| 5178979               | DA01016JP                | Japan   | 07/14/2000  | 01/18/2013 | METHOD FOR PROVIDING A DOPANT LEVEL FOR POLYSILICON FOR FLASH MEMORY DEVICES                                                                           |
| 509080/2001           | E0197JP                  | Japan   | 06/29/2000  |            | NEW METHOD OF FORMING SELECT GATE TO IMPROVE RELIABILITY AND PERFORMANCE FOR NAND-TYPE FLASH MEMORY DEVICES                                            |
| 4832691               | E0251JP                  | Japan   | 07/14/2000  | 09/30/2011 | FLASH MEMORY ARCHITECTURE EMPLOYING THREE LAYER METAL INTERCONNECT                                                                                     |
| 4606682               | E0264JP                  | Japan   | 02/07/2001  | 10/15/2010 | TRIMMING METHOD FOR WORDLINE BOOSTER TO MINIMIZE PROCESS VARIATION OF BOOSTED WORDLINE VOLTAGE                                                         |
| 5016769               | E0302JP                  | Japan   | 05/01/2001  | 06/15/2012 | UNIFORM BITLINE STRAPPING OF A NON-VOLATILE MEMORY CELL                                                                                                |
| 569884/2001           | E0370JP                  | Japan   | 03/12/2001  |            | METHOD FOR FORMING DUAL SPACERS AND NON-VOLATILE MEMORY DEVICE MADE THEREBY                                                                            |
| 4606694               | E0462JP                  | Japan   | 05/21/2001  | 10/15/2010 | DUAL PORTED CAMS FOR SIMULTANEOUS OPERATION FLASH MEMORY                                                                                               |
| 564161/2001           | E1030JP                  | Japan   | 02/07/2001  |            | TEMPERATURE COMPENSATED BIAS GENERATOR                                                                                                                 |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                     |
|-----------------------|---------------------------|---------|-------------|------------|-----------------------------------------------------------------------------------------------------------|
| 4698119               | F0004JP                   | Japan   | 06/08/2001  | 03/11/2011 | AUTOMATED DETERMINATION AND DISPLAY OF THE PHYSICAL LOCATION OF A FAILED CELL IN AN ARRAY OF MEMORY CELLS |
| 4601250               | F0257JP                   | Japan   | 08/07/2001  | 10/08/2010 | METHOD AND SYSTEM FOR EMBEDDED CHIP ERASE VERIFICATION                                                    |
| 2003-562937           | F0258                     | Japan   | 12/17/2002  |            | METHOD AND APPARATUS FOR SOFT PROGRAM VERIFICATION IN A MEMORY DEVICE                                     |
| 4128950               | F0260JP                   | Japan   | 12/12/2001  | 05/23/2008 | METHOD AND APPARATUS FOR BOOSTING BITLINES FOR LOW VCC READ                                               |
| 2007-211874           | F0260JP DIV               | Japan   | 12/12/2001  |            | METHOD AND APPARATUS FOR BOOSTING BITLINES FOR LOW VCC READ                                               |
| 4106028               | F0262JP                   | Japan   | 12/17/2002  | 04/04/2008 | METHOD AND APPARATUS FOR SOFT PROGRAM VERIFICATION IN A MEMORY DEVICE                                     |
| 2003-562936           | F0272JP                   | Japan   | 12/17/2002  |            | CHARGE INJECTION                                                                                          |
| 3955530               | F0274JP                   | Japan   | 11/01/2001  | 05/11/2007 | HIGHER PROGRAM VT AND FASTER PROGRAMMING RATES BASED ON IMPROVED ERASE METHODS                            |
| 4482704               | F0282JP                   | Japan   | 09/30/2002  | 04/02/2010 | DOUBLE DENSED CORE GATES IN SONOS FLASH MEMORY                                                            |
| 5113316               | F0283JP                   | Japan   | 09/27/2002  | 10/19/2012 | SALICIDED GATE FOR VIRTUAL GROUND ARRAYS                                                                  |
| 4955902               | F0499JP                   | Japan   | 08/06/2001  | 03/23/2012 | METHOD FOR MANUFACTURING FLASH MEMORY CELL                                                                |
| 4944352               | F0932JP                   | Japan   | 08/06/2001  | 03/09/2012 | METHOD FOR MANUFACTURING FLASH MEMORY CELL                                                                |
| 4-182512              | FMA13-0001US              | Japan   | 07/09/1992  |            | SEMICONDUCTOR INTEGRATED CIRCUIT                                                                          |
| 3-199182              | FMA13-0002EP              | Japan   | 08/08/1991  |            | PLL SYNTHESIZER CIRCUIT                                                                                   |
| 3,318,365             | FMA13-0003US CON          | Japan   | 10/20/1992  | 06/14/2002 | CONSTANT VOLTAGE CIRCUIT                                                                                  |
| 3693681               | FMA13-0004JP              | Japan   | 03/18/1993  | 07/01/2005 | ARITHMETIC UNIT                                                                                           |
| 2980142               | FMA13-0005US              | Japan   | 12/10/1992  | 09/17/1999 | SEMICONDUCTOR CAPACITANCE ELEMENT AND CIRCUIT USING THE SAME                                              |
| 2963270               | FMA13-0006JP              | Japan   | 03/13/1992  | 08/06/1999 | MICROCONTROLLER FOR SPECIFIC APPLICATION                                                                  |
| 3449749               | FMA13-0007JP              | Japan   | 06/25/1993  | 07/11/2003 | INFORMATION PROCESSING APPARATUS                                                                          |
| 5-334973              | FMA13-0008US              | Japan   | 12/28/1993  |            | POTENTIAL GENERATING CIRCUIT                                                                              |
| 3538442               | FMA13-0009US              | Japan   | 09/20/1993  | 03/26/2004 | ECL-TO-CMOS SIGNAL LEVEL CONVERTER                                                                        |
| 3282907               | FMA13-0010JP              | Japan   | 01/27/1994  | 03/01/2002 | REFERENCE VOLTAGE GENERATION CIRCUIT                                                                      |
| 3335455               | FMA13-0011EP              | Japan   | 01/19/1994  | 08/02/2002 | TRANSIMPEDANCE AMPLIFIER                                                                                  |
| 3647481               | FMA13-0012JP              | Japan   | 04/28/1994  | 02/18/2005 | MICROCONTROLLER                                                                                           |
| 3437274               | FMA13-0013JP              | Japan   | 08/12/1994  | 06/06/2003 | REFERENCE VOLTAGE CIRCUIT                                                                                 |
| 3727670               | FMA13-0014US              | Japan   | 04/28/1994  | 10/07/2005 | MULTIPLE OPERATION MODE MICROCONTROLLER                                                                   |
| 3478596               | FMA13-0015GB              | Japan   | 05/27/1993  | 10/03/2003 | POWER SUPPLY CONNECTION CIRCUIT AND SWITCHING IC FOR POWER SUPPLY LINE                                    |
| 3481323               | FMA13-0016JP              | Japan   | 11/07/1994  | 10/10/2003 | CURRENT DETECTION CIRCUIT AND CURRENT MONITOR DEVICE                                                      |
| 3404127               | FMA13-0017US              | Japan   | 06/17/1994  | 02/28/2003 | SEMICONDUCTOR MEMORY DEVICE HAVING BIT LINE PRECHARGER                                                    |
| 3411120               | FMA13-0018JP              | Japan   | 03/08/1995  | 03/20/2003 | PLL CIRCUIT                                                                                               |
| 3512895               | FMA13-0019JP DIV          | Japan   | 04/08/1994  | 01/16/2004 | REFERENCE VOLTAGE GENERATION CIRCUIT                                                                      |
| 3614198               | FMA13-0020JP              | Japan   | 01/26/1995  | 11/12/2004 | METHOD FOR SCHEDULING INSTRUCTION IN ASSEMBLER                                                            |
| 3930576               | FMA13-0021JP              | Japan   | 07/11/1995  | 03/16/2007 | COMPUTER SYSTEM WITH A FUNCTION PREVENTING ILLEGAL USE OF SOFTWARE                                        |
| 2005-162431           | FMA13-0021JP DIV          | Japan   | 07/11/1995  |            | STORAGE MEDIUM HAVING SOFTWARE MISUSE PREVENTIVE FUNCTION                                                 |
| 3514532               | FMA13-0022US              | Japan   | 11/30/1994  | 01/23/2004 | CLOCK SIGNAL GENERATING DEVICE                                                                            |
| 3567510               | FMA13-0023JP              | Japan   | 12/16/1994  | 06/25/2004 | INTERRUPT PRIORITY DECISION CIRCUIT                                                                       |
| 2004-317466           | FMA13-0024JP              | Japan   | 12/12/1994  |            | INFORMATION PROCESSING APPARATUS                                                                          |
| 2004-317493           | FMA13-0024JP DIV          | Japan   | 12/12/1994  |            | INFORMATION PROCESSOR                                                                                     |
| 3724001               | FMA13-0024US DIV          | Japan   | 12/12/1994  | 09/30/2005 | INFORMATION PROCESSING DEVICE WITH DECISION CIRCUITS AND ...                                              |
| 3544243               | FMA13-0025JP              | Japan   | 05/11/1995  | 04/16/2004 | DIFFERENTIAL AMPLIFIER                                                                                    |
| 3487003               | FMA13-0026JP              | Japan   | 02/08/1995  | 10/31/2003 | BIAS VOLTAGE GENERATION CIRCUIT                                                                           |
| 3630796               | FMA13-0027JP              | Japan   | 10/04/1995  | 12/24/2004 | SWITCHED CAPACITOR OPERATIONAL CIRCUIT                                                                    |
| 3538483               | FMA13-0028JP              | Japan   | 07/27/1995  | 03/26/2004 | OUTPUT CIRCUIT                                                                                            |
| 3665395               | FMA13-0029JP              | Japan   | 10/13/1995  | 04/08/2005 | INTERFACE CIRCUIT                                                                                         |
| 4866158               | FMA13-0030JP              | Japan   | 06/20/2006  | 11/18/2011 | REGULATOR CIRCUIT                                                                                         |
| 4846493               | FMA13-00304JP             | Japan   | 09/05/2006  | 10/21/2011 | DEBUGGING SYSTEM, DEBUGGING CIRCUIT AND INFORMATION PROCESSING APPARATUS                                  |
| 2005-268216           | FMA13-00305JP             | Japan   | 09/15/2005  |            | IMAGE PROCESSOR AND IMAGE PROCESSING METHOD                                                               |
| 2006-181692           | FMA13-00305JP DIV         | Japan   | 09/15/2005  |            | IMAGE PROCESSOR AND IMAGE PROCESSING METHOD                                                               |
| 2006-269854           | FMA13-00306JP             | Japan   | 09/29/2006  |            | STEPPING MOTOR CONTROLLER, STEPPING MOTOR CONTROL METHOD AND STEPPING MOTOR CONTROL SYSTEM                |
| 4814950               | FMA13-00307JP             | Japan   | 09/29/2006  | 09/02/2011 | TRANSMITTING/RECEIVING SYSTEM, NODE AND COMMUNICATION METHOD                                              |
| 5098367               | FMA13-00308JP             | Japan   | 03/06/2007  | 10/05/2012 | POWER SUPPLY VOLTAGE REGULATOR CIRCUIT AND MICROCOMPUTER                                                  |
| 4930510               | FMA13-00309JP             | Japan   | 09/28/2006  | 02/24/2012 | SIGNAL RECEIVER APPARATUS AND WAVEFORM SHAPING METHOD                                                     |
| 3288553               | FMA13-0030JP              | Japan   | 05/25/1995  | 03/15/2002 | RESISTOR ARRAY FOR A/D CONVERTER AND N-M BITS SERIES-PARALLEL A/D CONVERTER                               |
| 5245237               | FMA13-00310JP             | Japan   | 09/29/2006  | 04/19/2013 | ERROR PROCESSING METHOD AND INFORMATION PROCESSING APPARATUS                                              |
| 4978233               | FMA13-00311JP             | Japan   | 02/22/2007  | 04/27/2012 | A simulator development system and the simulator development method                                       |
| 4888056               | FMA13-00312JP             | Japan   | 10/30/2006  | 12/22/2011 | POWER SUPPLY CIRCUIT, POWER SUPPLY CONTROL CIRCUIT, AND POWER ...                                         |
| 4899624               | FMA13-00313JP             | Japan   | 05/11/2006  | 01/13/2012 | CIRCUIT FOR PREVENTING THROUGH CURRENT IN DC-DC CONVERTER                                                 |
| 2006-192600           | FMA13-00314JP             | Japan   | 07/13/2006  |            | DC-DC CONVERTER                                                                                           |
| 4823003               | FMA13-00315JP             | Japan   | 09/28/2006  | 09/16/2011 | CONTROL CIRCUIT OF SYNCHRONOUS RECTIFICATION TYPE POWER SUPPLY UNIT, ...                                  |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                        |
|-----------------------|---------------------------|---------|-------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 5595633               | FMA13-00316JP             | Japan   | 02/26/2007  | 08/15/2014 | SIMULATION METHOD AND SIMULATION APPARATUS                                                                                                   |
| 4791260               | FMA13-00317JP             | Japan   | 06/09/2006  | 07/29/2011 | DC-DC CONVERTER WITH OSCILLATOR AND MONITORING FUNCTION                                                                                      |
| 5076381               | FMA13-00318JP             | Japan   | 07/07/2006  | 09/07/2012 | SOFTWARE DEVELOPMENT APPARATUS AND METHOD                                                                                                    |
| 4967526               | FMA13-00319JP             | Japan   | 08/22/2006  | 04/13/2012 | CONTROL CIRCUIT OF POWER SUPPLY UNIT WHICH CONTROL<br>OUTPUT POWER ...                                                                       |
| 3218914               | FMA13-0031JP              | Japan   | 04/27/1995  | 08/10/2001 | TERMINATION CIRCUIT FOR SIGNAL LINE                                                                                                          |
| 5076536               | FMA13-00320JP             | Japan   | 02/16/2007  | 09/07/2012 | DC-DC CONVERTER WITH PLURALITY OF SOFT-START CONTROL<br>CIRCUITS                                                                             |
| 5023731               | FMA13-00321JP             | Japan   | 02/16/2007  | 06/29/2012 | POWER SUPPLY CIRCUIT, POWER SUPPLY CONTROL CIRCUIT, AND<br>POWER ...                                                                         |
| 4827764               | FMA13-00322JP             | Japan   | 02/20/2007  | 09/22/2011 | FRACTIONAL FREQUENCY DIVIDER PLL DEVICE AND CONTROL<br>METHOD THEREOF                                                                        |
| 4997891               | FMA13-00323JP             | Japan   | 09/15/2006  | 05/25/2012 | METHOD AND CIRCUIT FOR CONTROLLING DC-DC CONVERTER                                                                                           |
| 4962060               | FMA13-00324JP             | Japan   | 03/14/2007  | 04/06/2012 | Parity error restoration circuit                                                                                                             |
| 5292706               | FMA13-00325JP             | Japan   | 02/28/2007  | 06/21/2013 | COMPUTER SYSTEM AND MEMORY SYSTEM                                                                                                            |
| 4985035               | FMA13-00326JP             | Japan   | 03/30/2007  | 05/11/2012 | OSCILLATOR CIRCUIT                                                                                                                           |
| 5261919               | FMA13-00327JP             | Japan   | 11/10/2006  | 05/10/2013 | CONTROL CIRCUIT FOR DETECTING A REVERSE CURRENT IN A DC-<br>DC CONVERTER                                                                     |
| 5263380               | FMA13-00327JP DIV         | Japan   | 12/26/2011  | 05/10/2013 | CONTROL CIRCUIT FOR DETECTING A REVERSE CURRENT IN A DC-<br>DC CONVERTER                                                                     |
| 5125066               | FMA13-00328JP             | Japan   | 11/10/2006  | 11/09/2012 | CONTROL CIRCUIT FOR SYNCHRONOUS RECTIFIER-TYPE DC-DC<br>CONVERTER, SYNCHRONOUS RECTIFIER-TYPE DC-DC CONVERTER<br>AND CONTROL METHOD THEREOF  |
| 5034451               | FMA13-00329JP             | Japan   | 11/10/2006  | 07/13/2012 | CONTROL CIRCUIT FOR CURRENT MODE DC-DC CONVERTER AND<br>CONTROL METHOD OF CURRENT MODE DC-DC CONVERTER                                       |
| 3437322               | FMA13-0032JP              | Japan   | 04/07/1995  | 06/06/2003 | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                                                                                                      |
| 4918874               | FMA13-00330JP             | Japan   | 03/14/2007  | 02/10/2012 | CLOCK SIGNAL TRANSMISSION CIRCUIT                                                                                                            |
| 2009-508777           | FMA13-00331US             | Japan   | 03/29/2007  |            | DISPLAY CONTROL DEVICE, INFORMATION PROCESSOR, AND<br>DISPLAY CONTROL PROGRAM                                                                |
| 4667525               | FMA13-00332JP             | Japan   | 06/22/2007  | 01/21/2011 | A PLL control circuit, a PLL apparatus, and a PLL control method                                                                             |
| 5028972               | FMA13-00333JP             | Japan   | 11/27/2006  | 07/06/2012 | OPERATION AMPLIFIER CIRCUIT                                                                                                                  |
| 2006-318638           | FMA13-00334US DIV         | Japan   | 11/27/2006  |            | PLL CIRCUIT                                                                                                                                  |
| 4952783               | FMA13-00335JP             | Japan   | 03/14/2007  | 03/23/2012 | OUTPUT CIRCUIT                                                                                                                               |
| 5045167               | FMA13-00336JP             | Japan   | 03/16/2007  | 07/27/2012 | OSCILLATION CIRCUIT AND SEMICONDUCTOR DEVICE                                                                                                 |
| 4789835               | FMA13-00337JP             | Japan   | 03/15/2007  | 07/29/2011 | IEEE 1394 TRANSMITTER, IEEE 1394 RECEIVER AND AUDIO DATA<br>CONTENT TRANSMISSION METHOD                                                      |
| 4984997               | FMA13-00338JP             | Japan   | 03/16/2007  | 05/11/2012 | The control circuit, power supply voltage supply system, and the power supply<br>voltage supply method of a DC-DC converter                  |
| 5352964               | FMA13-00339US             | Japan   | 03/29/2007  | 09/06/2013 | DC-DC CONVERTER, METHOD AND SYSTEM FOR SUPPLYING POWER<br>SUPPLY VOLTAGE                                                                     |
| 3456303               | FMA13-0033JP              | Japan   | 05/19/1995  | 08/01/2003 | SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                                             |
| 5211523               | FMA13-00340JP             | Japan   | 03/27/2007  | 03/08/2013 | DC-DC CONVERTER, POWER SUPPLY SYSTEM, AND POWER SUPPLY<br>METHOD                                                                             |
| 5167665               | FMA13-00341JP             | Japan   | 03/26/2007  | 01/11/2013 | CONTROL CIRCUIT FOR STEP-DOWN DC-DC CONVERTER, STEP-<br>DOWN DC-DC CONVERTER AND CONTROL METHOD THEREOF                                      |
| 4968325               | FMA13-00342JP             | Japan   | 03/08/2007  | 04/13/2012 | SOFTWARE OPTIMIZATION DEVICE AND SOFTWARE OPTIMIZATION<br>METHOD                                                                             |
| 5458208               | FMA13-00343JP             | Japan   | 03/20/2007  | 01/17/2014 | PROCESSOR SYSTEM OPTIMIZATION SUPPORTING APPARATUS AND<br>SUPPORTING METHOD                                                                  |
| 5595577               | FMA13-00343JP DIV         | Japan   | 03/20/2007  | 08/15/2014 | PROCESSOR SYSTEM OPTIMIZATION SUPPORTING APPARATUS AND<br>SUPPORTING METHOD                                                                  |
| 5413969               | FMA13-00343US<br>CON      | Japan   | 03/20/2007  | 11/22/2013 | PROCESSOR SYSTEM OPTIMIZATION SUPPORTING APPARATUS AND<br>SUPPORTING METHOD                                                                  |
| 3838180               | FMA13-00344EP             | Japan   | 09/12/2002  | 08/11/2006 | A CLOCK GENERATING CIRCUIT AND THE CLOCK PRODUCTION                                                                                          |
| 4198722               | FMA13-00344JP             | Japan   | 05/24/2006  | 10/10/2008 | THE CLOCK GENERATING CIRCUIT, PLL AND THE CLOCK<br>PRODUCTION                                                                                |
| 4836844               | FMA13-00345JP             | Japan   | 03/22/2007  | 10/07/2011 | RESET CIRCUIT AND SYSTEM                                                                                                                     |
| 4888272               | FMA13-00346EP             | Japan   | 07/30/2007  | 12/22/2011 | SIMULATION OF PROGRAM EXECUTION TO DETECT PROBLEM SUCH<br>AS DEADLOCK                                                                        |
| 5029055               | FMA13-00347JP             | Japan   | 02/16/2007  | 07/06/2012 | A detection circuit and a power source system                                                                                                |
| 5411415               | FMA13-00348EP             | Japan   | 08/16/2007  | 11/15/2013 | Temperature characteristic correction circuit                                                                                                |
| 5425257               | FMA13-00348JP DIV         | Japan   | 04/16/2012  | 12/06/2013 | Temperature characteristic correction circuit                                                                                                |
| 5034703               | FMA13-00349JP             | Japan   | 06/15/2007  | 07/13/2012 | The error generation method and CAN communication apparatus of CAN                                                                           |
| 3560696               | FMA13-0034JP              | Japan   | 07/10/1995  | 06/04/2004 | PLL CIRCUIT                                                                                                                                  |
| 5029056               | FMA13-00350JP             | Japan   | 02/16/2007  | 07/06/2012 | A detection circuit and a power source system                                                                                                |
| 4909144               | FMA13-00351JP             | Japan   | 03/22/2007  | 01/20/2012 | IMAGE RECOGNITION DEVICE AND IMAGE ROTATING METHOD                                                                                           |
| 5056852               | FMA13-00352US             | Japan   | 09/04/2007  | 08/10/2012 | CHARGING CIRCUIT                                                                                                                             |
| 4781471               | FMA13-00353EP             | Japan   | 11/02/2007  | 07/15/2011 | A signal processing apparatus and a communication apparatus                                                                                  |
| 5266705               | FMA13-00354JP             | Japan   | 10/01/2007  | 05/17/2013 | COMMUNICATION SYSTEM                                                                                                                         |
| 5459937               | FMA13-00355JP             | Japan   | 04/19/2007  | 01/24/2014 | INTEGRATED CIRCUIT AND AUDIO APPARATUS                                                                                                       |
| 2012-088276           | FMA13-00357JP DIV         | Japan   | 06/15/2007  | 04/09/2009 | STEP-UP/STEP-DOWN TYPE DC-DC CONVERTER, AND CONTROL<br>CIRCUIT AND CONTROL METHOD OF THE SAME                                                |
| 5023819               | FMA13-00357US             | Japan   | 06/16/2006  | 06/29/2012 | The control method of a buck-boost DC-DC converter, the control circuit of a<br>buck-boost DC-DC converter, and a buck-boost DC-DC converter |
| 5163332               | FMA13-00358JP             | Japan   | 07/15/2008  | 12/28/2012 | PROGRAM, DESIGN APPARATUS, AND DESIGN METHOD FOR<br>DYNAMIC RECONFIG ...                                                                     |
| 5040421               | FMA13-00359JP             | Japan   | 05/07/2007  | 07/20/2012 | CONSTANT VOLTAGE CIRCUIT, CONSTANT VOLTAGE SUPPLY SYSTEM<br>AND CONSTANT VOLTAGE SUPPLY METHOD                                               |
| 3699517               | FMA13-0035JP              | Japan   | 01/16/1996  | 07/15/2005 | SEMICONDUCTOR SWITCHING CONTROL CIRCUIT                                                                                                      |
| 5411959               | FMA13-00360JP             | Japan   | 03/30/2012  | 11/15/2013 | DC-DC CONVERTER AND CONTROL METHOD THEREOF                                                                                                   |
| 5029156               | FMA13-00360US             | Japan   | 06/11/2007  | 07/06/2012 | A DC-DC converter and its control method                                                                                                     |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                         |
|-----------------------|---------------------------|---------|-------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 5067111               | FMA13-00361JP             | Japan   | 10/18/2007  | 08/24/2012 | SEMICONDUCTOR INTEGRATED CIRCUIT AND DEBUG MODE DETERMINATION METHOD                                                                          |
| 5050786               | FMA13-00362JP             | Japan   | 11/05/2007  | 08/03/2012 | A drawing processing apparatus, a drawing processing method, and a drawing processing program                                                 |
| 5194804               | FMA13-00363JP             | Japan   | 01/08/2008  | 02/15/2013 | SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                                              |
| 5115307               | FMA13-00364JP             | Japan   | 04/25/2008  | 10/26/2012 | SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                                              |
| 5320817               | FMA13-00365JP             | Japan   | 05/23/2008  | 07/26/2013 | METHOD AND DEVICE FOR TRANSMITTING PACKETS                                                                                                    |
| 5211678               | FMA13-00366JP             | Japan   | 12/26/2007  | 03/08/2013 | DC-DC CONVERTER, DC-DC CONVERTER CONTROL METHOD, AND ELECTRONIC DEVICE                                                                        |
| 5176646               | FMA13-00367JP             | Japan   | 03/28/2008  | 01/18/2013 | An error correction function checking circuit, the error correction function confirmation method and its computer program, and a memory       |
| 2007-289876           | FMA13-00368US             | Japan   | 11/07/2007  |            | LINEAR REGULATOR CIRCUIT, LINEAR REGULATION METHOD, AND SEMICONDUCTOR DEVICE                                                                  |
| 5262158               | FMA13-00369US DIV         | Japan   | 02/13/2008  | 05/10/2013 | THE SYNCHRONOUS LOSS-PREVENTION METHOD AND A SYNCHRONOUS LOSS-PREVENTION APPARATUS                                                            |
| 3643421               | FMA13-0036US              | Japan   | 01/29/1996  | 02/04/2005 | OUTPUT CIRCUIT                                                                                                                                |
| 4968121               | FMA13-00370JP             | Japan   | 03/10/2008  | 04/13/2012 | CAPACITANCE SENSOR FOR DETECTING A CHARGE VOLTAGE OF A MULTI-CAPACITOR CIRCUIT                                                                |
| 5146009               | FMA13-00371JP             | Japan   | 02/28/2008  | 12/07/2012 | POWER SUPPLY CONTROL DEVICE AND POWER SUPPLY CONTROL METHOD                                                                                   |
| 5286944               | FMA13-00372JP             | Japan   | 05/30/2008  | 06/14/2013 | PACKET COMMUNICATION DEVICE FOR COMMUNICATING PACKET TO BE ...                                                                                |
| 5509357               | FMA13-00372JP DIV         | Japan   | 02/12/2013  | 03/28/2014 | RECEIVING DEVICE AND PACKET COMMUNICATION METHOD                                                                                              |
| 2014-059645           | FMA13-00372JP DIV2        | Japan   | 05/30/2008  |            | TRANSMISSION APPARATUS AND PACKET COMMUNICATION METHOD                                                                                        |
| 5082908               | FMA13-00373JP             | Japan   | 02/13/2008  | 09/14/2012 | POWER SUPPLY CIRCUIT, OVERCURRENT PROTECTION CIRCUIT FOR THE SAME, AND ELECTRONIC DEVICE                                                      |
| 5018570               | FMA13-00374JP             | Japan   | 03/10/2008  | 06/22/2012 | A linear correction circuit and a sensor apparatus                                                                                            |
| 4998386               | FMA13-00375JP             | Japan   | 06/27/2008  | 05/25/2012 | LINE PLOTTING METHOD                                                                                                                          |
| 5251594               | FMA13-00376JP             | Japan   | 02/26/2009  | 04/26/2013 | POWER SUPPLY CONTROL APPARATUS/METHOD                                                                                                         |
| 5141393               | FMA13-00377JP             | Japan   | 06/23/2008  | 11/30/2012 | IMPROVEMENT CONVERTING CIRCUIT                                                                                                                |
| 2000-078132           | FMA13-00378JP             | Japan   | 03/20/2000  |            | SEMICONDUCTOR MEMORY                                                                                                                          |
| 4568299               | FMA13-00378JP DIV         | Japan   | 03/23/2007  | 08/13/2010 | SEMICONDUCTOR MEMORY DEVICE                                                                                                                   |
| 4485546               | FMA13-00379JP             | Japan   | 06/18/2007  | 04/02/2010 | SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                                              |
| 2007-160029           | FMA13-00379JP DIV         | Japan   | 10/27/2003  |            | SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                                              |
| 2003-366085           | FMA13-00379US             | Japan   | 10/27/2003  |            | SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                                              |
| 3765856               | FMA13-0037JP              | Japan   | 12/20/1995  | 02/03/2006 | CURRENT-VOLTAGE CONVERSION CIRCUIT AND PHOTOELECTRONIC CONVERSION DEVICE                                                                      |
| 4668957               | FMA13-00380JP             | Japan   | 04/15/2002  | 01/21/2011 | CHARGE-DISCHARGE CONTROL METHOD AND ELECTRONIC APPARATUS                                                                                      |
| 4846755               | FMA13-00380JP DIV         | Japan   | 04/21/2008  | 10/21/2011 | SIGNAL DETECTION APPARATUS, SIGNAL DETECTION METHOD, SIGNAL TRANSMISSION SYSTEM, AND COMPUTER READABLE PROGRAM TO EXECUTE SIGNAL TRANSMISSION |
| 2010-087014           | FMA13-00380JP DIV1        | Japan   | 04/05/2010  |            | POWER SUPPLY CONTROL METHOD                                                                                                                   |
| 4137496               | FMA13-00380US             | Japan   | 04/15/2002  | 06/13/2008 | METHOD FOR PREDICTING REMAINING CHARGE OF PORTABLE ELECTRONICS BATTERY                                                                        |
| 4808195               | FMA13-00381JP             | Japan   | 08/09/2007  | 08/26/2011 | OPERATION AMPLIFIER, LINE DRIVER, AND LIQUID CRYSTAL DISPLAY DEVICE                                                                           |
| 4068040               | FMA13-00381US DIV2        | Japan   | 10/10/2003  | 01/18/2008 | OPERATION AMPLIFIER, LINE DRIVER, AND LIQUID CRYSTAL DISPLAY DEVICE                                                                           |
| 3873062               | FMA13-00382JP             | Japan   | 04/09/2004  | 10/27/2006 | A SELECTING CIRCUIT AND A SEMICONDUCTOR DEVICE PROVIDED WITH THE SAME, A D/A-CONVERSION CIRCUIT, AND A LIQUID CRYSTAL DISPLAY                 |
| 4669501               | FMA13-00382JP DIV         | Japan   | 09/20/2007  | 01/21/2011 | SEMICONDUCTOR DEVICE HAVING SELECTING CIRCUIT, D/A CONVERTER ...                                                                              |
| 2004-280500           | FMA13-00382JP DIV         | Japan   | 11/20/1998  |            | SEMICONDUCTOR DEVICE                                                                                                                          |
| 10-330507             | FMA13-00382US             | Japan   | 11/20/1998  |            | SELECTION CIRCUIT, SEMICONDUCTOR DEVICE PROVIDED WITH IT, D/A CONVERTER AND LIQUID CRYSTAL DISPLAY DEVICE                                     |
| 9-324515              | FMA13-00383JP             | Japan   | 11/26/1997  |            | OUTPUT CIRCUIT USING DIFFERENTIAL AMPLIFIER CIRCUIT                                                                                           |
| 4713560               | FMA13-00383JP DIV         | Japan   | 10/29/2007  | 04/01/2011 | DIFFERENTIAL AMPLIFIER CIRCUIT                                                                                                                |
| 5461025               | FMA13-00385JP             | Japan   | 02/17/2009  | 01/24/2014 | METHOD FOR CONTROLLING DC-DC CONVERTER, CIRCUIT FOR CONTROLLING DC-DC CONVERTER AND DC-DC CONVERTER                                           |
| 5092997               | FMA13-00386JP             | Japan   | 08/27/2008  | 09/28/2012 | DC-DC CONVERTER AND POWER SUPPLY FOR SYSTEM                                                                                                   |
| 5627856               | FMA13-00387JP             | Japan   | 01/26/2009  | 10/10/2014 | POWER SUPPLY CONTROLLING CIRCUIT, POWER SUPPLY CONTROLLING METHOD AND ELECTRONIC DEVICE                                                       |
| 5168082               | FMA13-00388JP             | Japan   | 10/24/2008  | 01/11/2013 | STEP-UP/STEP-DOWN TYPE DC-DC CONVERTER, AND CONTROL CIRCUIT ...                                                                               |
| 5277913               | FMA13-00389US CON         | Japan   | 11/28/2008  | 05/31/2013 | THE CONTROL CIRCUIT OF A DC-DC CONVERTER AND A DC-DC CONTROLLER                                                                               |
| 3920371               | FMA13-0038US              | Japan   | 01/29/1996  | 02/23/2007 | A CHARGER, AN ELECTRIC-CURRENT DETECTION CIRCUIT, AND A VOLTAGE DETECTION CIRCUIT                                                             |
| 5083117               | FMA13-00390JP             | Japan   | 08/20/2008  | 09/14/2012 | DC-DC CONVERTER AND CONTROL CIRCUIT FOR DC-DC CONVERTER                                                                                       |
| 5287185               | FMA13-00391JP             | Japan   | 12/01/2008  | 06/14/2013 | STEP-UP/STEP-DOWN POWER SUPPLY CONTROL DEVICE, AND METHOD FOR ...                                                                             |
| 5223497               | FMA13-00392JP             | Japan   | 06/27/2008  | 03/22/2013 | PEAK HOLD CIRCUIT                                                                                                                             |
| 5125605               | FMA13-00393JP             | Japan   | 02/27/2008  | 11/09/2012 | INTEGRATED CIRCUIT DEVICE HAVING RESET CONTROL                                                                                                |
| 5272719               | FMA13-00394JP             | Japan   | 12/24/2008  | 05/24/2013 | DATA TRANSFER APPARATUS AND DATA TRANSFER METHOD                                                                                              |
| 5245653               | FMA13-00395JP             | Japan   | 09/01/2008  | 04/19/2013 | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                                                                                                       |
| 5125786               | FMA13-00396JP             | Japan   | 06/12/2008  | 11/09/2012 | INFORMATION PROCESSING SYSTEM                                                                                                                 |
| 5163307               | FMA13-00397JP             | Japan   | 06/20/2008  | 12/28/2012 | POWER-ON DETECTION CIRCUIT AND MICROCONTROLLER                                                                                                |

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| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                           |
|-----------------------|--------------------------|---------|-------------|------------|-----------------------------------------------------------------------------------------------------------------|
| 5251455               | FMA13-00398JP            | Japan   | 11/27/2008  | 04/26/2013 | CONTROL CIRCUIT FOR DC-DC CONVERTER                                                                             |
| 2008-276747           | FMA13-00399JP            | Japan   | 10/28/2008  |            | FILTERING CIRCUIT AND METHOD FOR ITS ADJUSTMENT                                                                 |
| 3765868               | FMA13-0039JP             | Japan   | 03/25/1996  | 02/03/2006 | PLL FREQUENCY SYNTHESIZER                                                                                       |
| 5486222               | FMA13-00400JP            | Japan   | 06/25/2009  | 02/28/2014 | A semiconductor integrated circuit and a power supply device                                                    |
| 5304173               | FMA13-00401JP            | Japan   | 10/27/2008  | 07/05/2013 | POWER SUPPLY VOLTAGE CONTROL CIRCUIT, POWER SUPPLY<br>VOLTAGE CONTROL METHOD AND DC-DC CONVERTER                |
| 2013-100145           | FMA13-00401JP DIV        | Japan   | 10/27/2008  |            | POWER SUPPLY VOLTAGE CONTROL CIRCUIT AND POWER SUPPLY<br>VOLTAGE CONTROL METHOD                                 |
| 5340721               | FMA13-00402JP            | Japan   | 12/26/2008  | 08/16/2013 | POWER SUPPLY DEVICE                                                                                             |
| 5115347               | FMA13-00402US<br>CON     | Japan   | 06/12/2008  | 10/26/2012 | CONTROL CIRCUIT OF DC-DC CONVERTER, DC-DC CONVERTER AND<br>CONTROL METHOD OF DC-DC CONVERTER                    |
| 5451094               | FMA13-00403US            | Japan   | 02/02/2009  | 01/10/2014 | A charging circuit, a charging device, an electronic device, and the charge<br>method                           |
| 5239633               | FMA13-00404JP            | Japan   | 08/27/2008  | 04/12/2013 | VEHICLE-MOUNTED IMAGE DATA TRANSFER APPARATUS                                                                   |
| 5056644               | FMA13-00405JP            | Japan   | 07/18/2008  | 08/10/2012 | DATA CONVERSION APPARATUS, METHOD, AND COMPUTER-<br>READABLE RECORDING MEDIUM ...                               |
| 5136328               | FMA13-00406JP            | Japan   | 09/26/2008  | 11/22/2012 | MEMORY, MEMORY OPERATING METHOD, AND MEMORY SYSTEM                                                              |
| 5272692               | FMA13-00407JP            | Japan   | 12/08/2008  | 05/24/2013 | SEMICONDUCTOR INTEGRATED CIRCUIT AND POWER SUPPLY<br>DEVICE                                                     |
| 5115628               | FMA13-00408JP            | Japan   | 11/13/2008  | 10/26/2012 | MICROCOMPUTER                                                                                                   |
| 5126010               | FMA13-00409JP            | Japan   | 11/14/2008  | 11/09/2012 | MEMORY ACCESS CONTROL CIRCUIT AND IMAGE PROCESSING<br>SYSTEM                                                    |
| 3799050               | FMA13-0040JP             | Japan   | 03/31/2005  | 04/28/2006 | THE CACHE MEMORY APPARATUS AND METHOD WHICH STORES THE<br>HIERARCHIZED MEMORY ITEM AND CASH                     |
| 3709235               | FMA13-0040US             | Japan   | 03/14/1996  | 08/12/2005 | THE CACHE MEMORY APPARATUS AND METHOD WHICH STORES THE<br>HIERARCHIZED MEMORY ITEM AND CASH                     |
| 5239647               | FMA13-00410JP            | Japan   | 09/01/2008  | 04/12/2013 | A verification assistance program, a verification assistance apparatus, and a<br>verification assistance method |
| 5315981               | FMA13-00411JP            | Japan   | 12/24/2008  | 07/19/2013 | CURRENT PRODUCING CIRCUIT, CURRENT PRODUCING METHOD,<br>AND ELECTRONIC DEVICE                                   |
| 5315982               | FMA13-00412JP            | Japan   | 12/24/2008  | 07/19/2013 | CONTROL CIRCUIT OF DC-DC CONVERTER, DC-DC CONVERTER AND<br>ELECTRONIC DEVICE                                    |
| 2008-3263323          | FMA13-00413JP            | Japan   | 12/22/2008  |            | CONTROL METHOD OF NETWORK AND INTERFACE APPARATUS                                                               |
| 5287291               | FMA13-00414JP            | Japan   | 01/26/2009  | 06/14/2013 | SUCCESSIVE APPROXIMATION A/D CONVERTER                                                                          |
| 5347761               | FMA13-00415JP            | Japan   | 06/29/2009  | 08/30/2013 | A NETWORK CONTROL METHOD AND INTERFACE APPARATUS                                                                |
| 5326551               | FMA13-00416JP DIV        | Japan   | 12/23/2008  | 08/02/2013 | POWER SUPPLY APPARATUS AND POWER SUPPLY METHOD                                                                  |
| 5376512               | FMA13-00417JP            | Japan   | 05/21/2009  | 10/04/2013 | POWER SUPPLY DEVICE                                                                                             |
| 5366127               | FMA13-00417US            | Japan   | 11/28/2008  | 09/20/2013 | ANALOG INTEGRATED CIRCUIT (AS AMENDED)                                                                          |
| 5370991               | FMA13-00418JP            | Japan   | 01/23/2009  | 09/27/2013 | COMMUNICATION APPARATUS AND COMMUNICATION SYSTEM                                                                |
| 5370989               | FMA13-00418US            | Japan   | 12/18/2008  | 09/27/2013 | COMMUNICATION APPARATUS, DATA COMMUNICATION METHOD, AND<br>NETWORK SYSTEM                                       |
| 5251541               | FMA13-00419JP            | Japan   | 01/26/2009  | 04/26/2013 | CONSTANT-VOLTAGE GENERATION CIRCUIT AND REGULATOR<br>CIRCUIT                                                    |
| 3625572               | FMA13-0041US             | Japan   | 05/21/1996  | 12/10/2004 | AN OSCILLATION CIRCUIT AND A PLL CIRCUIT USING THE SAME                                                         |
| 5376509               | FMA13-00420US<br>CON     | Japan   | 03/16/2009  | 10/04/2013 | The run history trace method                                                                                    |
| 5553479               | FMA13-00421JP            | Japan   | 02/18/2008  | 06/06/2014 | SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD<br>THEREOF                                                    |
| 5400443               | FMA13-00421US<br>CON     | Japan   | 03/25/2009  | 11/01/2013 | INTEGRATED CIRCUIT, DEBUGGING CIRCUIT, AND DEBUGGING<br>COMMAND CONTROL METHOD                                  |
| 5431003               | FMA13-00422US            | Japan   | 04/03/2009  | 12/13/2013 | A reconfigurable circuit and a reconfigurable circuit system                                                    |
| 5599987               | FMA13-00423US            | Japan   | 06/12/2009  | 08/22/2014 | AUXILIARY PE FOR MULTIPLEXING AND SEMICONDUCTOR<br>INTEGRATED CIRCUIT                                           |
| 5169773               | FMA13-00424JP            | Japan   | 11/27/2008  | 01/11/2013 | SEMICONDUCTOR MEMORY AND METHOD AND SYSTEM FOR<br>ACTUATING ...                                                 |
| 5098984               | FMA13-00425US            | Japan   | 12/10/2008  | 10/05/2012 | INTERFACE APPARATUS AND RESYNCHRONIZATION METHOD                                                                |
| 5198316               | FMA13-00426JP            | Japan   | 02/19/2009  | 02/15/2013 | PLL CIRCUIT AND OSCILLATION DEVICE                                                                              |
| 5115472               | FMA13-00427JP            | Japan   | 12/26/2008  | 10/26/2012 | ASK DEMODULATION CIRCUIT                                                                                        |
| 5239912               | FMA13-00428JP            | Japan   | 01/30/2009  | 04/12/2013 | SQUARE CIRCUIT                                                                                                  |
| 5310078               | FMA13-00429JP            | Japan   | 02/23/2009  | 07/12/2013 | IMAGE DEPICTION APPARATUS                                                                                       |
| 3647147               | FMA13-0042FR DIV         | Japan   | 06/28/1996  | 02/18/2005 | AN OSCILLATION CIRCUIT AND A PLL CIRCUIT USING THE SAME                                                         |
| 2009-113914           | FMA13-00430JP            | Japan   | 05/08/2009  |            | CLOCK GENERATING CIRCUIT, POWER SUPPLY SYSTEM AND CLOCK<br>SIGNAL FREQUENCY CHANGING METHOD                     |
| 5310079               | FMA13-00431JP            | Japan   | 02/24/2009  | 07/12/2013 | IMAGE DEPICTION APPARATUS                                                                                       |
| 5399734               | FMA13-00432CN            | Japan   | 09/30/2008  | 11/01/2013 | OUTPUT-VOLTAGE CONTROL APPARATUS, OUTPUT-VOLTAGE<br>CONTROL METHOD, AND ELECTRONIC EQUIPMENT                    |
| 2013-221507           | FMA13-00432JP DIV        | Japan   | 02/18/2009  |            | OUTPUT-VOLTAGE CONTROL APPARATUS, OUTPUT-VOLTAGE<br>CONTROL METHOD, AND ELECTRONIC EQUIPMENT                    |
| 5395562               | FMA13-00432JP<br>DIV2    | Japan   | 08/06/2009  | 10/25/2013 | SLAVE CONTROL APPARATUS, COMMUNICATION CONTROL SYTEM<br>AND COMMUNICATION CONTROL METHOD                        |
| 5206594               | FMA13-00433US DIV        | Japan   | 06/05/2009  | 03/01/2013 | A voltage adjustment circuit and a display apparatus drive circuit                                              |
| 5359610               | FMA13-00434US            | Japan   | 06/29/2009  | 09/13/2013 | A transmitting/receiving apparatus and a power wire communication method                                        |
| 5519195               | FMA13-00435US            | Japan   | 06/19/2009  | 04/11/2014 | A timing controller, a timing control method, and a timing control system                                       |
| 5347748               | FMA13-00436US            | Japan   | 06/18/2009  | 08/30/2013 | The control method of a DC/DC converter and a DC/DC converter                                                   |
| 5553540               | FMA13-00437JP            | Japan   | 06/24/2009  | 06/06/2014 | DRIVER CIRCUIT AND CONTROL CIRCUIT                                                                              |
| 2013-226606           | FMA13-00438JP            | Japan   | 05/08/2009  |            | POWER SUPPLY DEVICE, CONTROL CIRCUIT, AND METHOD OF<br>CONTROLLING POWER SUPPLY DEVICE                          |
| 5566626               | FMA13-00438JP DIV        | Japan   | 05/19/2009  | 06/27/2014 | The network connection method and interface apparatus                                                           |
| 5405891               | FMA13-00438US            | Japan   | 05/08/2009  | 11/08/2013 | POWER SUPPLY DEVICE, CONTROL CIRCUIT, AND METHOD OF<br>CONTROLLING POWER SUPPLY DEVICE                          |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                             |
|-----------------------|---------------------------|---------|-------------|------------|-----------------------------------------------------------------------------------------------------------------------------------|
| 5332675               | FMA13-00439JP DIV         | Japan   | 02/06/2009  | 08/09/2013 | ELECTRONIC DEVICE, DETECTION CIRCUIT AND VOLTAGE CONTROL METHOD                                                                   |
| 3291198               | FMA13-0043EP              | Japan   | 05/08/1996  | 03/22/2002 | SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                                  |
| 3601711               | FMA13-0043JP              | Japan   | 05/08/1996  | 10/01/2004 | SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                                  |
| 5634028               | FMA13-00440US             | Japan   | 03/05/2009  | 10/24/2014 | DC-DC CONVERTER CONTROL CIRCUIT, DC-DC CONVERTER, AND METHOD FOR CONTROLLING A DC-DC CONVERTER                                    |
| 5451205               | FMA13-00441JP             | Japan   | 06/23/2009  | 01/10/2014 | SEMICONDUCTOR DEVICE                                                                                                              |
| 5529450               | FMA13-00442US             | Japan   | 07/15/2009  | 04/25/2014 | A body bias control circuit and a body bias control method                                                                        |
| 5466026               | FMA13-00443JP             | Japan   | 01/27/2010  | 01/31/2014 | THE CONTROL METHOD OF A PHASE LOCKED LOOP CIRCUIT AND A PHASE LOCKED LOOP CIRCUIT                                                 |
| 5486221               | FMA13-00443US             | Japan   | 06/23/2009  | 02/28/2014 | CONTROL CIRCUIT FOR DC-DC CONVERTERS, DC-DC CONVERTER, AND ELECTRONIC DEVICE                                                      |
| 2009-069184           | FMA13-00445JP DIV         | Japan   | 06/09/2008  |            | DC-DC CONVERTER CONTROL CIRCUIT AND DC-DC CONVERTER CONTROL METHOD                                                                |
| 2009-151161           | FMA13-00446US             | Japan   | 06/25/2009  |            | COMPUTER SYSTEM INCLUDING RECONFIGURABLE ARITHMETIC DEVICE, AND RECONFIGURABLE ARITHMETIC DEVICE                                  |
| 4146006               | FMA13-00448EP             | Japan   | 09/28/1998  | 06/27/2008 | THE ELECTRONIC DEVICE WHICH HAS FLASH MEMORY                                                                                      |
| 4421659               | FMA13-00448JP             | Japan   | 05/26/2008  | 12/11/2009 | ELECTRONIC APPARATUS HAVING FLASH MEMORY                                                                                          |
| 4741632               | FMA13-00449JP             | Japan   | 04/27/2001  | 05/13/2011 | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                                                                                           |
| 2001-133036           | FMA13-00449US             | Japan   | 04/27/2001  |            | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                                                                                           |
| 3653892               | FMA13-0044US              | Japan   | 11/21/1996  | 03/11/2005 | FRACTIONAL N-FREQUENCY SYNTHESIZER                                                                                                |
| 5012731               | FMA13-00450JP             | Japan   | 08/18/2008  | 06/15/2012 | THE ADJUSTMENT METHOD OF A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                  |
| 2003-192151           | FMA13-00450US CON         | Japan   | 08/28/2002  |            | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND METHOD OF ADJUSTING SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                           |
| 5316148               | FMA13-00453JP             | Japan   | 03/24/2009  | 07/19/2013 | Information processing apparatus and a data recovery method                                                                       |
| 5240015               | FMA13-00454JP             | Japan   | 04/01/2009  | 04/12/2013 | VIDEO DATA COMMUNICATION SYSTEM                                                                                                   |
| 5528733               | FMA13-00455JP             | Japan   | 07/08/2009  | 04/25/2014 | DRIVER CIRCUIT AND ADJUSTMENT METHOD THEREFOR                                                                                     |
| 5686913               | FMA13-00455JP DIV         | Japan   | 07/08/2009  | 01/30/2015 | DRIVER CIRCUIT AND ADJUSTMENT METHOD THEREFOR                                                                                     |
| 5438378               | FMA13-00456JP             | Japan   | 05/20/2009  | 12/20/2013 | COMMUNICATION APPARATUS, SEMICONDUCTOR DEVICE AND COMMUNICATION SYSTEM                                                            |
| 5451123               | FMA13-00459JP             | Japan   | 03/17/2009  | 01/10/2014 | POWER SUPPLY APPARATUS, POWER CONTROL APPARATUS AND CONTROL METHOD OF POWER SUPPLY                                                |
| 3699536               | FMA13-0045JP              | Japan   | 07/02/1996  | 07/15/2005 | A data transmission apparatus and the data-transmission method                                                                    |
| 5376516               | FMA13-00462JP             | Japan   | 07/27/2009  | 10/04/2013 | SEMICONDUCTOR DEVICE                                                                                                              |
| 2009-293178           | FMA13-00463JP             | Japan   | 12/24/2009  |            | OSCILLATING APPARATUS                                                                                                             |
| 2010-047339           | FMA13-00465JP             | Japan   | 03/04/2010  |            | ANALYSIS SYSTEM AND SEMICONDUCTOR DEVICE                                                                                          |
| 5442380               | FMA13-00465US             | Japan   | 09/29/2009  | 12/27/2013 | A STEP-UP CIRCUIT AND A SEMICONDUCTOR MEMORY                                                                                      |
| 5316299               | FMA13-00466JP             | Japan   | 08/07/2009  | 07/19/2013 | SEMICONDUCTOR MEMORY, SYSTEM, AND METHOD OF CONTROLLING ...                                                                       |
| 5353548               | FMA13-00467JP             | Japan   | 08/14/2009  | 09/06/2013 | BAND GAP REFERENCE CIRCUIT                                                                                                        |
| 5359810               | FMA13-00467JP             | Japan   | 11/19/2009  | 09/13/2013 | SEMICONDUCTOR DEVICE AND RADIO COMMUNICATION APPARATUS                                                                            |
| 5304505               | FMA13-00468JP             | Japan   | 07/21/2009  | 07/05/2013 | SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                                  |
| 5576078               | FMA13-00469JP             | Japan   | 09/10/2009  | 07/11/2014 | DC-DC-CONVERTER CONTROL CIRCUIT                                                                                                   |
| 3237554               | FMA13-0046JP              | Japan   | 12/27/1996  | 10/05/2001 | Conversational mode debugging apparatus                                                                                           |
| 2009-176644           | FMA13-00470JP             | Japan   | 07/29/2009  |            | DC-DC CONVERTER, CONTROL CIRCUIT AND POWER SUPPLY VOLTAGE CONTROL METHOD                                                          |
| 2009-174625           | FMA13-00471CN             | Japan   | 07/27/2009  |            | OUTPUT VOLTAGE CONTROLLER, ELECTRONIC DEVICE, AND OUTPUT VOLTAGE CONTROL METHOD                                                   |
| 5400167               | FMA13-00472GB             | Japan   | 11/11/2008  | 11/01/2013 | The method to detect the operating state of an electric stepper motor                                                             |
| 5321343               | FMA13-00473JP             | Japan   | 08/13/2009  | 07/26/2013 | CONNECTER DETECTION CIRCUIT                                                                                                       |
| 5427663               | FMA13-00474JP             | Japan   | 03/24/2010  | 12/06/2013 | ANALOG-TO-DIGITAL CONVERTER                                                                                                       |
| 5623618               | FMA13-00474JP DIV         | Japan   | 03/24/2010  | 10/03/2014 | ANALOG-TO-DIGITAL CONVERTER                                                                                                       |
| 2010-036110           | FMA13-00476JP             | Japan   | 02/22/2010  |            | SEMICONDUCTOR MEMORY AND SYSTEM                                                                                                   |
| 5607963               | FMA13-00477US             | Japan   | 03/19/2010  | 09/05/2014 | REFERENCE VOLTAGE CIRCUIT AND SEMICONDUCTOR INTEGRATED CIRCUIT                                                                    |
| 5553927               | FMA13-00478JP             | Japan   | 07/19/2009  | 06/06/2014 | SEMICONDUCTOR DEVICE AND WIRELESS COMMUNICATION APPARATUS                                                                         |
| 5590934               | FMA13-00479JP             | Japan   | 03/24/2010  | 08/08/2014 | CONTROL CIRCUIT FOR SWITCHING POWER SUPPLY AND ELECTRONIC DEVICE                                                                  |
| 3596172               | FMA13-0047JP              | Japan   | 06/19/1996  | 09/17/2004 | PLL FREQUENCY SYNTHESIZER                                                                                                         |
| 5484037               | FMA13-00480US             | Japan   | 12/24/2009  | 02/28/2014 | DATA TRANSMISSION METHOD, DATA TRANSMITTING APPARATUS, AND NETWORK SYSTEM                                                         |
| 5537192               | FMA13-00481US             | Japan   | 03/04/2010  | 05/09/2014 | RECEIVING APPARATUS AND METHOD FOR SETTING GAIN                                                                                   |
| 5711889               | FMA13-00482US             | Japan   | 01/27/2010  | 03/13/2015 | RECONFIGURABLE CIRCUIT AND SEMICONDUCTOR INTEGRATED CIRCUIT                                                                       |
| 5632651               | FMA13-00483US             | Japan   | 05/19/2010  | 10/17/2014 | SEMICONDUCTOR CIRCUIT AND DESIGNING DEVICE                                                                                        |
| 2011-005018           | FMA13-00485JP             | Japan   | 01/13/2011  |            | DESIGN SUPPORT DEVICE AND DESIGN SUPPORT METHOD                                                                                   |
| 5507980               | FMA13-00486US             | Japan   | 11/27/2009  | 03/28/2014 | THE CONTROL CIRCUIT OF A SWITCHED-MODE POWER SUPPLY, AN ELECTRONIC DEVICE, AND THE CONTROL METHOD OF A SWITCHED-MODE POWER SUPPLY |
| 2014-106692           | FMA13-00487JP             | Japan   | 04/01/2010  |            | SYSTEM AND METHOD FOR TRANSFERRING DATA                                                                                           |
| 2010-085270           | FMA13-00487JP DIV         | Japan   | 04/01/2010  |            | APPARATUS AND METHOD FOR TRANSFERRING DATA                                                                                        |
| 2010-044211           | FMA13-00488JP             | Japan   | 03/01/2010  |            | PLL CIRCUIT                                                                                                                       |
| 5438567               | FMA13-00489JP             | Japan   | 03/19/2010  | 12/20/2013 | OSCILLATOR CIRCUIT                                                                                                                |
| 3560438               | FMA13-0048US              | Japan   | 03/14/1997  | 06/04/2004 | A STEP-UP CIRCUIT AND A STEP-DOWN CIRCUIT                                                                                         |
| 5501074               | FMA13-00490JP             | Japan   | 04/01/2010  | 03/20/2014 | RECONFIGURABLE CIRCUIT, AND METHOD OF DRIVING THE SAME                                                                            |
| 5645466               | FMA13-00492JP             | Japan   | 05/07/2010  | 11/14/2014 | The control circuit and electronic device of a power supply                                                                       |
| 5456495               | FMA13-00493US             | Japan   | 01/19/2010  | 01/17/2014 | CONTROL CIRCUIT AND METHOD FOR SWITCHING SUPPLY AND SWITCHING SUPPLY                                                              |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                  |
|-----------------------|---------------------------|---------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2010-127653           | FMA13-00494US<br>CON      | Japan   | 06/03/2010  |            | SEMICONDUCTOR INTEGRATED CIRCUIT, METHOD OF<br>SEMICONDUCTOR CIRCUIT OPERATION AND DEBUG SYSTEM                                                        |
| 2010-105879           | FMA13-00495JP             | Japan   | 04/30/2010  |            | POWER SOURCE CIRCUIT                                                                                                                                   |
| 2014-137695           | FMA13-00496JP             | Japan   | 03/31/2010  |            | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                                                                                                                |
| 5456457               | FMA13-00496JP DIV         | Japan   | 12/24/2009  | 01/17/2014 | A PROGRAM DEVELOPMENT SUPPORT APPARATUS AND A<br>PROGRAM DEVELOPMENT ASSISTANCE METHOD                                                                 |
| 2010-081152           | FMA13-00496US             | Japan   | 03/31/2010  |            | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                                                                                                                |
| 5045692               | FMA13-00497JP DIV         | Japan   | 02/06/2009  | 07/27/2012 | OPERATION MODE CONTROL CIRCUIT AND A MICROCOMPUTER                                                                                                     |
| 4294503               | FMA13-00497US             | Japan   | 01/26/2004  | 04/17/2009 | A MICROCOMPUTER INCLUDING AN OPERATION MODE CONTROL<br>CIRCUIT AND AN OPERATION MODE CONTROL CIRCUIT AND THE<br>CONTROL SYSTEM USING THE MICROCOMPUTER |
| 5003740               | FMA13-00498JP             | Japan   | 10/02/2009  | 06/01/2012 | DETECTION CIRCUIT                                                                                                                                      |
| 4455201               | FMA13-00498US DIV         | Japan   | 07/20/2004  | 02/12/2010 | DETECTION CIRCUIT                                                                                                                                      |
| 4924701               | FMA13-00499JP             | Japan   | 11/17/2004  | 02/17/2012 | RESET CONTROL CIRCUIT AND RESET CONTROL METHOD                                                                                                         |
| 4437541               | FMA13-00499US             | Japan   | 11/17/2004  | 01/15/2010 | RESET CONTROL CIRCUIT AND RESET CONTROL METHOD                                                                                                         |
| 3687217               | FMA13-0049JP              | Japan   | 09/17/1996  | 06/17/2005 | SEMICONDUCTOR DEVICE                                                                                                                                   |
| 5539776               | FMA13-00500JP             | Japan   | 03/31/2010  | 05/09/2014 | SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                                                       |
| 5520098               | FMA13-00501US             | Japan   | 03/24/2010  | 04/11/2014 | DATA-PROCESSING METHOD, PROGRAM, AND SYSTEM                                                                                                            |
| 2010-096089           | FMA13-00502US<br>CON      | Japan   | 04/19/2010  |            | DATA WRITING METHOD AND SYSTEM                                                                                                                         |
| 5343916               | FMA13-00503GB             | Japan   | 04/16/2010  | 08/23/2013 | SEMICONDUCTOR MEMORY                                                                                                                                   |
| 5519837               | FMA13-00503JP             | Japan   | 06/27/2013  | 04/11/2014 | SEMICONDUCTOR MEMORY                                                                                                                                   |
| 5542234               | FMA13-00503JP DIV         | Japan   | 06/27/2013  | 05/16/2014 | SEMICONDUCTOR MEMORY                                                                                                                                   |
| 2014-095405           | FMA13-00503JP<br>DIV1     | Japan   | 04/16/2010  |            | SEMICONDUCTOR MEMORY                                                                                                                                   |
| 5437174               | FMA13-00504JP             | Japan   | 06/16/2010  | 12/20/2013 | LED DRIVING CIRCUIT, AND SEMICONDUCTOR DEVICE                                                                                                          |
| 5629219               | FMA13-00505US             | Japan   | 01/13/2011  | 10/10/2014 | COMMUNICATION DEVICE, COMMUNICATION SYSTEM, AND<br>COMMUNICATION METHOD                                                                                |
| 5620718               | FMA13-00506JP             | Japan   | 06/07/2010  | 09/26/2014 | INTEGRATED CIRCUIT DEVICE WITH VOLTAGE REGULATOR                                                                                                       |
| 2014-191979           | FMA13-00506JP Div         | Japan   | 06/07/2010  |            | INTEGRATED CIRCUIT DEVICE WITH VOLTAGE REGULATOR                                                                                                       |
| 2010-094293           | FMA13-00507JP             | Japan   | 04/15/2010  |            | CONTROL CIRCUIT AND CONTROL METHOD OF SWITCHING POWER<br>SOURCE                                                                                        |
| 5662119               | FMA13-00508EP             | Japan   | 11/29/2010  | 12/12/2014 | A node system and the monitoring node                                                                                                                  |
| 5567389               | FMA13-00509JP             | Japan   | 05/17/2010  | 06/27/2014 | CLOCK GENERATION CIRCUIT                                                                                                                               |
| 3851404               | FMA13-0050JP              | Japan   | 03/13/1997  | 09/08/2006 | DIFFERENTIAL AMPLIFIER CIRCUIT                                                                                                                         |
| 5636235               | FMA13-00510JP DIV         | Japan   | 09/21/2010  | 10/24/2014 | DC-DC CONVERTER                                                                                                                                        |
| 5451541               | FMA13-00511CN             | Japan   | 06/28/2010  | 01/10/2014 | OSCILLATION CIRCUIT                                                                                                                                    |
| 2011-037832           | FMA13-00512JP             | Japan   | 02/24/2011  |            | PLL                                                                                                                                                    |
| 5511594               | FMA13-00514JP             | Japan   | 08/31/2010  | 04/04/2014 | OUTPUT SWITCHING CIRCUIT                                                                                                                               |
| 5676961               | FMA13-00515US             | Japan   | 07/30/2010  | 01/09/2015 | CONTROL CIRCUIT OF POWER SOURCE, ELECTRONIC APPARATUS,<br>AND CONTROL METHOD OF POWER SOURCE                                                           |
| 2010-233213           | FMA13-00516CN             | Japan   | 10/18/2010  |            | SWITCHING REGULATOR                                                                                                                                    |
| 2010-197530           | FMA13-00517CN             | Japan   | 09/03/2010  |            | SWITCHING REGULATOR                                                                                                                                    |
| 2011-011243           | FMA13-00518CN             | Japan   | 01/21/2011  |            | SEMICONDUCTOR DEVICE                                                                                                                                   |
| 5634236               | FMA13-00519CN             | Japan   | 11/30/2010  | 10/24/2014 | LEVEL SHIFT CIRCUIT AND SEMICONDUCTOR DEVICE                                                                                                           |
| 5551958               | FMA13-00519JP             | Japan   | 04/01/2010  | 05/30/2014 | SYSTEM AND METHOD FOR TRANSFERRING DATA                                                                                                                |
| 3705880               | FMA13-0051EP              | Japan   | 11/28/1996  | 08/05/2005 | LEVEL CONVERTER AND SEMICONDUCTOR DEVICE                                                                                                               |
| 5702573               | FMA13-00520US             | Japan   | 10/20/2010  | 02/27/2015 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND DATA<br>WRITING METHOD THEREOF                                                                             |
| 2011-028878           | FMA13-00521JP             | Japan   | 02/14/2011  |            | ELECTRONIC DEVICE, CONTROL CIRCUIT AND METHOD FOR<br>CONTROLLING LIGHT-EMITTING ELEMENT                                                                |
| 2010-254099           | FMA13-00522JP             | Japan   | 11/12/2010  |            | SEMICONDUCTOR DEVICE AND METHOD FOR RESET CONTROL OF<br>THE SAME                                                                                       |
| 5618805               | FMA13-00523US<br>CON      | Japan   | 12/10/2010  | 09/26/2014 | COMMUNICATION DEVICE, NETWORK SYSTEM, AND COMMUNICATION<br>METHOD                                                                                      |
| 2011-036712           | FMA13-00524JP             | Japan   | 02/23/2011  |            | REFERENCE VOLTAGE CIRCUIT AND SEMICONDUCTOR INTEGRATED<br>CIRCUIT                                                                                      |
| 2011-042267           | FMA13-00525JP             | Japan   | 02/28/2011  |            | MOTOR CONTROL APPARATUS, PROGRAM FOR MANUFACTURING<br>MOTOR CONTROL APPARATUS, AND METHOD FOR MANUFACTURING<br>MOTOR CONTROL APPARATUS                 |
| 2011-037678           | FMA13-00526JP             | Japan   | 02/23/2011  |            | CONTROL CIRCUIT, ELECTRONIC DEVICE, AND METHOD FOR<br>CONTROLLING POWER SUPPLY                                                                         |
| 2011-148214           | FMA13-00527JP             | Japan   | 07/04/2011  |            | MICROCOMPUTER                                                                                                                                          |
| 2011-122815           | FMA13-00528CN             | Japan   | 05/31/2011  |            | POWER SUPPLY DEVICE, CONTROL CIRCUIT, ELECTRONIC DEVICE<br>AND CONTROL METHOD FOR POWER SUPPLY                                                         |
| 2011-191481           | FMA13-00529CN             | Japan   | 09/02/2011  |            | ANALOG-TO-DIGITAL CONVERTER                                                                                                                            |
| 3711691               | FMA13-0052JP              | Japan   | 04/11/1997  | 08/26/2005 | MICROCONTROLLER                                                                                                                                        |
| 2011-142061           | FMA13-00530JP             | Japan   | 06/27/2011  |            | PROCESSOR AND METHOD FOR OPERATING THE SAME                                                                                                            |
| 2011-173233           | FMA13-00531CN             | Japan   | 08/08/2011  |            | SEMICONDUCTOR DEVICE AND VOLTAGE DIVIDER                                                                                                               |
| 2011-180456           | FMA13-00532JP             | Japan   | 08/22/2011  |            | PROCESSOR                                                                                                                                              |
| 4876624               | FMA13-00533CN             | Japan   | 02/22/2006  | 12/09/2011 | POWER SOURCE CONTROL CIRCUIT, POWER SUPPLY DEVICE, AND<br>CONTROL METHOD FOR THE SAME                                                                  |
| 5170285               | FMA13-00533JP             | Japan   | 05/27/2011  | 01/11/2013 | POWER SUPPLY CONTROL CIRCUIT, POWER SUPPLY DEVICE ...                                                                                                  |
| 5360153               | FMA13-00534JP             | Japan   | 07/29/2011  | 09/13/2013 | SURGE DETECTION CIRCUIT FOR SENSOR                                                                                                                     |
| 5506281               | FMA13-00534JP DIV         | Japan   | 08/17/2009  | 03/28/2014 | POWER SUPPLY CIRCUIT AND ELECTRONIC DEVICE                                                                                                             |
| 4893008               | FMA13-00534US             | Japan   | 02/08/2006  | 01/06/2012 | SURGE DETECTION CIRCUIT                                                                                                                                |
| 4463369               | FMA13-00535US             | Japan   | 02/24/2000  | 02/26/2010 | THE CONTROL CIRCUIT OF A DC-DC CONVERTER, AND A DC-DC<br>CONVERTER                                                                                     |
| 3681624               | FMA13-00536US             | Japan   | 08/31/2000  | 05/27/2005 | A CHARGING CIRCUIT, A CHARGING -AND-DISCHARGING CIRCUIT,<br>AND A BATTERY PACK                                                                         |
| 4073152               | FMA13-00537US<br>CON      | Japan   | 06/30/2000  | 02/01/2008 | VARIABLE-GAIN AMPLIFIER                                                                                                                                |

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| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                                 |
|-----------------------|--------------------------|---------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4629192               | FMA13-00538US            | Japan   | 07/07/2000  | 11/19/2010 | TRIMMING CIRCUIT OF SEMICONDUCTOR APPARATUS                                                                                                                                           |
| 4651832               | FMA13-00539EP            | Japan   | 03/05/2001  | 12/24/2010 | OVERVOLTAGE-PROTECTIVE DEVICE FOR POWER SYSTEM, AC/DC<br>CONVERTER AND DC/DC CONVERTER CONSTITUTING THE POWER<br>SYSTEM                                                               |
| 3937505               | FMA13-0053JP             | Japan   | 05/06/1997  | 04/06/2007 | SEMICONDUCTOR DEVICE                                                                                                                                                                  |
| 4287039               | FMA13-00540DE            | Japan   | 12/19/2000  | 04/03/2009 | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE WITH VARIABLE<br>GAIN AMPLIFIER                                                                                                               |
| 4850344               | FMA13-00541US            | Japan   | 03/05/2001  | 10/28/2011 | THE CONTROL CIRCUIT OF A DC-DC CONVERTER, AND A DC-DC<br>CONVERTER                                                                                                                    |
| 11-88383              | FMA13-00542US            | Japan   | 03/30/1999  |            | RESET CIRCUIT AND PLL FREQUENCY SYNTHESIZER                                                                                                                                           |
| 3930729               | FMA13-00543JP            | Japan   | 11/30/2001  | 03/16/2007 | SEMICONDUCTOR DEVICE AND FLAT PANEL DISPLAY DEVICE USING<br>THE SAME, AND DATA DRIVER THEREFOR                                                                                        |
| 2001-89880            | FMA13-00544JP            | Japan   | 03/27/2001  |            | MODE SWITCHING METHOD FOR PLL CIRCUIT AND MODE CONTROL<br>CIRCUIT FOR THE PLL CIRCUIT                                                                                                 |
| 4817539               | FMA13-00545JP            | Japan   | 06/19/2001  | 09/09/2011 | A SIGNAL DETECTION APPARATUS, THE SIGNAL DETECTION METHOD,<br>A SIGNAL-TRANSMISSION SYSTEM, AND A COMPUTER-READABLE<br>PROGRAM                                                        |
| 2001-185309           | FMA13-00545US DIV        | Japan   | 06/19/2001  |            | DIFFERENTIAL SIGNAL OUTPUTTING DEVICE, SEMICONDUCTOR<br>INTEGRATED CIRCUIT DEVICE HAVING THE DIFFERENTIAL SIGNAL<br>OUTPUTTING DEVICE, AND DIFFERENTIAL SIGNAL TRANSMITTING<br>SYSTEM |
| 4091410               | FMA13-00547US            | Japan   | 12/05/2002  | 03/07/2008 | SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                                                                                      |
| 4080396               | FMA13-00548US            | Japan   | 08/08/2003  | 02/15/2008 | A DC/DC CONVERTER, A SEMICONDUCTOR DEVICE, AND<br>ELECTRONIC DEVICE, AND A BATTERY PACK                                                                                               |
| 4124768               | FMA13-00549US            | Japan   | 04/18/2003  | 05/16/2008 | CONSTANT-VOLTAGE POWER SUPPLY CIRCUIT                                                                                                                                                 |
| 3652830               | FMA13-0054JP             | Japan   | 01/31/1997  | 03/04/2005 | DC-DC CONVERTER                                                                                                                                                                       |
| 2005-62660            | FMA13-00550JP            | Japan   | 03/07/2005  |            | SEMICONDUCTOR INTEGRATED CIRCUIT AND RESET CANCELING<br>METHOD OF THE SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                |
| 3888895               | FMA13-00551EP            | Japan   | 12/21/2001  | 12/08/2006 | A POSITIVE-AND/OR- NEGATIVE POWER-SUPPLY GENERATOR AND A<br>SEMICONDUCTOR DEVICE                                                                                                      |
| 2005-369586           | FMA13-00552EP            | Japan   | 12/22/2005  |            | ANALOG MULTIPLE STAGE AMPLIFYING CIRCUIT FOR SENSOR                                                                                                                                   |
| 4328319               | FMA13-00553US            | Japan   | 08/02/2005  | 06/19/2009 | CLOCK SUPPLY CIRCUIT AND METHOD                                                                                                                                                       |
| 4731309               | FMA13-00554US            | Japan   | 12/20/2005  | 04/28/2011 | DC-DC CONVERTER CONTROL CIRCUIT AND DC-DC CONVERTER<br>CONTROL METHOD                                                                                                                 |
| 4646840               | FMA13-00555US            | Japan   | 03/22/2006  | 12/17/2010 | PARALLEL PROCESSING APPARATUS DYNAMICALLY SWITCHING<br>OVER CIRCUIT CONFIGURATION                                                                                                     |
| 4716895               | FMA13-00556CN            | Japan   | 02/22/2006  | 04/08/2011 | DC LINEAR REGULATOR SINGLE CONTROLLER WITH PLURAL LOADS                                                                                                                               |
| 5061593               | FMA13-00557US CIP        | Japan   | 11/21/2006  | 08/17/2012 | CONTROL APPARATUS, SEMICONDUCTOR INTEGRATED CIRCUIT<br>APPARATUS, AND SOURCE VOLTAGE SUPPLY CONTROL SYSTEM                                                                            |
| 2004-95696            | FMA13-00558US            | Japan   | 03/29/2004  |            | MICROCOMPUTER WHOSE INTERNAL MEMORY CAN BE MONITORED                                                                                                                                  |
| 2005-007546           | FMA13-00559US            | Japan   | 01/14/2005  |            | MICROCONTROLLER                                                                                                                                                                       |
| 3847401               | FMA13-0055JP             | Japan   | 02/26/1997  | 09/01/2006 | SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                                                                                      |
| 4879043               | FMA13-00560JP            | Japan   | 02/22/2007  | 12/09/2011 | AD CONVERTER CIRCUIT AND MICROCONTROLLER                                                                                                                                              |
| 4837408               | FMA13-00561CN            | Japan   | 03/20/2006  | 10/07/2011 | CIRCUIT AND METHOD FOR CONTROLLING DC-DC CONVERTER                                                                                                                                    |
| 5404991               | FMA13-00562CN            | Japan   | 02/07/2006  | 11/08/2013 | CONTROL CIRCUIT FOR DC-DC CONVERTER, DC-DC CONVERTER,<br>AND CONTROL METHOD FOR DC-DC CONVERTER                                                                                       |
| 4484839               | FMA13-00563JP            | Japan   | 03/30/2006  | 04/02/2010 | CONTROL CIRCUIT OF POWER SUPPLY AND CONTROL METHOD OF<br>THE POWER SUPPLY                                                                                                             |
| 4800808               | FMA13-00564JP            | Japan   | 03/24/2006  | 08/12/2011 | ELECTRONIC DEVICE INCORPORATING SYSTEM POWER SUPPLY UNIT<br>AND METHOD FOR SUPPLYING POWER SUPPLY VOLTAGE                                                                             |
| 4984777               | FMA13-00565CN            | Japan   | 09/15/2006  | 05/11/2012 | POWER SUPPLY SYSTEM AND METHOD FOR CONTROLLING OUTPUT<br>VOLTAGE                                                                                                                      |
| 4887841               | FMA13-00566CN            | Japan   | 03/06/2006  | 12/22/2011 | DC-DC CONVERTER CONTROL CIRCUIT, DC-DC CONVERTER, POWER<br>SUPPLY UNIT, AND DC-DC CONVERTER CONTROL METHOD                                                                            |
| 4619252               | FMA13-00568US            | Japan   | 09/29/2005  | 11/05/2010 | ENHANCED PROCESSOR ELEMENT STRUCTURE IN A<br>RECONFIGURABLE INTEGRATED CIRCUIT DEVICE                                                                                                 |
| 4789662               | FMA13-00569CN            | Japan   | 03/17/2006  | 07/29/2011 | CONTROL CIRCUIT OF POWER SUPPLY, POWER SUPPLY AND<br>CONTROL METHOD THEREOF                                                                                                           |
| 3562189               | FMA13-0056JP             | Japan   | 01/16/1997  | 06/11/2004 | CHARGE PUMP CIRCUIT                                                                                                                                                                   |
| 4838009               | FMA13-00570EP            | Japan   | 02/22/2006  | 10/07/2011 | RECONFIGURABLE CIRCUIT                                                                                                                                                                |
| 2006-188631           | FMA13-00571JP            | Japan   | 07/07/2006  |            | PROGRAM ADJUSTING DEVICE AND PROGRAM ADJUSTING METHOD                                                                                                                                 |
| 5028967               | FMA13-00572JP            | Japan   | 11/15/2006  | 07/06/2012 | METHOD FOR CONTROLLING SEMICONDUCTOR MEMORY DEVICE                                                                                                                                    |
| 4642792               | FMA13-00573JP            | Japan   | 02/16/2007  | 12/10/2010 | POWER SUPPLY CIRCUIT, POWER SUPPLY CONTROL CIRCUIT, AND<br>POWER SUPPLY CONTROL METHOD                                                                                                |
| 2012-206381           | FMA13-00574JP            | Japan   | 09/19/2012  |            | ADJUSTING DEVICE AND ADJUSTING METHOD                                                                                                                                                 |
| 2013-109855           | FMA13-00575JP            | Japan   | 05/24/2013  |            | POWER SUPPLY DEVICE, CONTROL CIRCUIT, AND CONTROL METHOD                                                                                                                              |
| 2013-007357           | FMA13-00576JP            | Japan   | 01/18/2013  |            | SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                           |
| 2013-004919           | FMA13-00577JP            | Japan   | 01/15/2013  |            | CONTROL METHOD AND CONTROL DEVICE                                                                                                                                                     |
| 2013-037066           | FMA13-00578JP            | Japan   | 02/27/2013  |            | POWER SUPPLY DEVICE, POWER SUPPLY CONTROL CIRCUIT, AND<br>POWER SUPPLY CONTROL METHOD                                                                                                 |
| 2013-118836           | FMA13-00579JP            | Japan   | 06/05/2013  |            | RING OSCILLATOR                                                                                                                                                                       |
| 3627423               | FMA13-0057JP DIV         | Japan   | 03/28/1996  | 12/17/2004 | LOW-VOLTAGE PLL SEMICONDUCTOR DEVICE                                                                                                                                                  |
| 2013-122887           | FMA13-00580JP            | Japan   | 06/11/2013  |            | POWER SUPPLY CONTROL CIRCUIT, POWER SUPPLY DEVICE, AND<br>POWER SUPPLY CONTROL METHOD                                                                                                 |
| 2013-095769           | FMA13-00581JP            | Japan   | 04/30/2013  |            | CONTROL METHOD, CONTROL PROGRAM AND CONTROL DEVICE                                                                                                                                    |
| 2013-059666           | FMA13-00582JP            | Japan   | 03/22/2013  |            | SEMICONDUCTOR DEVICE AND ERASING METHOD THEREOF                                                                                                                                       |
| 2013-113039           | FMA13-00583JP            | Japan   | 05/29/2013  |            | MEMORY CIRCUIT                                                                                                                                                                        |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                               |
|-----------------------|---------------------------|---------|-------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 2013-117673           | FMA13-00584JP             | Japan   | 06/04/2013  |            | PLL CIRCUIT                                                                                                                                         |
| 2013-118587           | FMA13-00585JP             | Japan   | 06/05/2013  |            | SWITCHING REGULATOR                                                                                                                                 |
| 2013-101149           | FMA13-00586JP             | Japan   | 05/13/2013  |            | SEMICONDUCTOR MEMORY AND OPERATING METHOD THEREOF                                                                                                   |
| 2013-083875           | FMA13-00587JP             | Japan   | 04/12/2013  |            | MICROCOMPUTER FOR CONTROLLING ACTUATOR                                                                                                              |
| 2013-124047           | FMA13-00588JP             | Japan   | 06/12/2013  |            | SEMICONDUCTOR CIRCUIT, OSCILLATING CIRCUIT, AND POWER SUPPLY CIRCUIT                                                                                |
| 2013-112789           | FMA13-00589JP             | Japan   | 05/29/2013  |            | MICROCONTROLLER AND ERROR DETECTION METHOD                                                                                                          |
| 4015232               | FMA13-0058US              | Japan   | 07/25/1997  | 09/21/2007 | A PRE-SCALER, A FREQUENCY DIVIDER, AND A PLL CIRCUIT                                                                                                |
| 2013-062432           | FMA13-00590JP             | Japan   | 03/25/2013  |            | SERIAL COMMUNICATION SYSTEM, RECEIVING DEVICE, AND SERIAL COMMUNICATION METHOD                                                                      |
| 2013-106770           | FMA13-00591JP             | Japan   | 05/21/2013  |            | SUCCESSIVE-APPROXIMATION TYPE A/D CONVERTER AND DRIVING METHOD THEREOF                                                                              |
| 2013-119458           | FMA13-00592JP             | Japan   | 06/06/2013  |            | ELECTRIC CIRCUIT AND DRIVING METHOD THEREOF                                                                                                         |
| 2013-089731           | FMA13-00593JP             | Japan   | 04/22/2013  |            | TEST METHOD, TEST APPARATUS, AND SEMICONDUCTOR MEMORY DEVICE                                                                                        |
| 2013-095125           | FMA13-00594JP             | Japan   | 04/30/2013  |            | DELAY DIFFERENCE DETECTION CIRCUIT, SEMICONDUCTOR DEVICE, DELAY DIFFERENCE DETECTION METHOD THEREOF                                                 |
| 2013-110807           | FMA13-00595JP             | Japan   | 05/27/2013  |            | POWER AMPLIFIER DEVICE AND METHOD OF COMPENSATING THE SAME                                                                                          |
| 2013-117218           | FMA13-00596JP             | Japan   | 06/03/2013  |            | SEMICONDUCTOR DEVICE                                                                                                                                |
| 2013-125493           | FMA13-00597JP             | Japan   | 06/14/2013  |            | NOISE DETECTION CIRCUIT AND RECEIVING CIRCUIT                                                                                                       |
| 2013-100275           | FMA13-00598JP             | Japan   | 05/10/2013  |            | SEMICONDUCTOR DEVICE                                                                                                                                |
| 2013-124547           | FMA13-00599JP             | Japan   | 06/13/2013  |            | SEMICONDUCTOR MEMORY AND METHOD OF TESTING SEMICONDUCTOR MEMORY                                                                                     |
| 3399770               | FMA13-0059JP              | Japan   | 02/25/1997  | 02/21/2003 | The demodulation method, demodulation circuit, and disk apparatus of data to be demodulated                                                         |
| 2013-132689           | FMA13-00600JP             | Japan   | 06/25/2013  |            | CONTROL CIRCUIT AND CONTROL METHOD                                                                                                                  |
| 2013-139110           | FMA13-00601JP             | Japan   | 07/02/2013  |            | POWER SUPPLY CIRCUIT                                                                                                                                |
| 2013-133931           | FMA13-00602JP             | Japan   | 06/26/2013  |            | SEMICONDUCTOR INTEGRATED CIRCUIT AND METHOD OF OPERATING THE SAME                                                                                   |
| 2013-139759           | FMA13-00603JP             | Japan   | 07/03/2013  |            | RECONFIGURABLE LSI                                                                                                                                  |
| 2013-142695           | FMA13-00604JP             | Japan   | 07/08/2013  |            | LED DIMMER CONTROL DEVICE                                                                                                                           |
| 2013-147451           | FMA13-00605JP             | Japan   | 07/16/2013  |            | SEMICONDUCTOR DEVICE AND SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                           |
| 2013-144444           | FMA13-00606JP             | Japan   | 07/10/2013  |            | POWER SUPPLY DEVICE AND SEMICONDUCTOR DEVICE                                                                                                        |
| 2013-149187           | FMA13-00607JP             | Japan   | 07/18/2013  |            | DRAWING METHOD, DRAWING DEVICE AND DRAWING PROGRAM                                                                                                  |
| 2013-150161           | FMA13-00608JP             | Japan   | 07/19/2013  |            | SECURE BOOT METHOD, EMBEDDED DEVICE, SECURE BOOT DEVICE, AND SECURE BOOT PROGRAM                                                                    |
| 2013-150534           | FMA13-00609JP             | Japan   | 07/19/2013  |            | SIMULATION CONTROL METHOD, SIMULATION CONTROL PROGRAM, AND SIMULATION CONTROL APPARATUS                                                             |
| 3607044               | FMA13-0060JP              | Japan   | 06/16/1997  | 10/15/2004 | VOLTAGE SWITCHING CIRCUIT                                                                                                                           |
| 2013-150680           | FMA13-00610JP             | Japan   | 07/19/2013  |            | PROCESSOR SYSTEM AND SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                               |
| 2013-149644           | FMA13-00611JP             | Japan   | 07/18/2013  |            | DETECTION PROGRAM, DETECTING APPARATUS, AND DETECTION METHOD OF PROGRAM                                                                             |
| 2013-148631           | FMA13-00612JP             | Japan   | 07/17/2013  |            | CHARGE-DISCHARGE TYPE OSCILLATING CIRCUIT                                                                                                           |
| 2013-147446           | FMA13-00613JP             | Japan   | 07/16/2013  |            | DC-DC CONVERTER AND DRIVING METHOD OF THE SAME                                                                                                      |
| 2013-148209           | FMA13-00614JP             | Japan   | 07/17/2013  |            | EXTERNAL ELEMENT DRIVING CONTROL CIRCUIT                                                                                                            |
| 2013-149785           | FMA13-00615JP             | Japan   | 07/18/2013  |            | CAPACITANCE CONTROL CIRCUIT, SEMICONDUCTOR DEVICE, AND CAPACITANCE CONTROL METHOD                                                                   |
| 2013-149473           | FMA13-00616JP             | Japan   | 07/18/2013  |            | SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                                                    |
| 2013-150175           | FMA13-00617JP             | Japan   | 07/19/2013  |            | SEMICONDUCTOR DEVICE                                                                                                                                |
| 2013-150648           | FMA13-00618JP             | Japan   | 07/19/2013  |            | SEMICONDUCTOR DEVICE, CHARGE-DISCHARGE CONTROL SYSTEM, AND CHARGE-DISCHARGE CONTROL METHOD                                                          |
| 2013-145259           | FMA13-00619JP             | Japan   | 07/11/2013  |            | SEMICONDUCTOR MEMORY AND OPERATING METHOD THEREOF                                                                                                   |
| 3757518               | FMA13-0061JP DIV2         | Japan   | 01/30/1997  | 01/13/2006 | POWER ON/RESET CIRCUIT                                                                                                                              |
| 2013-151101           | FMA13-00620JP             | Japan   | 07/19/2013  |            | CONVERSION PROGRAM AND CONVERSION METHOD                                                                                                            |
| 2013-150567           | FMA13-00621JP             | Japan   | 07/19/2013  |            | DRAWING DEVICE AND DRAWING METHOD                                                                                                                   |
| 2013-155057           | FMA13-00622JP             | Japan   | 07/25/2013  |            | SYSTEM, EMULATOR, DEBUG SYSTEM, AND METHOD IN DEBUG SYSTEM                                                                                          |
| 3795626               | FMA13-0062JP              | Japan   | 04/22/1997  | 04/21/2006 | RECEIVER CIRCUIT                                                                                                                                    |
| 3708284               | FMA13-0063EP              | Japan   | 05/16/1997  | 08/12/2005 | A SKEW DECREASING CIRCUIT AND A SEMICONDUCTOR DEVICE                                                                                                |
| 3708285               | FMA13-0063JP              | Japan   | 05/16/1997  | 08/12/2005 | A SKEW DECREASING CIRCUIT AND A SEMICONDUCTOR DEVICE                                                                                                |
| 3727753               | FMA13-0063JP-1            | Japan   | 05/16/1997  | 10/07/2005 | A SKEW DECREASING CIRCUIT AND A SEMICONDUCTOR DEVICE                                                                                                |
| 3789598               | FMA13-0063JP-2            | Japan   | 05/20/1997  | 04/07/2006 | THE CIRCUIT AND SEMICONDUCTOR DEVICE WHICH DECREASE MANY KINDS OF SKEW                                                                              |
| 3494849               | FMA13-0064US              | Japan   | 05/29/1997  | 11/21/2003 | THE DATA READING METHOD OF A SEMICONDUCTOR MEMORY DEVICE, A SEMICONDUCTOR MEMORY DEVICE, AND THE CONTROL APPARATUS OF A SEMICONDUCTOR MEMORY DEVICE |
| 4056611               | FMA13-0065US              | Japan   | 03/17/1998  | 12/21/2007 | NTHE REPRODUCTION                                                                                                                                   |
| 4015254               | FMA13-0066FR              | Japan   | 01/16/1998  | 09/21/2007 | PLL FREQUENCY SYNTHESIZER WITH LOCK DETECTION CIRCUIT                                                                                               |
| 3693504               | FMA13-0067US              | Japan   | 07/31/1998  | 07/01/2005 | MEMORY DEVICE                                                                                                                                       |
| 4299381               | FMA13-0068JP              | Japan   | 06/02/1998  | 04/24/2009 | CONSTANT VOLTAGE GENERATION CIRCUIT                                                                                                                 |
| 3566060               | FMA13-0069FR              | Japan   | 01/29/1998  | 06/18/2004 | SEMICONDUCTOR DEVICE                                                                                                                                |
| 3954198               | FMA13-0070FR              | Japan   | 06/01/1998  | 05/11/2007 | AN OUTPUT CIRCUIT, A LEVEL CONVERTER CIRCUIT, A LOGIC CIRCUIT, AND AN OPERATIONAL-AMPLIFIER CIRCUIT                                                 |
| 3544859               | FMA13-0071US              | Japan   | 05/11/1998  | 04/16/2004 | THE SECONDARY STORAGE APPARATUS WHICH USES A NON-VOLATILE SEMICONDUCTOR MEMORY                                                                      |
| 3910983               | FMA13-0072JP              | Japan   | 09/21/2004  | 02/02/2007 | VOLTAGE SELECTION CIRCUIT AND D/A CONVERTER                                                                                                         |
| 3621249               | FMA13-0072US              | Japan   | 02/27/1998  | 11/26/2004 | A VOLTAGE SELECTING CIRCUIT, AN LCD DRIVE CIRCUIT, AND A D/A CONVERTER                                                                              |
| 3698550               | FMA13-0073US              | Japan   | 07/02/1998  | 07/15/2005 | BOOSTING CIRCUIT AND SEMICONDUCTOR DEVICE USING THE SAME                                                                                            |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                                   |
|-----------------------|---------------------------|---------|-------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4518443               | FMA13-0074JP              | Japan   | 09/21/1998  | 05/28/2010 | OPTICAL COMMUNICATION APPARATUS                                                                                                                                                         |
| 10-261420             | FMA13-0074US              | Japan   | 09/16/1998  |            | RECEIVING CIRCUIT                                                                                                                                                                       |
| 4121640               | FMA13-0075US              | Japan   | 11/12/1998  | 05/09/2008 | A LOCAL OSCILLATION CIRCUIT AND A RECEIVING CIRCUIT INCLUDING<br>THE LOCAL OSCILLATION CIRCUIT                                                                                          |
| 3736980               | FMA13-0076EP              | Japan   | 12/28/1998  | 11/04/2005 | THE EVALUATION EQUIPMENT AND THE EVALUATION METHOD OF A<br>MICROCONTROLLER                                                                                                              |
| 3741870               | FMA13-0077US              | Japan   | 08/07/1998  | 11/18/2005 | A COMMAND AND THE PREFETCH METHOD OF DATA, A<br>MICROCONTROLLER, A PSEUDO COMMAND DETECTOR CIRCUIT                                                                                      |
| 3573630               | FMA13-0078JP              | Japan   | 10/23/1998  | 07/09/2004 | AN INTEGRATED CIRCUIT DEVICE PROVIDED WITH A TRANSMISSION-<br>AND-RECEPTION BUFFER                                                                                                      |
| 3487759               | FMA13-0078US DIV          | Japan   | 04/20/1998  | 10/31/2003 | THE SYSTEM LSI WHICH HAS A COMMUNICATION FUNCTION                                                                                                                                       |
| 10-211391             | FMA13-0079US              | Japan   | 07/27/1998  |            | BUS ARBITRATING METHOD OF BUS CONTROLLER, BUS<br>CONTROLLER, AND SYSTEM OF ELECTRONIC EQUIPMENT                                                                                         |
| 4984337               | FMA13-0080JP              | Japan   | 06/03/1998  |            | DRIVER CIRCUIT OF DISPLAY PANEL AND DISPLAY DEVICE                                                                                                                                      |
| 10-154810             | FMA13-0080JP              | Japan   | 06/30/1998  | 05/11/2012 | LIQUID CRYSTAL PANEL DRIVE CIRCUIT AND LIQUID CRYSTAL<br>DISPLAY DEVICE                                                                                                                 |
| 10-196233             | FMA13-0080JP              | Japan   | 07/10/1998  |            | METHOD AND CIRCUIT TO DRIVE DISPLAY PANEL, AND DISPLAY<br>DEVICE                                                                                                                        |
| 3598008               | FMA13-0082JP              | Japan   | 12/25/1998  | 09/17/2004 | SEMICONDUCTOR DEVICE HAVING CURRENT AUXILIARY CIRCUIT ...                                                                                                                               |
| 3623379               | FMA13-0083DE              | Japan   | 12/01/1998  | 12/03/2004 | MICROPROCESSOR                                                                                                                                                                          |
| 4116176               | FMA13-0084JP              | Japan   | 01/14/1999  | 04/25/2008 | SEMICONDUCTOR DEVICE                                                                                                                                                                    |
| 4456190               | FMA13-0085JP DIV          | Japan   | 11/17/1998  | 02/12/2010 | DRIVER CIRCUIT OF LCD PANEL AND LCD DEVICE                                                                                                                                              |
| 4439023               | FMA13-0086JP              | Japan   | 11/20/1998  | 01/15/2010 | SEMICONDUCTOR DEVICE AND DISPLAY DEVICE                                                                                                                                                 |
| 2008-293753           | FMA13-0086JP DIV2         | Japan   | 11/20/1998  |            | SEMICONDUCTOR DEVICE                                                                                                                                                                    |
| 3762558               | FMA13-0087US DIV          | Japan   | 12/28/1998  | 01/20/2006 | THE CONTROL METHOD AND OUTPUT-SIGNAL CONTROL CIRCUIT OF<br>THE OUTPUT SIGNAL IN SEMICONDUCTOR MEMORY DEVICE AND A<br>SEMICONDUCTOR MEMORY DEVICE                                        |
| 3522584               | FMA13-0088US              | Japan   | 04/27/1999  | 02/20/2004 | A PHASE COMPARATOR, ITS POWER SAVING OPERATION CONTROL<br>METHOD, AND A SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                |
| 4141587               | FMA13-0089EP DIV          | Japan   | 06/01/1999  | 06/20/2008 | COMPARATOR                                                                                                                                                                              |
| 3779843               | FMA13-0089JP              | Japan   | 06/01/1999  | 03/10/2006 | VOLTAGE-CONTROLLED OSCILLATOR CIRCUIT                                                                                                                                                   |
| 4806481               | FMA13-0091US              | Japan   | 08/19/1999  | 08/19/2011 | DRIVING CIRCUIT FOR SUPPLYING TONE VOLTAGE TO LCD PANEL                                                                                                                                 |
| 11-228678             | FMA13-0092DE              | Japan   | 08/12/1999  |            | CLOCK CONTROL CIRCUIT                                                                                                                                                                   |
| 3691310               | FMA13-0093EP              | Japan   | 10/21/1999  | 06/24/2005 | FREQUENCY MEASUREMENT CIRCUIT                                                                                                                                                           |
| 4323460               | FMA13-0093JP              | Japan   | 05/19/2005  | 06/12/2009 | FREQUENCY MEASUREMENT CIRCUIT??                                                                                                                                                         |
| 4603088               | FMA13-0094JP              | Japan   | 12/01/2009  | 10/08/2010 | THE NETWORK CONSTRUCTION                                                                                                                                                                |
| 4444397               | FMA13-0094US              | Japan   | 06/25/1999  | 01/22/2010 | METHOD OF CONSTRUCTING NETWORK TOPOLOGY                                                                                                                                                 |
| 4456194               | FMA13-0095US              | Japan   | 03/02/1999  | 02/12/2010 | OUTPUT CIRCUIT AND A BATTERY PACK                                                                                                                                                       |
| 3592130               | FMA13-0096JP              | Japan   | 04/19/1999  | 09/03/2004 | ELECTRONIC CIRCUIT                                                                                                                                                                      |
| 4071395               | FMA13-0097US              | Japan   | 07/22/1999  | 01/25/2008 | VARIABLE GAIN AMPLIFIER                                                                                                                                                                 |
| 2008-150733           | FMA13-0098JP              | Japan   | 11/01/1999  |            | PLL CIRCUIT                                                                                                                                                                             |
| 11-311636             | FMA13-0098US              | Japan   | 11/01/1999  |            | PRESALER AND PLL CIRCUIT                                                                                                                                                                |
| 3935922               | FMA13-0099US              | Japan   | 12/03/1999  | 03/30/2007 | THE CHARGE-AND-DISCHARGE CONTROL CIRCUIT OF A SECONDARY<br>BATTERY                                                                                                                      |
| 4647747               | FMA13-0100US              | Japan   | 06/08/2000  | 12/17/2010 | THE SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE FOR A DC-DC<br>CONVERTER AND DC-DC CONVERTERS                                                                                               |
| 3782283               | FMA13-0101EP              | Japan   | 04/19/2000  | 03/17/2006 | INTERFACE UNIT                                                                                                                                                                          |
| 3069498               | FMA13-0102GB DIV2         | Japan   | 09/01/1994  | 05/19/2000 | CHARGING-AND-DISCHARGING DEVICE FOR AN ELECTRONIC<br>APPARATUS, AND AN ELECTRONIC APPARATUS INCLUDING THE<br>SAME, UTILIZING A CHARGING DEVICE PROVIDING A CONSTANT<br>CHARGING CURRENT |
| 3294819               | FMA13-0102JP              | Japan   | 09/01/1994  | 04/05/2002 | CHARGING-AND-DISCHARGING DEVICE FOR AN ELECTRONIC<br>APPARATUS, AND AN ELECTRONIC APPARATUS INCLUDING THE<br>SAME, UTILIZING A CHARGING DEVICE PROVIDING A CONSTANT<br>CHARGING CURRENT |
| 3392371               | FMA13-0102JP DIV1         | Japan   | 09/01/1994  | 01/24/2003 | CHARGING-AND-DISCHARGING DEVICE FOR AN ELECTRONIC<br>APPARATUS, AND AN ELECTRONIC APPARATUS INCLUDING THE<br>SAME, UTILIZING A CHARGING DEVICE PROVIDING A CONSTANT<br>CHARGING CURRENT |
| 3297022               | FMA13-0102JP DIV2         | Japan   | 09/01/1994  | 04/12/2002 | CHARGING-AND-DISCHARGING DEVICE FOR AN ELECTRONIC<br>APPARATUS, AND AN ELECTRONIC APPARATUS INCLUDING THE<br>SAME, UTILIZING A CHARGING DEVICE PROVIDING A CONSTANT<br>CHARGING CURRENT |
| 3844295               | FMA13-0102JP DIV3         | Japan   | 09/01/1994  | 08/25/2006 | CHARGING-AND-DISCHARGING DEVICE FOR AN ELECTRONIC<br>APPARATUS, AND AN ELECTRONIC APPARATUS INCLUDING THE<br>SAME, UTILIZING A CHARGING DEVICE PROVIDING A CONSTANT<br>CHARGING CURRENT |
| 4454772               | FMA13-0103US              | Japan   | 03/17/2000  | 02/12/2010 | THE ABNORMALITY DETECTOR AND MICROCOMPUTER OF A<br>COMMUNICATION BUS                                                                                                                    |
| 4615100               | FMA13-0104US              | Japan   | 07/18/2000  | 10/29/2010 | A DATA DRIVER AND A DISPLAY APPARATUS UTILIZING THE SAME                                                                                                                                |
| 3864031               | FMA13-0105JP              | Japan   | 04/06/2000  | 10/06/2006 | THE SEMICONDUCTOR INTEGRATED CIRCUIT FOR A LIQUID CRYSTAL<br>PANEL DRIVE                                                                                                                |
| 3833043               | FMA13-0105US DIV          | Japan   | 04/06/2000  | 07/28/2006 | THE GRADATION WIRING FOR INDICATORS, THE DRIVER FOR LIQUID<br>CRYSTAL DISPLAYS, AND ITS STRESS TEST METHOD                                                                              |
| 4605871               | FMA13-0106US              | Japan   | 08/25/2000  | 10/15/2010 | MICROPROCESSOR                                                                                                                                                                          |
| 4771572               | FMA13-0108US DIV          | Japan   | 04/10/2000  | 07/01/2011 | A PLL SEMICONDUCTOR DEVICE AND THE METHOD AND APPARATUS<br>OF THE TEST                                                                                                                  |
| 4073157               | FMA13-0109US              | Japan   | 08/21/2000  | 02/01/2008 | THE CASH                                                                                                                                                                                |
| 4472155               | FMA13-0110EP              | Japan   | 10/31/2000  | 03/12/2010 | THE DATA DRIVER FOR LIQUID CRYSTAL DISPLAY DEVICES                                                                                                                                      |
| 3962524               | FMA13-0111US              | Japan   | 02/29/2000  | 05/25/2007 | DISCHARGE CONTROL CIRCUIT OF BATTERIES                                                                                                                                                  |
| 4265865               | FMA13-0112US              | Japan   | 09/14/2000  | 02/27/2009 | ACTIVE LOAD CIRCUIT                                                                                                                                                                     |
| 4883832               | FMA13-0113JP              | Japan   | 10/05/2000  | 12/16/2011 | NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                |

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|-----------------------|---------------------------|---------|-------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4717991               | FMA13-0114JP              | Japan   | 11/08/2000  | 09/17/2002 | The test method of a phase calculation apparatus and a phase calculation apparatus                                                                                               |
| 4287037               | FMA13-0114JP DIV          | Japan   | 11/15/2000  | 04/03/2009 | SERVO CONTROL DEVICE AND SERVO CONTROL METHOD                                                                                                                                    |
| 2000-183297           | FMA13-0114US DIV          | Japan   | 06/19/2000  |            | SERVO CONTROL DEVICE AND SERVO CONTROL METHOD                                                                                                                                    |
| 4198303               | FMA13-0115EP              | Japan   | 06/15/2000  | 10/10/2008 | THE PHASE DIFFERENCE                                                                                                                                                             |
| 4446568               | FMA13-0116US              | Japan   | 07/21/2000  | 01/29/2010 | PLL FREQUENCY SYNTHESIZER CIRCUIT                                                                                                                                                |
| 4668430               | FMA13-0117JP              | Japan   | 01/17/2001  | 01/21/2011 | PRESALE AND PLL CIRCUIT                                                                                                                                                          |
| 2001-116174           | FMA13-0118US              | Japan   | 04/13/2001  |            | BINARY CARRY ARITHMETIC CIRCUIT, HALF ADDITION CIRCUIT AND INCREMENTER USING THE SAME, BINARY BORROW ARITHMETIC CIRCUIT, HALF SUBTRACTION CIRCUIT AND DECREMENTER USING THE SAME |
| 4342111               | FMA13-0119US DIV          | Japan   | 10/09/2003  | 05/10/2005 | CURRENT PULSE RECEIVING CIRCUIT                                                                                                                                                  |
| 3913991               | FMA13-0120US              | Japan   | 02/13/2001  | 02/09/2007 | A MICROCOMPUTER AND A COMPUTER SYSTEM                                                                                                                                            |
| 4321976               | FMA13-0121US              | Japan   | 05/31/2001  | 06/12/2009 | A MICROCOMPUTER WITH A DEBUG ASSISTANCE FUNCTION                                                                                                                                 |
| 3872331               | FMA13-0122EP              | Japan   | 11/28/2001  | 10/27/2006 | A DC-DC CONVERTER AND POWER SUPPLY CIRCUIT                                                                                                                                       |
| 4686065               | FMA13-0123US              | Japan   | 07/05/2001  | 02/18/2011 | A CLOCK CONTROL APPARATUS AND A CLOCK CONTROL METHOD                                                                                                                             |
| 4437881               | FMA13-0124US              | Japan   | 06/22/2001  | 01/15/2010 | A MICROCOMPUTER WHICH HAS A DEBUG SUPPORT UNIT                                                                                                                                   |
| 4838458               | FMA13-0125US              | Japan   | 09/13/2001  | 10/07/2011 | SEMICONDUCTOR DEVICE                                                                                                                                                             |
| 4421148               | FMA13-0126JP              | Japan   | 07/18/2001  | 12/11/2009 | DEBUGGING SYSTEM                                                                                                                                                                 |
| 3898481               | FMA13-0127US              | Japan   | 10/03/2001  | 01/05/2007 | SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                      |
| 4629279               | FMA13-0129CN              | Japan   | 08/17/2001  | 11/19/2010 | THE OPERATIONAL AMPLIFIER WHICH HAS AN OFFSET CANCELLATION FUNCTION                                                                                                              |
| 3987715               | FMA13-0130US              | Japan   | 12/06/2001  | 07/20/2007 | THE PROGRAM VOLTAGE-CONTROL METHOD OF A NON-VOLATILE SEMICONDUCTOR MEMORY AND A NON-VOLATILE SEMICONDUCTOR MEMORY                                                                |
| 4745559               | FMA13-0131US DIV          | Japan   | 08/29/2001  | 05/20/2011 | OPERATIONAL AMPLIFIER                                                                                                                                                            |
| 2001-262882           | FMA13-0132US              | Japan   | 08/31/2001  |            | NONVOLATILE SEMICONDUCTOR MEMORY                                                                                                                                                 |
| 3968228               | FMA13-0133US              | Japan   | 10/05/2001  | 06/08/2007 | REGULATOR CIRCUIT                                                                                                                                                                |
| 3968237               | FMA13-0134JP DIV          | Japan   | 12/13/2001  | 06/08/2007 | EVALUATION DEVICE FOR MICROCOMPUTER                                                                                                                                              |
| 3984482               | FMA13-0135US              | Japan   | 02/04/2002  | 07/13/2007 | DC OFFSET CANCEL CIRCUIT                                                                                                                                                         |
| 3963258               | FMA13-0136CN              | Japan   | 02/26/2002  | 06/01/2007 | A DC/DC CONVERTER CONTROL CIRCUITS AND DC/DC CONVERTER SYSTEMS ...                                                                                                               |
| 3968250               | FMA13-0137US              | Japan   | 02/05/2002  | 06/08/2007 | DC OFFSET CANCEL CIRCUIT                                                                                                                                                         |
| 4077240               | FMA13-0138JP              | Japan   | 05/10/2002  | 02/08/2008 | A semiconductor device including pull-up/pull-down option circuit and its manufacturing method                                                                                   |
| 4056768               | FMA13-0139US DIV          | Japan   | 03/04/2002  | 12/21/2007 | A MICROCOMPUTER, THE CACHE MEMORY CONTROL METHOD, AND THE CLOCK CONTROL METHOD                                                                                                   |
| 2002-79714            | FMA13-0140US              | Japan   | 03/20/2002  |            | SEMICONDUCTOR DEVICE HAVING VOLTAGE MONITORING CIRCUIT                                                                                                                           |
| 4116805               | FMA13-0141US              | Japan   | 03/20/2002  | 04/25/2008 | AN INTERNAL BUS TEST DEVICE AND INTERNAL BUS TEST METHOD                                                                                                                         |
| 3895163               | FMA13-0142US DIV          | Japan   | 11/29/2001  | 12/22/2006 | LIQUID CRYSTAL PANEL DRIVER APPARATUS                                                                                                                                            |
| 4046987               | FMA13-0143DE              | Japan   | 11/27/2001  | 11/30/2007 | RECEIVING CIRCUIT                                                                                                                                                                |
| 3939136               | FMA13-0145JP              | Japan   | 11/28/2001  | 04/06/2007 | VOICE REPRODUCTION CIRCUIT, DECODING CIRCUIT ...                                                                                                                                 |
| 3998465               | FMA13-0146US DIV          | Japan   | 11/30/2001  | 08/17/2007 | A VOLTAGE FOLLOWER, ITS OFFSET CANCELLATION CIRCUIT, A LIQUID CRYSTAL DISPLAY, AND ITS DATA                                                                                      |
| 3930332               | FMA13-0147CN DIV          | Japan   | 01/29/2002  | 03/16/2007 | A INTEGRATED CIRCUIT, A LIQUID CRYSTAL DISPLAY, AND A SIGNAL TRANSMISSION SYSTEM                                                                                                 |
| 4070492               | FMA13-0148US              | Japan   | 04/01/2002  | 01/25/2008 | A CIRCUIT WITH A DISPERSION                                                                                                                                                      |
| 4791435               | FMA13-0149JP              | Japan   | 11/19/2007  | 07/29/2011 | DIRECT-CURRENT COMPONENT CANCELING CIRCUIT                                                                                                                                       |
| 4060597               | FMA13-0149US              | Japan   | 01/07/2002  | 12/28/2007 | PULSE WIDTH DETECTION CIRCUIT FILTERING THE INPUT SIGNAL AND ...                                                                                                                 |
| 2002-155653           | FMA13-0150US              | Japan   | 05/29/2002  |            | VOLTAGE-CONTROLLED OSCILLATOR, PLL CIRCUIT AND SEMICONDUCTOR DEVICE                                                                                                              |
| 3963257               | FMA13-0151US              | Japan   | 02/14/2002  | 06/01/2007 | A DC-DC CONVERTER, AND ELECTRONIC DEVICE, A DUTY-RATIO SETTING CIRCUIT                                                                                                           |
| 3992543               | FMA13-0152JP              | Japan   | 06/03/2002  | 08/03/2007 | REGISTER CIRCUIT                                                                                                                                                                 |
| 3916994               | FMA13-0153US              | Japan   | 04/26/2002  | 02/16/2007 | A DIFFERENTIAL CIRCUIT, A PEAK HOLD CIRCUIT AND A COMPARATOR                                                                                                                     |
| 4608143               | FMA13-0154JP              | Japan   | 07/23/2001  | 10/15/2010 | CALLING INFORMATION PROCESSING APPARATUS                                                                                                                                         |
| 2001-260407           | FMA13-0155US              | Japan   | 08/29/2001  |            | SIGNAL PROCESSING APPARATUS AND SIGNAL PROCESSING METHOD, AND MULTIPLEXER                                                                                                        |
| 3541029               | FMA13-0156JP              | Japan   | 12/26/1994  | 04/02/2004 | CHARGING CONTROL APPARATUS                                                                                                                                                       |
| 3624180               | FMA13-0156JP DIV          | Japan   | 12/26/1994  | 12/03/2004 | CHARGING CONTROL DEVICE AND ELECTRONIC DEVICE                                                                                                                                    |
| 3727942               | FMA13-0156JP DIV          | Japan   | 04/19/2004  | 10/07/2005 | CHARGING CONTROL DEVICE                                                                                                                                                          |
| 2003-432670           | FMA13-0156JP DIV1         | Japan   | 12/26/1994  |            | ELECTRONIC EQUIPMENT                                                                                                                                                             |
| 2004-016929           | FMA13-0156JP DIV2         | Japan   | 12/26/1994  |            | ELECTRONIC APPARATUS, CHARGER, AND CHARGE CONTROL CIRCUIT                                                                                                                        |
| 2006-084713           | FMA13-0156JP DIV3         | Japan   | 12/26/1994  |            | ELECTRONIC APPARATUS, CHARGING SET, AND CHARGING CONTROL CIRCUIT                                                                                                                 |
| 3863546               | FMA13-0156JP DIV4         | Japan   | 08/29/2005  | 10/06/2006 | AN ELECTRONIC DEVICE, A CHARGER, AND A CHARGE CONTROL CIRCUIT                                                                                                                    |
| 3863557               | FMA13-0156JP DIV5         | Japan   | 06/26/2006  | 10/06/2006 | AN ELECTRONIC DEVICE, A CHARGER, AND A CHARGE CONTROL CIRCUIT                                                                                                                    |
| 4126329               | FMA13-0156JP DIV6         | Japan   | 10/22/2007  | 10/22/2007 | AN ELECTRONIC DEVICE, A CHARGER, AND A CHARGE CONTROL CIRCUIT                                                                                                                    |
| 4257395               | FMA13-0156JP DIV7         | Japan   | 12/26/1994  | 02/13/2009 | CHARGING CONTROL DEVICE                                                                                                                                                          |
| 03541029              | FMA13-0156US              | Japan   | 12/26/1994  | 04/02/2004 | CHARGING CONTROL APPARATUS                                                                                                                                                       |
| 4022090               | FMA13-0158IT              | Japan   | 03/27/2002  | 10/05/2007 | THE DETECTION METHOD AND DETECTOR OF A MOTION OF A FINGER                                                                                                                        |
| 4005401               | FMA13-0161US              | Japan   | 04/19/2002  | 08/31/2007 | AN AMPLIFICATION CIRCUIT AND OPTICAL COMMUNICATION APPARATUS                                                                                                                     |
| 3968274               | FMA13-0162US              | Japan   | 07/08/2002  | 06/08/2007 | SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                      |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                   |
|-----------------------|---------------------------|---------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4131651               | FMA13-0163US              | Japan   | 08/21/2002  | 06/06/2008 | THE LAYOUT METHOD OF AN INTEGRATED CIRCUIT OF HAVING A<br>SCANNING FUNCTION                                                                             |
| 4353676               | FMA13-0164CN              | Japan   | 05/24/2002  | 08/07/2009 | AN ACCUMULATION                                                                                                                                         |
| 2002-204686           | FMA13-0165US              | Japan   | 07/12/2002  |            | METHOD FOR ADJUSTING THRESHOLD VOLTAGE OF NONVOLATILE<br>SEMICONDUCTOR MEMORY AND NONVOLATILE SEMICONDUCTOR<br>MEMORY                                   |
| 4773671               | FMA13-0166JP              | Japan   | 07/24/2002  | 07/01/2011 | INPUT METHOD USING POINTING DEVICE                                                                                                                      |
| 3949027               | FMA13-0167US              | Japan   | 08/06/2002  | 04/27/2007 | ANALOG SWITCH CIRCUIT                                                                                                                                   |
| 4040405               | FMA13-0168US              | Japan   | 09/20/2002  | 11/16/2007 | THE CONTROL METHOD OF A NON-VOLATILE SEMICONDUCTOR<br>MEMORY CELL, AND A NON-VOLATILE SEMICONDUCTOR MEMORY<br>DEVICE                                    |
| 4029138               | FMA13-0169CN              | Japan   | 05/20/2002  | 10/26/2007 | FREQUENCY SYNTHESIZER CIRCUIT                                                                                                                           |
| 3905005               | FMA13-0170US              | Japan   | 09/18/2002  | 01/19/2007 | A PORTABLE APPARATUS AND A SEMICONDUCTOR INTEGRATED<br>CIRCUIT DEVICE                                                                                   |
| 4265894               | FMA13-0171US              | Japan   | 08/22/2002  | 02/27/2009 | CONTROL CIRCUIT OF A DC/DC CONVERTER, AND DC/DC<br>CONVERTER                                                                                            |
| 3792706               | FMA13-0172JP              | Japan   | 12/26/2002  | 04/14/2006 | SIGMA DELTA MODULATOR FOR PLL CIRCUIT                                                                                                                   |
| 3958675               | FMA13-0173JP              | Japan   | 11/29/2002  | 05/18/2007 | MICROCONTROLLER AND ITS CONTROLLING METHOD                                                                                                              |
| 4299530               | FMA13-0174JP              | Japan   | 11/19/2002  | 04/24/2009 | CONTROL CIRCUIT, DC-DC CONVERTER AND ELECTRONIC DEVICE                                                                                                  |
| 4037212               | FMA13-0175JP              | Japan   | 08/19/2002  | 11/09/2007 | SEMICONDUCTOR DEVICE                                                                                                                                    |
| 4067422               | FMA13-0176JP              | Japan   | 02/18/2003  | 01/18/2008 | DATA TRANSMISSION APPARATUS                                                                                                                             |
| 4141247               | FMA13-0177GB2             | Japan   | 12/24/2002  | 06/20/2008 | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT                                                                                                                |
| 4141248               | FMA13-0177JP              | Japan   | 12/25/2002  | 06/20/2008 | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT                                                                                                                |
| 4141250               | FMA13-0177JP-1            | Japan   | 12/26/2002  | 06/20/2008 | SPREAD-SPECTRUM CLOCK GENERATION CIRCUIT                                                                                                                |
| 4245136               | FMA13-0177JP-2            | Japan   | 03/07/2003  | 01/16/2009 | A JITTER GENERATING CIRCUIT AND SEMICONDUCTOR DEVICE                                                                                                    |
| 4229749               | FMA13-0177JP-3 DIV        | Japan   | 04/23/2003  | 12/12/2008 | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT                                                                                                                |
| 4252539               | FMA13-0178IT              | Japan   | 03/03/2003  | 01/30/2009 | MOS TYPE VARIABLE CAPACITANCE DEVICE                                                                                                                    |
| 4127375               | FMA13-0179JP              | Japan   | 09/25/2002  | 05/23/2008 | MICROCOMPUTER                                                                                                                                           |
| 3859608               | FMA13-0180JP              | Japan   | 03/31/2003  | 09/29/2006 | BATTERY PACK, ELECTRONIC APPARATUS, AND CALCULATION<br>SYSTEM FOR REMAIN ...                                                                            |
| 4044455               | FMA13-0181JP              | Japan   | 02/18/2003  | 11/22/2007 | DEBUG SUPPORTING DEVICE                                                                                                                                 |
| 4328084               | FMA13-0182JP              | Japan   | 11/26/2002  | 06/19/2009 | PULL-UP VOLTAGE CONTROL CIRCUIT                                                                                                                         |
| 4016034               | FMA13-0185CN              | Japan   | 04/10/2003  | 09/21/2007 | PULSE WIDTH MEASURING DEVICE WITH AUTO RANGE SETTING<br>FUNCTION                                                                                        |
| 4202116               | FMA13-0186US              | Japan   | 12/26/2002  | 10/17/2008 | A MEMORY CONTROL CIRCUIT, AND A MEMORY DEVICE, AND A<br>MICROCOMPUTER                                                                                   |
| 3999687               | FMA13-0188JP              | Japan   | 03/07/2003  | 08/17/2007 | CONSTANT CURRENT PULSE OSCILLATION CIRCUIT AND OPTICAL<br>COMMUNICATION ...                                                                             |
| 3980502               | FMA13-0189JP              | Japan   | 03/07/2003  | 07/06/2007 | AMPLIFYING CIRCUIT                                                                                                                                      |
| 2007-319087           | FMA13-0190JP              | Japan   | 04/15/2003  |            | CRYSTAL OSCILLATOR CIRCUIT                                                                                                                              |
| 4073436               | FMA13-0190US              | Japan   | 04/15/2003  | 02/01/2008 | QUARTZ CRYSTAL OSCILLATION CIRCUIT                                                                                                                      |
| 4408648               | FMA13-0191JP              | Japan   | 04/17/2003  | 11/20/2009 | An encryption and a authentication processing apparatus, a data<br>communication apparatus, and an encryption and a authentication processing<br>method |
| 4514411               | FMA13-0191US<br>CON2      | Japan   | 03/28/2003  | 05/21/2010 | INTER-BUS COMMUNICATION INTERFACE DEVICE AND DATA<br>SECURITY DEVICE                                                                                    |
| 4027874               | FMA13-0193US              | Japan   | 10/15/2003  | 10/19/2007 | CLOCK CHANGE CIRCUIT                                                                                                                                    |
| 3789448               | FMA13-0194US              | Japan   | 10/09/2003  | 04/07/2006 | THE MICROCONTROLLER WHICH MOUNTED THE SYSTEM RESOURCE<br>PRE-SCALER                                                                                     |
| 4698136               | FMA13-0195US              | Japan   | 09/11/2003  | 03/11/2011 | BAND DISTRIBUTION TEST                                                                                                                                  |
| 4364621               | FMA13-0196US              | Japan   | 12/04/2003  | 08/28/2009 | CLOCK GENERATOR                                                                                                                                         |
| 4050298               | FMA13-0197JP              | Japan   | 11/28/2003  | 12/07/2007 | SIGMA-DELTA MODULATOR FOR PLL CIRCUITS                                                                                                                  |
| 4474929               | FMA13-0198JP              | Japan   | 01/28/2004  | 03/19/2010 | DATA COMMUNICATION DEVICE                                                                                                                               |
| 4440658               | FMA13-0200EP DIV          | Japan   | 01/20/2004  | 01/15/2010 | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                                                                                                                 |
| 3966852               | FMA13-0201US              | Japan   | 12/03/2003  | 06/08/2007 | SERIAL COMMUNICATION APPARATUS                                                                                                                          |
| 4615233               | FMA13-0202US              | Japan   | 03/29/2004  | 10/29/2010 | MICROCOMPUTER WITH INTERNAL DMA                                                                                                                         |
| 5045730               | FMA13-0203JP              | Japan   | 11/02/2009  | 07/27/2012 | LEVEL CONVERSION CIRCUIT                                                                                                                                |
| 4421365               | FMA13-0203US DIV          | Japan   | 04/21/2004  | 12/11/2009 | LEVEL CONVERSION CIRCUIT                                                                                                                                |
| 4514460               | FMA13-0204US              | Japan   | 01/29/2004  | 05/21/2010 | AN OSCILLATION CIRCUIT AND SEMICONDUCTOR DEVICE                                                                                                         |
| 4198089               | FMA13-0205US              | Japan   | 05/21/2004  | 10/10/2008 | COMMUNICATION SYSTEM                                                                                                                                    |
| 4335056               | FMA13-0206US              | Japan   | 04/13/2004  | 07/03/2009 | VOLTAGE CONTROLLED OSCILLATOR AND PLL CIRCUIT                                                                                                           |
| 4652729               | FMA13-0207US              | Japan   | 06/28/2004  | 12/24/2010 | SEMICONDUCTOR DEVICE                                                                                                                                    |
| 4832721               | FMA13-0208US              | Japan   | 02/25/2004  | 09/30/2011 | A SEMICONDUCTOR DEVICE AND MICROCONTROLLER                                                                                                              |
| 4868710               | FMA13-0209US              | Japan   | 03/24/2004  | 11/25/2011 | HORIZONTAL MOS TRANSISTOR                                                                                                                               |
| 4252485               | FMA13-0210CN DIV          | Japan   | 03/29/2004  | 01/30/2009 | A SWITCHING-REGULATOR CONTROL CIRCUIT, A SWITCHING<br>REGULATOR, AND THE SWITCHING-REGULATOR CONTROL METHOD                                             |
| 4437699               | FMA13-0211GB              | Japan   | 05/14/2004  | 01/15/2010 | SENSOR                                                                                                                                                  |
| 4197678               | FMA13-0212US              | Japan   | 12/24/2004  | 10/10/2008 | SEMICONDUCTOR DEVICE WITH MECHANISM FOR LEAK DEFECT<br>DETECTION                                                                                        |
| 4533089               | FMA13-0213JP              | Japan   | 11/01/2004  | 06/18/2010 | Dynamic image data production                                                                                                                           |
| 4458923               | FMA13-0214JP              | Japan   | 05/11/2004  | 02/19/2010 | IMAGE PROCESSING DEVICE                                                                                                                                 |
| 2004-178532           | FMA13-0216US              | Japan   | 06/16/2004  |            | SEMICONDUCTOR DEVICE                                                                                                                                    |
| 4094045               | FMA13-0217CN              | Japan   | 09/08/2004  | 03/14/2008 | PLL FREQUENCY SYNTHESIZER                                                                                                                               |
| 4393317               | FMA13-0218US              | Japan   | 09/06/2004  | 10/23/2009 | MEMORY CONTROL CIRCUIT                                                                                                                                  |
| 4675082               | FMA13-0219US DIV          | Japan   | 10/21/2004  | 02/04/2011 | THE CONTROL METHOD OF A SEMICONDUCTOR MEMORY DEVICE<br>AND A SEMICONDUCTOR MEMORY DEVICE                                                                |
| 4559148               | FMA13-0220JP              | Japan   | 07/22/2004  | 07/30/2010 | MICROCONTROLLER AND POWER SUPPLY METHOD FOR<br>MICROCONTROLLER                                                                                          |
| 4137011               | FMA13-0221US              | Japan   | 06/14/2004  | 06/13/2008 | THE ELECTRIC CHARGING CONTROL CIRCUIT, A BATTERY PACK, AND<br>AN ELECTRONIC APPARATUS                                                                   |

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| 4723215               | FMA13-0222US              | Japan   | 09/02/2004  | 04/15/2011 | THE FILTER CIRCUIT WHICH ENABLED ADJUSTMENT OF CUTOFF<br>FREQUENCY                                                                          |
| 4583850               | FMA13-0223JP              | Japan   | 09/16/2004  | 09/10/2010 | SEMICONDUCTOR DEVICE AND METHOD FOR ITS MANUFACTURING                                                                                       |
| 4613040               | FMA13-0224CN              | Japan   | 09/09/2004  | 10/22/2010 | SEMICONDUCTOR DEVICE                                                                                                                        |
| 4485272               | FMA13-0225EP              | Japan   | 06/30/2004  | 04/02/2010 | SEMICONDUCTOR DEVICE                                                                                                                        |
| 4652726               | FMA13-0226US              | Japan   | 06/11/2004  | 12/24/2010 | THE CONTROL CIRCUIT, DC-DC CONVERTER, AND ELECTRONIC<br>DEVICE OF A DC-DC CONVERTER                                                         |
| 4451733               | FMA13-0227GB              | Japan   | 06/30/2004  | 02/05/2010 | SEMICONDUCTOR DEVICE HAVING A DYNAMICALLY<br>RECONFIGURABLE CIRCUIT CONFIGURATION                                                           |
| 4651977               | FMA13-0228US              | Japan   | 06/25/2004  | 12/24/2010 | THE CONTROL CIRCUIT OF A DC-DC CONVERTER, AND A METHOD<br>OF CONTROLLING THE SAME                                                           |
| 4472453               | FMA13-0229JP              | Japan   | 07/29/2004  | 03/12/2010 | A micro power converter device and a magnetic device                                                                                        |
| 4578889               | FMA13-0231JP              | Japan   | 08/16/2004  | 09/03/2010 | SEMICONDUCTOR DEVICE, PRINTED-CIRCUIT BOARD AND<br>ELECTRONICS DEVICE                                                                       |
| 4266012               | FMA13-0232US              | Japan   | 01/31/2005  | 02/27/2009 | DC-DC CONVERTER AND CONTROL CIRCUIT DEVICE FOR DC-DC<br>CONVERTER                                                                           |
| 4347231               | FMA13-0233US              | Japan   | 01/27/2005  | 07/24/2009 | MULTI-PHASE DC-DC CONVERTER AND CONTROL CIRCUIT FOR MULTI-<br>PHASE ...                                                                     |
| 4713143               | FMA13-0234CN DIV          | Japan   | 12/15/2004  | 04/01/2011 | SEMICONDUCTOR MEMORY DEVICE                                                                                                                 |
| 4533776               | FMA13-0235JP              | Japan   | 02/28/2005  | 06/18/2010 | SEMICONDUCTOR DEVICE                                                                                                                        |
| 4443424               | FMA13-0236EP              | Japan   | 01/06/2005  | 01/22/2010 | ANALOG FILTER CIRCUIT AND ADJUSTMENT METHOD THEREOF                                                                                         |
| 4178279               | FMA13-0237EP              | Japan   | 01/11/2005  | 09/05/2008 | SIGNAL DETECTION METHOD, FREQUENCY DETECTION METHOD,<br>POWER ...                                                                           |
| 2005-030917           | FMA13-0238JP              | Japan   | 02/07/2005  |            | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT AND METHOD OF<br>CONTROLLING SAME                                                                  |
| 4606216               | FMA13-0239US              | Japan   | 03/24/2005  | 10/15/2010 | COMMUNICATION DATA CONTROLLER                                                                                                               |
| 4347230               | FMA13-0240CN              | Japan   | 01/19/2005  | 07/24/2009 | MULTIPHASE DC-DC CONVERTER                                                                                                                  |
| 4721726               | FMA13-0241CN              | Japan   | 02/25/2005  | 04/15/2011 | EARLY EFFECT CANCELING CIRCUIT, DIFFERENTIAL AMPLIFIER,<br>LINEAR REGULATOR ...                                                             |
| 4190503               | FMA13-0242US              | Japan   | 01/20/2005  | 09/26/2008 | VOLTAGE CONTROL OSCILLATION CIRCUIT AND ADJUSTING METHOD<br>FOR THE SAME                                                                    |
| 4368321               | FMA13-0243US              | Japan   | 03/16/2005  | 09/04/2009 | AMPLIFIER CIRCUIT AND CONTROL METHOD THEREOF                                                                                                |
| 4536557               | FMA13-0244JP              | Japan   | 03/11/2005  | 06/25/2010 | MULTI-UNIT APPARATUS HAVING INTER-UNITS MONITORING<br>FUNCTION                                                                              |
| 4342464               | FMA13-0245US              | Japan   | 03/29/2005  | 07/17/2009 | MICROCONTROLLER                                                                                                                             |
| 4311564               | FMA13-0246US              | Japan   | 03/10/2005  | 05/22/2009 | CONTROL CIRCUIT AND CONTROL METHOD OF CURRENT MODE ...<br>DC-DC CONVERTER                                                                   |
| 2005-156035           | FMA13-0247US              | Japan   | 05/27/2005  |            | SEMICONDUCTOR DEVICE AND TESTING MODE SETTING METHOD                                                                                        |
| 4592470               | FMA13-0248EP              | Japan   | 03/30/2005  | 09/24/2010 | AMPLIFICATION CIRCUIT AND CONTROL METHOD OF AMPLIFICATION<br>CIRCUIT                                                                        |
| 4667924               | FMA13-0249US              | Japan   | 03/29/2005  | 01/21/2011 | VARIABLE CAPACITY CIRCUIT AND CONTROL METHOD OF VARIABLE<br>CAPACITY CIRCUIT                                                                |
| 4522299               | FMA13-0250US              | Japan   | 03/29/2005  | 06/04/2010 | CONSTANT CURRENT CIRCUIT AND CONSTANT CURRENT<br>GENERATING METHOD                                                                          |
| 4805594               | FMA13-0251JP              | Japan   | 03/30/2005  | 08/19/2011 | MANAGING APPARATUS FOR DEVELOPING PROGRAM                                                                                                   |
| 3655171               | FMA13-0254JP              | Japan   | 06/22/2000  | 03/11/2005 | CHARGE-DISCHARGE CONTROL CIRCUIT                                                                                                            |
| 3739005               | FMA13-0254JP DIV          | Japan   | 10/18/2004  | 11/11/2005 | CHARGE-DISCHARGE CONTROL CIRCUIT                                                                                                            |
| 4188931               | FMA13-0255US DIV          | Japan   | 03/09/2005  | 09/19/2008 | OPERATIONAL AMPLIFIER AND METHOD FOR CANCELING OFFSET<br>VOLTAGE OF ...                                                                     |
| 4860209               | FMA13-0256DE              | Japan   | 08/24/2005  | 11/11/2011 | SEMICONDUCTOR DEVICE WITH OPERATION MODE SET BY<br>EXTERNAL RESISTOR                                                                        |
| 4421534               | FMA13-0257CN              | Japan   | 09/05/2005  | 12/11/2009 | DC-DC CONVERTER AND ITS CONTROL METHOD, AND SWITCHING<br>REGULATOR ...                                                                      |
| 4359280               | FMA13-0258JP              | Japan   | 10/07/2005  | 08/14/2009 | PLL CIRCUIT                                                                                                                                 |
| 4376212               | FMA13-0259JP              | Japan   | 06/22/2005  | 09/18/2009 | DEVICE AND METHOD FOR CAPACITANCE CHANGE DETECTION                                                                                          |
| 4751667               | FMA13-0260CN              | Japan   | 08/12/2005  | 05/27/2011 | SUCCESSIVE APPROXIMATION A/D CONVERTER PROVIDED WITH<br>SAMPLE-HOLD ...                                                                     |
| 4904780               | FMA13-0261US              | Japan   | 11/07/2005  | 01/20/2012 | NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE PERFORMING<br>ERASE OPERATION...                                                                   |
| 4681983               | FMA13-0262US              | Japan   | 08/19/2005  | 02/10/2011 | BAND GAP CIRCUIT                                                                                                                            |
| 4536618               | FMA13-0263JP              | Japan   | 08/02/2005  | 06/25/2010 | RECONFIGURABLE INTEGRATED CIRCUIT DEVICE                                                                                                    |
| 4712503               | FMA13-0264CN              | Japan   | 09/29/2005  | 04/01/2011 | RECONFIGURABLE ADDRESS GENERATION CIRCUIT FOR IMAGE<br>PROCESSING, ...                                                                      |
| 4252561               | FMA13-0266GB              | Japan   | 06/23/2005  | 01/30/2009 | CLOCK GENERATING CIRCUIT AND CLOCK GENERATING METHOD                                                                                        |
| 4327144               | FMA13-0267US              | Japan   | 09/30/2005  | 06/19/2009 | ACTIVE FILTER IN PLL CIRCUIT                                                                                                                |
| 4783612               | FMA13-0268US              | Japan   | 10/12/2005  | 07/15/2011 | An extended language specification designation method, the program<br>development method, a program, and a computer-readable storage medium |
| 5140915               | FMA13-0269EP              | Japan   | 09/29/2005  | 11/30/2012 | NOISE FILTER AND FILTERING METHOD                                                                                                           |
| 4298688               | FMA13-0269US              | Japan   | 09/15/2005  | 04/24/2009 | CLOCK GENERATING CIRCUIT AND CLOCK GENERATING METHOD                                                                                        |
| 4542020               | FMA13-0270JP              | Japan   | 10/28/2005  | 07/02/2010 | FREQUENCY DIVIDING CIRCUIT                                                                                                                  |
| 4800733               | FMA13-0271JP              | Japan   | 10/13/2005  | 08/12/2011 | OUTPUT CIRCUIT                                                                                                                              |
| 4796360               | FMA13-0272US              | Japan   | 09/07/2005  | 08/05/2011 | REDUNDANCY SUBSTITUTION METHOD, SEMICONDUCTOR MEMORY<br>DEVICE ...                                                                          |
| 4440869               | FMA13-0273CN              | Japan   | 10/25/2005  | 01/15/2010 | DC-DC CONVERTER AND METHOD OF CONTROLLING DC-DC<br>CONVERTER                                                                                |
| 5182351               | FMA13-0274JP              | Japan   | 11/15/2010  | 01/25/2013 | ANALOG-TO-DIGITAL CONVERTER                                                                                                                 |
| 4652214               | FMA13-0274US              | Japan   | 11/18/2005  | 12/24/2010 | ANALOG-TO-DIGITAL CONVERTER                                                                                                                 |
| 4988190               | FMA13-0275US              | Japan   | 12/02/2005  | 05/11/2012 | NONVOLATILE SEMICONDUCTOR MEMORY HAVING VOLTAGE<br>ADJUSTING CIRCUIT                                                                        |
| 4421536               | FMA13-0276CN              | Japan   | 09/09/2005  | 12/11/2009 | CONTROLLER AND CONTROL METHOD FOR DC-DC CONVERTER                                                                                           |
| 4820654               | FMA13-0277US              | Japan   | 02/06/2006  | 09/09/2011 | CYCLE SIMULATION METHOD, CYCLE SIMULATION, AND COMPUTER<br>PRODUCT                                                                          |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                 |
|-----------------------|---------------------------|---------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 4757007               | FMA13-0278CN              | Japan   | 12/08/2005  | 06/10/2011 | STEP-UP (BOOST) DC REGULATOR WITH TWO-LEVEL BACK BIAS SWITCH GATE ...                                                                                 |
| 4640985               | FMA13-0279CN              | Japan   | 12/20/2005  | 12/10/2010 | PLURAL OUTPUT SWITCHING REGULATOR WITH PHASE COMPARISON AND DELAY ...                                                                                 |
| 4640984               | FMA13-0280CN              | Japan   | 12/07/2005  | 12/10/2010 | CONTROL CIRCUIT AND CONTROL METHOD FOR DC/DC CONVERTER                                                                                                |
| 4753723               | FMA13-0281CN              | Japan   | 01/09/2006  | 06/03/2011 | CONTROL CIRCUIT HAVING ERROR AMPLIFIER FOR DC-DC CONVERTER AND ...                                                                                    |
| 4983096               | FMA13-0282JP              | Japan   | 05/24/2006  | 05/11/2012 | NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE, ERASE METHOD FOR SAME, ...                                                                                  |
| 4750564               | FMA13-0283US DIV          | Japan   | 01/26/2006  | 05/27/2011 | CIRCUIT FOR ASYNCHRONOUSLY RESETTING SYNCHRONOUS CIRCUIT                                                                                              |
| 2006-72659            | FMA13-0284EP              | Japan   | 03/16/2006  |            | METHOD OF CORRECTING TEMPERATURE CHARACTERISTIC AND AMPLIFICATION CIRCUIT FOR SENSOR                                                                  |
| 4800816               | FMA13-0285JP              | Japan   | 03/31/2006  | 08/12/2011 | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                                                                                                               |
| 4580879               | FMA13-0286JP              | Japan   | 03/02/2006  | 09/03/2010 | RECONFIGURABLE CIRCUIT                                                                                                                                |
| 4782591               | FMA13-0287EP              | Japan   | 03/10/2006  | 07/15/2011 | RECONFIGURABLE CIRCUIT                                                                                                                                |
| 4704260               | FMA13-0288JP              | Japan   | 03/27/2006  | 03/18/2011 | PULSE WIDTH MODULATION CIRCUIT                                                                                                                        |
| 4653000               | FMA13-0289JP              | Japan   | 03/27/2006  | 12/24/2010 | PRESALER AND BUFFER                                                                                                                                   |
| 2006-40186            | FMA13-0290US              | Japan   | 02/17/2006  |            | SEMICONDUCTOR MEMORY DEVICE AND ITS CONTROL METHOD                                                                                                    |
| 4606315               | FMA13-0292JP              | Japan   | 11/29/2005  | 10/15/2010 | SEMICONDUCTOR DEVICE                                                                                                                                  |
| 4598691               | FMA13-0293US              | Japan   | 02/22/2006  | 10/01/2010 | PLL CIRCUIT AND SEMICONDUCTOR DEVICE                                                                                                                  |
| 4940684               | FMA13-0294US              | Japan   | 02/10/2006  | 03/09/2012 | PHASE ADJUSTER CIRCUIT AND PHASE ADJUSTING METHOD                                                                                                     |
| 2005-373175           | FMA13-0295EP              | Japan   | 12/26/2005  |            | COMPARATOR CIRCUIT AND CONTROL METHOD THEREOF                                                                                                         |
| 4978022               | FMA13-0296US              | Japan   | 02/16/2006  | 04/27/2012 | OPERATIONAL AMPLIFIER                                                                                                                                 |
| 4086049               | FMA13-0297JP DIV          | Japan   | 04/08/2005  | 02/29/2008 | POWER-ON/RESET CIRCUIT                                                                                                                                |
| 5143370               | FMA13-0299GB              | Japan   | 03/23/2006  | 11/30/2012 | DELAY CONTROL CIRCUIT                                                                                                                                 |
| 4699927               | FMA13-0300JP              | Japan   | 03/27/2006  | 03/11/2011 | COMMON INPUT/OUTPUT TERMINAL CONTROL CIRCUIT                                                                                                          |
| 5040136               | FMA13-0301US              | Japan   | 03/27/2006  | 07/20/2012 | The computer-readable recording medium and tuning assistance method which recorded the tuning assistance apparatus, and the tuning assistance program |
| 4850540               | FMA13-0302CN              | Japan   | 03/02/2006  | 10/28/2011 | DC-DC CONVERTER AND CONTROL CIRCUIT FOR DC-DC CONVERTER                                                                                               |
| 2002-586354           | G0063JP                   | Japan   | 11/14/2001  |            | ACCURATE VERIFY APPARATUS AND METHOD FOR NOR FLASH MEMORY CELLS IN THE PRESENCE OF HIGH COLUMN LEAKAGE                                                |
| 4885420               | G0074JP                   | Japan   | 12/14/2001  | 12/16/2011 | SOURCE DRAIN IMPLANT DURING ONO FORMATION FOR IMPROVED ISOLATION OF SONOS DEVICES                                                                     |
| 2002-592134           | G0259JP                   | Japan   | 02/19/2002  |            | FLASH MEMORY DEVICE WITH INCREASE OF EFFICIENCY DURING AN APDE (AUTOMATIC PROGRAM DISTURB AFTER ERASE) PROCESS                                        |
| 2004-522988           | G0391JP                   | Japan   | 06/10/2003  |            | BUILT-IN-SELF-TEST (BIST) OF FLASH MEMORY CELLS AND IMPLEMENTATION OF BIST INTERFACE                                                                  |
| 2003-558921           | G0689JP                   | Japan   | 12/11/2002  |            | SHALLOW TRENCH ISOLATION APPROACH FOR IMPROVED STI CORNER ROUNDING                                                                                    |
| 2004-559060           | G0730                     | Japan   | 09/24/2003  |            | METHOD AND SYSTEM FOR REDUCING CONTACT DEFECTS USING NON CONVENTIONAL CONTACT FORMATION METHOD FOR SEMICONDUCTOR CELLS                                |
| 4698598               | G0752JP                   | Japan   | 01/08/2004  | 03/11/2011 | IMPROVED PERFORMANCE IN FLASH MEMORY DEVICES                                                                                                          |
| 4235115               | G0861JP                   | Japan   | 02/14/2003  | 12/19/2008 | IMPROVED ERASE METHOD FOR SINGLE SIDED MIRROR OPERATION                                                                                               |
| 4252464               | G0862JP                   | Japan   | 02/14/2003  | 01/30/2009 | REFRESH SCHEME FOR DYNAMIC PAGE PROGRAMMING                                                                                                           |
| 2003-585103           | G0864JP                   | Japan   | 02/14/2003  |            | REFRESH SCHEME FOR DYNAMIC PAGE PROGRAMMING                                                                                                           |
| 4461281               | G0865JP                   | Japan   | 07/10/2003  | 02/26/2010 | MOCVD FORMATION OF Cu <sub>2</sub> S                                                                                                                  |
| 2004-508353           | G0866JP                   | Japan   | 04/22/2003  |            | STEPPED PRE-ERASE VOLTAGE FOR MIRRORBIT ERASE                                                                                                         |
| 2004-555270           | G0871                     | Japan   | 07/10/2003  |            | LATERAL DOPED CHANNEL                                                                                                                                 |
| 5095081               | G0878JP                   | Japan   | 07/10/2003  | 09/28/2012 | MEMORY DEVICE AND METHOD FOR FABRICATING THE SAME                                                                                                     |
| 2003-568662           | G1255JP                   | Japan   | 02/05/2003  |            | PARTIAL PAGE PROGRAMMING OF MULTI LEVEL FLASH                                                                                                         |
| 4974462               | H0297JP                   | Japan   | 07/10/2003  | 04/20/2012 | MEMORY CELL ARRAY, SEMICONDUCTOR DEVICE, AND METHOD OF FABRICATING ORGANIC SEMICONDUCTOR DEVICE                                                       |
| 5176018               | H0325JP                   | Japan   | 09/19/2005  | 01/18/2013 | CONTROL OF MEMORY DEVICES POSSESSING VARIABLE RESISTANCE CHARACTERISTICS                                                                              |
| 4708793               | H0343JP                   | Japan   | 07/10/2003  | 03/25/2011 | MOCVD FORMATION OF Cu <sub>2</sub> S                                                                                                                  |
| 5144254               | H0346JP                   | Japan   | 02/11/2005  | 11/30/2012 | IN-SITU SURFACE TREATMENT FOR MEMORY CELL FORMATION                                                                                                   |
| 5324042               | H0354JP                   | Japan   | 03/01/2004  | 07/26/2013 | SPIN ON POLYMERS FOR ORGANIC MEMORY DEVICES                                                                                                           |
| 5525132               | H0368JP                   | Japan   | 02/11/2005  | 04/18/2014 | POLYMER DIELECTRICS FOR ME ARRAY INTERN CONNECT                                                                                                       |
| 2011-219250           | H0368JP DIV               | Japan   | 02/11/2005  |            | SEMICONDUCTOR DEVICE                                                                                                                                  |
| 2004-559054           | H0385JP                   | Japan   | 09/08/2003  |            | AN ORGANIC MEMORY DEVICE AND METHOD FOR FORMING A MEMORY CELL                                                                                         |
| 2006-537996           | H0416JP                   | Japan   | 09/23/2004  |            | SIDEWALL FORMATION FOR HIGH DENSITY POLYMER MEMORY ELEMENT ARRAY                                                                                      |
| 4861172               | H0422JP                   | Japan   | 05/11/2004  | 11/11/2011 | METHOD AND SYSTEM FOR MANUFACTURING POLYMER MEMORY DEVICE IN VIA OPENING                                                                              |
| 5311740               | H0423JP                   | Japan   | 09/16/2004  | 07/12/2013 | ORGANIC MEMORY DEVICE                                                                                                                                 |
| 5443246               | H0423JP DIV               | Japan   | 04/06/2010  | 12/27/2013 | METHOD OF PROCESSING ORGANIC MEMORY DEVICE                                                                                                            |
| 4995422               | H0434JP                   | Japan   | 07/10/2003  | 05/18/2012 | STACKED ORGANIC MEMORY DEVICES AND METHOD OF FABRICATING                                                                                              |
| 5058596               | H0437JP                   | Japan   | 05/11/2004  | 08/10/2012 | PLANAR ORGANIC MEMORY DEVICE AND METHOD FOR MANUFACTURING SAME                                                                                        |
| 4903562               | H0442JP                   | Japan   | 05/21/2004  | 01/13/2012 | ORGANIC MEMORY DEVICE AND METHODS OF USING AND MAKING THE DEVICE                                                                                      |
| 2004-549909           | H0514                     | Japan   | 06/10/2003  |            | NITROGEN OXIDATION TO REDUCE ENCROACHMENT                                                                                                             |
| 2006-522575           | H0541                     | Japan   | 07/15/2004  |            | LOW POWER CHARGE PUMP                                                                                                                                 |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                               |
|-----------------------|---------------------------|---------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------|
| 4252536               | H0570JP                   | Japan   | 07/24/2003  | 01/30/2009 | IMPROVED SYSTEM FOR PROGRAMMING A NON-VOLATILE MEMORY CELL                                                                          |
| 2004-557106           | H0575                     | Japan   | 07/24/2003  |            | IMPROVED PRE-CHARGE METHOD FOR READING A NON-VOLATILE MEMORY CELL ARRAY WITH STAGGERED LOCAL INTERCONNECT STRUCTURE                 |
| 2006-535499           | H0576JP                   | Japan   | 09/16/2004  |            | MEMORY CELL AND FABRICATION METHOD THEREOF                                                                                          |
| 2006-533937           | H0577JP                   | Japan   | 09/16/2004  |            | METHOD OF PROGRAMMIN DUAL CELL MEMORY DEVICE TO STORE MULTIPLE DATA STATES PER CELL                                                 |
| 4450330               | H0587JP                   | Japan   | 03/08/2004  | 02/05/2010 | METHOD OF PROGRAMMING CHARGE TRAPPING DIELECTRIC MEMORY DEVICE AND CHARGE TRAPPING DIELECTRIC                                       |
| 2006-506976           | H0588JP                   | Japan   | 03/08/2004  |            | METHOD OF DUAL CELL MEMORY DEVICE OPERATION FOR IMPROVED END-OF-LIFE READ MARGIN                                                    |
| 5281599               | H0588JP DIV               | Japan   | 03/08/2004  | 05/31/2013 | IMPROVED METHOD FOR READING A NON-VOLATILE MEMORY CELL ADJACENT TO AN INACTIVE REGION OF A NON-VOLATILE MEMORY CELL ARRAY           |
| 4392026               | H0625JP                   | Japan   | 01/08/2004  | 10/16/2009 | MEMORY DEVICE AND METHOD USING POSITIVE GATE STRESS TO RECOVER OVERERASED CELL                                                      |
| 5160787               | H0626JP                   | Japan   | 09/16/2004  | 12/21/2012 | IMPROVED PERFORMANCE IN FLASH MEMORY DEVICES                                                                                        |
| 4731488               | H0671JP                   | Japan   | 01/08/2004  | 04/28/2011 | CASCADE AMPLIFIER CIRCUIT FOR PRODUCING A FAST, STABLE AND ACCURATE BITLINE VOLTAGE                                                 |
| 2004-555269           | H1203                     | Japan   | 08/22/2003  |            | SELECTION CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS                                                                               |
| 5085934               | H1204JP                   | Japan   | 01/08/2004  | 09/14/2012 | CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS                                                                                         |
| 2004-559036           | H1205JP                   | Japan   | 07/24/2003  |            | CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS                                                                                         |
| 4871127               | H1368JP                   | Japan   | 06/18/2004  | 11/25/2011 | PECVD SILICON-RICH OXIDE LAYER FOR REDUCED UV CHARGING                                                                              |
| 4927550               | H1414JP                   | Japan   | 06/05/2004  | 02/17/2012 | NON-VOLATILE MEMORY DEVICE, METHOD OF MANUFACTURING NON-VOLATILE MEMORY DEVICE, AND NON-VOLATILE MEMORY ARRAY                       |
| 2006-542575           | H1415JP                   | Japan   | 10/26/2004  |            | FLASH MEMORY DEVICE                                                                                                                 |
| 4520982               | H1513JP                   | Japan   | 03/01/2004  | 05/28/2010 | CIRCUIT FOR FAST AND ACCURATE MEMORY READ OPERATIONS                                                                                |
| 5290517               | H1862JP                   | Japan   | 08/31/2004  | 06/14/2013 | METHOD FOR FABRICATING MEMORY CELL STRUCTURE                                                                                        |
| 4495723               | H1892JP                   | Japan   | 03/08/2004  | 04/16/2010 | FAST, ACCURATE AND LOW POWER SUPPLY VOLTAGE BOOSTER USING A/D CONVERTER                                                             |
| 2002-588554           | H1971                     | Japan   | 05/07/2002  |            | A MEMORY DEVICE WITH A SELF-ASSEMBLED POLYMER FILM AND METHOD OF MAKING THE SAME                                                    |
| 2002-588633           | H1973                     | Japan   | 05/07/2002  |            | FLOATING GATE MEMORY DEVICE USING COMPOSITE MOLECULAR MATERIAL                                                                      |
| 2002-588649           | H1975                     | Japan   | 05/07/2002  |            | MEMORY SWITCH                                                                                                                       |
| 2004-537736           | H1978                     | Japan   | 09/08/2003  |            | ORGANIC THIN FILM ZENER DIODES                                                                                                      |
| 2003-522101           | H1979JP                   | Japan   | 08/13/2001  |            | MEMORY CELL                                                                                                                         |
| 2007-511353           | H1984JP                   | Japan   | 02/11/2005  |            | METHODS AND APPARATUS FOR WORDLINE PROTECTION IN FLASH MEMORY DEVICES                                                               |
| 2011-237023           | H1984JP DIV               | Japan   | 02/11/2005  |            | METHODS AND APPARATUS FOR WORDLINE PROTECTION IN FLASH MEMORY DEVICES                                                               |
| 4698612               | H1985JP                   | Japan   | 12/17/2004  | 03/11/2011 | POCKET IMPLANT FOR COMPLEMENTARY BIT DISTURB IMPROVEMENT AND CHARGING IMPROVEMENT OF SONOS MEMORY CELL                              |
| 4642848               | H1990JP                   | Japan   | 04/29/2005  | 12/10/2010 | METHOD OF FORMING NARROWLY SPACED FLASH MEMORY CONTACT OPENINGS                                                                     |
| 5053398               | H1990JP DIV               | Japan   | 04/29/2005  | 08/03/2012 | METHOD FOR CREATING PLURALITY OF OPTICAL FEATURES SEPARATED FROM ONE ANOTHER ON LITHOGRAPHY MASK                                    |
| 4922926               | H1993JP                   | Japan   | 02/11/2005  | 02/10/2012 | METHOD OF FORMING AT LEAST PORTION OF DUAL BIT MEMORY CORE ARRAY UPON SEMICONDUCTOR SUBSTRATE                                       |
| 4757909               | H1998JP                   | Japan   | 04/04/2006  | 06/10/2011 | METHOD FOR POLYSILICON-1 DEFINITION OF FLASH MEMORY DEVICE                                                                          |
| HEI 8-334141          | JC137496JP                | Japan   | 12/13/1996  |            | SEMICONDUCTOR DEVICE AND THE METHOD FOR FABRICATING THEREOF                                                                         |
| 2000-587371           | JC684497JP                | Japan   | 11/29/1999  |            | HIGH YIELD, HIGH PERFORMANCE SEMICONDUCTOR PROCESS FLOW FOR NAND FLASH MEMORY PRODUCTS                                              |
| 2000-572920           | JC685497JP                | Japan   | 09/28/1999  |            | HIGH TEMPERATURE DEPOSITION OF OXIDE LAYER THAT PROTECTS AGAINST IMPLANTATION DAMAGE                                                |
| 5289650               | JC688497JP                | Japan   | 02/11/1999  | 06/14/2013 | THE MANUFACTURING METHOD OF THE NAND-FLASH-MEMORY APPARATUS WITH WHICH POLY 1 EASY CONTACT IS OBTAINED BY THE REMOVAL OF A POLY CAP |
| 4718007               | JC818597JP                | Japan   | 12/17/1998  | 04/08/2011 | PROCESS FOR FABRICATING AN INTEGRATED CIRCUIT WITH A SELF-ALIGNED CONTACT                                                           |
| 60265163              | M84-003                   | Japan   | 11/27/1985  |            | METHOD AND STRUCTURE FOR DISABLING AND REPLACING DEFECTIVE MEMORY IN A PROM                                                         |
| 2000-229200           | P-1164JP                  | Japan   | 07/28/2000  |            | AN NROM FABRICATION METHOD                                                                                                          |
| 2001-338271           | P-2448WO                  | Japan   | 04/03/2002  |            | PROGRAMMING AND ERASING METHOD FOR NROM ARRAY                                                                                       |
| 2001-338308           | P-2448WO                  | Japan   | 04/03/2002  |            | PROGRAMMING AND ERASING METHOD FOR NROM ARRAY                                                                                       |
| 2001-581281           | P-2448WO                  | Japan   | 11/02/2001  |            | ARCHITECTURE AND SCHEME FOR A NON-STROBED READ SEQUENCE                                                                             |
| 2002-101411           | P-2448WO                  | Japan   | 05/03/2001  |            | PROGRAMMING AND ERASING METHOD FOR NROM ARRAY                                                                                       |
| 2002-101471           | P-2448WO                  | Japan   | 05/03/2001  |            | PROGRAMMING AND ERASING METHOD FOR NROM ARRAY                                                                                       |
| 2003-539051           | P-4006JP                  | Japan   | 10/24/2002  |            | METHOD FOR ERASING A MEMORY CELL                                                                                                    |
| 2002-334684           | P-4007JP                  | Japan   | 11/19/2002  |            | PROTECTIVE LAYER IN MEMORY DEVICE AND METHOD THEREFOR                                                                               |
| 2003-272960           | P-4629JP                  | Japan   | 07/10/2003  |            | A MULTIPLE USE MEMORY CHIP                                                                                                          |
| 2003-023064           | P-4676JP1                 | Japan   | 01/31/2003  |            | METHOD FOR OPERATING A MEMORY DEVICE                                                                                                |
| 2006-001351           | P-4676JP3                 | Japan   | 01/06/2006  |            | METHOD FOR OPERATING A MEMORY DEVICE                                                                                                |
| 2006-537552           | P-5484US                  | Japan   | 10/27/2004  |            | METHOD SYSTEM AND CIRCUIT FOR PROGRAMMING A NON-VOLATILE MEMORY ARRAY                                                               |
| 2006-537553           | P-5487-TW                 | Japan   | 10/27/2004  |            | METHOD CIRCUIT AND SYSTEM FOR DETERMINING A REFERENCE VOLTAGE                                                                       |

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| PATENT OR APPL NO. | SPANSION REFERENCE NO. | COUNTRY    | FILING DATE | ISSUE DATE | TITLE                                                                                                                                        |
|--------------------|------------------------|------------|-------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 2006-537554        | P-5487-TW1             | Japan      | 10/28/2004  | 01/01/2013 | METHOD FOR READ ERROR DETECTION IN A NON-VOLATILE MEMORY ARRY                                                                                |
| 4164324            | P-6343US               | Japan      | 09/19/2002  | 08/01/2008 | METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE                                                                                               |
| 2005-355621        | P-6628US               | Japan      | 12/09/2005  |            | MEMORY FOR READING NON-VOLATILE MEMORY CELLS                                                                                                 |
| 2006-222247        | P-6628US CIP           | Japan      | 07/09/2008  |            | METHOD FOR READING NON-VOLATILE MEMORY CELLS                                                                                                 |
| 2008-178796        | P-6628US CIP           | Japan      | 08/17/2005  | 07/10/2007 | METHOD FOR READING NON-VOLATILE MEMORY CELLS                                                                                                 |
| 4249131            | SE0002JP               | Japan      | 03/11/2003  | 01/23/2009 | A SYSTEM AND METHOD OF ERASE VOLTAGE CONTROL DURING MULTIPLE SECTOR ERASE OF A FLASH MEMORY DEVICE                                           |
| 2015-515096        | SP09-0030JP            | Japan      | 05/24/2013  |            | METHOD, APPARATUS, AND MANUFACTURE FOR FLASH MEMORY ADAPTIVE ALGORITHM                                                                       |
| 4260461            | SP09-0038US            | Japan      | 11/13/2002  | 02/20/2009 | INFRARED COMMUNICATION SYSTEM, INFRARED GATEWAY UNIT, AND PROGRAM FOR INFRARED COMMUNICATION                                                 |
| 2014-546120        | SP09-0056EP            | Japan      | 12/07/2012  |            | HIGH SPEED SERIAL PERIPHERAL INTERFACE MEMORY SUBSYSTEM                                                                                      |
| 2007-110264        | SP09-0056WO            | Japan      | 04/19/2007  |            | EXHAUST SYSTEM                                                                                                                               |
| 2013-544818        | SP10-0007JP            | Japan      | 12/17/2010  |            | SELF-ALIGNED NAND FLASH SELECT-GATE WORDLINES FOR SPACER DOUBLE PATTERNING                                                                   |
| 2013-544874        | SP10-0008JP            | Japan      | 12/19/2011  |            | EDGE ROUNDED FIELD EFFECT TRANSISTORS AND METHODS OF MANUFACTURING                                                                           |
| 2013-544873        | SP10-0009JP            | Japan      | 12/19/2011  |            | PROCESS MARGIN ENGINEERING IN CHARGE TRAPPING FIELD EFFECT TRANSISTORS                                                                       |
| 2013-547676        | SP10-0012JP            | Japan      | 12/29/2011  |            | MEMORY WITH EXTENDED CHARGE TRAPPING LAYER                                                                                                   |
| 2015-512745        | SP11-0015EP            | Japan      | 05/14/2013  |            | SOFT ERROR RESISTANT CIRCUITRY                                                                                                               |
| 2013-000647        | SP11-0021JP            | Japan      | 01/07/2013  |            | APPARATUS AND METHOD FOR A REDUCED PIN COUNT (RPC) MEMORY BUS INTERFACE INCLUDING A READ DATA STROBE SIGNAL                                  |
| 2014-557699        | SP11-0027JP            | Japan      | 02/08/2013  |            | IMPROVING REDUNDANCY LOADING EFFICIENCY                                                                                                      |
| 5528869            | SP11-0032US            | Japan      | 03/23/2010  | 04/25/2014 | ANTI GLARE FILM AND METHOD FOR READING THE SAME                                                                                              |
| 2012-271622        | SP11-0034GB            | Japan      | 12/12/2012  |            | CONTINUOUS READ BURST SUPPORT AT HIGH CLOCK RATES                                                                                            |
| 2014-547494        | SP11-0042JP            | Japan      | 12/14/2012  |            | ACOUSTIC PROCESSING UNIT                                                                                                                     |
| 2015-504651        | SP12-0013JP            | Japan      | 04/01/2013  |            | ADAPTIVELY PROGRAMMING OR ERASING FLASH MEMORY BLOCKS                                                                                        |
| 4695158            | SP12-0080US            | Japan      | 04/23/2008  | 03/04/2011 | METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE                                                                                                 |
| 5405927            | SP13-0035US            | Japan      | 07/15/2009  | 11/08/2013 | NETWORK NODE                                                                                                                                 |
| 2015-031330        | SP13-0036JP            | Japan      | 02/20/2015  |            | MEMORY SUBSYSTEM WITH WRAPPED-TO-CONTINUOUS READ                                                                                             |
| 306190/1994        | TT0313US               | Japan      | 12/09/1994  |            | ROM ARRAY CONTROLLER CAPABLE OF CONTROLLING ROM BANKS HAVING VARIABLE BIT Width.                                                             |
| 3866778            | TT0347FR               | Japan      | 12/09/1994  | 10/13/2006 | METHOD FOR ETCHING AND IMPLANTING SOURCE REGIONS                                                                                             |
| 4458498            | TT0497GB               | Japan      | 02/20/1996  | 02/19/2010 | A NON-VOLATILE MEMORY DEVICES HAVING A FLOATING GATE WITH ENHANCED CHARGE RETENTION                                                          |
| 102638/1996        | TT0607EP               | Japan      | 04/24/1996  |            | METHOD FOR READING A NON-VOLATILE MEMORY ARRAY                                                                                               |
| 1203378            | C725497                | Netherland | 08/01/2000  | 03/05/2003 | CIRCUIT IMPLEMENTATION TO QUENCH BIT LINE LEAKAGE CURRENT IN PROGRAM AND AUTO PROGRAM DISTURB MODE IN FLASH EPROM USING RESISTOR SOURCE LOAD |
| 1116239            | D168                   | Netherland | 08/16/1999  | 05/15/2002 | SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                                |
| 88050              | AF01002SG              | Singapore  | 10/07/2000  | 05/31/2004 | LOW VOLTAGE READ CASCODE FOR 2V/3V AND DIFFERENT BANK COMBINATIONS WITHOUT METAL OPTIONS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE    |
| 88046              | AF01054SG              | Singapore  | 10/16/2000  | 05/31/2004 | HIGH TEMPERATURE OXIDE DEPOSITION PROCESS FOR FABRICATING AN ONO FLOATING-GATE ELECTRODE IN A TWO BIT EEPROM DEVICE                          |
| 93394              | AF01076SG              | Singapore  | 05/21/2001  | 04/28/2006 | BURST ARCHITECTURE FOR A FLASH MEMORY                                                                                                        |
| 93681              | AF01085SG              | Singapore  | 06/04/2001  | 05/31/2005 | METHOD TO REDUCE CAPACITIVE LOADING IN FLASH MEMORY X-DECODER FOR ACCURATE VOLTAGE CONTROL AT WORDLINES AND SELECT LINES                     |
| 105202             | AF01124SG              | Singapore  | 12/11/2002  | 05/31/2006 | MONOS DEVICE HAVING BURIED METAL SILICIDE BIT LINE                                                                                           |
| 115033             | AF01186SG              | Singapore  | 01/08/2004  | 09/28/2007 | CHARGE-TRAPPING MEMORY ARRAYS RESISTANT TO DAMAGE FROM CONTACT HOLE FORMATION                                                                |
| 124437             | AF01209SG              | Singapore  | 04/13/2004  | 09/30/2008 | METHOD FOR REDUCING SHORT CHANNEL EFFECTS IN MEMORY CELLS AND RELATED STRUCTURE                                                              |
| 87395              | C656497SG              | Singapore  | 08/31/2000  | 05/31/2004 | TUNGSTEN GATE MOS TRANSISTOR AND MEMORY CELL AND METHOD OF MAKING SAME                                                                       |
| 86825              | C725497                | Singapore  | 08/13/1999  |            | CIRCUIT IMPLEMENTATION TO QUENCH BIT LINE LEAKAGE CURRENT IN PROGRAM AND AUTO PROGRAM DISTURB MODE IN FLASH EPROM USING RESISTOR SOURCE LOAD |
| 88410              | D838SG                 | Singapore  | 10/24/2000  | 04/30/2004 | SOLID-SOURCE DOPING FOR SOURCE/DRAIN OF FLASH MEMORY                                                                                         |
| 89582              | D853SG                 | Singapore  | 12/05/2000  | 08/31/2004 | METHOD TO PROVIDE A REDUCED CONSTANT E-FIELD DURING ERASE OF EEPROMS FOR RELIABILITY IMPROVEMENT                                             |
| 88054              | D894SG                 | Singapore  | 09/29/2000  | 04/30/2004 | METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITH REDUCED ARC LOSS IN PERIPHERAL CIRCUITRY REGION                                          |
| 90473              | D958SG                 | Singapore  | 12/13/2000  | 07/30/2004 | NOVEL NITRIDATION BARRIERS FOR NITRIDATED TUNNEL OXIDE FOR CIRCUITRY FOR FLASH TECHNOLOGY AND FOR LOCOS/STI ISOLATION                        |
| 86829              | DA01016SG              | Singapore  | 07/14/2000  | 12/31/2003 | METHOD FOR PROVIDING A DOPANT LEVEL FOR POLYSILICON FOR FLASH MEMORY DEVICES                                                                 |
| 87297              | E0251                  | Singapore  | 07/14/2000  | 05/31/2004 | FLASH MEMORY ARCHITECTURE EMPLOYING THREE LAYER METAL INTERCONNECT                                                                           |
| 90972              | E0264                  | Singapore  | 02/07/2001  | 10/29/2004 | TRIMMING METHOD FOR WORDLINE BOOSTER TO MINIMIZE PROCESS VARIATION OF BOOSTED WORDLINE VOLTAGE                                               |
| 92963              | E0302SG                | Singapore  | 05/01/2001  | 07/29/2005 | UNIFORM BITLINE STRAPPING OF NON-VOLATILE MEMORY CELL                                                                                        |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY     | FILING DATE | ISSUE DATE | TITLE                                                                                                                                     |
|-----------------------|---------------------------|-------------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 92996                 | E0462SG                   | Singapore   | 05/21/2001  | 07/29/2005 | DUAL PORTED CAMS FOR SIMULTANEOUS OPERATION FLASH MEMORY                                                                                  |
| 94125                 | F0004SG                   | Singapore   | 06/08/2001  | 10/31/2005 | AUTOMATED DETERMINATION AND DISPLAY OF THE PHYSICAL LOCATION OF A FAILED CELL IN AN ARRAY OF MEMORY CELLS                                 |
| 103213                | F0282SG                   | Singapore   | 09/30/2002  | 06/30/2006 | DOUBLE DENSED CORE GATES IN SONOS FLASH MEMORY                                                                                            |
| 103214                | F0283SG                   | Singapore   | 09/27/2002  | 08/31/2006 | SALICIDED GATE FOR VIRTUAL GROUND ARRAYS                                                                                                  |
| 95712                 | F0499SG                   | Singapore   | 08/06/2001  | 08/31/2007 | A SOURCE SIDE BORON IMPLANTING AND DIFFUSING DEVICE ARCHITECTURE FOR DEEP SUBSTANCE 0.18UM FLASH MEMORY TECHNOLOGIES                      |
| 104823                | G0689SG                   | Singapore   | 12/11/2002  | 08/31/2006 | SHALLOW TRENCH ISOLATION APPROACH FOR IMPROVED STI CORNER ROUNDING                                                                        |
| 112465                | G0865SG                   | Singapore   | 07/10/2003  | 11/30/2007 | MOCVD FORMATION OF Cu <sub>2</sub> S                                                                                                      |
| 107309                | G0866SG                   | Singapore   | 04/22/2003  | 11/30/2006 | STEPPED PRE-ERASE VOLTAGE FOR MIRRORBIT ERASE                                                                                             |
| 111829                | G0871SG                   | Singapore   | 07/10/2003  | 08/31/2007 | LATERAL DOPED CHANNEL                                                                                                                     |
| 112467                | G0878SG                   | Singapore   | 07/10/2003  | 08/31/2007 | A METHOD AND SYSTEM FOR ERASING A NITRIDE MEMORY DEVICE                                                                                   |
| 112466                | H0343SG                   | Singapore   | 07/10/2003  | 07/31/2007 | MOCVD FORMATION OF Cu <sub>2</sub> S                                                                                                      |
| 200505789-8           | H0354SG                   | Singapore   | 03/01/2004  |            | SPIN ON POLYMERS FOR ORGANIC MEMORY DEVICES                                                                                               |
| 113211                | H0385SG                   | Singapore   | 09/08/2003  | 12/31/2007 | AN ORGANIC MEMORY DEVICE AND METHOD FOR FORMING A MEMORY CELL                                                                             |
| 118781                | H0422SG                   | Singapore   | 05/11/2004  | 01/31/2008 | METHOD AND SYSTEM FOR MANUFACTURING POLYMER MEMORY DEVICE IN VIA OPENING                                                                  |
| 112222                | H0434SG                   | Singapore   | 07/10/2003  | 04/30/2007 | STACKED ORGANIC MEMORY DEVICES AND METHODS OF OPERATING AND FABRICATING                                                                   |
| 117306                | H0437SG                   | Singapore   | 05/11/2004  | 11/30/2007 | PLANAR POLYMER MEMORY DEVICE                                                                                                              |
| 118782                | H0442SG                   | Singapore   | 05/21/2004  | 03/31/2008 | ORGANIC MEMORY DEVICE AND METHODS OF USING AND MAKING THE DEVICE                                                                          |
| 111365                | H0514SG                   | Singapore   | 06/10/2003  | 10/31/2007 | NITROGEN OXIDATION TO REDUCE ENCROACHMENT                                                                                                 |
| 111889                | H0570SG                   | Singapore   | 07/24/2003  | 10/31/2007 | IMPROVED SYSTEM FOR PROGRAMMING A NON-VOLATILE MEMORY CELL                                                                                |
| 121233                | H0576SG                   | Singapore   | 09/16/2004  | 11/28/2008 | MEMORY CELL ARRAY WITH STAGGERED LOCAL INTERCONNECT STRUCTURE                                                                             |
| 114127                | H0671SG                   | Singapore   | 01/08/2004  | 09/28/2007 | IMPROVED PERFORMANCE IN FLASH MEMORY DEVICES                                                                                              |
| 115936                | H1204SG                   | Singapore   | 01/08/2004  | 08/31/2007 | SELECTION CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS                                                                                     |
| 118784                | H1368SG                   | Singapore   | 06/18/2004  | 12/31/2007 | PECVD SILICON-RICH OXIDE LAYER FOR REDUCED UV CHARGING                                                                                    |
| 119992                | H1862SG                   | Singapore   | 08/31/2004  | 10/31/2008 | MEMORY CELL STRUCTURE HAVING NITRIDE LAYER WITH REDUCED CHARGE LOSS AND METHOD FOR FABRICATING SAME                                       |
| 317647                | A887KR                    | South Korea | 09/25/1993  | 12/03/2001 | VPP POWER SUPPLY                                                                                                                          |
| 277136                | A888/1987KR               | South Korea | 09/25/1993  | 10/06/2000 | DRAIN POWER SUPPLY                                                                                                                        |
| 283019                | A889/1988KR               | South Korea | 09/25/1993  | 12/04/2000 | NEGATIVE POWER SUPPLY                                                                                                                     |
| 345878                | A900/1996KR               | South Korea | 06/08/1994  | 07/11/2002 | IMPROVED OUTPUT BUFFER CIRCUIT FOR LOW VOLTAGE EPROM                                                                                      |
| 357444                | A938/2033KR               | South Korea | 11/25/1994  | 10/07/2002 | PROGRAMMED REFERENCE                                                                                                                      |
| 333257                | A939/2034KR               | South Korea | 11/25/1994  | 04/08/2002 | BOOSTED AND REGULATED GATE POWER SUPPLY WITH REFERENCE TRACKING FOR MULTI-DENSITY AND LOW VOLTAGE SUPPLY MEMORIES                         |
| 357443                | A960/2054KR               | South Korea | 04/08/1995  | 10/07/2002 | METHOD AND APPARATUS FOR PROGRAMMING MEMORY DEVICES                                                                                       |
| 366599                | A976/2067KR               | South Korea | 06/24/1995  | 12/16/2002 | HIGH ENERGY BURIED LAYER IMPLANT TO PROVIDE A LOW RESISTANCE P-WELL IN A FLASH EPROM ARRAY                                                |
| 645573                | AF01002KR                 | South Korea | 10/07/2000  | 11/06/2006 | LOW VOLTAGE READ CASCODE FOR 2V/3V AND DIFFERENT BANK COMBINATIONS WITHOUT METAL OPTIONS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE |
| 725649                | AF01036KR                 | South Korea | 02/07/2001  | 05/30/2007 | WORDLINE DRIVER FOR FLASH MEMORY READ MODE                                                                                                |
| 784472                | AF01054KR                 | South Korea | 10/16/2000  | 12/04/2007 | HIGH TEMPERATURE OXIDE DEPOSITION PROCESS FOR FABRICATING AN ONO FLOATING-GATE ELECTRODE IN A TWO BIT EEPROM DEVICE                       |
| 737984                | AF01064KR                 | South Korea | 03/20/2001  | 07/04/2007 | METHOD FOR FORMING HIGH QUALITY MULTIPLE THICKNESS OXIDE LAYERS USING HIGH TEMPERATURE DESCUM                                             |
| 785107                | AF01066KR                 | South Korea | 03/20/2001  | 12/05/2007 | METHOD FOR FORMING HIGHQUALITY MULTIPLE THICKNESS OXIDE LAYERS BY REDUCING DESCUM INDUCED DEFECTS                                         |
| 725648                | AF01072KR                 | South Korea | 02/05/2001  | 05/30/2007 | VOLTAGE BOOST LEVEL CLAMPING CIRCUIT FOR A FLASH MEMORY                                                                                   |
| 784473                | AF01073KR                 | South Korea | 07/31/2001  | 12/04/2007 | WORD LINE DECODING ARCHITECTURE IN A FLASH MEMORY                                                                                         |
| 675959                | AF01075KR                 | South Korea | 03/12/2001  | 01/23/2007 | MULTIPLE BANK SIMULTANEOUS OPERATION FOR A FLASH MEMORY                                                                                   |
| 717412                | AF01076KR                 | South Korea | 05/21/2001  | 05/04/2007 | BURST ARCHITECTURE FOR A FLASH MEMORY                                                                                                     |
| 822486                | AF01078KR                 | South Korea | 07/17/2001  | 04/08/2008 | BURST READ INCORPORATING OUTPUT BASED REDUNDANCY                                                                                          |
| 708915                | AF01085KR                 | South Korea | 06/04/2001  | 04/11/2007 | METHOD TO REDUCE CAPACITIVE LOADING IN FLASH MEMORY X-DECODER FOR ACCURATE VOLTAGE CONTROL AT WORDLINES AND SELECT LINES                  |
| 708914                | AF01086KR                 | South Korea | 09/29/2000  | 04/11/2007 | A WORD LINE TRACKING STRUCTURE FOR USE IN AN ARRAY OF FLASH EEPROM MEMORY CELLS                                                           |
| 796041                | AF01090KR                 | South Korea | 11/14/2001  | 01/11/2008 | I/O PARTITIONING AND METHODOLOGY TO REDUCE BAND-TO-BAND TUNNELING CURRENT DURING ERASE                                                    |
| 865587                | AF01094KR                 | South Korea | 03/14/2002  | 10/21/2008 | VOLTAGE BOOST CIRCUIT USING SUPPLY VOLTAGE DETECTION TO COMPENSATE FOR SUPPLY VOLTAGE VARIATION IN READ MODE VOLTAGES                     |
| 828196                | AF01096KR                 | South Korea | 12/12/2001  | 04/30/2008 | SOFT PROGRAM AND SOFT PROGRAM VERIFY OF THE CORE CELLS IN FLASH MEMORY ARRAY                                                              |
| 810710                | AF01102KR                 | South Korea | 08/07/2001  | 02/28/2008 | SIMULTANEOUS FORMATION CHARGE STORAGE AND BITLINE TO WORDLINE ISOLATION                                                                   |
| 10-0953208            | AF01116KR                 | South Korea | 03/03/2003  | 04/08/2010 | SYSTEM AND METHOD FOR MULTI-BIT FLASH READS USING DUAL DYNAMIC REFERENCES                                                                 |

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| PATENT OR APPL<br>NO. | SPANION<br>REFERENCE NO. | COUNTRY     | FILING DATE | ISSUE DATE | TITLE                                                                                                    |
|-----------------------|--------------------------|-------------|-------------|------------|----------------------------------------------------------------------------------------------------------|
| 10-0948199            | AF01124KR                | South Korea | 12/11/2002  | 03/10/2010 | MONOS DEVICE HAVING BURIED METAL SILICIDE BIT LINE                                                       |
| 10-1059234            | AF01132KR                | South Korea | 01/21/2003  | 08/18/2011 | HARD MASK PROCESS FOR MEMORY DEVICE WITHOUT BITLINE SHORTS                                               |
| 10-0987505            | AF01134KR                | South Korea | 01/21/2003  | 10/06/2011 | METHOD OF MAKING MEMORY WORDLINE HARD MASK EXTENSION                                                     |
| 7016142/2004          | AF01137KR                | South Korea | 02/14/2003  |            | MEMORY MANUFACTURING PROCESS WITH BITLINE ISOLATION                                                      |
| 10-0973788            | AF01165KR                | South Korea | 06/10/2003  | 07/28/2010 | COLUMN-DECODING AND PRECHARGING IN A FLASH MEMORY DEVICE                                                 |
| 702499/2005           | AF01169                  | South Korea | 05/21/2004  |            | MEMORY WITH A CORE-BASED VIRTUAL GROUND AND DYNAMIC REFERENCE SENSING SCHEME                             |
| 10-1017713            | AF01186KR                | South Korea | 01/08/2004  | 01/18/2011 | CHARGE-TRAPPING MEMORY ARRAYS RESISTANT TO DAMAGE FROM CONTACT HOLE FORMATION                            |
| 7020925/2005          | AF01209KR                | South Korea | 04/13/2004  |            | METHOD FOR REDUCING SHORT CHANNEL EFFECTS IN MEMORY CELLS AND RELATED STRUCTURE                          |
| 7014331/2006          | AF01214KR                | South Korea | 12/17/2004  |            | EFFICIENT USE OF WAFER AREA WITH DEVICE UNDER THE PAD APPROACH                                           |
| 10-1092010            | AF01220KR                | South Korea | 01/22/2004  | 12/02/2011 | STRUCTURE AND METHOD FOR LOW VSS RESISTANCE AND REDUCED DIBL IN A FLOATING GATE MEMORY CELL              |
| 835382                | AF01232US                | South Korea | 04/29/2005  | 05/29/2008 | BOND PAD STRUCTURE FOR COPPER METALLIZATION HAVING INCREASED RELIABILITY AND METHOD FOR FABRICATING SAME |
| 7022382/2006          | AF01240KR                | South Korea | 03/26/2004  |            | ABORT CIRCUIT FOR MLC PROGRAMMING                                                                        |
| 7023673/2006          | AF01241KR                | South Korea | 04/13/2004  |            | NEW COMMAND FOR SECTOR PROTECTION                                                                        |
| 7023788/2006          | AF01248                  | South Korea | 04/21/2004  |            | NON-VOLATILE SEMICONDUCTOR DEVICE AND METHOD FOR AUTOMATICALLY RECOVERING ERASE FAILURE IN THE DEVICE    |
| 850368                | AF01274KR                | South Korea | 08/30/2004  | 07/29/2008 | IMPROVEMENT OF THE REDUNDANT EFFICIENCY FOR THE SEMICONDUCTOR MEMORY                                     |
| 869862                | AF01306KR                | South Korea | 06/30/2005  | 11/14/2008 | SWITCHABLE MEMORY DIODE- A NEW MEMORY DEVICE                                                             |
| 10-0923580            | AF01329KR                | South Korea | 08/30/2004  | 10/19/2009 | ERASE METHOD OF A NON-VOLATILE MEMORY DEVICE AND A NON-VOLATILE MEMORY DEVICE                            |
| 903695                | AF01338KR                | South Korea | 10/26/2004  | 06/11/2009 | METHOD OF SETTING INFORMATION OF NON-VOLATILE MEMORY AND NON-VOLATILE MEMORY                             |
| 928736                | AF01361KR                | South Korea | 06/30/2005  | 11/19/2009 | METHOD OF IMPROVING ERASE VOLTAGE DISTRIBUTION FOR A FLASH MEMORY ARRAY HAVING DUMMY WORDLINES           |
| 928737                | AF01365KR                | South Korea | 04/29/2005  | 11/19/2009 | FLASH MEMORY UNIT AND METHOD OF PROGRAMMING A FLASH MEMORY DEVICE                                        |
| 7019209/2006          | AF01372                  | South Korea | 02/19/2004  |            | CURRENT-VOLTAGE CONVERTER CIRCUIT AND CONTROL METHOD THEREOF                                             |
| 7019211/2006          | AF01376KR                | South Korea | 02/20/2004  |            | A SEMICONDUCTOR MEMORY STORAGE DEVICE AND ITS REDUNDANT METHOD                                           |
| 838387                | AF01379KR                | South Korea | 04/29/2005  | 06/09/2008 | FLOATING GATE MEMORY CELL                                                                                |
| 7019210/2006          | AF01380KR                | South Korea | 02/20/2004  |            | A SEMICONDUCTOR MEMORY STORAGE DEVICE AND ITS CONTROL METHOD                                             |
| 873206                | AF01383KR                | South Korea | 09/20/2005  | 12/03/2008 | READ APPROACH FOR MULTI-LEVEL VIRTUAL GROUND MEMORY                                                      |
| 10-1134691            | AF01386KR                | South Korea | 02/11/2005  | 04/02/2012 | ERASE ALGORITHM FOR MULTI-LEVEL BIT FLASH MEMORY                                                         |
| 10-917690             | AF01390KR                | South Korea | 12/20/2005  | 09/09/2009 | MULTI-LEVEL ONO FLASH PROGRAM ALGORITHM FOR THRESHOLD WIDTH CONTROL                                      |
| 10-1176219            | AF01402KR                | South Korea | 07/30/2004  | 08/16/2012 | SEMICONDUCTOR DEVICE AND METHOD FOR GENERATING SENSE SIGNAL                                              |
| 10-1092012            | AF01403KR                | South Korea | 07/30/2004  | 12/02/2011 | METHODS AND SYSTEMS FOR HIGH WRITE PERFORMANCE IN MULTI-BIT FLASH MEMORY DEVICES                         |
| 928738                | AF01404KR                | South Korea | 08/30/2004  | 11/19/2009 | APPARATUS FOR ADJUSTING RAMP GATE PGM CONDITION IN MANUAL PGM                                            |
| 7024784/2006          | AF01416                  | South Korea | 05/12/2004  |            | IMPROVED NEGATIVE DECODING                                                                               |
| 7024209/2006          | AF01417                  | South Korea | 05/11/2004  |            | HIGH SPEED BOOST OPERATION                                                                               |
| 7023674/2006          | AF01422                  | South Korea | 05/11/2004  |            | DUMMY CELL ARRAY BETWEEN CORE AND REFERENCE ARRAYS                                                       |
| 7024210/2006          | AF01423                  | South Korea | 05/11/2004  |            | MULTI BIT PROGRAMMING FOR VIRTUAL GROUND ARRAY                                                           |
| 7024939/2006          | AF01425                  | South Korea | 05/11/2004  |            | IMPROVED APPARATUS FOR ADVANCED SECTOR PROTECTION (1)                                                    |
| 7024211/2006          | AF01427KR                | South Korea | 05/12/2004  |            | IMPROVED SLATCH AND THE LAYOUT                                                                           |
| 870752                | AF01432KR                | South Korea | 08/31/2004  | 11/20/2008 | THE SEMICONDUCTOR MEMORY STORAGE DEVICE WHICH CARRIED THE NEGATIVE VOLTAGE GENERATING CIRCUIT            |
| 7014682/2007          | AF01439KR                | South Korea | 11/30/2004  |            | NON-VOLATILE SELECT GATE IN NAND FLASH MEMORY                                                            |
| 10-1092013            | AF01441KR                | South Korea | 07/29/2004  | 12/02/2011 | METHOD FOR INITIALIZING NON-VOLATILE STORAGE DEVICE, AND NON-VOLATILE STORAGE DEVICE                     |
| 7023675/2006          | AF01443                  | South Korea | 05/11/2004  |            | CARRIER FOR SEMICONDUCTOR DEVICES TO BE STACKED AND FABRICATION METHOD OF THE DEVICE                     |
| 10-0955720            | AF01445KR                | South Korea | 12/28/2004  | 05/28/2010 | SONOS WITH USE OF SWITCH GATE, WITHOUT BURIED DIFFUSION LAYER BITLINE                                    |
| 7024940/2006          | AF01446                  | South Korea | 05/20/2004  |            | SEMICONDUCTOR CHIP ASSEMBLY AND FABRICATION METHOD OF THE SAME                                           |
| 10-1036669            | AF01451KR                | South Korea | 04/24/2006  | 05/17/2011 | THE FORMATION METHOD OF AN ARRAY SOURCE LINE IN NAND FLASH                                               |
| 10-1092011            | AF01453KR                | South Korea | 02/11/2005  | 12/02/2011 | METHOD AND SYSTEMS FOR HIGH WRITE PERFORMANCE IN MULTI-BIT FLASH MEMORY DEVICES                          |
| 912517                | AF01454KR                | South Korea | 11/30/2004  | 08/10/2009 | NEW MEMORY CELL STRUCTURE IN WHICH HIGH-SPEED WRITING IS POSSIBLE                                        |
| 903694                | AF01463KR                | South Korea | 09/30/2004  | 06/11/2009 | SEMICONDUCTOR DEVICE AND DATA WRITING METHOD                                                             |
| 903696                | AF01468KR                | South Korea | 10/29/2004  | 06/11/2009 | SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME                                                  |
| 7030213/2007          | AF01482                  | South Korea | 05/26/2006  |            | PAGE BUFFER ARCHITECTURE FOR PROGRAMMING, ERASING AND READING NANOSCALE RESISTIVE MEMORY DEVICES         |
| 912516                | AF01500KR                | South Korea | 11/10/2005  | 08/10/2009 | PROTECTION OF ACTIVE LAYERS OF MEMORY CELLS DURING PROCESSING OF OTHER ELEMENTS                          |
| 903697                | AF01645KR                | South Korea | 10/26/2004  | 06/11/2009 | NON-VOLATILE MEMORY DEVICE                                                                               |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY     | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                                            |
|-----------------------|---------------------------|-------------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10-0953991            | AF01668KR                 | South Korea | 09/08/2006  | 04/13/2010 | HIGH PERFORMANCE FLASH MEMORY DEVICE CAPABLE OF HIGH DENSITY DATA STORAGE                                                                                                                        |
| 926835                | AF01669KR                 | South Korea | 09/07/2006  | 11/06/2009 | MULTI-BIT FLASH MEMORY DEVICE HAVING IMPROVED PROGRAM RATE                                                                                                                                       |
| 870753                | AF01691KR                 | South Korea | 12/24/2004  | 11/20/2008 | SYNCHRONOUS STORAGE DEVICE AND CONTROLLING METHOD THEREOF                                                                                                                                        |
| 912518                | AF01698KR                 | South Korea | 01/27/2005  | 08/10/2009 | A NON-VOLATILE MEMORY STORAGE DEVICE AND ITS CONTROL METHOD (PLACEMENT FORMATION (STRUCTURE) OF "AN INFORMATION MEMORY CELL OF OPERATION", AND ITS READ/WRITE APPARATUS, AND ITS CONTROL METHOD) |
| 7021003/2007          | AF01709KR                 | South Korea | 03/22/2006  |            | VARIABLE BREAKDOWN CHARACTERISTIC DIODE                                                                                                                                                          |
| 10-1008371            | AF01729KR                 | South Korea | 05/30/2005  | 01/07/2011 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING SAME                                                                                                                                           |
| 10-1000111            | AF01730KR                 | South Korea | 03/24/2006  | 12/03/2010 | MULTI CHIP MODULE AND METHOD OF MANUFACTURE                                                                                                                                                      |
| 7030212/2007          | AF01741KR                 | South Korea | 05/25/2006  |            | READ-ONLY MEMORY ARRAY WITH DIELECTRIC BREAKDOWN PROGRAMMABILITY                                                                                                                                 |
| 7006407/2008          | AF01746                   | South Korea | 09/15/2005  |            | METHOD FOR FORMING SPACERS BETWEEN BITLINES IN A VIRTUAL GROUND MEMORY ARRAY AND REALTED STRUCTURE                                                                                               |
| 925255                | AF01775KR                 | South Korea | 04/26/2006  | 10/29/2009 | RESISTIVE MEMORY DEVICE WITH IMPROVED DATA RETENTION AND REDUCED POWER                                                                                                                           |
| 10-0940605            | AF01777KR                 | South Korea | 10/06/2006  | 01/28/2010 | METHOD FOR MANUFACTURING A SEMICONDUCTOR COMPONENT USING A SACRIFICIAL MASKING STRUCTURE                                                                                                         |
| 10-0952718            | AF01792KR                 | South Korea | 06/28/2005  | 04/06/2010 | MIRRORBIT DEVICE HAVING STI AND DUAL POLY FILMS                                                                                                                                                  |
| 10-0935949            | AF01802KR                 | South Korea | 06/28/2005  | 12/30/2009 | CASCODE AMPLIFIER FOR FAST READ                                                                                                                                                                  |
| 10-1078013            | AF01810KR                 | South Korea | 09/16/2008  | 10/24/2011 | VERTICAL EEPROM DEVICE                                                                                                                                                                           |
| 10-0962702            | AF01852KR                 | South Korea | 07/07/2006  | 06/03/2010 | INTEGRATED CIRCUIT TEST SOCKET                                                                                                                                                                   |
| 10-0964352            | AF01853KR                 | South Korea | 10/06/2006  | 06/09/2010 | MEMORY ARRAY                                                                                                                                                                                     |
| 1375797               | AF01907KR                 | South Korea | 04/05/2007  | 03/12/2014 | MULTI MEDIA CARD WITH HIGH STORAGE CAPACITY                                                                                                                                                      |
| 10-1074143            | AF01954KR                 | South Korea | 04/05/2007  | 10/10/2011 | MEMORY CELL ARRAY WITH LOW RESISTANCE COMMON SOURCE AND HIGH CURRENT DRIVABILITY                                                                                                                 |
| 10-1348374            | AF02071KR                 | South Korea | 05/21/2007  | 12/30/2013 | MEMORY SYSTEM WITH SWITCH ELEMENT                                                                                                                                                                |
| 7027179/2008          | AF02136KR                 | South Korea | 11/05/2008  |            | REDUCTION OF LEAKAGE CURRENT AND PROGRAM DISTURBS IN FLASH MEMORY DEVICES                                                                                                                        |
| 7026872/2008          | AF02137KR                 | South Korea | 11/18/2008  |            | METHODS FOR ERASING AND PROGRAMMING MEMORY DEVICES                                                                                                                                               |
| 7027181/2008          | AF02138KR                 | South Korea | 04/05/2007  |            | METHODS FOR ERASING MEMORY DEVICES AND MULTI-LEVEL PROGRAMMING MEMORY DEVICE                                                                                                                     |
| 10-2008-7027073       | AF02146KR                 | South Korea | 11/04/2008  |            | FLASH MEMORY PROGRAMMING AND VERIFICATION WIHT REDUCED LEAKAGE CURRENT                                                                                                                           |
| 271566                | AF02173KR                 | South Korea | 06/30/1997  | 08/17/2000 | MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE                                                                                                                                                     |
| 0551933               | AF02175KR                 | South Korea | 05/16/2000  | 02/07/2006 | NONVOLATILE MEMORY ALLOW ENCRYPTED                                                                                                                                                               |
| 0633752               | AF02177KR                 | South Korea | 02/28/2000  | 10/04/2006 | MULTI-LEVEL NONVOLATILE MEMORY USING                                                                                                                                                             |
| 0702922               | AF02178KR                 | South Korea | 11/24/2000  | 03/28/2007 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                          |
| 727445                | AF02180KR                 | South Korea | 05/30/2000  | 06/05/2007 | SEMICONDUCTOR MEMORY DEVICE AND                                                                                                                                                                  |
| 727446                | AF02181KR                 | South Korea | 05/30/2000  | 06/05/2007 | SEMICONDUCTOR MEMORY DEVICE AND USING                                                                                                                                                            |
| 0721295               | AF02182KR                 | South Korea | 08/18/2000  | 05/17/2007 | NONVOLATILE MEMORY CIRCUIT STORAGE MULTI-                                                                                                                                                        |
| 0674454               | AF02183KR                 | South Korea | 02/16/2000  | 01/19/2007 | NONVOLATILE MEMORY                                                                                                                                                                               |
| 706849                | AF02184KR                 | South Korea | 07/17/2000  | 04/05/2007 | NONVOLATILE MEMORY DEVICE AND                                                                                                                                                                    |
| 0597060               | AF02185KR                 | South Korea | 08/03/2000  | 06/28/2006 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                          |
| 0698341               | AF02186KR                 | South Korea | 06/29/2000  | 03/15/2007 | SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                                      |
| 0676722               | AF02188KR                 | South Korea | 12/21/2000  | 01/25/2007 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                          |
| 628901                | AF02189KR                 | South Korea | 01/03/2001  | 09/20/2006 | MANUFACTURING METHOD OF NONVOLATILE                                                                                                                                                              |
| 0744586               | AF02191KR                 | South Korea | 09/28/2001  | 07/25/2007 | NONVOLATILE SEMICONDUCTOR DEVICE AND                                                                                                                                                             |
| 10-0864860            | AF02192KR                 | South Korea | 02/06/2002  | 10/16/2008 | SEMICONDUCTOR MEMORY AND MANUFACTURING                                                                                                                                                           |
| 0629193               | AF02193KR                 | South Korea | 05/25/2001  | 09/21/2006 | NONVOLATILE SEMICONDUCTOR DEVICE                                                                                                                                                                 |
| 739084                | AF02195KR                 | South Korea | 09/19/2001  | 07/06/2007 | SEMICONDUCTOR DEVICE AND MANUFACTURING                                                                                                                                                           |
| 728141                | AF02198KR                 | South Korea | 09/05/2001  | 06/07/2007 | SEMICONDUCTOR MEMORY DEVICE AND DRIVING                                                                                                                                                          |
| 0873656               | AF02200KR                 | South Korea | 04/18/2002  | 12/05/2008 | MEMORY CONTROLLER FOR MULTI LEVEL                                                                                                                                                                |
| 0874175               | AF02208KR                 | South Korea | 04/09/2003  | 12/09/2008 | NONVOLATILE SEMICONDUCTOR MEMORY AND                                                                                                                                                             |
| 0958901               | AF02209KR                 | South Korea | 02/19/2003  | 05/12/2010 | NONVOLATILE SEMICONDUCTOR DEVICE                                                                                                                                                                 |
| 0829034               | AF02212KR                 | South Korea | 05/20/2003  | 05/06/2008 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                          |
| 10-1010982            | AF02214KR                 | South Korea | 03/21/2003  | 01/19/2011 | SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                                      |
| 0942487               | AF02222KR                 | South Korea | 08/12/2003  | 02/08/2010 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                                                                                                                 |
| 660459                | AF02223KR                 | South Korea | 02/24/2003  | 12/15/2006 | VOLTAGE DETECTION CIRCUIT, SEMICONDUCTOR DEVICE, METHOD FOR CONTROLLING VOLTAGE DETECTION CIRCUIT                                                                                                |
| 0642104               | AF02224KR                 | South Korea | 02/18/2003  | 10/27/2006 | SEMICONDUCTOR MEMORY DEVICE AND DATA RESD                                                                                                                                                        |
| 0704596               | AF02226KR                 | South Korea | 02/27/2003  | 04/02/2007 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                                                                                                                 |
| 0597063               | AF02229KR                 | South Korea | 02/28/2003  | 06/28/2006 | FLASH MEMORY AND MEMORY CONTROL                                                                                                                                                                  |
| 0793221               | AF02230KR                 | South Korea | 12/17/2003  | 01/03/2008 | SEMICONDUCTOR DEVICE AND TEST METHOD                                                                                                                                                             |
| 0774275               | AF02232KR                 | South Korea | 03/11/2003  | 11/01/2007 | MEMORY DEVICE                                                                                                                                                                                    |
| 757290                | AF02233KR                 | South Korea | 12/17/2003  | 09/04/2007 | NONVOLATILE MEMORY AND METHOD AND WRITE METHOD OF THE SAME                                                                                                                                       |
| 0627087               | AF02238KR                 | South Korea | 04/24/2003  | 09/15/2006 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                                                                                                                 |
| 628827                | AF02241KR                 | South Korea | 06/06/2003  | 09/20/2006 | SEMICONDUCTOR MEMORY DEVICE AND SELECT                                                                                                                                                           |
| 7025665/2009          | AF02453KR                 | South Korea | 05/09/2008  |            | SELF ALIGNED NARROW STORAGE ELEMENTS FOR ADVANCED MEMORY DEVICE                                                                                                                                  |
| 10-1205589            | AF02465KR                 | South Korea | 01/18/2010  | 11/21/2012 | TERMINATE CYCLE FOR BURST WRITE OPERATION                                                                                                                                                        |
| 675072                | AF02649KR                 | South Korea | 11/03/2000  | 01/22/2007 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                          |
| 10-2013-7005998       | AF03209KR                 | South Korea | 08/10/2011  |            | STITCH BUMP STACKING DESIGN FOR OVERALL PACKAGE SIZE REDUCTION FOR MULTIPLE STACK                                                                                                                |
| 10-2013-7002452       | AF03219KR                 | South Korea | 06/29/2011  |            | METHOD AND SYSTEM FOR THIN MULTI CHIP STACK PACKAGE WITH FILM ON WIRE AND COPPER WIRE                                                                                                            |
| 1018371               | AF04009US                 | South Korea | 08/28/2003  | 02/22/2011 | SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD THEREOF                                                                                                                                     |

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|-----------------------|---------------------------|-------------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10-2011-7010635       | AF04027KR                 | South Korea | 10/07/2009  |            | REAL-TIME DATA PATTERN ANALYSIS SYSTEM AND METHOD OF OPERATION THEREOF                                                                                 |
| 10-2014-7020294       | AF04035KR                 | South Korea | 12/18/2012  |            | ACOUSTIC PROCESSING UNIT INTERFACE                                                                                                                     |
| 10-2014-7020295       | AF04036KR                 | South Korea | 12/18/2012  |            | ARITHMETIC LOGIC UNIT ARCHITECTURE                                                                                                                     |
| 718903                | AF04052CN                 | South Korea | 08/29/2003  | 05/10/2007 | SEMICONDUCTOR MEMORY DEVICE                                                                                                                            |
| 397048                | B002KR                    | South Korea | 08/30/1995  | 08/23/2003 | A SELF-ALIGNED BURIED CHANNEL/JUNCTION STACKED GATE FLASH MEMORY CELL                                                                                  |
| 392900                | B015KR                    | South Korea | 09/29/1995  | 07/15/2003 | LAYERED LOW DIELECTRIC CONSTANT TECHNOLOGY                                                                                                             |
| 383392                | B047KR                    | South Korea | 11/22/1995  | 04/25/2003 | NOVEL PROCESSING TECHNIQUES FOR ACHIEVING PRODUCTION WORTHY LOW DIELECTRIC LOW INTERCONNECT RESISTANCE AND HIGH PERFORMANCE                            |
| 418430                | B111KR                    | South Korea | 06/21/1996  | 01/31/2004 | PROCESS FOR SELF-ALIGNED SOURCE FOR HIGH DENSITY MEMORY                                                                                                |
| 445197                | B128KR                    | South Korea | 08/30/1996  | 08/10/2004 | A FLASH EEPROM MEMORY WITH SEPARATE REFERENCE ARRAY                                                                                                    |
| 391117                | B132KR                    | South Korea | 06/18/1996  | 06/30/2003 | CHANNEL HOT CARRIER PAGE WRITE                                                                                                                         |
| 440745                | B255KR                    | South Korea | 08/08/1996  | 07/07/2004 | POWER SUPPLY INDEPENDENT CURRENT SOURCE FOR FLASH EPROM ERASE                                                                                          |
| 433686                | B260KR                    | South Korea | 07/19/1996  | 05/19/2004 | A NEW PROGRAM ALGORITHM FOR LOW VOLTAGE (3V) SINGLE POWER SUPPLY FLASH MEMORIES                                                                        |
| 437651                | B277KR                    | South Korea | 03/25/1997  | 06/16/2004 | A NOVEL PROCESS FOR RELIABLE ULTRATHIN OXYNITRIDE FORMATION                                                                                            |
| 578584                | C061296KR                 | South Korea | 01/23/1998  | 05/03/2006 | HIGH VOLTAGE CMOS LEVEL SHIFTER                                                                                                                        |
| 494377                | C141496KR                 | South Korea | 04/10/1998  | 05/31/2005 | A DUAL SOURCE SIDE POLYSILICON SELECT GATE STRUCTURE AND PROGRAMMING METHOD UTILIZING SINGLE TUNNEL OXIDE FOR NAND ARRAY FLASH MEMORY                  |
| 7007909/1999          | C144496KR                 | South Korea | 02/05/1998  |            | HIGH VOLTAGE NMOS PASS GATE FOR INTEGRATED CIRCUIT WITH HIGH VOLTAGE GENERATOR AND FLASH NON-VOLATILE MEMORY DEVICE HAVING THE PASS GATE               |
| 472741                | C196596KR                 | South Korea | 11/13/1997  | 02/11/2005 | BANK ARCHITECTURE FOR A NON-VOLATILE MEMORY ENABLING SIMULTANEOUS READING AND WRITING                                                                  |
| 554708                | C369297KR                 | South Korea | 12/18/1998  | 02/16/2006 | BIASING METHOD AND STRUCTURE FOR REDUCING BAND-TO-BAND AND/OR AVALANCHE CURRENTS DURING THE ERASE OF FLASH MEMORY DEVICE                               |
| 505857                | C526397KR                 | South Korea | 08/25/1998  | 07/26/2005 | REDUCTION OF CHARGE LOSS IN NONVOLATILE MEMORY CELLS BY PHOSPHOROUS IMPLANTATION INTO PECVD NITRIDE/OXYNITRIDE FILMS                                   |
| 675962                | C608497KR                 | South Korea | 05/20/1999  | 01/23/2007 | SHALLOW TRENCH ISOLATION FILLED WITH THERMAL OXIDE                                                                                                     |
| 655942                | C614497KR                 | South Korea | 03/02/1999  | 12/04/2006 | STEPPER ALIGNMENT MARK FORMATION WITH DUAL FIELD OXIDE PROCESS                                                                                         |
| 554707                | C627497KR                 | South Korea | 12/18/1998  | 02/16/2006 | METHODS AND ARRANGEMENTS FOR IMPROVED FORMATION OF CONTROL AND FLOATING GATES IN NON-VOLATILE MEMORY SEMICONDUCTOR DEVICES                             |
| 773994                | C656497KR                 | South Korea | 08/31/2000  | 10/31/2007 | TUNGSTEN GATE MOS TRANSISTOR AND MEMORY CELL AND METHOD OF MAKING SAME                                                                                 |
| 727617                | C695497KR                 | South Korea | 06/29/2000  | 06/05/2007 | THIN FLOATING GATE AND CONDUCTIVE SELECT GATE IN SITU                                                                                                  |
| 578581                | C715497KR                 | South Korea | 09/21/1999  | 05/03/2006 | WORDLINE DRIVER FOR FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EEPROM)                                                                 |
| 489421                | C725497KR                 | South Korea | 08/01/2000  | 05/03/2005 | CIRCUIT IMPLEMENTATION TO QUENCH BIT LINE LEAKAGE CURRENT IN PROGRAM AND AUTO PROGRAM DISTURB MODE IN FLASH EPROM USING RESISTOR SOURCE LOAD           |
| 604457                | D016KR                    | South Korea | 10/05/1999  | 07/18/2006 | BIT LINE BIASING METHOD TO ELIMINATE PROGRAM DISTURBANCE IN A NON-VOLATILE MEMORY DEVICE AND MEMORY DEVICE EMPLOYING THE SAME                          |
| 564378                | D138KR                    | South Korea | 10/05/1999  | 03/20/2006 | SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON-VOLATILE MEMORY ARRAY                                                                                  |
| 604462                | D140KR                    | South Korea | 08/03/1999  | 07/18/2006 | VT REFERENCE VOLTAGE FOR EXTREMELY LOW POWER-SUPPLY                                                                                                    |
| 544756                | D168KR                    | South Korea | 08/16/1999  | 01/12/2006 | SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                                          |
| 586930                | D169KR                    | South Korea | 08/16/1999  | 05/29/2006 | METHOD OF MAKING FLEXIBLY PARTITIONED METAL LINE SEGMENTS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE |
| 544755                | D170KR                    | South Korea | 08/16/1999  | 01/12/2006 | MEMORY ADDRESS DECODING CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                           |
| 645572                | D802KR                    | South Korea | 10/27/1999  | 11/06/2006 | METHOD FOR IMPROVING ELECTROSTATIC DISCHARGE (ESD) ROBUSTNESS                                                                                          |
| 578582                | D832KR                    | South Korea | 05/05/2000  | 05/03/2006 | RAMPED OR STEPPED GATE CHANNEL ERASE FOR FLASH MEMORY APPLICATION                                                                                      |
| 639827                | D833KR                    | South Korea | 08/29/2000  | 10/23/2006 | 1 TRANSISTOR FOR EEPROM APPLICATION                                                                                                                    |
| 743694                | D838KR                    | South Korea | 10/24/2000  | 07/23/2007 | SOLID-SOURCE DOPING FOR SOURCE/DRAIN OF FLASH MEMORY                                                                                                   |
| 761091                | D844KR                    | South Korea | 07/14/2000  | 09/17/2007 | RAMPED GATE TECHNIQUE FOR SOFT PROGRAMMING TO TIGHTEN THE VT DISTRIBUTION                                                                              |
| 655944                | D853KR                    | South Korea | 12/05/2000  | 12/04/2006 | METHOD TO PROVIDE A REDUCED CONSTANT E-FIELD DURING ERASE OF EEPROMS FOR RELIABILITY IMPROVEMENT                                                       |
| 724154                | D877KR                    | South Korea | 07/17/2000  | 05/25/2007 | INTEGRATED CIRCUIT HAVING INCREASED GATE COUPLING CAPACITANCE                                                                                          |
| 717409                | D894KR                    | South Korea | 09/29/2000  | 05/04/2007 | METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITH REDUCED ARC LOSS IN PERIPHERAL CIRCUITRY REGION                                                    |
| 717411                | D958KR                    | South Korea | 12/13/2000  | 05/04/2007 | NOVEL NITRIDATION BARRIERS FOR NITRIDATED TUNNEL OXIDE FOR CIRCUITRY FOR FLASH TECHNOLOGY AND FOR LOCOS/STI ISOLATION                                  |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY     | FILING DATE | ISSUE DATE | TITLE                                                                                                                                            |
|-----------------------|---------------------------|-------------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 697353                | DA01016KR                 | South Korea | 07/14/2000  | 03/13/2007 | METHOD FOR PROVIDING A DOPANT LEVEL FOR POLYSILICON FOR FLASH MEMORY DEVICES                                                                     |
| 724153                | E0197KR                   | South Korea | 06/29/2000  | 05/25/2007 | NEW METHOD OF FORMING SELECT GATE TO IMPROVE RELIABILITY AND PERFORMANCE FOR NAND-TYPE FLASH MEMORY DEVICES                                      |
| 629987                | E0251KR                   | South Korea | 07/14/2000  | 09/22/2006 | FLASH MEMORY ARCHITECTURE EMPLOYING THREE LAYER METAL INTERCONNECT                                                                               |
| 658215                | E0264KR                   | South Korea | 02/07/2001  | 12/08/2006 | TRIMMING METHOD FOR WORDLINE BOOSTER TO MINIMIZE PROCESS VARIATION OF BOOSTED WORDLINE VOLTAGE                                                   |
| 824442                | E0370KR                   | South Korea | 03/12/2001  | 04/16/2008 | A DUAL SPACER PROCESS NON-VOLATILE MEMORY DEVICES                                                                                                |
| 915450                | E0462KR                   | South Korea | 05/21/2001  | 08/27/2009 | DUAL PORTED CAMS FOR SIMULTANEOUS OPERATION FLASH MEMORY                                                                                         |
| 743695                | E1030KR                   | South Korea | 02/07/2001  | 07/23/2007 | TEMPERATURE COMPENSATED BIAS GENERATOR                                                                                                           |
| 788491                | F0257KR                   | South Korea | 08/07/2001  | 12/17/2007 | METHOD AND SYSTEM FOR EMBEDDED CHIP ERASE VERIFICATION                                                                                           |
| 7010943/2004          | F0258                     | South Korea | 12/17/2002  |            | METHOD AND APPARATUS FOR SOFT PROGRAM VERIFICATION IN A MEMORY DEVICE                                                                            |
| 928735                | F0262KR                   | South Korea | 12/17/2002  | 11/19/2009 | METHOD AND APPARATUS FOR SOFT PROGRAM VERIFICATION IN A MEMORY DEVICE                                                                            |
| 7011031/2004          | F0272                     | South Korea | 12/17/2002  |            | CHARGE INJECTION                                                                                                                                 |
| 7004809/2004          | F0283                     | South Korea | 09/27/2002  |            | SALICIDED GATE FOR VIRTUAL GROUND ARRAYS                                                                                                         |
| 810709                | F0499KR                   | South Korea | 08/06/2001  | 02/28/2008 | A SOURCE SIDE BORON IMPLANTING AND DIFFUSING DEVICE ARCHITECTURE FOR DEEP SUBSTANCE 0.18UM FLASH MEMORY TECHNOLOGIES                             |
| 838382                | F0932KR                   | South Korea | 08/06/2001  | 06/09/2008 | SOURCE SIDE BORON IMPLANT AND DRAIN SIDE MDD IMPLANT FOR DEEP SUB 0.18 MICRON FLASH MEMORY                                                       |
| 10-1014036            | F1104KR                   | South Korea | 11/26/2003  | 02/01/2011 | SEMICONDUCTOR MEMORY DEVICE AND METHOD OF FABRICATING THE SAME                                                                                   |
| 1051987               | F1114KR                   | South Korea | 09/19/2003  | 07/20/2011 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME                                                                                       |
| 10-0185214            | FMA13-0011JP              | South Korea | 12/26/1994  | 12/23/1998 | TRANSIMPEDANCE AMPLIFIER                                                                                                                         |
| 10-0148528            | FMA13-0014JP              | South Korea | 03/21/1995  | 05/27/1998 | MICROCONTROLLER                                                                                                                                  |
| 10-0161308            | FMA13-0015JP DIV          | South Korea | 05/27/1994  | 08/24/1998 | POWER SOURCE CONNECTING CIRCUIT AND SWITCH IC FOR POWER SUPPLY LINE                                                                              |
| 199958                | FMA13-0017JP              | South Korea | 06/07/1995  | 03/08/1999 | SEMICONDUCTOR MEMORY DEVICE                                                                                                                      |
| 179998                | FMA13-0022JP              | South Korea | 08/30/1995  | 11/30/1998 | CLOCK SIGNAL GENERATOR                                                                                                                           |
| 1002963680000         | FMA13-0024JP DIV2         | South Korea | 10/18/1995  | 05/09/2001 | INFORMATION PROCESSING APPARATUS                                                                                                                 |
| 873880                | FMA13-00305KR             | South Korea | 09/14/2006  | 12/08/2008 | IMAGE PROCESSING APPARATUS AND METHOD FOR IMAGE RESIZING MATCHING DATA SUPPLY SPEED                                                              |
| 932723                | FMA13-00312KR             | South Korea | 10/26/2007  | 12/10/2009 | POWER SUPPLY CIRCUIT, POWER SUPPLY CONTROL CIRCUIT, AND POWER SUPPLY CONTROL METHOD                                                              |
| 1004303               | FMA13-00313KR             | South Korea | 05/04/2007  | 12/21/2010 | CONTROLLER FOR DC-DC CONVERTER                                                                                                                   |
| 1036867               | FMA13-00314KR             | South Korea | 07/10/2007  | 05/18/2011 | DC-DC CONVERTER                                                                                                                                  |
| 948328                | FMA13-00315KR             | South Korea | 09/27/2007  | 03/11/2010 | CONTROL CIRCUIT OF SYNCHRONOUS RECTIFICATION TYPE POWER SUPPLY UNIT, SYNCHRONOUS RECTIFICATION TYPE POWER SUPPLY UNIT AND CONTROL METHOD THEREOF |
| 955017                | FMA13-00317KR             | South Korea | 05/14/2007  | 04/20/2010 | DC-DC CONVERTER, CONTROL CIRCUIT FOR DC-DC CONVERTER, AND CONTROL METHOD FOR DC-DC CONVERTER                                                     |
| 937180                | FMA13-00319KR             | South Korea | 08/20/2007  | 01/08/2010 | CONTROL CIRCUIT OF POWER SUPPLY UNIT, POWER SUPPLY UNIT AND CONTROL METHOD THEREOF                                                               |
| 983069                | FMA13-00320KR             | South Korea | 01/22/2008  | 09/13/2010 | DC-DC CONVERTER, DC-DC CONVERTER CONTROL CIRCUIT, DC-DC CONVERTER CONTROL METHOD                                                                 |
| 968802                | FMA13-00321KR             | South Korea | 01/29/2008  | 07/01/2010 | POWER CIRCUIT, POWER CONTROLLING CIRCUIT, AND POWER CONTROLLING METHOD                                                                           |
| 964857                | FMA13-00322KR             | South Korea | 01/25/2008  | 06/11/2010 | FRACTIONAL FREQUENCY DIVIDER PLL DEVICE AND CONTROL METHOD THEREOF                                                                               |
| 927882                | FMA13-00323KR             | South Korea | 09/11/2007  | 11/13/2009 | METHOD AND CIRCUIT FOR CONTROLLING DC-DC CONVERTER                                                                                               |
| 1164308               | FMA13-00335KR             | South Korea | 03/14/2007  | 07/03/2012 | OUTPUT CIRCUIT                                                                                                                                   |
| 935840                | FMA13-00344JP DIV         | South Korea | 09/04/2003  | 12/30/2009 | CLOCK GENERATOR CIRCUIT, PLL AND CLOCK GENERATION METHOD                                                                                         |
| 1068182               | FMA13-00347KR             | South Korea | 01/25/2008  | 09/21/2011 | DETECTION CIRCUIT AND POWER SUPPLY SYSTEM                                                                                                        |
| 1086104               | FMA13-00350KR             | South Korea | 01/29/2008  | 11/16/2011 | DETECTION CIRCUIT AND POWER SUPPLY SYSTEM                                                                                                        |
| 1072337               | FMA13-00353JP             | South Korea | 11/02/2007  | 10/05/2011 | SIGNAL PROCESSOR UNIT AND COMMUNICATION DEVICE                                                                                                   |
| 100893704             | FMA13-00357JP DIV         | South Korea | 06/16/2006  |            | STEP-UP/STEP-DOWN TYPE DC-DC CONVERTER, AND CONTROL CIRCUIT AND CONTROL METHOD OF THE SAME                                                       |
| 1030100               | FMA13-00375KR             | South Korea | 05/18/2009  | 04/12/2011 | LINE PLOTTING METHOD                                                                                                                             |
| 674457                | FMA13-00381JP DIV         | South Korea | 04/23/2004  | 01/19/2007 | OPERATIONAL AMPLIFIER, LINE DRIVER, AND LIQUID CRYSTAL DISPLAY DEVICE                                                                            |
| 1002700330000         | FMA13-0038JP              | South Korea | 01/29/1997  | 07/27/2000 | CHARGING APPARATUS AND CURRENT/VOLTAGE DETECTOR FOR USE THEREIN                                                                                  |
| 1077190               | FMA13-00424KR             | South Korea | 11/19/2009  | 10/20/2011 | SEMICONDUCTOR MEMORY AND METHOD AND SYSTEM FOR ACTUATING SEMICONDUCTOR MEMORY                                                                    |
| 1002113420000         | FMA13-0042JP              | South Korea | 01/29/1997  | 05/03/1999 | OSCILLATOR AND PLL CIRCUIT EMPLOYING SAME                                                                                                        |
| 1002838410000         | FMA13-0043JP DIV          | South Korea | 11/29/1996  | 12/13/2000 | SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                                                 |
| 777196                | FMA13-00449JP DIV         | South Korea | 02/08/2002  | 11/12/2007 | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                                                                                                          |
| 647095                | FMA13-00451JP             | South Korea | 11/18/1999  | 11/10/2006 | SELECTOR CIRCUIT, AND SEMICONDUCTOR DEVICE AND LIQUID CRYSTAL DISPLAY DEVICE COMPRISING THE SAME                                                 |
| 253726                | FMA13-0048JP              | South Korea | 08/22/1997  | 01/26/2000 | A VOLTAGE BOOSTER CIRCUIT AND A VOLTAGE DROP CIRCUIT                                                                                             |
| 362762                | FMA13-0051JP              | South Korea | 05/28/1997  | 11/15/2002 | LEVEL CONVERTER AND SEMICONDUCTOR DEVICE                                                                                                         |
| 806157                | FMA13-00533JP DIV         | South Korea | 06/13/2006  | 02/15/2008 | POWER SOURCE CONTROL CIRCUIT, POWER SUPPLY DEVICE, AND CONTROL METHOD FOR THE SAME                                                               |
| 10-0652852            | FMA13-00542JP             | South Korea | 03/21/2000  | 11/24/2006 | RESET CIRCUIT AND PLL FREQUENCY SYNTHESIZER                                                                                                      |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY     | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                                                    |
|-----------------------|---------------------------|-------------|-------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 801513                | FMA13-00543KR             | South Korea | 11/21/2002  | 01/30/2008 | SEMICONDUCTOR DEVICE EQUIPPED WITH TRANSFER CIRCUIT FOR CASCADE CONNECTION                                                                                                                               |
| 2002-0015535          | FMA13-00544KR             | South Korea | 03/22/2002  |            | MODE SWITCHING METHOD FOR PLL CIRCUIT AND MODE CONTROL CIRCUIT FOR THE PLL CIRCUIT                                                                                                                       |
| 949131                | FMA13-00547JP             | South Korea | 12/02/2003  | 03/16/2010 | SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                                                                                                         |
| 894667                | FMA13-00551JP             | South Korea | 12/20/2002  | 04/16/2009 | BIPOLAR SUPPLY VOLTAGE GENERATOR AND SEMICONDUCTOR DEVICE FOR THE SAME                                                                                                                                   |
| 793678                | FMA13-00556JP             | South Korea | 06/16/2006  | 01/04/2008 | DC-DC CONVERTER CONTROL CIRCUIT, DC-DC CONVERTER, AND DC-DC CONVERTER CONTROL METHOD                                                                                                                     |
| 0905983               | FMA13-00561JP             | South Korea | 09/19/2006  | 06/26/2009 | CIRCUIT AND METHOD FOR CONTROLLING DC-DC CONVERTER CURRENT-CONTROLLED DC-DC CONVERTER CONTROL CIRCUIT, CURRENT-CONTROLLED DC-DC CONVERTER, AND METHOD FOR CONTROLLING CURRENT-CONTROLLED DC-DC CONVERTER |
| 793677                | FMA13-00562JP             | South Korea | 06/15/2006  | 01/04/2008 | CONTROL CIRCUIT OF POWER SUPPLY AND CONTROL METHOD OF THE POWER SUPPLY                                                                                                                                   |
| 10-0895252            | FMA13-00563KR             | South Korea | 10/20/2006  | 04/21/2009 | ELECTRONIC DEVICE INCORPORATING SYSTEM POWER SUPPLY UNIT AND METHOD FOR SUPPLYING POWER SUPPLY VOLTAGE                                                                                                   |
| 902809                | FMA13-00564KR             | South Korea | 08/30/2006  | 06/08/2009 | POWER SUPPLY SYSTEM AND METHOD FOR CONTROLLING OUTPUT VOLTAGE                                                                                                                                            |
| 963309                | FMA13-00565JP             | South Korea | 09/13/2007  | 06/04/2010 | DC-DC CONVERTER CONTROL CIRCUIT, DC-DC CONVERTER, POWER SUPPLY UNIT, AND DC-DC CONVERTER CONTROL METHOD                                                                                                  |
| 786162                | FMA13-00566JP             | South Korea | 10/18/2006  | 12/10/2007 | CONTROL CIRCUIT OF POWER SUPPLY, POWER SUPPLY AND CONTROL METHOD THEREOF                                                                                                                                 |
| 895472                | FMA13-00569JP             | South Korea | 09/27/2006  | 04/22/2009 | POWER CIRCUIT, POWER CONTROL CIRCUIT AND POWER CONTROL METHOD                                                                                                                                            |
| 1073595               | FMA13-00573KR             | South Korea | 01/28/2008  | 10/07/2011 | SKREW-REDUCTION CIRCUIT                                                                                                                                                                                  |
| 100381121             | FMA13-0063JP-3            | South Korea | 11/18/1997  | 04/08/2003 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND METHOD OF REPRODUCING DATA OF NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                        |
| 1003215950000         | FMA13-0065JP              | South Korea | 01/12/1999  | 01/09/2002 | MEMORY DEVICE                                                                                                                                                                                            |
| 1999-0008821          | FMA13-0067JP              | South Korea | 07/31/1998  |            | SEMICONDUCTOR DEVICE                                                                                                                                                                                     |
| 1003325100000         | FMA13-0069JP              | South Korea | 08/19/1998  | 04/01/2002 | OUTPUT CIRCUIT, LEVEL CONVERTER CIRCUIT, LOGIC CIRCUIT AND OPERATIONAL AMP CIRCUIT                                                                                                                       |
| 360704                | FMA13-0070JP              | South Korea | 12/28/1998  | 10/30/2002 | VOLTAGE SELECTOR AND A D/A CONVERTER, ESPECIALLY CAPABLE OF REDUCING RESPONSE TIME OF OUTPUT                                                                                                             |
| 1003164280000         | FMA13-0072JP DIV          | South Korea | 08/06/1999  | 11/21/2001 | VOLTAGE BOOSTING CIRCUIT                                                                                                                                                                                 |
| 586750                | FMA13-0073JP              | South Korea | 06/30/1999  | 05/29/2006 | LOCAL OSCILLATION CIRCUIT AND A RECEIVING CIRCUIT INCLUDING THE LOCAL OSCILLATION CIRCUIT                                                                                                                |
| 335748                | FMA13-0075JP              | South Korea | 05/27/1999  | 04/24/2002 | SYSTEM LSI HAVING COMMUNICATION FUNCTION                                                                                                                                                                 |
| 100334044             | FMA13-0078JP-1            | South Korea | 04/12/1999  | 04/11/2002 | DRIVER FOR LIQUID CRYSTAL DISPLAY PANEL                                                                                                                                                                  |
| 1998-0062701          | FMA13-0080KR              | South Korea | 12/31/1998  |            | SEMICONDUCTOR DEVICE HAVING CURRENT AUXILIARY CIRCUIT FOR OUTPUT CIRCUIT                                                                                                                                 |
| 600542                | FMA13-0082KR              | South Korea | 12/23/1999  | 07/06/2006 | SEMICONDUCTOR MEMORY AND OUTPUT SIGNAL CONTROL METHOD AND CIRCUIT IN SEMICONDUCTOR MEMORY                                                                                                                |
| 594409                | FMA13-0087JP              | South Korea | 12/22/1999  | 06/21/2006 | COMPARATOR                                                                                                                                                                                               |
| 722747                | FMA13-0089JP-1            | South Korea | 03/29/2000  | 05/22/2007 | VOLTAGE CONTROLLED OSCILLATOR CIRCUIT                                                                                                                                                                    |
| 629196                | FMA13-0089KR              | South Korea | 06/28/2006  | 09/21/2006 | LCD PANEL DRIVING CIRCUIT                                                                                                                                                                                |
| 614471                | FMA13-0091JP              | South Korea | 02/11/2000  | 08/14/2006 | FREQUENCY MEASUREMENT CIRCUIT                                                                                                                                                                            |
| 768050                | FMA13-0093JP DIV          | South Korea | 04/17/2002  | 10/11/2007 | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND ELECTRONIC CIRCUIT                                                                                                                                           |
| 596612                | FMA13-0096KR              | South Korea | 03/30/2000  | 06/27/2006 | CHARGING AND DISCHARGING CONTROL DEVICE                                                                                                                                                                  |
| 254478                | FMA13-0102JP DIV4         | South Korea | 09/01/1995  | 02/02/2000 | CHARGING-AND-DISCHARGING CONTROL DEVICE AND CONSTANT-VOLTAGE-AND-CONSTANT-CURRENT CONTROL CIRCUIT                                                                                                        |
| 264086                | FMA13-0102KR              | South Korea | 10/21/1999  | 05/25/2000 | CHARGE/DISCHARGE CONTROLLER AND CONSTANT-VOLTAGE CONSTANT-CURRENT CONTROL CIRCUIT                                                                                                                        |
| 303927                | FMA13-0102KR DIV1         | South Korea | 10/21/1999  | 07/16/2001 | CHARGE/DISCHARGE CONTROLLER AND CONSTANT-VOLTAGE CONSTANT-CURRENT CONTROL CIRCUIT                                                                                                                        |
| 297608                | FMA13-0102KR DIV2         | South Korea | 10/21/1999  | 05/23/2001 | DATA DRIVER AND DISPLAY DEVICE USING IT                                                                                                                                                                  |
| 647111                | FMA13-0104JP              | South Korea | 12/20/2000  | 11/10/2006 | SEMICONDUCTOR INTEGRATED CIRCUIT FOR DRIVING LIQUID CRYSTAL PANEL                                                                                                                                        |
| 100746933             | FMA13-0105JP-1            | South Korea | 01/16/2001  | 08/01/2007 | A GRADATION WIRING FOR DISPLAY, A DRIVER FOR A LIQUID CRYSTAL DISPLAY, AND A STRESS TEST METHOD FOR THE SAME DRIVER                                                                                      |
| 786167                | FMA13-0105KR              | South Korea | 03/28/2007  | 12/10/2007 | PLL SEMICONDUCTOR DEVICE WITH TESTABILITY, AND METHOD AND APPARATUS FOR TESTING SAME                                                                                                                     |
| 774266                | FMA13-0108JP              | South Korea | 02/15/2001  | 11/01/2007 | DOT-INVERSION DATA DRIVER FOR LIQUID CRYSTAL DISPLAY DEVICE                                                                                                                                              |
| 734337                | FMA13-0110JP              | South Korea | 04/13/2001  | 06/26/2007 | DC-DC CONVERTER, POWER SUPPLY CIRCUIT, METHOD FOR CONTROLLING DC-DC CONVERTER, AND METHOD FOR CONTROLLING POWER SUPPLY CIRCUIT                                                                           |
| 703643                | FMA13-0122JP DIV          | South Korea | 03/06/2002  | 03/29/2007 | OPERATIONAL AMPLIFIER HAVING OFFSET CANCEL FUNCTION                                                                                                                                                      |
| 783445                | FMA13-0129JP              | South Korea | 04/12/2002  | 12/03/2007 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                                                                                                                         |
| 689738                | FMA13-0132KR              | South Korea | 02/19/2002  | 02/26/2007 | REGULATOR CIRCUIT AND CONTROL METHOD THEREOF                                                                                                                                                             |
| 844052                | FMA13-0133JP              | South Korea | 04/12/2002  | 06/30/2008 | DC/DC CONVERTER CONTROL CIRCUIT AND DC/DC CONVERTER SYSTEM                                                                                                                                               |
| 840633                | FMA13-0136JP DIV          | South Korea | 05/28/2002  | 06/17/2008 | INTEGRATED CIRCUIT, LIQUID CRYSTAL DISPLAY APPARATUS, AND SIGNAL TRANSMISSION SYSTEM                                                                                                                     |
| 803184                | FMA13-0147JP              | South Korea | 01/09/2003  | 02/04/2008 | VOLTAGE-CONTROLLED OSCILLATOR, PLL CIRCUIT INCLUDING VOLTAGE CONTROLLED OSCILLATOR                                                                                                                       |
| 0933965               | FMA13-0150KR              | South Korea | 05/26/2003  | 12/17/2009 | DC-DC CONVERTER, DUTY-RATIO SETTING CIRCUIT AND ELECTRIC APPLIANCE USING THEM                                                                                                                            |
| 888412                | FMA13-0151JP              | South Korea | 02/07/2003  | 03/05/2009 |                                                                                                                                                                                                          |

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|-----------------------|---------------------------|-------------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 884012                | FMA13-0164JP              | South Korea | 05/21/2003  | 02/10/2009 | SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND SIGNAL TRANSMISSION SYSTEM                                                                                  |
| 891475                | FMA13-0169JP              | South Korea | 05/15/2003  | 03/26/2009 | FREQUENCY SYNTHESIZER CIRCUIT                                                                                                                         |
| 963310                | FMA13-0171JP              | South Korea | 08/14/2003  | 06/04/2010 | CONTROL CIRCUIT FOR DC/DC CONVERT                                                                                                                     |
| 101077745             | FMA13-0177JP-4            | South Korea | 12/24/2003  | 10/21/2011 | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT FOR GENERATING CLOCK SIGNAL CHANGED ACCORDING TO PERIOD, JITTER GENERATION CIRCUIT, AND SEMICONDUCTOR DEVICE |
| 670722                | FMA13-0178JP              | South Korea | 05/12/2005  | 01/11/2007 | MOS VARIABLE CAPACITIVE DEVICE                                                                                                                        |
| 647504                | FMA13-0200JP              | South Korea | 07/08/2004  | 11/13/2006 | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                                                                                                               |
| 665638                | FMA13-0211JP              | South Korea | 05/02/2005  | 12/29/2006 | CAPACITANCE DIFFERENCE DETECTING CIRCUIT AND MEMS SENSOR                                                                                              |
| 901400                | FMA13-0217JP              | South Korea | 02/28/2007  | 06/01/2009 | PLL FREQUENCY SYNTHESIZER                                                                                                                             |
| 616352                | FMA13-0224JP              | South Korea | 02/04/2005  | 08/21/2006 | SEMICONDUCTOR DEVICE                                                                                                                                  |
| 630855                | FMA13-0226JP              | South Korea | 11/23/2004  | 09/26/2006 | CIRCUIT AND METHOD FOR CONTROLLING DC-DC CONVERTER                                                                                                    |
| 637106                | FMA13-0228JP              | South Korea | 11/22/2004  | 10/16/2006 | CONTROL CIRCUIT OF DC-DC CONVERTER AND ITS CONTROL METHOD                                                                                             |
| 756613                | FMA13-0236JP              | South Korea | 06/09/2005  | 09/03/2007 | ANALOG FILTER CIRCUIT AND ADJUSTMENT METHOD THEREOF                                                                                                   |
| 2005-0041754          | FMA13-0238KR              | South Korea | 05/18/2005  |            | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT AND A METHOD OF CONTROLLING THEREOF                                                                          |
| 848843                | FMA13-0238KR DIV          | South Korea | 08/13/2007  | 07/22/2008 | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT AND A METHOD OF CONTROLLING THEREOF                                                                          |
| 766352                | FMA13-0243JP              | South Korea | 07/29/2005  | 10/05/2007 | AMPLIFIER CIRCUIT AND CONTROL METHOD THEREOF                                                                                                          |
| 804567                | FMA13-0256JP              | South Korea | 02/24/2006  | 02/12/2008 | SEMICONDUCTOR DEVICE                                                                                                                                  |
| 725475                | FMA13-0257JP              | South Korea | 02/27/2006  | 05/30/2007 | DC-DC CONVERTER AND ITS CONTROL METHOD, AND SWITCHING REGULATOR AND ITS CONTROL METHOD                                                                |
| 660958                | FMA13-0260JP              | South Korea | 12/07/2005  | 12/18/2006 | SUCCESSIVE APPROXIMATION A/D CONVERTER                                                                                                                |
| 698864                | FMA13-0265JP              | South Korea | 01/06/2006  | 03/16/2007 | CLOCK GENERATION CIRCUIT AND CLOCK GENERATION METHOD                                                                                                  |
| 758191                | FMA13-0266JP              | South Korea | 11/28/2005  | 09/06/2007 | CLOCK GENERATING CIRCUIT AND CLOCK GENERATING METHOD                                                                                                  |
| 744592                | FMA13-0273JP              | South Korea | 02/17/2006  | 07/25/2007 | DC-DC CONVERTER, DC-DC CONVERTER CONTROL CIRCUIT, AND DC-DC CONVERTER CONTROL METHOD                                                                  |
| 737793                | FMA13-0276JP              | South Korea | 04/13/2006  | 07/04/2007 | CONTROLLER AND CONTROL METHOD FOR DC-DC CONVERTER                                                                                                     |
| 725476                | FMA13-0278JP              | South Korea | 03/21/2006  | 05/30/2007 | STEP-UP TYPE DC-DC CONVERTER AND METHOD FOR CONTROLLING STEP-UP TYPE DC-DC CONVERTER                                                                  |
| 718905                | FMA13-0280JP              | South Korea | 04/07/2006  | 05/10/2007 | CONTROL CIRCUIT AND CONTROL METHOD FOR DC-DC CONVERTER                                                                                                |
| 769869                | FMA13-0281JP              | South Korea | 05/03/2006  | 10/18/2007 | CONTROL CIRCUIT FOR DC-DC CONVERTER AND CONTROL METHOD THEREFOR                                                                                       |
| 769102                | FMA13-0282KR              | South Korea | 09/28/2006  | 10/16/2007 | NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE, ERASE METHOD FOR SAME, AND TEST METHOD FOR SAME                                                             |
| 732141                | FMA13-0288KR              | South Korea | 08/29/2006  | 06/19/2007 | PULSE WIDTH MODULATION CIRCUIT                                                                                                                        |
| 742581                | FMA13-0289KR              | South Korea | 08/30/2006  | 07/19/2007 | PRESALER AND BUFFER                                                                                                                                   |
| 785721                | FMA13-0299JP              | South Korea | 08/14/2006  | 12/07/2007 | DELAY CONTROL CIRCUIT                                                                                                                                 |
| 776937                | FMA13-0300KR              | South Korea | 08/08/2006  | 11/09/2007 | COMMON INPUT/OUTPUT TERMINAL CONTROL CIRCUIT                                                                                                          |
| 805179                | FMA13-0302JP DIV          | South Korea | 06/07/2006  | 02/13/2008 | DC-DC CONVERTER AND CONTROL CIRCUIT FOR DC-DC CONVERTER                                                                                               |
| 924377                | G0063KR                   | South Korea | 11/14/2001  | 10/23/2009 | ACCURATE VERIFY APPARATUS AND METHOD FOR NOR FLASH MEMORY CELLS IN THE PRESENCE OF HIGH COLUMN LEAKAGE                                                |
| 7014898/2003          | G0259KR                   | South Korea | 02/19/2002  |            | FLASH MEMORY DEVICE WITH INCREASE OF EFFICIENCY DURING AN APDE (AUTOMATIC PROGRAM DISTURB AFTER ERASE) PROCESS                                        |
| 10-0941745            | G0391KR                   | South Korea | 06/10/2003  | 02/03/2010 | BUILT-IN-SELF-TEST (BIST) OF FLASH MEMORY CELLS AND IMPLEMENTATION OF BIST INTERFACE                                                                  |
| 10-0951463            | G0689KR                   | South Korea | 12/11/2002  | 03/30/2010 | SHALLOW TRENCH ISOLATION APPROACH FOR IMPROVED STI CORNER ROUNDING                                                                                    |
| 7010299/2005          | G0730KR                   | South Korea | 09/24/2003  |            | METHOD AND SYSTEM FOR REDUCING CONTACT DEFECTS USING NON CONVENTIONAL CONTACT FORMATION METHOD FOR SEMICONDUCTOR CELLS                                |
| 10-1071387            | G0752KR                   | South Korea | 01/08/2004  | 09/30/2011 | IMPROVED PERFORMANCE IN FLASH MEMORY DEVICES                                                                                                          |
| 10-0936087            | G0861KR                   | South Korea | 02/14/2003  | 12/31/2009 | IMPROVED ERASE METHOD FOR SINGLE SIDED MIRROR OPERATION                                                                                               |
| 10-0953993            | G0862KR                   | South Korea | 02/14/2003  | 04/13/2010 | REFRESH SCHEME FOR DYNAMIC PAGE PROGRAMMING                                                                                                           |
| 10-0935948            | G0864KR                   | South Korea | 02/14/2003  | 12/30/2009 | REFRESH SCHEME FOR DYNAMIC PAGE PROGRAMMING                                                                                                           |
| 10-0949198            | G0865KR                   | South Korea | 07/10/2003  | 03/23/2010 | MOCVD FORMATION OF Cu <sub>2</sub> S                                                                                                                  |
| 10-0960352            | G0866KR                   | South Korea | 04/22/2003  | 04/22/2010 | STEPPED PRE-ERASE VOLTAGE FOR MIRRORBIT ERASE                                                                                                         |
| 10-1037775            | G0871KR                   | South Korea | 07/10/2003  | 05/23/2011 | LATERAL DOPED CHANNEL                                                                                                                                 |
| 10-1024079            | G0878KR                   | South Korea | 07/10/2003  | 03/15/2011 | SILICON NITRADE CHARGE TRAPPING MEMORY DEVICE                                                                                                         |
| 7012003/2004          | G1255KR                   | South Korea | 02/05/2003  |            | PARTIAL PAGE PROGRAMMING OF MULTI LEVEL FLASH                                                                                                         |
| 10-0988353            | H0297KR                   | South Korea | 07/10/2003  | 10/11/2010 | CONTROL OF MEMORY ARRAYS UTILIZING ZENER DIODE-LIKE DEVICES                                                                                           |
| 915451                | H0325KR                   | South Korea | 09/19/2005  | 08/27/2009 | CONTROL OF MEMORY DEVICES POSSESSING VARIABLE RESISTANCE CHARACTERISTICS                                                                              |
| 10-1163681            | H0343KR                   | South Korea | 07/10/2003  | 07/02/2012 | MOCVD FORMATION OF Cu <sub>2</sub> S                                                                                                                  |
| 10-1415283            | H0346KR                   | South Korea | 02/11/2005  | 06/27/2014 | IN-SITU SURFACE TREATMENT FOR MEMORY CELL FORMATION                                                                                                   |
| 7016965/2005          | H0354KR                   | South Korea | 03/01/2004  |            | SPIN ON POLYMERS FOR ORGANIC MEMORY DEVICES                                                                                                           |
| 10-1134156            | H0368KR                   | South Korea | 02/11/2005  | 03/30/2012 | POLYMER DIELECTRICS FOR MEMORY ELEMENT ARRAY INTERCONNECT                                                                                             |
| 10-1018053            | H0385KR                   | South Korea | 09/08/2003  | 02/25/2011 | AN ORGANIC MEMORY DEVICE AND METHOD FOR FORMING A MEMORY CELL                                                                                         |
| 10-1087299            | H0416KR                   | South Korea | 09/23/2004  | 11/21/2011 | SIDEWALL FORMATION FOR HIGH DENSITY POLYMER MEMORY ELEMENT ARRAY                                                                                      |
| 7000426/2006          | H0422KR                   | South Korea | 05/11/2004  |            | METHOD AND SYSTEM FOR MANUFACTURING POLYMER MEMORY DEVICE IN VIA OPENING                                                                              |

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|-----------------------|---------------------------|-------------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------|
| 10-1043054            | H0423KR                   | South Korea | 09/16/2004  | 06/21/2011 | SELF ASSEMBLY OF CONDUCTING POLYMER FOR FORMATION OF POLYMER MEMORY CELL                                                  |
| 10-0988060            | H0434KR                   | South Korea | 07/10/2003  | 10/08/2010 | STACKED ORGANIC MEMORY DEVICES AND METHODS OF OPERATING AND FABRICATING                                                   |
| 7023230/2005          | H0437                     | South Korea | 05/11/2004  |            | PLANAR POLYMER MEMORY DEVICE                                                                                              |
| 7000425/2006          | H0442                     | South Korea | 05/21/2004  |            | ORGANIC MEMORY DEVICE AND METHODS OF USING AND MAKING THE DEVICE                                                          |
| 10-0960136            | H0514KR                   | South Korea | 06/10/2003  | 05/19/2010 | NITROGEN OXIDATION TO REDUCE ENCROACHMENT                                                                                 |
| 10-1027784            | H0541KR                   | South Korea | 07/15/2004  | 03/31/2011 | LOW POWER CHARGE PUMP                                                                                                     |
| 10-0957830            | H0570KR                   | South Korea | 07/24/2003  | 05/06/2010 | IMPROVED SYSTEM FOR PROGRAMMING A NON-VOLATILE MEMORY CELL                                                                |
| 10-0952972            | H0575KR                   | South Korea | 07/24/2003  | 04/07/2010 | IMPROVED PRE-CHARGE METHOD FOR READING A NON-VOLATILE MEMORY CELL ARRAY WITH STAGGERED LOCAL INTERCONNECT STRUCTURE       |
| 10-1012128            | H0576KR                   | South Korea | 09/16/2004  | 01/25/2011 | RECESS CHANNEL FLASH ARCHITECTURE FOR REDUCED SHORT CHANNEL EFFECT                                                        |
| 10974160000           | H0577KR                   | South Korea | 09/16/2004  | 12/15/2011 | IMPROVED METHOD FOR READING A NON-VOLATILE MEMORY CELL ADJACENT TO AN INACTIVE REGION OF A NON-VOLATILE MEMORY CELL ARRAY |
| 10-1060742            | H0625KR                   | South Korea | 01/08/2004  | 08/24/2011 | MEMORY DEVICE AND METHOD USING POSITIVE GATE STRESS TO RECOVER OVERERASED CELL                                            |
| 10-1099772            | H0626KR                   | South Korea | 09/16/2004  | 12/21/2011 | IMPROVED PERFORMANCE IN FLASH MEMORY DEVICES                                                                              |
| 10-1071965            | H0671KR                   | South Korea | 01/08/2004  | 10/04/2011 | CASCADE AMPLIFIER CIRCUIT FOR PRODUCING A FAST, STABLE AND ACCURATE BITLINE VOLTAGE                                       |
| 10-0955089            | H1203KR                   | South Korea | 07/10/2003  | 04/20/2010 | SELECTION CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS                                                                     |
| 10-1050521            | H1204KR                   | South Korea | 01/08/2004  | 07/13/2011 | CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS                                                                               |
| 10-0950569            | H1205KR                   | South Korea | 07/24/2003  | 03/24/2010 | PECVD SILICON-RICH OXIDE LAYER FOR REDUCED UV CHARGING                                                                    |
| 700275/2006           | H1368KR                   | South Korea | 06/18/2004  |            | NON-VOLATILE MEMORY DEVICE                                                                                                |
| 7023373/2005          | H1414KR                   | South Korea | 06/05/2004  |            | FLASH MEMORY DEVICE                                                                                                       |
| 10-1142990            | H1415KR                   | South Korea | 10/26/2004  | 04/27/2012 | CIRCUIT FOR FAST AND ACCURATE MEMORY READ OPERATIONS                                                                      |
| 7017062/2005          | H1513KR                   | South Korea | 03/01/2004  |            | MEMORY CELL STRUCTURE HAVING NITRIDE LAYER WITH REDUCED CHARGE LOSS AND METHOD FOR FABRICATING SAME                       |
| 10-1217260            | H1862KR                   | South Korea | 08/31/2004  | 12/24/2012 | FAST, ACCURATE AND LOW POWER SUPPLY VOLTAGE BOOSTER USING A/D CONVERTER                                                   |
| 7018828/2005          | H1892JP                   | South Korea | 03/08/2004  |            | MEMORY CELL                                                                                                               |
| 10-0860134            | H1979KR                   | South Korea | 08/13/2001  | 09/18/2008 | METHODS AND APPARATUS FOR WORDLINE PROTECTION IN FLASH MEMORY DEVICES                                                     |
| 10-1056151            | H1984KR                   | South Korea | 02/11/2005  | 08/04/2011 | POCKET IMPLANT FOR COMPLEMENTARY BIT DISTURB IMPROVEMENT AND CHARGING IMPROVEMENT OF SONOS MEMORY CELL                    |
| 10-1135715            | H1985KR                   | South Korea | 12/17/2004  | 04/04/2012 | METHOD OF FORMING NARROWLY SPACED FLASH MEMORY CONTACT OPENINGS                                                           |
| 7003268/2007          | H1990KR                   | South Korea | 04/29/2005  |            | BITLINE IMPLANT UTILIZING DUAL POLY                                                                                       |
| 10-1136140            | H1993KR                   | South Korea | 02/11/2005  | 04/05/2012 | NON-CRITICAL COMPLEMENTARY MASKING METHOD FOR POLY-1 DEFINITION IN FLASH MEMORY DEVICE FABRICATION                        |
| 7025572/2007          | H1998                     | South Korea | 04/04/2006  |            | USE OF SUPERCRITICAL FLUID TO DRY WAFER AND CLEAN LANS IN IMMERSION LITHOGRAPHY                                           |
| 10-2008-7002830       | H2114KR                   | South Korea | 06/23/2006  |            | SEMICONDUCTOR DEVICE AND THE METHOD FOR FABRICATING THEREOF                                                               |
| 323622                | JC137496KR                | South Korea | 05/29/1997  | 01/25/2002 | HIGH YIELD, HIGH PERFORMANCE SEMICONDUCTOR PROCESS FLOW FOR NAND FLASH MEMORY PRODUCTS                                    |
| 627928                | JC684497KR                | South Korea | 11/29/1999  | 09/18/2006 | ELIMINATION OF POLY-CAP FOR EASY POLY1 CONTACT FOR NAND PRODUCT                                                           |
| 554089                | JC688497KR                | South Korea | 02/11/1999  | 02/14/2006 | PROCESS FOR FABRICATING AN INTEGRATED CIRCUIT WITH A SELF-ALIGNED CONTACT                                                 |
| 578579                | JC818597KR                | South Korea | 12/17/1998  | 05/03/2006 | PORTABLE WIRELESS DATA STORAGE DEVICE                                                                                     |
| 10-1238431            | JDE0584KR                 | South Korea | 04/21/2006  | 02/22/2013 | METHOD FOR READING NON-VOLATILE MEMORY CELLS                                                                              |
| 10-2008-0066467       | P-6628US CIP              | South Korea | 08/17/2006  |            | NON-VOLATILE SEMICONDUCTOR MEMORY CELL UTILIZING ASYMMETRICAL CHARGE TRAPPING                                             |
| 433994                | P-878KR                   | South Korea | 06/24/1997  | 05/21/2004 | A SYSTEM AND METHOD OF ERASE VOLTAGE CONTROL DURING MULTIPLE SECTOR ERASE OF A FLASH MEMORY DEVICE                        |
| 10-0953330            | SE0002KR                  | South Korea | 03/11/2003  | 04/09/2010 | METHOD, APPARATUS, AND MANUFACTURE FOR FLASH MEMORY ADAPTIVE ALGORITHM                                                    |
| 10-2014-7037178       | SP09-0030KR               | South Korea | 05/24/2013  |            | HIGH SPEED SERIAL PERIPHERAL INTERFACE MEMORY SUBSYSTEM                                                                   |
| 10-2014-7018662       | SP09-0056JP               | South Korea | 12/07/2012  |            | POWER SAVINGS APPARATUS AND METHOD FOR MEMORY DEVICE USING DELAY LOCKED LOOP                                              |
| 10-2015-7005488       | SP09-0058KR               | South Korea | 07/31/2013  |            | SELF-ALIGNED NAND FLASH SELECT-GATE WORDLINES FOR SPACER DOUBLE PATTERNING                                                |
| 10-2013-7018650       | SP10-0007KR               | South Korea | 12/17/2010  |            | EDGE ROUNDED FIELD EFFECT TRANSISTORS AND METHODS OF MANUFACTURING                                                        |
| 10-2013-7019143       | SP10-0008KR               | South Korea | 12/19/2011  |            | PROCESS MARGIN ENGINEERING IN CHARGE TRAPPING FIELD EFFECT TRANSISTORS                                                    |
| 10-2013-7019144       | SP10-0009KR               | South Korea | 12/19/2011  |            | MEMORY WITH EXTENDED CHARGE TRAPPING LAYER                                                                                |
| 10-2013-7020128       | SP10-0012KR               | South Korea | 12/29/2011  |            | SOFT ERROR RESISTANT CIRCUITRY                                                                                            |
| 10-2014-7034452       | SP11-0015JP               | South Korea | 05/14/2013  |            | APPARATUS AND METHOD FOR A REDUCED PIN COUNT (RPC) MEMORY BUS INTERFACE INCLUDING A READ DATA STROBE SIGNAL               |
| 10-2013-0027798       | SP11-0021KR               | South Korea | 03/15/2013  |            | CONTINUOUS READ BURST SUPPORT AT HIGH CLOCK RATES                                                                         |
| 10-2013-0008915       | SP11-0034JP               | South Korea | 01/25/2013  |            | ACOUSTIC PROCESSING UNIT                                                                                                  |
| 10-2014-7020293       | SP11-0042KR               | South Korea | 12/14/2012  |            | ADAPTIVELY PROGRAMMING OR ERASING FLASH MEMORY BLOCKS                                                                     |
| 10-2014-7030822       | SP12-0013KR               | South Korea | 04/01/2013  |            | LEAKAGE REDUCING WRITELINE CHARGE PROTECTION CIRCUIT                                                                      |
| 10-2015-7003190       | SP12-0017KR               | South Korea | 07/08/2013  |            |                                                                                                                           |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY     | FILING DATE | ISSUE DATE | TITLE                                                                                                                                        |
|-----------------------|---------------------------|-------------|-------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 10-2015-7005000       | SP12-0021KR               | South Korea | 07/29/2013  |            | BITLENE VOLTAGE REGULATION IN NON-VOLATILE MEMORY                                                                                            |
| 10-2015-0025999       | SP13-0036KR               | South Korea | 02/24/2015  |            | MEMORY SUBSYSTEM WITH WRAPPED-TO-CONTINUOUS READ                                                                                             |
| 10-2014-7025593       | SPNSP110027KR             | South Korea | 02/08/2013  |            | IMPROVING REDUNDANCY LOADING EFFICIENCY                                                                                                      |
| 431551                | TT0497JP                  | South Korea | 02/14/1996  | 05/03/2004 | A NON-VOLATILE MEMORY DEVICES HAVING A FLOATING GATE WITH ENHANCED CHANGE RETENTION                                                          |
| 14127/1996            | TT0607JP                  | South Korea | 05/01/1996  |            | METHOD FOR READING A NON-VOLATILE MEMORY ARRAY                                                                                               |
| 1116239               | D168                      | Spain       | 08/16/1999  | 05/15/2002 | SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                                |
| 1203378               | C725497                   | Sweden      | 08/01/2000  | 06/30/2004 | CIRCUIT IMPLEMENTATION TO QUENCH BIT LINE LEAKAGE CURRENT IN PROGRAM AND AUTO PROGRAM DISTURB MODE IN FLASH EPROM USING RESISTOR SOURCE LOAD |
| 085865                | A938/2033TW               | Taiwan      | 03/10/1994  | 04/11/1997 | PROGRAMMED REFERENCE                                                                                                                         |
| 094852                | A960/2054TW               | Taiwan      | 07/26/1994  | 09/25/1998 | METHOD AND APPARATUS FOR PROGRAMMING MEMORY DEVICES                                                                                          |
| 173010                | AF01002TW                 | Taiwan      | 10/16/2000  | 07/02/2003 | LOW VOLTAGE READ CASCODE FOR 2V/3V AND DIFFERENT BANK COMBINATIONS WITHOUT METAL OPTIONS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE    |
| 1235380               | AF01027TW                 | Taiwan      | 07/24/2000  | 07/01/2005 | OUTPUT MULTIPLEXING IMPLEMENTATION FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE                                                          |
| 161524                | AF01036TW                 | Taiwan      | 02/19/2001  | 12/10/2002 | WORDLINE DRIVER FOR FLASH MEMORY READ MODE                                                                                                   |
| 175452                | AF01054TW                 | Taiwan      | 10/18/2000  | 08/01/2003 | HIGH TEMPERATURE OXIDE DEPOSITION PROCESS FOR FABRICATING AN ONO FLOATING-GATE ELECTRODE IN A TWO BIT EEPROM DEVICE                          |
| 157893                | AF01064TW                 | Taiwan      | 03/21/2001  | 10/14/2002 | METHOD FOR FORMING HIGH QUALITY MULTIPLE THICKNESS OXIDE LAYERS USING HIGH TEMPERATURE DESCUM                                                |
| 190221                | AF01066TW                 | Taiwan      | 03/22/2001  | 03/08/2004 | METHOD FOR FORMING HIGHQUALITY MULTIPLE THICKNESS OXIDE LAYERS BY REDUCING DESCUM INDUCED DEFECTS                                            |
| 170606                | AF01072TW                 | Taiwan      | 01/18/2001  | 05/23/2003 | VOLTAGE BOOST LEVEL CLAMPING CIRCUIT FOR A FLASH MEMORY                                                                                      |
| 183451                | AF01073TW                 | Taiwan      | 08/27/2001  | 12/08/2003 | WORD LINE DECODING ARCHITECTURE IN A FLASH MEMORY                                                                                            |
| 207260                | AF01074TW                 | Taiwan      | 06/06/2001  | 11/15/2004 | POWER SAVING SCHEME FOR BURST MODE IMPLEMENTATION DURING READING OF DATA FROM A MEMORY DEVICE                                                |
| 1222073               | AF01075TW                 | Taiwan      | 03/14/2001  | 10/11/2004 | MULTIPLE BANK SIMULTANEOUS OPERATION FOR A FLASH MEMORY                                                                                      |
| 167339                | AF01076TW                 | Taiwan      | 04/09/2001  | 05/30/2001 | BURST ARCHITECTURE FOR A FLASH MEMORY                                                                                                        |
| 179541                | AF01078TW                 | Taiwan      | 07/20/2001  | 10/09/2003 | BURST READ INCORPORATING OUTPUT BASED REDUNDANCY                                                                                             |
| 173070                | AF01081TW                 | Taiwan      | 08/09/2001  | 07/02/2003 | BURST READ WORDLINE BOOSTING                                                                                                                 |
| 168872                | AF01085TW                 | Taiwan      | 06/11/2001  | 04/23/2003 | METHOD TO REDUCE CAPACITIVE LOADING IN FLASH MEMORY X-DECODER FOR ACCURATE VOLTAGE CONTROL AT WORDLINES AND SELECT LINES                     |
| 167308                | AF01086TW                 | Taiwan      | 09/29/2000  | 04/03/2003 | WORD LINE TRACKING IN WHOLE CHIP                                                                                                             |
| 153870                | AF01088TW                 | Taiwan      | 03/07/2001  | 08/06/2002 | SINGLE TUNNEL GATE OXIDATION PROCESS FOR FABRICATING NAND FLASH MEMORY                                                                       |
| 197919                | AF01090TW                 | Taiwan      | 03/08/2002  | 07/06/2004 | I/O PARTITIONING AND METHODOLOGY TO REDUCE BAND-TO-BAND TUNNELING CURRENT DURING ERASE                                                       |
| 203031                | AF01091TW                 | Taiwan      | 10/09/2002  | 09/27/2004 | DRAIN SIDE SENSING SCHEME FOR VIRTUAL GROUND FLASH EPROM ARRAY WITH ADJACENT BIT CHARGE AND HOLD                                             |
| 192693                | AF01094TW                 | Taiwan      | 06/12/2002  | 04/08/2004 | VOLTAGE BOOST CIRCUIT USING SUPPLY VOLTAGE DETECTION TO COMPENSATE FOR SUPPLY VOLTAGE VARIATIONS IN READ MODE VOLTAGES                       |
| 201733                | AF01096TW                 | Taiwan      | 03/13/2002  | 09/08/2004 | SOFT PROGRAM AND SOFT PROGRAM VERIFY OF THE CORE CELLS IN FLASH MEMORY ARRAY                                                                 |
| 172356                | AF01112TW                 | Taiwan      | 11/27/2001  | 06/17/2003 | PLANAR STRUCTURE FOR NON-VOLATILE MEMORY DEVICES                                                                                             |
| 1286755               | AF01116TW                 | Taiwan      | 03/28/2003  | 09/11/2007 | SYSTEM AND METHOD FOR MULTI-BIT FLASH READS USING DUAL DYNAMIC REFERENCES                                                                    |
| 1267942               | AF01124TW                 | Taiwan      | 12/18/2002  | 12/01/2006 | MONOS DEVICE HAVING BURIED METAL SILICIDE BIT LINE                                                                                           |
| 1295835               | AF01132TW                 | Taiwan      | 02/13/2003  | 04/11/2008 | HARD MASK PROCESS FOR MEMORY DEVICE WITHOUT BITLENE SHORTS                                                                                   |
| 1261338               | AF01134TW                 | Taiwan      | 03/24/2003  | 09/01/2006 | METHOD OF MAKING MEMORY WORDLINE HARD MASK EXTENSION                                                                                         |
| 1326878               | AF01165TW                 | Taiwan      | 07/30/2003  | 07/01/2010 | SYSTEM AND METHOD FOR Y-DECODEING IN A FLASH MEMORY DEVICE                                                                                   |
| 1369682               | AF01169TW                 | Taiwan      | 06/17/2004  | 08/01/2012 | MEMORY WITH A CORE-BASED VIRTUAL GROUND AND DYNAMIC REFERENCE SENSING SCHEME                                                                 |
| 1337354               | AF01182TW                 | Taiwan      | 06/30/2004  | 02/11/2011 | MEMORY DEVICE HAVING HIGH WORK FUNCTION GATE AND METHOD OF ERASING SAME                                                                      |
| 1334631               | AF01186TW                 | Taiwan      | 01/19/2004  | 12/11/2010 | CHARGE-TRAPPING MEMORY ARRAYS RESISTANT TO DAMAGE FROM CONTACT HOLE FORMATION                                                                |
| 1339437               | AF01209TW                 | Taiwan      | 04/23/2004  | 03/21/2011 | METHOD FOR REDUCING SHORT CHANNEL EFFECTS IN MEMORY CELLS AND RELATED STRUCTURE                                                              |
| 94100806              | AF01214TW                 | Taiwan      | 01/12/2005  |            | EFFICIENT USE OF WAFER AREA WITH DEVICE UNDER THE PAD APPROACH                                                                               |
| 1362114               | AF01220TW                 | Taiwan      | 01/13/2005  | 04/11/2012 | STRUCTURE AND METHOD FOR LOW VSS RESISTANCE AND REDUCED DIBL IN A FLOATING GATE MEMORY CELL                                                  |
| 368954                | AF01232TW                 | Taiwan      | 07/04/2005  | 07/21/2012 | BOND PAD STRUCTURE FOR COPPER METALLIZATION HAVING INCREASED RELIABILITY AND METHOD FOR FABRICATING SAME                                     |
| 95109801              | AF01278TW                 | Taiwan      | 03/22/2006  |            | TEMPERATURE COMPENSATION OF THIN FILM DIODE VOLTAGE THRESHOLD IN MEMORY SENSING CIRCUIT                                                      |
| 1392098               | AF01279TW                 | Taiwan      | 09/07/2005  | 04/01/2013 | VERTICAL JFET AS USED FOR SELECTIVE COMPONENT IN MEMORY ARRAY                                                                                |
| 1355089               | AF01286TW                 | Taiwan      | 03/22/2006  | 12/21/2011 | VARIABLE BREAKDOWN CHARACTERISTIC DIODE                                                                                                      |
| 95124125              | AF01293TW                 | Taiwan      | 07/03/2006  |            | PREAMORPHIZATION TO MINIMIZE VOID FORMATION                                                                                                  |

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| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                            |
|-----------------------|--------------------------|---------|-------------|------------|------------------------------------------------------------------------------------------------------------------|
| I375952               | AF01306TW                | Taiwan  | 07/01/2005  | 11/01/2012 | SWITCHABLE MEMORY DIODE- A NEW MEMORY DEVICE                                                                     |
| I392081               | AF01310TW                | Taiwan  | 09/11/2006  | 04/01/2013 | SEMICONDUCTOR MEMORY DEVICE COMPRISING ONE OR MORE<br>INJECTING BILAYER ELECTRODES                               |
| I401684               | AF01320TW                | Taiwan  | 08/12/2005  | 07/11/2013 | SYSTEMS AND METHODS FOR ADJUSTING PROGRAMMING<br>THRESHOLDS OF POLYMER MEMORY CELLS                              |
| I368911               | AF01321JP                | Taiwan  | 08/12/2005  | 07/21/2012 | METHOD OF PROVIDING VARIABLE RETENTION TIME TO A MEMORY<br>DEVICE AND A MEMORY DEVICE THAT USES THE METHOD       |
| I405210               | AF01329TW                | Taiwan  | 08/30/2005  | 08/11/2013 | NON-VOLATILE MEMORY DEVICE AND ERASING METHOD THEREFOR                                                           |
| 102121311             | AF01329TW DIV            | Taiwan  | 08/30/2005  |            | NON-VOLATILE MEMORY DEVICE AND ERASING METHOD THEREFOR                                                           |
| 102121312             | AF01329TW DIV2           | Taiwan  | 08/30/2005  |            | NON-VOLATILE MEMORY DEVICE AND ERASING METHOD THEREFOR                                                           |
| I395229               | AF01338TW                | Taiwan  | 10/20/2005  | 05/01/2013 | METHOD AND APPARATUS FOR SETTING OPERATIONAL<br>INFORMATION OF A NON-VOLATILE MEMORY                             |
| 95129323              | AF01360TW                | Taiwan  | 08/10/2006  |            | METHOD OF FORMING GATE ELECTRODE STRUCTURES                                                                      |
| I367488               | AF01361TW                | Taiwan  | 07/01/2005  | 07/01/2012 | ERASE DISTRIBUTION IMPROVEMENT WITH ENHANCED DUMMY<br>WORDLINES IN FLASH MEMORY                                  |
| I373047               | AF01365TW                | Taiwan  | 07/29/2005  | 09/21/2012 | FLASH MEMORY UNIT AND METHOD OF PROGRAMMING A FLASH<br>MEMORY DEVICE                                             |
| I382473               | AF01379TW                | Taiwan  | 08/02/2005  | 01/11/2013 | MEMORY CELL WITH REDUCED DIBL AND VSS RESISTANCE                                                                 |
| 402857                | AF01383TW                | Taiwan  | 09/21/2005  | 07/21/2013 | READ APPROACH FOR MULTI-LEVEL VIRTUAL GROUND MEMORY                                                              |
| I363345               | AF01386TW                | Taiwan  | 06/02/2005  | 05/01/2012 | ERASE ALGORITHM FOR MULTI-LEVEL BIT FLASH MEMORY                                                                 |
| 94127445              | AF01411TW                | Taiwan  | 08/12/2005  |            | DEPOSITION OF HARD-MASK WITH MINIMIZED HILLOCKS AND<br>BUBBLES                                                   |
| I423260               | AF01412TW                | Taiwan  | 07/27/2005  | 01/11/2014 | METHOD AND APPARATUS FOR INFORMATION SETTING IN A NON-<br>VOLATILE MEMORY DEVICE                                 |
| 102147874             | AF01412TW DIV            | Taiwan  | 07/27/2005  |            | METHOD AND APPARATUS FOR INFORMATION SETTING IN A NON-<br>VOLATILE MEMORY DEVICE                                 |
| 395228                | AF01438TW                | Taiwan  | 12/23/2005  | 05/01/2013 | METHOD AND APPARATUS FOR APPLYING BIAS TO A STORAGE<br>DEVICE                                                    |
| 397914                | AF01453TW                | Taiwan  | 04/06/2005  | 06/01/2013 | METHOD AND SYSTEMS FOR HIGH WRITE PERFORMANCE IN MULTI-<br>BIT FLASH MEMORY DEVICES                              |
| I404173               | AF01455TW                | Taiwan  | 11/29/2005  | 08/01/2013 | NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                         |
| 95114640              | AF01459TW                | Taiwan  | 04/25/2006  |            | SELF-ALIGNED STI SONOS                                                                                           |
| 405300                | AF01468TW                | Taiwan  | 10/20/2005  | 08/11/2013 | SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME                                                          |
| 420649                | AF01479TW                | Taiwan  | 12/27/2005  | 12/21/2013 | SEMICONDUCTOR DEVICE AND METHOD FOR CONTROLLING<br>OPERATION THEREOF                                             |
| I420719               | AF01484TW                | Taiwan  | 02/07/2006  | 12/21/2013 | MEMORY ELEMENT USING ACTIVE LAYERS OF BLENDED MATERIALS                                                          |
| I404062               | AF01485TW                | Taiwan  | 12/22/2005  | 08/01/2013 | METHOD OF PROGRAMMING, READING AND ERASING MEMORY-<br>DIODE IN A MEMORY-DIODE ARRAY                              |
| 95111152              | AF01490TW                | Taiwan  | 03/30/2006  |            | WRITE-ONCE READ-MANY TIMES MEMORY                                                                                |
| 402840                | AF01491TW                | Taiwan  | 11/14/2005  | 07/21/2013 | DIODE ARRAYS ARCHITECTURE FOR ADDRESSING NANOSCALE<br>RESISTIVE MEMORY ARRAYS                                    |
| 95110016              | AF01492TW                | Taiwan  | 03/23/2006  |            | MEMORY DEVICE WITH IMPROVED DATA RETENTION                                                                       |
| 94139371              | AF01500TW                | Taiwan  | 11/10/2005  |            | PROTECTION OF ACTIVE LAYERS OF MEMORY CELLS DURING<br>PROCESSING OF OTHER ELEMENTS                               |
| 95124259              | AF01501TW                | Taiwan  | 07/04/2006  |            | MEMORY DEVICE WITH IMPROVED DATA RETENTION                                                                       |
| 95124260              | AF01514TW                | Taiwan  | 07/04/2006  |            | STACKABLE MEMORY DEVICE AND ORGANIC TRANSISTOR<br>STRUCTURE                                                      |
| 387200                | AF01523TW                | Taiwan  | 12/22/2005  | 02/21/2013 | SENSE AMPLIFIER WITH HIGH VOLTAGE SWING                                                                          |
| 95107722              | AF01524TW                | Taiwan  | 03/08/2006  |            | DECODER FOR MEMORY DEVICE                                                                                        |
| I440189               | AF01535TW                | Taiwan  | 07/31/2006  | 06/01/2014 | SONOS MEMORY CELL HAVING HIGH-K DIELECTRIC                                                                       |
| 95138512              | AF01543TW                | Taiwan  | 10/19/2006  |            | BIT LINE IMPLANT                                                                                                 |
| I422016               | AF01543TW DIV            | Taiwan  | 10/20/2010  | 01/01/2014 | BIT LINE IMPLANT                                                                                                 |
| I402916               | AF01548TW                | Taiwan  | 10/18/2006  | 07/21/2013 | TRIPLE LAYER ANTI-REFLECTIVE HARD MASK                                                                           |
| 95136503              | AF01553TW                | Taiwan  | 10/02/2006  |            | CONTACT SPACER FORMATION USING ATOMIC LAYER DEPOSITION                                                           |
| I407532               | AF01578TW                | Taiwan  | 10/31/2005  | 09/01/2013 | SYSTEM AND METHOD FOR PROTECTING SEMICONDUCTOR DEVICES                                                           |
| 95124416              | AF01586TW                | Taiwan  | 07/05/2006  |            | METHOD FOR PROGRAMMING A MEMORY DEVICE                                                                           |
| 396251                | AF01602TW                | Taiwan  | 07/31/2006  | 05/11/2013 | SYSTEM AND METHOD FOR IMPROVING MESA WIDTH IN A<br>SEMICONDUCTOR DEVICE                                          |
| 95110020              | AF01625TW                | Taiwan  | 03/23/2006  |            | HIGH K STACK FOR NON-VOLATILE MEMORY                                                                             |
| I440141               | AF01638TW                | Taiwan  | 07/31/2006  | 06/01/2014 | MEMORY DEVICE WITH BARRIER LAYER                                                                                 |
| I378552               | AF01653TW                | Taiwan  | 01/24/2006  | 12/01/2012 | SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF                                                              |
| 392079                | AF01663TW                | Taiwan  | 01/27/2006  | 04/01/2013 | CARRIER FOR STACKED TYPE SEMICONDUCTOR DEVICE AND<br>METHOD OF FABRICATING STACKED TYPE SEMICONDUCTOR<br>DEVICES |
| I337358               | AF01668TW                | Taiwan  | 09/13/2006  | 02/11/2011 | HIGH PERFORMANCE FLASH MEMORY DEVICE CAPABLE OF HIGH<br>DENSITY DATA STORAGE                                     |
| I342025               | AF01669TW                | Taiwan  | 09/15/2006  | 05/11/2011 | MULTI-BIT FLASH MEMORY DEVICE HAVING IMPROVED PROGRAM<br>RATE                                                    |
| I379301               | AF01673TW                | Taiwan  | 09/15/2006  | 12/11/2012 | FLASH MEMORY PROGRAMMING USING AN INDICATION BIT TO<br>INTERPRET STATE                                           |
| I351034               | AF01682TW                | Taiwan  | 12/29/2006  | 10/21/2011 | RANDOM CACHE READ USING A DOUBLE MEMORY                                                                          |
| I407440               | AF01698TW                | Taiwan  | 01/27/2006  | 09/01/2013 | SEMICONDUCTOR DEVICE, ADDRESS ALLOTING METHOD, AND<br>VERIFICATION METHOD                                        |
| 102127390             | AF01698TW DIV            | Taiwan  | 01/27/2006  |            | SEMICONDUCTOR DEVICE, ADDRESS ALLOTING METHOD, AND<br>VERIFICATION METHOD                                        |

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|-----------------------|---------------------------|---------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------|
| 95111153              | AF01713TW                 | Taiwan  | 03/30/2006  |            | SEMICONDUCTOR DEVICE AND METHOD OF GENERATING A<br>REFERENCE VOLTAGE THEREFOR                                                   |
| I383499               | AF01735TW                 | Taiwan  | 04/27/2006  | 01/21/2013 | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD<br>THEREFOR                                                                       |
| 95108917              | AF01743TW                 | Taiwan  | 03/16/2006  |            | MEMORY DEVICE AND ITS CONTROL METHOD                                                                                            |
| 95133426              | AF01746                   | Taiwan  | 09/06/2006  |            | METHOD FOR FORMING SPACERS BETWEEN BITLINES IN A VIRTUAL<br>GROUND MEMORY ARRAY AND REALTED STRUCTURE                           |
| 95136177              | AF01757JP                 | Taiwan  | 09/29/2006  |            | STORAGE DEVICE AND CONTROL METHOD THEREOF                                                                                       |
| I371851               | AF01766TW                 | Taiwan  | 03/20/2007  | 09/01/2012 | MEMORY CELL SYSTEM USING SILICON-RICH NITRIDE                                                                                   |
| I334608               | AF01770TW                 | Taiwan  | 12/06/2006  | 12/11/2010 | A NON VOLATILE MEMORY DEVICE AND ITS CONTROL METHOD                                                                             |
| I 348201              | AF01772TW                 | Taiwan  | 09/22/2006  | 09/01/2011 | METHOD FOR FORMING NARROW STRUCTURES IN A<br>SEMICONDUCTOR DEVICE                                                               |
| I 344176              | AF01777TW                 | Taiwan  | 10/20/2006  | 06/21/2011 | METHOD FOR MANUFACTURING A SEMICONDUCTOR COMPONENT                                                                              |
| I368992               | AF01810TW                 | Taiwan  | 03/16/2007  | 07/21/2012 | VERTICAL SEMICONDUCTOR DEVICE                                                                                                   |
| 371081                | AF01812TW                 | Taiwan  | 10/02/2006  | 08/21/2012 | SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF                                                                             |
| I338841               | AF01828TW                 | Taiwan  | 10/02/2006  | 03/11/2011 | SYSTEM THAT FACILITATES DATE TRANSFER BETWEEN DIFFERENT<br>CLOCK DOMAINS                                                        |
| I362099               | AF01829TW                 | Taiwan  | 09/28/2006  | 04/11/2012 | PACKAGE USING AC INTERPOSERS                                                                                                    |
| 96137782              | AF01836TW                 | Taiwan  | 10/09/2007  |            | NORNAND                                                                                                                         |
| 420526                | AF01840TW                 | Taiwan  | 10/04/2006  | 12/21/2013 | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREFOR                                                                                |
| 102141615             | AF01840TW DIV             | Taiwan  | 10/04/2006  |            | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREFOR                                                                                |
| I365454               | AF01853TW                 | Taiwan  | 10/19/2006  | 06/01/2012 | MEMORY ARRAY                                                                                                                    |
| I 354290              | AF01854TW                 | Taiwan  | 04/25/2007  | 12/11/2011 | SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD                                                                                     |
| I404194               | AF01869TW                 | Taiwan  | 12/14/2007  | 08/01/2013 | CONVEX SHAPED THIN-FILM-TRANSISTOR DEVICE                                                                                       |
| 366832                | AF01889TW                 | Taiwan  | 11/28/2007  | 06/21/2012 | MEMORY DEVICE AND PASSWORD STORING METHOD THEREOF                                                                               |
| I376781               | AF01890TW                 | Taiwan  | 12/24/2007  | 11/11/2012 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE<br>SAME                                                                    |
| I 344183              | AF01895TW                 | Taiwan  | 01/17/2007  | 06/21/2011 | SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD                                                                                     |
| I359425               | AF01897                   | Taiwan  | 12/28/2006  |            | SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE<br>SAME                                                                      |
| I376024               | AF01898TW                 | Taiwan  | 12/14/2007  | 11/01/2012 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE<br>SAME (AS AMENDED)                                                      |
| I373839               | AF01906TW                 | Taiwan  | 12/24/2007  | 10/01/2012 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING SAME                                                                           |
| I375172               | AF01907TW                 | Taiwan  | 04/09/2007  | 10/21/2012 | MULTI MEDIA CARD WITH HIGH STORAGE CAPACITY                                                                                     |
| I348741               | AF01908TW                 | Taiwan  | 12/06/2006  | 09/11/2011 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE<br>SAME                                                                    |
| 96132834              | AF01938TW                 | Taiwan  | 09/04/2007  |            | DAMASCENE METAL-INSULATOR-METAL (MIM) DEVICE WITH<br>IMPROVED SCALEABILITY                                                      |
| I357079               | AF01944TW                 | Taiwan  | 11/27/2007  | 01/21/2012 | METHODS OF PROGARMING AND ERASING RESISTIVE MEMORY<br>DEVICES                                                                   |
| I 345789              | AF01949TW                 | Taiwan  | 12/06/2006  | 07/21/2011 | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREFOR                                                                                |
| I357637               | AF01954TW                 | Taiwan  | 04/24/2007  | 02/01/2012 | MEMORY CELL ARRAY WITH LOW RESISTANCE COMMON SOURCE<br>AND HIGH CURRENT DRIVABILITY                                             |
| I364837               | AF01965TW                 | Taiwan  | 11/27/2007  | 05/21/2012 | BARRIER REGION FOR MEMORY DEVICES                                                                                               |
| I381488               | AF01989TW                 | Taiwan  | 11/27/2007  | 01/01/2013 | MEMORY DEVICE PROTECTION LAYER                                                                                                  |
| I420673               | AF02037TW                 | Taiwan  | 07/24/2007  | 12/21/2013 | INTEGRATED CIRCUIT MEMORY SYSTEM EMPLOYING SILICON RICH<br>LAYERS                                                               |
| 102134239             | AF02037TW DIV             | Taiwan  | 07/24/2007  |            | INTEGRATED CIRCUIT MEMORY SYSTEM EMPLOYING SILICON RICH<br>LAYERS                                                               |
| 416669                | AF02041TW                 | Taiwan  | 07/11/2007  | 11/21/2013 | MEMORY CELL SYSTEM WITH CHARGE TRAP                                                                                             |
| I368317               | AF02044TW                 | Taiwan  | 07/11/2007  | 07/11/2012 | MEMORY CELL SYSTEM WITH MULTIPLE NITRIDE LAYERS                                                                                 |
| I423265               | AF02067TW                 | Taiwan  | 08/13/2007  | 01/11/2014 | MEMORY ERASE MANAGEMENT SYSTEM                                                                                                  |
| 392088                | AF02071TW                 | Taiwan  | 05/21/2007  | 04/01/2013 | MEMORY SYSTEM WITH SWITCH ELEMENT AND METHOD OF<br>MANUFACTURING THE MEMORY SYSTEM                                              |
| I 342024              | AF02079                   | Taiwan  | 07/03/2007  | 05/11/2011 | NONVOLATILE STORAGE AND ERASE CONTROL                                                                                           |
| I365514               | AF02117TW                 | Taiwan  | 11/29/2007  | 06/01/2012 | A SEMICONDUCTOR MEMORY COMPRISING DUAL CHARGE STORAGE<br>NODES AND METHODS FOR ITS FABRICATION                                  |
| I364819               | AF02131TW                 | Taiwan  | 12/07/2007  | 05/21/2012 | FLASH MEMORY DEVICES AND METHODS FOR FABRICATING THE<br>SAME                                                                    |
| I355662               | AF02136TW                 | Taiwan  | 04/04/2007  | 01/01/2012 | REDUCTION OF LEAKAGE CURRENT AND PROGRAM DISTURBS IN<br>FLASH MEMORY DEVICES                                                    |
| 371101                | AF02137TW                 | Taiwan  | 04/04/2007  | 08/21/2012 | METHODS FOR ERASING AND PROGRAMMING MEMORY DEVICES AND<br>SEMICONDUCTOR DEVICE                                                  |
| I390709               | AF02138TW                 | Taiwan  | 04/04/2007  | 03/21/2013 | METHODS FOR ERASING MEMORY DEVICES AND MULTI-LEVEL<br>PROGRAMMING MEMORY DEVICE                                                 |
| I373048               | AF02139TW                 | Taiwan  | 12/07/2007  | 09/21/2012 | ERASING FLASH MEMORY USING ADAPTIVE DRAIN AND/OR GATE BIAS<br>AND RELATED ERASE METHOD                                          |
| I366887               | AF02141TW                 | Taiwan  | 11/28/2007  | 06/21/2012 | DUAL-BIT MEMORY DEVICE HAVING TRENCH ISOLATION MATERIAL<br>DISPOSED NEAR BIT LINE CONTACT AREAS                                 |
| I367487               | AF02146TW                 | Taiwan  | 04/04/2007  | 07/01/2012 | FLASH MEMORY PROGRAMMING AND VERIFICATION WITH REDUCED<br>LEAKAGE CURRENT                                                       |
| I378464               | AF02150TW                 | Taiwan  | 06/09/2008  | 12/01/2012 | NON-VOLATILE MEMORY DEVICE, NON-VOLATILE MEMORY SYSTEM,<br>AND CONTROL METHOD FOR THE NON-VOLATILE MEMORY DEVICE                |
| I 341022              | AF02167TW                 | Taiwan  | 05/23/2007  | 04/21/2011 | MEMORY CELLS HAVING SPLIT CHARGE STORAGE NODES AND<br>METHODS FOR FABRICATING MEMORY CELLS HAVING SPLIT CHARGE<br>STORAGE NODES |
| 176246                | AF02175TW                 | Taiwan  | 03/23/2000  | 04/01/2003 | NONVOLATILE MEMORY ALLOW ENCRYPTED                                                                                              |
| 149946                | AF02178TW                 | Taiwan  | 11/24/2000  | 01/21/2002 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                         |
| 156259                | AF02189TW                 | Taiwan  | 12/14/2000  | 05/11/2002 | MANUFACTURING METHOD OF NONVOLATILE                                                                                             |
| 172137                | AF02191TW                 | Taiwan  | 09/26/2001  | 02/01/2003 | NONVOLATILE SEMICONDUCTOR DEVICE AND                                                                                            |
| 161056                | AF02192TW                 | Taiwan  | 09/25/2001  | 08/01/2002 | SEMICONDUCTOR MEMORY AND MANUFACTURING                                                                                          |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                                       |
|-----------------------|---------------------------|---------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 172465                | AF02195TW                 | Taiwan  | 08/29/2001  | 02/01/2003 | SEMICONDUCTOR DEVICE AND MANUFACTURING                                                                                                                                                      |
| 160393                | AF02198TW                 | Taiwan  | 08/28/2001  | 07/21/2002 | SEMICONDUCTOR MEMORY DEVICE AND DRIVING                                                                                                                                                     |
| 1222228               | AF02208TW                 | Taiwan  | 03/06/2003  | 10/11/2004 | NONVOLATILE SEMICONDUCTOR MEMORY AND                                                                                                                                                        |
| 200429                | AF02209TW                 | Taiwan  | 02/10/2003  | 09/01/2003 | Nonvolatile semiconductor memory device programming second dynamic reference cell according to threshold value of first dynamic reference cell                                              |
| 1269435               | AF02212TW                 | Taiwan  | 05/15/2003  | 12/21/2006 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                     |
| 203546                | AF02214TW                 | Taiwan  | 03/14/2003  | 05/21/2004 | SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                                 |
| 1233129               | AF02219TW                 | Taiwan  | 09/04/2003  | 05/21/2005 | SEMICONDUCTOR MEMORY FOR FUNCTION WELL                                                                                                                                                      |
| 1221292               | AF02220TW                 | Taiwan  | 08/01/2003  | 09/21/2004 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                                                                                                            |
| 1239009               | AF02221TW                 | Taiwan  | 08/29/2003  | 09/01/2005 | MEMORY CIRCUIT HAVING                                                                                                                                                                       |
| 1224794               | AF02222TW                 | Taiwan  | 08/05/2003  | 12/01/2004 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                                                                                                            |
| 206705                | AF02238TW                 | Taiwan  | 04/29/2003  | 06/21/2004 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                                                                                                            |
| 1368913               | AF02246TW                 | Taiwan  | 06/12/2008  | 07/21/2012 | COMPENSATION METHOD TO ACHIEVE UNIFORM PROGRAMMING SPEED OF FLASH MEMORY DEVICES AND A SYSTEM THAT USES THE METHOD (AS AMENDED)                                                             |
| 1373828               | AF02248TW                 | Taiwan  | 05/09/2008  | 10/01/2012 | FLASH MEMORY CELL WITH A FLAIR GATE                                                                                                                                                         |
| 1366825               | AF02267TW                 | Taiwan  | 12/25/2007  | 06/21/2012 | MULTI-LEVEL OPERATION IN DUAL ELEMENT CELLS USING A SUPPLEMENTAL PROGRAMMING LEVEL                                                                                                          |
| 1387054               | AF02272TW                 | Taiwan  | 09/06/2007  | 02/21/2013 | METHOD OF SELECTING OPERATING CHARACTERISTICS OF A RESISTIVE MEMORY DEVICE                                                                                                                  |
| 1454107               | AF02282TW                 | Taiwan  | 08/13/2007  | 09/21/2014 | MULTIPLE COMMUNICATION CHANNELS ON MMC OR SD CMD LINE                                                                                                                                       |
| 1379304               | AF02286TW                 | Taiwan  | 11/28/2007  | 12/11/2012 | METHODS AND SYSTEMS FOR MEMORY DEVICES                                                                                                                                                      |
| 1368847               | AF02301TW                 | Taiwan  | 09/06/2007  | 07/21/2012 | VIRTUAL MEMORY CARD CONTROLLER                                                                                                                                                              |
| 96140925              | AF02315TW                 | Taiwan  | 10/31/2007  |            | ERASURE SUSPENSION FEATURE                                                                                                                                                                  |
| 1374519               | AF02322TW                 | Taiwan  | 12/21/2007  | 10/11/2012 | A SELF-ALIGNED PATTERNING METHOD BY USING NON-CONFORMAL FILM AND ETCH BACK FOR FLASH MEMORY AND OTHER SEMICONDUCTOR APPLICATIONS                                                            |
| 370983                | AF02329TW                 | Taiwan  | 11/02/2007  | 08/21/2012 | SYSTEM AND METHOD THAT EFFECTUATE SECURE ACCESS TO A FLASH MEMORY COMPONENT AND A SYSTEM THAT DIVIDES A FLASH MEMORY COMPONENT INTO ONE OR MORE PARTITIONS                                  |
| 1393148               | AF02335TW                 | Taiwan  | 11/02/2007  | 04/11/2013 | SECURE CO-PROCESSING MEMORY CONTROLLER INTEGRATED INTO AN EMBEDDED MEMORY SUBSYSTEM AND METHOD OF OPTIMIZING PROCESSOR UTILIZATION AND CREATING A HEIGHTENED LEVEL OF SECURITY (AS AMENDED) |
| 1356994               | AF02337TW                 | Taiwan  | 11/02/2007  | 01/21/2012 | USING SHARED MEMORY WITH AN EXECUTE-IN-PLACE PROCESSOR AND A CO-PROCESSOR                                                                                                                   |
| 443670                | AF02436TW                 | Taiwan  | 12/25/2007  | 07/01/2014 | RESISTANCE CHANGING MEMORY CELL ARCHITECTURE AND OPERATION METHOD THEREOF                                                                                                                   |
| 1392097               | AF02453TW                 | Taiwan  | 05/09/2008  | 04/01/2013 | SELF ALIGNED NARROW STORAGE ELEMENTS FOR ADVANCED MEMORY DEVICE                                                                                                                             |
| 1407449               | AF02465TW                 | Taiwan  | 06/12/2008  | 09/01/2013 | TERMINATE CYCLE FOR BURST WRITE OPERATION                                                                                                                                                   |
| 1368918               | AF02477TW                 | Taiwan  | 12/26/2007  | 07/21/2012 | DIVISION-BASED SENSING AND PARTITIONING OF ELECTRONIC MEMORY                                                                                                                                |
| 97150015              | AF02503TW                 | Taiwan  | 12/22/2008  |            | CONTROLLING AC DISTURBANCE WHILE PROGRAMMING                                                                                                                                                |
| 97133058              | AF02517TW                 | Taiwan  | 12/29/2008  |            | SACRIFICIAL NITRIDE AND GATE REPLACEMENT                                                                                                                                                    |
| 1441258               | AF02518TW                 | Taiwan  | 12/29/2008  | 06/11/2014 | GATE REPLACEMENT WITH TOP OXIDE REGROWTH FOR THE TOP OXIDE IMPROVEMENT                                                                                                                      |
| 1441283               | AF02527TW                 | Taiwan  | 08/06/2008  | 06/11/2014 | ORO AND ORPRO WITH BITLINE TRENCH TO SUPPRESS TRANSPORT PROGRAM DISTURB                                                                                                                     |
| 97140795              | AF02531TW                 | Taiwan  | 02/23/2009  |            | SELECTIVE SILICIDE FORMATION USING RESIST ETCHBACK                                                                                                                                          |
| 416676                | AF02559TW                 | Taiwan  | 08/05/2008  | 11/21/2013 | THE MANUFACTURING METHOD FOR A CHIP WHICH HAS A THROUGH-HOLE ELECTRODE                                                                                                                      |
| 97121849              | AF02560TW                 | Taiwan  | 06/12/2008  |            | DIE ATTACHMENT, DIE STACKING, AND WIRE EMBEDDING USING FILM                                                                                                                                 |
| 404068                | AF02563TW                 | Taiwan  | 10/13/2008  | 08/01/2013 | NON-VOLATILE MEMORY ARRAY PARTITIONING ARCHITECTURE                                                                                                                                         |
| 97139850              | AF02566                   | Taiwan  | 10/17/2007  | 05/17/2011 | TAMPER REACTIVE MEMORY DEVICE TO SECURE DATA FROM TAMPER ATTACKS                                                                                                                            |
| 97134629              | AF02572TW                 | Taiwan  | 09/10/2008  |            | SECURE MODULAR EXPONENTIATION BY RANDOMIZATION OF EXPONENT SCANNING                                                                                                                         |
| 1473095               | AF02584TW                 | Taiwan  | 12/05/2008  | 02/11/2015 | MIRRORBIT PROGRAM / REFRESH ALGORITHM                                                                                                                                                       |
| 148511                | AF02649TW                 | Taiwan  | 10/13/2000  | 12/01/2001 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                     |
| 473280                | AF02681TW                 | Taiwan  | 12/26/2008  | 02/11/2015 | ARRAYED NEUTRON DETECTOR WITH MULTI SHIELDING ALLOWING FOR DISCRIMINATION BETWEEN RADIATION TYPES                                                                                           |
| 1464884               | AF02813TW                 | Taiwan  | 12/31/2008  | 12/11/2014 | MIRROR BIT MEMORY DEVICE HAVING TOP INSULATING FILM WITH HIGH ETCHING SELECTIVITY TO GATE OXIDE FILM                                                                                        |
| 97150017              | AF02814TW                 | Taiwan  | 04/21/2009  |            | EXTENDING FLASH MEMORY DATA RETENTION VIA REWRITE REFRESH                                                                                                                                   |
| 97144628              | AF02824TW                 | Taiwan  | 11/19/2008  |            | A MEMORY BUFFERING SYSTEM THAT IMPROVES READ/WRITE PERFORMANCE AND PROVIDES LOW LATENCY FOR MOBILE SYSTEMS                                                                                  |
| 97137135              | AF02827TW                 | Taiwan  | 01/20/2009  |            | OPO MIRROR BIT MEMORY DEVICE HAVING SHALLOW TRENCH ISOLATION                                                                                                                                |
| 473204                | AF02832TW                 | Taiwan  | 10/09/2008  | 02/11/2015 | FABRICATING METHOD OF OPO MIRROR BIT MEMORY DEVICE HAVING SHALLOW TRENCH ISOLATION                                                                                                          |
| 097148156             | AF02839TW                 | Taiwan  | 12/11/2008  |            | CONTROL METHOD OF GBL AND LBL IN A READ                                                                                                                                                     |
| 407448                | AF02850TW                 | Taiwan  | 10/13/2008  | 09/01/2013 | CONTROLLED RAMP RATES FOR METAL BITLINES DURING WRITE OPERATIONS FROM HIGH VOLTAGE DRIVER FOR MEMORY APPLICATIONS                                                                           |
| 458019                | AF02862TW                 | Taiwan  | 12/16/2008  | 10/21/2014 | HETERO-STRUCTURE VARIABLE SILICON RICHNESS NITRIDE FOR MLC FLASH MEMORY DEVICE                                                                                                              |
| 97131679              | AF02865TW                 | Taiwan  | 08/20/2008  |            | PROCESS OF FORMING AN ELECTRONIC DEVICE INCLUDING DEPOSITING LAYERS WITHIN OPENINGS                                                                                                         |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                       |
|-----------------------|---------------------------|---------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 97145619              | AF02875TW                 | Taiwan  | 11/26/2008  |            | A METHOD FOR SETTING PARAMETERS AND DETERMINING LATENCY IN A CHAINED DEVICE SYSTEM                                                                          |
| 1464614               | AF02907TW                 | Taiwan  | 12/29/2008  | 12/11/2014 | METHOD FOR PROTECTING DATA AGAINST DIFFERENTIAL FAULT ANALYSIS INVOLVED IN RSA USING THE CHINESE REMAINDER THEOREM                                          |
| 97146131              | AF02908TW                 | Taiwan  | 11/28/2008  |            | SONOS-NAND DEVICE HAVING COMPLETELY SEPARATED STORAGE REGIONS                                                                                               |
| 583664                | AF04003TW                 | Taiwan  | 02/10/2003  | 04/11/2004 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE PROGRAMMING SECOND DYNAMIC REFERENCE CELL ACCORDING TO THRESHOLD VALUE OF FIRST DYNAMIC REFERENCE CELL              |
| 356587                | AF04006TW                 | Taiwan  | 06/23/1997  | 04/21/1999 | Semiconductor device having interlayer insulator and the method for fabricating thereof                                                                     |
| 94137782              | AF04031PCT                | Taiwan  | 10/28/2005  |            | Non-volatile memory and pseudo-sram based on resonant tunneling concept                                                                                     |
| 1289929               | AF04052KR                 | Taiwan  | 08/29/2003  | 11/11/2007 | SEMICONDUCTOR MEMORY DEVICE                                                                                                                                 |
| 080501                | B038TW                    | Taiwan  | 12/28/1995  | 12/24/1996 | METHODS FOR BULK (OR BYTE) CHARGING & DISCHARGING AN ARRAY OF FLASH EEPROM MEMORY CELLS (AS AMENDED)                                                        |
| 085073                | B047TW                    | Taiwan  | 07/29/1995  | 07/15/1997 | NOVEL PROCESSING TECHNIQUES FOR ACHIEVING PRODUCTION WORTHY LOW DIELECTRIC LOW INTERCONNECT RESISTANCE AND HIGH PERFORMANCE                                 |
| 364997                | B247ATW                   | Taiwan  | 02/05/1997  | 07/21/1999 | A MULTI-LEVEL BITS-PER-CELL FLASH SHIFT REGISTER PAGE BUFFER                                                                                                |
| 089881                | B247TW                    | Taiwan  | 02/05/1997  | 01/23/1998 | A METHOD FOR DOUBLE DENSITY FLASH EPROM WITH PAGE MODE PROGRAM AND READ                                                                                     |
| 080099                | B257TW                    | Taiwan  | 12/26/1995  | 12/06/1996 | LOW SUPPLY VOLTAGE NEGATIVE CHARGE PUMP                                                                                                                     |
| 079936                | B258TW                    | Taiwan  | 12/26/1995  | 11/29/1996 | A FAST 3 STATE BOOSTER CIRCUIT                                                                                                                              |
| 097126                | B261TW                    | Taiwan  | 12/22/1995  | 01/19/1999 | OVERERASE CORRECTION FOR FLASH MEMORY WHICH LIMITS OVERERASE AND PREVENTS ERASE VERIFY ERRORS                                                               |
| 117981                | B262TW                    | Taiwan  | 12/22/1995  | 11/28/2000 | TEMPERATURE COMPENSATED REFERENCE FOR OVER ERASE CORRECTION CIRCUITRY                                                                                       |
| 095140                | B287TW                    | Taiwan  | 05/13/1997  | 10/13/1998 | A METHOD AND SYSTEM FOR PROVIDING A DOUBLE DIFFUSE IMPLANT JUNCTION IN A VERY SHORT CHANNEL FLASH DEVICE                                                    |
| 103593                | C061296TW                 | Taiwan  | 02/04/1998  | 06/01/1999 | HIGH VOLTAGE CMOS LEVEL SHIFTER                                                                                                                             |
| 095042                | C072296TW                 | Taiwan  | 08/16/1996  | 10/03/1998 | USING FLOATING GATE CELLS AS SELECT GATE DEVICES FOR NAND FLASH MEMORY AND ITS BIAS SCHEME                                                                  |
| 116585                | C144496TW                 | Taiwan  | 02/26/1998  | 10/23/2000 | HIGH VOLTAGE NMOS PASS GATE FOR INTEGRATED CIRCUIT WITH HIGH VOLTAGE GENERATOR AND FLASH NON-VOLATILE MEMORY DEVICE HAVING THE PASS GATE                    |
| 127519                | C196596TW                 | Taiwan  | 12/18/1997  | 06/14/2001 | A FLASH MEMORY DEVICE, NON-VOLATILE MEMORY DEVICE AND METHOD FOR ENABLING SIMULTANEOUS READ AND WRITE OPERATION IN A FLASH OR THE LIKE SEMICONDUCTOR DEVICE |
| 172976                | C608497TW                 | Taiwan  | 05/11/1999  | 07/02/2003 | SHALLOW TRENCH ISOLATION FILLED WITH THERMAL OXIDE                                                                                                          |
| 154126                | C695497TW                 | Taiwan  | 07/13/2000  | 08/12/2002 | THIN FLOATING GATE AND CONDUCTIVE SELECT GATE IN SITU                                                                                                       |
| 141784                | C715497TW                 | Taiwan  | 09/28/1999  | 01/24/2002 | WORDLINE DRIVER FOR FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EEPROM)                                                                      |
| 152323                | C725497TW                 | Taiwan  | 08/11/2000  | 07/10/2002 | CIRCUIT IMPLEMENTATION TO QUENCH BIT LINE LEAKAGE CURRENT IN PROGRAM AND AUTO PROGRAM DISTURB MODE IN FLASH EPROM USING RESISTOR SOURCE LOAD                |
| 142628                | D138TW                    | Taiwan  | 10/19/1999  | 02/07/2002 | SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON-VOLATILE MEMORY ARRAY                                                                                       |
| 088116240             | D139US                    | Taiwan  | 09/23/1998  | 08/14/2001 | BANK SELECTOR CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                                          |
| 127139                | D140                      | Taiwan  | 06/24/1999  | 06/05/2001 | VT REFERENCE VOLTAGE FOR EXTREMELY LOW POWER-SUPPLY                                                                                                         |
| 135626                | D168TW                    | Taiwan  | 09/22/1999  | 10/26/2001 | SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                                               |
| 136567                | D169TW                    | Taiwan  | 09/22/1999  | 11/07/2001 | METHOD OF MAKING FLEXIBLY PARTITIONED METAL LINE SEGMENTS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE      |
| 136566                | D170TW                    | Taiwan  | 09/22/1999  | 11/07/2001 | MEMORY ADDRESS DECODING CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                                |
| 156301                | D802TW                    | Taiwan  | 11/02/1999  | 09/18/2002 | METHOD FOR IMPROVING ELECTROSTATIC DISCHARGE (ESD) ROBUSTNESS                                                                                               |
| 143916                | D832TW                    | Taiwan  | 05/04/2000  | 03/01/2002 | RAMPED OR STEPPED GATE CHANNEL ERASE FOR FLASH MEMORY APPLICATION                                                                                           |
| 150425                | D833TW                    | Taiwan  | 08/30/2000  | 06/04/2002 | 1 TRANSISTOR FOR EEPROM APPLICATION                                                                                                                         |
| 147880                | D838TW                    | Taiwan  | 10/27/2000  | 04/24/2002 | SOLID-SOURCE DOPING FOR SOURCE/DRAIN TO ELIMINATE IMPLANT DAMAGE                                                                                            |
| 145800                | D844TW                    | Taiwan  | 08/01/2000  | 03/26/2002 | RAMPED GATE TECHNIQUE FOR SOFT PROGRAMMING TO TIGHTEN THE Vt DISTRIBUTION                                                                                   |
| 155788                | D853TW                    | Taiwan  | 11/29/2000  | 09/10/2002 | METHOD TO PROVIDE A REDUCED CONSTANT E-FIELD DURING ERASE OF EEPROMS FOR RELIABILITY IMPROVEMENT                                                            |
| 170861                | D862TW                    | Taiwan  | 04/06/2001  | 05/26/2003 | NEW METHOD TO FABRICATE A HIGH COUPLING FLASH CELL WITH LESS SILICIDE SEAM PROBLEM                                                                          |
| 147966                | D877TW                    | Taiwan  | 08/30/2000  | 04/25/2002 | INTEGRATED CIRCUIT HAVING INCREASED GATE COUPLING CAPACITANCE                                                                                               |
| 150436                | D894TW                    | Taiwan  | 10/06/2000  | 06/04/2002 | METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITH REDUCED ARC LOSS IN PERIPHERAL CIRCUITRY REGION                                                         |
| 1248659               | D958TW                    | Taiwan  | 01/29/2001  | 02/01/2006 | NOVEL NITRIDATION BARRIERS FOR NITRIDATED TUNNEL OXIDE FOR CIRCUITRY FOR FLASH TECHNOLOGY AND FOR LOCOS/STI ISOLATION                                       |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                           |
|-----------------------|--------------------------|---------|-------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 168219                | DA01011TW                | Taiwan  | 04/27/2001  | 04/15/2003 | A SUBMICRON SEMICONDUCTOR DEVICE HAVING A SELF-ALIGNED CHANNEL STOP REGION AND A METHOD FOR FABRICATING THE SEMICONDUCTOR DEVICE USING A TRIM AND ETCH          |
| 142303                | DA01016TW                | Taiwan  | 08/05/2000  | 02/01/2002 | METHOD FOR PROVIDING A DOPANT LEVEL FOR POLYSILICON FOR FLASH MEMORY DEVICES                                                                                    |
| 142661                | DA01023TW                | Taiwan  | 08/18/2000  | 02/07/2002 | METHOD FOR CONTACT SIZE CONTROL FOR NAND TECHNOLOGY                                                                                                             |
| 155827                | DA01025TW                | Taiwan  | 04/30/2001  | 09/10/2002 | FLASH MEMORY ARRAY AND A METHOD AND SYSTEM OF FABRICATION THEREOF                                                                                               |
| 164455                | DA01028TW                | Taiwan  | 03/28/2001  | 02/24/2003 | METHOD AND SYSTEM FOR PROVIDING CONTACT TO A FIRST POLYSILICON LAYER IN A FLASH MEMORY DEVICE                                                                   |
| 178330                | E0197TW                  | Taiwan  | 07/07/2000  | 09/18/2003 | NEW METHOD OF FORMING SELECT GATE TO IMPROVE RELIABILITY AND PERFORMANCE FOR NAND-TYPE FLASH MEMORY DEVICES                                                     |
| 152316                | E0251TW                  | Taiwan  | 07/19/2000  | 07/10/2002 | FLASH MEMORY ARCHITECTURE EMPLOYING THREE LAYER METAL INTERCONNECT                                                                                              |
| 161339                | E0255TW                  | Taiwan  | 02/26/2001  | 12/06/2002 | CHARGE SHARING TO HELP BOOST THE WORDLINES DURING APDE VERIFY                                                                                                   |
| 161525                | E0264TW                  | Taiwan  | 02/21/2001  | 12/10/2002 | TRIMMING METHOD FOR WORDLINE BOOSTER TO MINIMIZE PROCESS VARIATION OF BOOSTED WORDLINE VOLTAGE                                                                  |
| 169357                | E0302TW                  | Taiwan  | 05/14/2001  | 04/29/2003 | UNIFORM BITLINE STRAPPING OF NON-VOLATILE MEMORY CELL                                                                                                           |
| 1340294               | E0310TW                  | Taiwan  | 02/10/2004  | 04/11/2011 | RADIATION SENSITIVE RESIN COMPOSITION, MANUFACTURING METHOD THEREOF AND FABRICATING METHOD OF SEMICONDUCTOR DEVICE USING THE SAME                               |
| 1271745               | E0310WO                  | Taiwan  | 10/03/2001  | 01/21/2007 | SELECT TRANSISTOR ARCHITECTURE FOR A VIRTUAL GROUND NON-VOLATILE MEMORY CELL ARRAY                                                                              |
| 172451                | E0322TW                  | Taiwan  | 02/26/2001  | 06/19/2003 | SELECTIVE ERASURE OF A NON-VOLATILE MEMORY CELL OF A FLASH MEMORY DEVICE                                                                                        |
| 161338                | E0324TW                  | Taiwan  | 02/26/2001  | 12/06/2002 | SELECTIVE ERASURE OF A NON-VOLATILE MEMORY CELL OF A FLASH MEMORY DEVICE                                                                                        |
| 207033                | E0370TW                  | Taiwan  | 03/14/2001  | 11/08/2004 | A DUAL SPACER PROCESS NON-VOLATILE MEMORY DEVICES                                                                                                               |
| 202116                | E0462TW                  | Taiwan  | 05/30/2001  | 09/15/2004 | DUAL PORTED CAMS FOR SIMULTANEOUS OPERATION FLASH MEMORY                                                                                                        |
| 182926                | E0470TW                  | Taiwan  | 06/06/2001  | 11/28/2003 | POWER SAVING ON THE FLY DURING READING OF DATA FROM A MEMORY DEVICE                                                                                             |
| 1222071               | E0485                    | Taiwan  | 03/01/2000  | 03/16/2004 | INTERLACED MULTI-LEVEL MEMORY                                                                                                                                   |
| 163498                | E1030TW                  | Taiwan  | 02/21/2001  | 09/01/2002 | TEMPERATURE COMPENSATED BIAS GENERATOR                                                                                                                          |
| 161049                | F0004TW                  | Taiwan  | 06/26/2001  | 12/03/2002 | AUTOMATED DETERMINATION AND DISPLAY OF THE PHYSICAL LOCATION OF A FAILED CELL IN AN ARRAY OF MEMORY CELLS                                                       |
| 1271822               | F01137TW                 | Taiwan  | 03/27/2003  | 01/21/2007 | MEMORY MANUFACTURING PROCESS WITH BITLINE ISOLATION                                                                                                             |
| 172520                | F0257TW                  | Taiwan  | 11/06/2001  | 06/20/2003 | METHOD AND SYSTEM FOR EMBEDDED CHIP ERASE VERIFICATION                                                                                                          |
| 1286753               | F0258TW                  | Taiwan  | 01/08/2003  | 09/11/2007 | SOURCE SIDE SENSING SCHEME FOR VIRTUAL GROUND READ OF FLASH EPROM ARRAY WITH ADJACENT BIT PRECHARGE                                                             |
| 201755                | F0259TW                  | Taiwan  | 05/16/2002  | 09/08/2004 | MODULATED CHARGE PUMP WHICH USES AN ANALOG TO DIGITAL CONVERTER TO COMPENSATE FOR SUPPLY VOLTAGE VARIATIONS                                                     |
| 1226067               | F0260TW                  | Taiwan  | 04/10/2002  | 01/01/2005 | METHOD AND APPARATUS FOR BOOSTING BITLINES FOR LOW VCC READ                                                                                                     |
| 1295060               | F0262TW                  | Taiwan  | 01/09/2003  | 03/21/2008 | METHOD AND APPARATUS FOR SOFT PROGRAM VERIFICATION IN A MEMORY DEVICE                                                                                           |
| 207158                | F0266TW                  | Taiwan  | 05/03/2002  | 11/09/2004 | ERASE METHOD FOR DUAL BIT VIRTUAL GROUND FLASH                                                                                                                  |
| 1260639               | F0272TW                  | Taiwan  | 01/08/2003  | 08/21/2006 | CHARGE INJECTION                                                                                                                                                |
| 183343                | F0274TW                  | Taiwan  | 12/07/2001  | 12/04/2003 | HIGHER PROGRAM VT AND FASTER PROGRAMMING RATES BASED ON IMPROVED ERASE METHODS                                                                                  |
| 1265599               | F0279TW                  | Taiwan  | 05/17/2002  | 11/01/2006 | ESD IMPLANT FOLLOWING SPACER DEPOSITION                                                                                                                         |
| 183392                | F0280TW                  | Taiwan  | 05/03/2002  | 12/04/2003 | METHOD OF MANUFACTURING SPACER ETCH MASK FOR SILICON-OXIDE-NITRIDE-OXIDE-SILICON (SONOS) TYPE NONVOLATILE MEMORY                                                |
| 202199                | F0282TW                  | Taiwan  | 10/03/2002  | 09/15/2004 | DOUBLE DENSED CORE GATES IN SONOS FLASH MEMORY                                                                                                                  |
| 191683                | F0283TW                  | Taiwan  | 10/01/2002  | 03/24/2004 | SALICIDED GATE FOR VIRTUAL GROUND ARRAYS                                                                                                                        |
| 188690                | F0499TW                  | Taiwan  | 10/08/2001  | 02/12/2004 | A SOURCE SIDE BORON IMPLANTING AND DIFFUSING DEVICE ARCHITECTURE FOR DEEP SUBSTANCE 0.18UM FLASH MEMORY TECHNOLOGIES                                            |
| 1266316               | F0919                    | Taiwan  | 12/07/2001  | 11/11/2006 | PIGGYBACK PROGRAMMING USING VOLTAGE CONTROL FOR MULTI-LEVEL CELL FLASH MEMORY DESIGNS                                                                           |
| 1248675               | F0932TW                  | Taiwan  | 10/08/2001  | 02/01/2006 | SOURCE SIDE BORON IMPLANT AND DRAIN SIDE MDD IMPLANT FOR DEEP SUB 0.18 MICRON FLASH MEMORY                                                                      |
| 1221916               | F1024TW                  | Taiwan  | 03/29/2002  | 10/11/2004 | SYSTEM AND METHOD FOR ERASE TEST OF INTEGRATED CIRCUIT DEVICE HAVING NON-HOMOGENEOUSLY SIZED SECTORS                                                            |
| 188956                | F1067TW                  | Taiwan  | 04/03/2002  | 02/16/2004 | THRESHOLD VOLTAGE COMPACTING FOR NON-VOLATILE SEMICONDUCTOR MEMORY DESIGNS                                                                                      |
| 202161                | FMA13-00136KR            | Taiwan  | 05/01/2002  | 05/11/2004 | DC/DC CONVERTER CONTROL CIRCUITS AND DC/DC CONVERTER SYSTEM                                                                                                     |
| 329561                | FMA13-0017KR             | Taiwan  | 05/18/1995  | 09/01/2010 | SEMICONDUCTOR MEMORY DEVICE                                                                                                                                     |
| 394864                | FMA13-0022KR             | Taiwan  | 12/05/2008  | 05/01/2013 | METAL SURFACE TREATMENT COMPOSITION, AND SURFACE-TREATED METAL MATERIAL WITH METAL SURFACE TREATMENT FILM OBTAINED FROM THE METAL SURFACE TREATMENT COMPOSITION |
| 1338836               | FMA13-00310TW            | Taiwan  | 07/26/2007  | 03/11/2011 | ERROR PROCESSING METHOD AND INFORMATION PROCESSING APPARATUS                                                                                                    |
| 1340319               | FMA13-00312TW            | Taiwan  | 10/11/2007  | 04/11/2011 | POWER SUPPLY CIRCUIT, POWER SUPPLY CONTROL CIRCUIT, AND POWER ...                                                                                               |
| 1354436               | FMA13-00313TW            | Taiwan  | 04/16/2007  | 12/11/2011 | CONTROLLER FOR DC-DC CONVERTER                                                                                                                                  |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                 |
|-----------------------|---------------------------|---------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| I357709               | FMA13-00314TW             | Taiwan  | 07/11/2007  | 02/01/2012 | DC-DC CONVERTER                                                                                                                                       |
| I363958               | FMA13-00315TW             | Taiwan  | 09/13/2007  | 05/11/2012 | CONTROL CIRCUIT OF SYNCHRONOUS RECTIFICATION TYPE POWER SUPPLY UNIT, ...                                                                              |
| I356569               | FMA13-00317TW             | Taiwan  | 04/23/2007  | 01/11/2012 | DC-DC CONVERTER WITH OSCILLATOR AND MONITORING FUNCTION                                                                                               |
| I357170               | FMA13-00319TW             | Taiwan  | 08/07/2007  | 01/21/2012 | CONTROL CIRCUIT OF POWER SUPPLY UNIT WHICH CONTROL OUTPUT POWER ...                                                                                   |
| I366333               | FMA13-00320TW             | Taiwan  | 01/28/2008  | 06/11/2012 | DC-DC CONVERTER WITH PLURALITY OF SOFT-START CONTROL CIRCUITS                                                                                         |
| I345357               | FMA13-00321TW             | Taiwan  | 01/14/2008  | 07/11/2011 | POWER SUPPLY CIRCUIT, POWER SUPPLY CONTROL CIRCUIT, AND POWER ...                                                                                     |
| I350060               | FMA13-00322TW             | Taiwan  | 12/28/2007  | 10/01/2011 | FRACTIONAL FREQUENCY DIVIDER PLL DEVICE AND CONTROL METHOD THEREOF                                                                                    |
| I338995               | FMA13-00323TW             | Taiwan  | 09/12/2007  | 03/11/2011 | METHOD AND CIRCUIT FOR CONTROLLING DC-DC CONVERTER                                                                                                    |
| I354434               | FMA13-00327TW             | Taiwan  | 11/09/2007  | 12/11/2011 | CONTROL CIRCUIT FOR DETECTING A REVERSE CURRENT IN A DC-DC CONVERTER                                                                                  |
| I349411               | FMA13-00328TW             | Taiwan  | 11/05/2007  | 09/21/2011 | CONTROL CIRCUIT FOR SYNCHRONOUS RECTIFIER-TYPE DC-DC CONVERTER, SYNCHRONOUS RECTIFIER-TYPE DC-DC CONVERTER AND CONTROL METHOD THEREOF                 |
| I349415               | FMA13-00329TW             | Taiwan  | 11/05/2007  | 09/21/2011 | CONTROL CIRCUIT FOR CURRENT MODE DC-DC CONVERTER AND CONTROL METHOD OF CURRENT MODE DC-DC CONVERTER                                                   |
| 304684                | FMA13-00344KR             | Taiwan  | 07/30/2003  | 12/21/2008 | PLL CLOCK GENERATOR CIRCUIT AND CLOCK GENERATION METHOD                                                                                               |
| I356174               | FMA13-00347TW             | Taiwan  | 12/28/2007  | 01/11/2012 | DETECTION CIRCUIT                                                                                                                                     |
| I356170               | FMA13-00350TW             | Taiwan  | 12/28/2007  | 01/11/2012 | DETECTION CIRCUIT                                                                                                                                     |
| I353102               | FMA13-00357KR             | Taiwan  | 05/25/2007  | 11/21/2011 | STEP-UP/STEP-DOWN TYPE DC-DC CONVERTER, AND CONTROL CIRCUIT AND CONTROL METHOD OF THE SAME                                                            |
| I231373               | FMA13-00380JP<br>DIV2     | Taiwan  | 04/14/2003  | 04/21/2005 | METHOD FOR PREDICTING REMAINING CHARGE OF PORTABLE ELECTRONICS BATTERY                                                                                |
| 234758                | FMA13-00381KR             | Taiwan  | 03/26/2004  | 06/21/2005 | OPERATION AMPLIFIER, LINE DRIVER, AND LIQUID CRYSTAL DISPLAY DEVICE                                                                                   |
| 439254                | FMA13-00382KR             | Taiwan  | 04/09/2009  | 06/01/2014 | SELECTOR AND MULTILAYER INTERCONNECTION WITH REDUCED OCCUPIED AREA ON SUBSTRATE                                                                       |
| 338870                | FMA13-0042KR              | Taiwan  | 12/20/2004  | 03/11/2011 | SCATTERING LIGHT SMOKE DETECTOR                                                                                                                       |
| 90048                 | FMA13-0043KR              | Taiwan  | 11/19/1996  | 10/01/1997 | SEMICONDUCTOR INTEGRATED CIRCUIT OPERABLE AS A PHASE-LOCKED LOOP                                                                                      |
| 192065                | FMA13-00449KR             | Taiwan  | 02/04/2002  | 12/01/2003 | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                                                                                                               |
| 227330                | FMA13-00450JP DIV         | Taiwan  | 08/27/2003  | 02/01/2005 | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, AND ADJUSTMENT METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                                             |
| I335713               | FMA13-00533KR             | Taiwan  | 05/23/2006  | 01/01/2011 | POWER SOURCE CONTROL CIRCUIT, POWER SUPPLY DEVICE, AND CONTROL METHOD FOR THE SAME                                                                    |
| 169106                | FMA13-00536JP             | Taiwan  | 03/23/2001  | 12/11/2002 | CHARGE CIRCUIT THAT PERFORMS CHARGE CONTROL BY COMPARING A PLURALITY OF BATTERY VOLTAGES                                                              |
| 279965                | FMA13-00539JP             | Taiwan  | 01/07/2002  | 04/21/2007 | OVERVOLTAGE-PROTECTIVE DEVICE FOR POWER SYSTEM, AC/DC CONVERTER AND DC/DC CONVERTER CONSTITUTING THE POWER SYSTEM                                     |
| 222556                | FMA13-00541JP             | Taiwan  | 02/26/2002  | 10/21/2004 | CONTROL CIRCUIT OF DC-DC CONVERTER                                                                                                                    |
| I224304               | FMA13-00543TW             | Taiwan  | 10/21/2002  | 11/21/2004 | SEMICONDUCTOR DEVICE EQUIPPED WITH TRANSFER CIRCUIT FOR CASCADE CONNECTION                                                                            |
| I306696               | FMA13-00544TW             | Taiwan  | 02/27/2002  | 02/21/2009 | MODE SWITCHING METHOD FOR PLL CIRCUIT AND MODE CONTROL CIRCUIT FOR PLL CIRCUIT                                                                        |
| 227944                | FMA13-00547KR             | Taiwan  | 11/18/2003  | 02/11/2005 | SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                                                      |
| I234338               | FMA13-00548JP             | Taiwan  | 03/17/2004  | 06/11/2005 | DC/DC CONVERTER                                                                                                                                       |
| I244582               | FMA13-00549PCT            | Taiwan  | 04/18/2003  | 12/01/2005 | CONSTANT-VOLTAGE POWER SUPPLY CIRCUIT                                                                                                                 |
| 203279                | FMA13-00551KR             | Taiwan  | 12/09/2002  | 05/21/2004 | BIPOLAR SUPPLY VOLTAGE GENERATOR AND SEMICONDUCTOR DEVICE FOR SAME                                                                                    |
| I328920               | FMA13-00554JP             | Taiwan  | 03/22/2006  | 08/11/2010 | DC-DC CONVERTER CONTROL CIRCUIT AND DC-DC CONVERTER CONTROL METHOD                                                                                    |
| I325677               | FMA13-00556KR             | Taiwan  | 05/24/2006  | 06/01/2010 | DC LINEAR REGULATOR SINGLE CONTROLLER WITH PLURAL LOADS                                                                                               |
| I342651               | FMA13-00561KR             | Taiwan  | 08/28/2006  | 05/21/2011 | CIRCUIT AND METHOD FOR CONTROLLING DC-DC CONVERTER                                                                                                    |
| I312609               | FMA13-00562KR             | Taiwan  | 05/24/2006  | 07/21/2009 | CURRENT-CONTROLLED DC-DC CONVERTER CONTROL CIRCUIT, CURRENT-CONTROLLED DC-DC CONVERTER, AND METHOD FOR CONTROLLING CURRENT-CONTROLLED DC-DC CONVERTER |
| I342650               | FMA13-00563TW             | Taiwan  | 09/22/2006  | 05/21/2011 | CONTROL CIRCUIT OF POWER SUPPLY AND CONTROL METHOD OF THE POWER SUPPLY                                                                                |
| I337696               | FMA13-00564TW             | Taiwan  | 08/23/2006  | 02/21/2011 | ELECTRONIC DEVICE INCORPORATING SYSTEM POWER SUPPLY UNIT AND METHOD FOR SUPPLYING POWER SUPPLY VOLTAGE                                                |
| I338832               | FMA13-00565KR             | Taiwan  | 09/07/2007  | 03/11/2011 | POWER SUPPLY SYSTEM AND METHOD FOR CONTROLLING OUTPUT VOLTAGE                                                                                         |
| I342657               | FMA13-00566KR             | Taiwan  | 09/22/2006  | 05/21/2011 | DC-DC CONVERTER CONTROL CIRCUIT, DC-DC CONVERTER, POWER SUPPLY UNIT, AND DC-DC CONVERTER CONTROL METHOD                                               |
| I326153               | FMA13-00569KR             | Taiwan  | 08/31/2006  | 06/11/2010 | CONTROL CIRCUIT OF POWER SUPPLY, POWER SUPPLY AND CONTROL METHOD THEREOF                                                                              |
| I368378               | FMA13-00573TW             | Taiwan  | 02/15/2008  | 07/11/2012 | POWER SUPPLY CIRCUIT, POWER SUPPLY CONTROL CIRCUIT, AND POWER SUPPLY CONTROL METHOD                                                                   |
| 179404                | FMA13-0070KR              | Taiwan  | 11/24/1998  | 06/01/2003 | TRANSISTOR OUTPUT CIRCUIT                                                                                                                             |
| 429601                | FMA13-0082TW              | Taiwan  | 01/06/2012  | 03/11/2014 | SEMICONDUCTOR DEVICE HAVING CURRENT AUXILIARY CIRCUIT FOR OUTPUT CIRCUIT                                                                              |
| 416239                | FMA13-0085TW00            | Taiwan  | 12/10/1998  | 12/21/2000 | DRIVER FOR A LIQUID-CRYSTAL DISPLAY PANEL                                                                                                             |

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| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                |
|-----------------------|--------------------------|---------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------|
| 180034                | FMA13-0087KR             | Taiwan  | 11/25/1999  | 06/11/2003 | SEMICONDUCTOR MEMORY AND OUTPUT SIGNAL CONTROL METHOD<br>AND CIRCUIT IN SEMICONDUCTOR MEMORY                                         |
| 191239                | FMA13-0091KR             | Taiwan  | 05/11/2000  | 11/11/2003 | LCD PANEL DRIVING CIRCUIT                                                                                                            |
| 152955                | FMA13-0095JP             | Taiwan  | 02/29/2000  | 03/11/2002 | OUTPUT CIRCUIT AND BATTERY PACK                                                                                                      |
| 166903                | FMA13-0100JP             | Taiwan  | 02/07/2001  | 11/01/2002 | DC-DC CONVERTER AND SEMICONDUCTOR INTEGRATED CIRCUIT<br>DEVICE FOR DC-DC CONVERTER                                                   |
| 552572                | FMA13-0105KR DIV         | Taiwan  | 12/15/2000  | 09/11/2003 | SEMICONDUCTOR INTEGRATED CIRCUIT FOR DRIVING LIQUID<br>CRYSTAL PANEL                                                                 |
| 1224894               | FMA13-0108KR             | Taiwan  | 01/05/2001  | 12/01/2004 | PLL SEMICONDUCTOR DEVICE WITH TESTABILITY, AND METHOD AND<br>APPARATUS FOR TESTING SAME                                              |
| 494383                | FMA13-0110KR             | Taiwan  | 03/26/2001  | 07/11/2002 | DOT-INVERSION DATA DRIVER FOR LIQUID CRYSTAL DISPLAY DEVICE                                                                          |
| 165803                | FMA13-0111JP             | Taiwan  | 02/05/2001  | 10/11/2002 | DISCHARGE CONTROL CIRCUIT OF BATTERIES                                                                                               |
| 193279                | FMA13-0122KR             | Taiwan  | 03/05/2002  | 12/21/2003 | DC-DC CONVERTER, POWER SUPPLY CIRCUIT, METHOD FOR<br>CONTROLLING DC-DC CONVERTER, AND METHOD FOR CONTROLLING<br>POWER SUPPLY CIRCUIT |
| 178799                | FMA13-0129KR             | Taiwan  | 03/19/2002  | 05/21/2003 | OPERATION AMPLIFIER HAVING OFFSET CANCEL FUNCTION                                                                                    |
| 552583                | FMA13-0132TW             | Taiwan  | 02/04/2002  | 09/11/2003 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                              |
| 200307                | FMA13-0133KR             | Taiwan  | 05/02/2002  | 04/11/2004 | REGULATOR CIRCUIT AND CONTROL METHOD THEREOF                                                                                         |
| 198454                | FMA13-0147KR             | Taiwan  | 01/09/2003  | 03/01/2004 | INTEGRATED CIRCUIT FREE FROM ACCUMULATION OF DUTY RATIO<br>ERRORS                                                                    |
| 1280745               | FMA13-0149JP DIV         | Taiwan  | 12/30/2002  | 05/01/2007 | PULSE WIDTH DETECTION CIRCUIT                                                                                                        |
| 204724                | FMA13-0151KR             | Taiwan  | 01/16/2003  | 06/11/2004 | DC-DC CONVERTER, DUTY-RATIO SETTING CIRCUIT AND ELECTRIC<br>APPLIANCE USING THEM                                                     |
| 222050                | FMA13-0164KR             | Taiwan  | 05/06/2003  | 10/11/2004 | SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND SIGNAL<br>TRANSMISSION SYSTEM                                                              |
| 225726                | FMA13-0171KR             | Taiwan  | 07/24/2003  | 12/21/2004 | CONTROL CIRCUIT FOR DC/DC CONVERTER                                                                                                  |
| 279988                | FMA13-0177KR             | Taiwan  | 12/23/2003  | 04/21/2007 | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT, JITTER<br>GENERATION CIRCUIT AND SEMICONDUCTOR DEVICE                                      |
| 221675                | FMA13-0178PCT            | Taiwan  | 03/03/2003  | 10/01/2004 | MOS TYPE VARIABLE CAPACITANCE DEVICE                                                                                                 |
| 276289                | FMA13-0210JP             | Taiwan  | 09/29/2004  | 03/11/2007 | SWITCHING REGULATOR CONTROL CIRCUIT, SWITCHING<br>REGULATOR AND SWITCHING REGULATOR CONTROL METHOD                                   |
| 275808                | FMA13-0211KR             | Taiwan  | 03/29/2005  | 03/11/2007 | CAPACITANCE DIFFERENCE DETECTING CIRCUIT AND MEMS SENSOR                                                                             |
| 281204                | FMA13-0224KR             | Taiwan  | 01/24/2005  | 05/11/2007 | SEMICONDUCTOR DEVICE                                                                                                                 |
| 288522                | FMA13-0226KR             | Taiwan  | 11/04/2004  | 10/11/2007 | CIRCUIT AND METHOD FOR CONTROLLING DC-DC CONVERTER                                                                                   |
| 1276290               | FMA13-0231TW             | Taiwan  | 03/17/2005  | 03/11/2007 | SEMICONDUCTOR DEVICE, PRINTED-CIRCUIT BOARD AND<br>ELECTRONICS DEVICE                                                                |
| 1294207               | FMA13-0232JP             | Taiwan  | 05/04/2005  | 03/01/2008 | DC-DC CONVERTER AND CONTROL CIRCUIT DEVICE FOR DC-DC<br>CONVERTER                                                                    |
| 1279068               | FMA13-0233JP             | Taiwan  | 05/04/2005  | 04/11/2007 | MULTI-PHASE DC-DC CONVERTER AND CONTROL CIRCUIT FOR MULTI-<br>PHASE ...                                                              |
| 1311008               | FMA13-0237JP             | Taiwan  | 05/09/2005  | 06/11/2009 | SIGNAL DETECTION METHOD, FREQUENCY DETECTION METHOD,<br>POWER ...                                                                    |
| 1322576               | FMA13-0238TW             | Taiwan  | 05/19/2005  | 03/21/2010 | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT AND A METHOD<br>OF CONTROLLING THEREOF                                                      |
| 1279067               | FMA13-0240JP             | Taiwan  | 05/25/2005  | 04/11/2007 | MULTIPHASE DC-DC CONVERTER                                                                                                           |
| 1281605               | FMA13-0241JP             | Taiwan  | 05/17/2005  | 05/21/2007 | EARLY EFFECT CANCELING CIRCUIT, DIFFERENTIAL AMPLIFIER,<br>LINEAR REGULATOR ...                                                      |
| 1277279               | FMA13-0246JP             | Taiwan  | 07/22/2005  | 03/21/2007 | CONTROL CIRCUIT AND CONTROL METHOD OF CURRENT MODE ...<br>DC-DC CONVERTER                                                            |
| 512571                | FMA13-0254TW             | Taiwan  | 03/21/2001  | 12/01/2002 | CHARGE-DISCHARGE CONTROL CIRCUIT AND SECONDARY BATTERY                                                                               |
| 1303516               | FMA13-0255JP             | Taiwan  | 08/31/2005  | 11/21/2008 | OPERATIONAL AMPLIFIER AND METHOD FOR CANCELING OFFSET<br>VOLTAGE OF ...                                                              |
| 1289206               | FMA13-0256KR             | Taiwan  | 01/18/2006  | 11/01/2007 | SEMICONDUCTOR DEVICE WITH OPERATION MODE SET BY<br>EXTERNAL RESISTOR                                                                 |
| 1309496               | FMA13-0257KR             | Taiwan  | 02/09/2006  | 05/01/2009 | DC-DC CONVERTER AND ITS CONTROL METHOD, AND SWITCHING<br>REGULATOR ...                                                               |
| 1294220               | FMA13-0260KR             | Taiwan  | 11/14/2005  | 03/01/2008 | SUCCESSIVE APPROXIMATION A/D CONVERTER PROVIDED WITH<br>SAMPLE-HOLD ...                                                              |
| 1308425               | FMA13-0266KR             | Taiwan  | 11/14/2005  | 04/01/2009 | CLOCK GENERATING CIRCUIT AND CLOCK GENERATING METHOD                                                                                 |
| 1304685               | FMA13-0269JP             | Taiwan  | 12/15/2005  | 12/21/2008 | CLOCK GENERATING CIRCUIT AND CLOCK GENERATING METHOD                                                                                 |
| 1315123               | FMA13-0273KR             | Taiwan  | 01/25/2006  | 09/21/2009 | DC-DC CONVERTER AND METHOD OF CONTROLLING DC-DC<br>CONVERTER                                                                         |
| 1347066               | FMA13-0276KR             | Taiwan  | 03/06/2006  | 08/11/2011 | CONTROLLER AND CONTROL METHOD FOR DC-DC CONVERTER                                                                                    |
| 1312226               | FMA13-0278KR             | Taiwan  | 02/24/2006  | 07/11/2009 | STEP-UP (BOOST) DC REGULATOR WITH TWO-LEVEL BACK BIAS<br>SWITCH GATE ...                                                             |
| 1309497               | FMA13-0279JP             | Taiwan  | 02/24/2006  | 05/01/2009 | DC-DC CONVERTER CONTROL CIRCUIT AND METHOD                                                                                           |
| 1307205               | FMA13-0280KR             | Taiwan  | 03/06/2006  | 03/01/2009 | CONTROL CIRCUIT AND CONTROL METHOD FOR DC/DC CONVERTER                                                                               |
| 1366973               | FMA13-0281KR             | Taiwan  | 04/04/2006  | 06/21/2012 | CONTROL CIRCUIT HAVING ERROR AMPLIFIER FOR DC-DC<br>CONVERTER AND ...                                                                |
| 1320264               | FMA13-0288TW             | Taiwan  | 07/31/2006  | 02/01/2010 | PULSE WIDTH MODULATION CIRCUIT                                                                                                       |
| 1317203               | FMA13-0296JP             | Taiwan  | 06/07/2006  | 11/11/2009 | OPERATIONAL AMPLIFIER                                                                                                                |
| 1327420               | FMA13-0300TW             | Taiwan  | 07/14/2006  | 07/11/2010 | COMMON INPUT/OUTPUT TERMINAL CONTROL CIRCUIT                                                                                         |
| 1331839               | FMA13-0302KR             | Taiwan  | 05/17/2006  | 10/11/2010 | DC-DC CONVERTER AND CONTROL CIRCUIT FOR DC-DC CONVERTER                                                                              |
| 1222075               | G0063TW                  | Taiwan  | 03/29/2002  | 10/11/2004 | ACCURATE VERIFY APPARATUS AND METHOD FOR NOR FLASH<br>MEMORY CELLS IN THE PRESENCE OF HIGH COLUMN LEAKAGE                            |
| 186537                | G0074TW                  | Taiwan  | 05/10/2002  | 01/29/2004 | SOURCE DRAIN IMPLANT DURING ONO FORMATION FOR IMPROVED<br>ISOLATION OF SONOS DEVICES                                                 |

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|-----------------------|---------------------------|---------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 192506                | G0259TW                   | Taiwan  | 04/03/2002  | 04/07/2004 | FLASH MEMORY DEVICE WITH INCREASE OF EFFICIENCY DURING AN APDE (AUTOMATIC PROGRAM DISTURB AFTER ERASE) PROCESS                                          |
| 92118440              | G0391                     | Taiwan  | 07/22/2002  |            | BUILT-IN-SELF-TEST (BIST) OF FLASH MEMORY CELLS AND IMPLEMENTATION OF BIST INTERFACE                                                                    |
| I278959               | G0689TW                   | Taiwan  | 12/19/2002  | 12/22/2006 | SHALLOW TRENCH ISOLATION APPROACH FOR IMPROVED STI CORNER ROUNDING                                                                                      |
| I336489               | G0730TW                   | Taiwan  | 11/10/2003  | 01/21/2011 | METHOD AND SYSTEM FOR REDUCING CONTACT DEFECTS USING NON CONVENTIONAL CONTACT FORMATION METHOD FOR SEMICONDUCTOR CELLS                                  |
| I 342062              | G0752TW                   | Taiwan  | 01/16/2004  | 05/11/2011 | IMPROVED PERFORMANCE IN FLASH MEMORY DEVICES                                                                                                            |
| I288417               | G0861TW                   | Taiwan  | 03/27/2003  | 10/11/2007 | IMPROVED ERASE METHOD FOR SINGLE SIDED MIRROR OPERATION                                                                                                 |
| I321324               | G0862TW                   | Taiwan  | 04/08/2002  | 03/01/2010 | REFRESH SCHEME FOR DYNAMIC PAGE PROGRAMMING                                                                                                             |
| 092105307             | G0863US                   | Taiwan  | 03/13/2002  | 10/28/2003 | OVERERASE CORRECTION METHOD                                                                                                                             |
| I286754               | G0864TW                   | Taiwan  | 03/28/2003  | 09/11/2007 | ALGORITHM DYNAMIC REFERENCE PROGRAMMING                                                                                                                 |
| 92123111              | G0865TW                   | Taiwan  | 08/22/2003  |            | METHOD AND SYSTEM FOR DEFINING A REDUNDANCY WINDOW AROUND A PARTICULAR COLUMN IN A MEMORY ARRAY                                                         |
| 300566                | G0866TW                   | Taiwan  | 04/29/2003  | 09/01/2008 | STEPPED PRE-ERASE VOLTAGE FOR MIRRORBIT ERASE                                                                                                           |
| 92123106              | G0871TW                   | Taiwan  | 08/22/2003  |            | LATERAL DOPED CHANNEL                                                                                                                                   |
| I262505               | G1255TW                   | Taiwan  | 02/11/2003  | 09/21/2006 | PARTIAL PAGE PROGRAMMING OF MULTI LEVEL FLASH                                                                                                           |
| 415257                | H0290TW                   | Taiwan  | 12/01/2005  | 11/11/2013 | POLYMER-BASED TRANSISTOR DEVICES, METHODS, AND SYSTEMS                                                                                                  |
| 92122216              | H0297TW                   | Taiwan  | 08/13/2003  |            | CONTROL OF MEMORY ARRAYS UTILIZING ZENER DIODE-LIKE DEVICES                                                                                             |
| I397918               | H0325TW                   | Taiwan  | 09/23/2005  | 06/01/2013 | CONTROL OF MEMORY DEVICES POSSESSING VARIABLE RESISTANCE CHARACTERISTICS                                                                                |
| I327338               | H0343TW                   | Taiwan  | 08/29/2003  | 07/11/2010 | MOCVD FORMATION OF Cu <sub>2</sub> S                                                                                                                    |
| I363370               | H0346TW                   | Taiwan  | 04/01/2005  | 05/01/2012 | IN-SITU SURFACE TREATMENT FOR MEMORY CELL FORMATION                                                                                                     |
| I 332719              | H0354TW                   | Taiwan  | 03/05/2004  | 11/01/2010 | SPIN ON POLYMERS FOR ORGANIC MEMORY DEVICES                                                                                                             |
| 389366                | H0368TW                   | Taiwan  | 03/31/2005  | 03/11/2013 | POLYMER DIELECTRICS FOR MEMORY ELEMENT ARRAY INTERCONNECT                                                                                               |
| I311764               | H0385TW                   | Taiwan  | 09/15/2003  | 07/01/2009 | SELF ALIGNED MEMORY ELEMENT AND WORDLINE                                                                                                                |
| I359495               | H0416TW                   | Taiwan  | 10/13/2004  | 03/01/2012 | SIDEWELL FORMATION FOR HIGH DENSITY POLYMER MEMORY ELEMENT ARRAY                                                                                        |
| I368296               | H0422TW                   | Taiwan  | 06/03/2004  | 07/11/2012 | POLYMER MEMORY DEVICE FORMED IN VIA OPENING                                                                                                             |
| I356470               | H0423TW                   | Taiwan  | 09/30/2004  | 01/11/2012 | SELF ASSEMBLY OF CONDUCTING POLYMER FOR FORMATION OF POLYMER MEMORY CELL                                                                                |
| 92122325              | H0434TW                   | Taiwan  | 08/14/2003  |            | STACKED ORGANIC MEMORY DEVICES AND METHODS OF OPERATING AND FABRICATING                                                                                 |
| I362720               | H0437TW                   | Taiwan  | 05/21/2004  | 04/21/2012 | PLANAR POLYMER MEMORY DEVICE                                                                                                                            |
| 95138344              | H0439TW                   | Taiwan  | 10/18/2006  |            | SYSTEM AND METHOD FOR PROCESSING AN ORGANIC MEMORY CELL                                                                                                 |
| I354388               | H0442TW                   | Taiwan  | 06/30/2004  | 12/11/2011 | ORGANIC MEMORY DEVICE AND METHODS OF USING AND MAKING THE DEVICE                                                                                        |
| I344194               | H0443TW                   | Taiwan  | 04/23/2004  | 06/21/2011 | ERASING AND PROGRAMMING AN ORGANIC MEMORY DEVICE AND METHODS OF OPERATING AND FABRICATING                                                               |
| I327372               | H0496TW                   | Taiwan  | 11/10/2003  | 07/11/2010 | MEMORY DEVICE HAVING A P+ GATE AND THIN BOTTOM OXIDE AND METHOD OF ERASING SAME                                                                         |
| I329339               | H0514TW                   | Taiwan  | 08/13/2003  | 08/21/2010 | NITROGEN OXIDATION TO REDUCE ENCROACHMENT                                                                                                               |
| I 351589              | H0541TW                   | Taiwan  | 08/04/2004  | 11/01/2011 | LOW POWER CHARGE PUMP                                                                                                                                   |
| I320182               | H0570TW                   | Taiwan  | 09/03/2003  | 02/01/2010 | IMPROVED SYSTEM FOR PROGRAMMING A NON-VOLATILE MEMORY CELL                                                                                              |
| I323894               | H0575TW                   | Taiwan  | 09/03/2003  | 04/21/2010 | IMPROVED PRE-CHARGE METHOD FOR READING A NON-VOLATILE MEMORY CELL ARRAY WITH STAGGERED LOCAL INTER-CONNECT STRUCTURE                                    |
| I 345241              | H0576TW                   | Taiwan  | 10/12/2004  | 07/11/2011 | RECESS CHANNEL FLASH ARCHITECTURE FOR REDUCED SHORT CHANNEL EFFECT                                                                                      |
| I359461               | H0577TW                   | Taiwan  | 10/11/2004  | 03/01/2012 | METHOD OF PROGRAMMIN DUAL CELL MEMORY DEVICE TO STORE MULTIPLE DATA STATES PER CELL                                                                     |
| I362666               | H0587TW                   | Taiwan  | 03/18/2004  | 04/21/2012 | METHOD OF DUAL CELL MEMORY DEVICE OPERATION FOR IMPROVED END-OF-LIFE READ MARGIN                                                                        |
| I326875               | H0588TW                   | Taiwan  | 03/24/2004  | 07/01/2010 | IMPROVED METHOD FOR READING A NON-VOLATILE MEMORY CELL ADJACENT TO AN INACTIVE REGION OF A NON-VOLATILE MEMORY CELL ARRAY AND RELATED MEMORY CELL ARRAY |
| I36474                | H0625TW                   | Taiwan  | 01/15/2004  | 01/21/2011 | MEMORY DEVICE AND METHOD USING POSITIVE GATE STRESS TO RECOVER OVERERASED CELL                                                                          |
| I363349               | H0626TW                   | Taiwan  | 09/30/2004  | 05/01/2012 | UV BLOCKING LAYER FOR REDUCING UV-INDUCED CHARGING OF SONOS DUAL-BIT FLASH MEMORY DEVICES IN BEOL PROCESSING                                            |
| I361474               | H0671TW                   | Taiwan  | 01/16/2004  | 04/01/2012 | CASCADE AMPLIFIER CIRCUIT FOR PRODUCING A FAST, STABLE AND ACCURATE BITLINE VOLTAGE                                                                     |
| 92123108              | H1203                     | Taiwan  | 07/10/2003  |            | SELECTION CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS                                                                                                   |
| I 348704              | H1204TW                   | Taiwan  | 01/16/2004  | 09/11/2011 | CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS                                                                                                             |
| I 328815              | H1205TW                   | Taiwan  | 09/03/2003  | 08/11/2010 | CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS                                                                                                             |
| I376729               | H1368TW                   | Taiwan  | 06/30/2004  | 11/11/2012 | PECVD SILICON-RICH OXIDE LAYER FOR REDUCED UV CHARGING                                                                                                  |
| I 344692              | H1414TW                   | Taiwan  | 06/10/2004  | 07/01/2011 | NON-VOLATILE MEMORY DEVICE                                                                                                                              |
| I358134               | H1415TW                   | Taiwan  | 12/03/2004  | 02/11/2012 | FLASH MEMORY DEVICE                                                                                                                                     |
| I333215               | H1513TW                   | Taiwan  | 03/05/2004  | 11/11/2010 | CIRCUIT FOR FAST AND ACCURATE MEMORY READ OPERATIONS                                                                                                    |
| I382529               | H1862TW                   | Taiwan  | 09/03/2004  | 01/11/2013 | MEMORY CELL STRUCTURE HAVING NITRIDE LAYER WITH REDUCED CHARGE LOSS AND METHOD FOR FABRICATING SAME                                                     |
| I325136               | H1892TW                   | Taiwan  | 03/18/2004  | 05/21/2010 | FAST, ACCURATE AND LOW POWER SUPPLY VOLTAGE BOOSTER USING A/D CONVERTER                                                                                 |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY        | FILING DATE | ISSUE DATE | TITLE                                                                                                                                     |
|-----------------------|---------------------------|----------------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 94114206              | H1984TW                   | Taiwan         | 05/03/2005  |            | METHODS AND APPARATUS FOR WORDLINE PROTECTION IN FLASH MEMORY DEVICES                                                                     |
| I357113               | H1985TW                   | Taiwan         | 01/07/2005  | 01/21/2012 | POCKET IMPLANT FOR COMPLEMENTARY BIT DISTURB IMPROVEMENT AND CHARGING IMPROVEMENT OF SONOS MEMORY CELL                                    |
| 387048                | H1990TW                   | Taiwan         | 08/02/2005  | 02/21/2013 | METHOD OF FORMING NARROWLY SPACED FLASH MEMORY CONTACT OPENINGS AND LITHOGRAPHY MASKS                                                     |
| I381457               | H1993TW                   | Taiwan         | 05/10/2005  | 01/01/2013 | BITLINE IMPLANT UTILIZING DUAL POLY                                                                                                       |
| 95111926              | H1998                     | Taiwan         | 04/04/2006  |            | NON-CRITICAL COMPLEMENTARY MASKING METHOD FOR POLY-1 DEFINITION IN FLASH MEMORY DEVICE FABRICATION                                        |
| 95123101              | H2114TW                   | Taiwan         | 07/01/2006  |            | USE OF SUPERCRITICAL FLUID TO DRY WAFER AND CLEAN LANS IN IMMERSION LITHOGRAPHY                                                           |
| 102740                | JC137496TW                | Taiwan         | 06/23/1997  | 08/31/1999 | SEMICONDUCTOR DEVICE HAVING INTERLAYER INSULATOR AND METHOD FOR FABRICATING THEREOF                                                       |
| 148296                | JC684497TW                | Taiwan         | 11/26/1999  | 05/01/2002 | HIGH YIELD, HIGH PERFORMANCE SEMICONDUCTOR PROCESS FLOW FOR NAND FLASH MEMORY PRODUCTS                                                    |
| I421878               | JDE0584TW                 | Taiwan         | 04/26/2006  | 01/01/2014 | PORTABLE WIRELESS DATA STORAGE DEVICE                                                                                                     |
| I371755               | P-5484-TW                 | Taiwan         | 10/28/2004  | 09/01/2012 | METHOD, SYSTEM AND CIRCUIT FOR PROGRAMMING A NON-VOLATILE MEMORY ARRAY                                                                    |
| I363350               | P-5487-TW                 | Taiwan         | 10/28/2004  | 05/01/2012 | METHOD CIRCUIT AND SYSTEM FOR DETERMINING A REFERENCE VOLTAGE                                                                             |
| I381382               | P-5487-TW1                | Taiwan         | 10/27/2004  |            | METHOD FOR READ ERROR DETECTION IN A NON-VOLATILE MEMORY ARRY                                                                             |
| I379306               | P-5675-TW                 | Taiwan         | 12/03/2004  | 12/11/2012 | APPARATUS AND METHODS FOR MULTI-LEVEL SENSING IN A MEMORY ARRAY                                                                           |
| 097122346             | P-6628US CIP              | Taiwan         | 07/09/2008  |            | METHOD FOR READING NON-VOLATILE MEMORY CELLS                                                                                              |
| NI-103163             | P-878TW                   | Taiwan         | 08/14/1997  | 05/21/1999 | NON-VOLATILE SEMICONDUCTOR MEMORY CELL UTILIZING ASYMMETRICAL CHARGE TRAPPING                                                             |
| I286758               | SE0002TW                  | Taiwan         | 04/15/2003  | 09/11/2007 | A SYSTEM AND METHOD OF ERASE VOLTAGE CONTROL DURING MULTIPLE SECTOR ERASE OF A FLASH MEMORY DEVICE                                        |
| 102135803             | SP09-0008TW               | Taiwan         | 10/03/2013  |            | IMPROVED SPACER DESIGN TO PREVENT TRAPPED ELECTRONS                                                                                       |
| 102127733             | SP09-0058TW               | Taiwan         | 08/02/2013  |            | POWER SAVINGS APPARATUS AND METHOD FOR MEMORY DEVICE USING DELAY LOCKED LOOP                                                              |
| 101148011             | SP11-0021TW               | Taiwan         | 12/18/2012  |            | APPARATUS AND METHOD FOR A REDUCED PIN COUNT (RPC) MEMORY BUS INTERFACE INCLUDING A READ DATA STROBE SIGNAL                               |
| 101148010             | SP11-0034KR               | Taiwan         | 12/18/2012  |            | CONTINUOUS READ BURST SUPPORT AT HIGH CLOCK RATES                                                                                         |
| 102115391             | SP11-0044TW               | Taiwan         | 04/30/2013  |            | POWER-EFFICIENT VOICE ACTIVATION                                                                                                          |
| 102111841             | SP12-0013TW               | Taiwan         | 04/02/2013  |            | ADAPTIVELY PROGRAMMING OR ERASING FLASH MEMORY BLOCKS                                                                                     |
| 102127388             | SP12-0021TW               | Taiwan         | 07/31/2013  |            | BITLINE VOLTAGE REGULATION IN NON-VOLATILE MEMORY                                                                                         |
| 102135802             | SP12-0034 TW              | Taiwan         | 10/03/2013  |            | SUPPLY POWER DEPENDENT CONTROLLABLE WRITE THROUGHPUT FOR MEMORY APPLICATIONS                                                              |
| 104105547             | SP13-0036TW               | Taiwan         | 02/17/2015  |            | MEMORY SUBSYSTEM WITH WRAPPED-TO-CONTINUOUS READ                                                                                          |
| I 448899              | SPSNP1223TW               | Taiwan         | 12/12/2008  | 08/11/2014 | REFERENCE-FREE SAMPLED SENSING                                                                                                            |
| EP0631285             | A901/1997GB               | United Kingdom | 04/11/1994  | 12/23/1998 | VOLTAGE SUPPLY DETECTION                                                                                                                  |
| 0656628               | A938GB                    | United Kingdom | 11/10/1994  | 04/09/2003 | PROGRAMMED REFERENCE                                                                                                                      |
| 0677850               | A960/2054GB               | United Kingdom | 03/23/1995  | 05/09/2001 | METHOD AND APPARATUS FOR PROGRAMMING MEMORY DEVICES                                                                                       |
| 0690508               | A976/2067GB               | United Kingdom | 06/20/1995  | 09/11/2002 | HIGH ENERGY BURIED LAYER IMPLANT TO PROVIDE A LOW RESISTANCE P-WELL IN A FLASH EPROM ARRAY                                                |
| 1222663               | AF01002GB                 | United Kingdom | 10/07/2000  | 06/30/2004 | LOW VOLTAGE READ CASCODE FOR 2V/3V AND DIFFERENT BANK COMBINATIONS WITHOUT METAL OPTIONS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE |
| 1234324               | AF01054GB                 | United Kingdom | 10/16/2000  | 10/04/2006 | HIGH TEMPERATURE OXIDE DEPOSITION PROCESS FOR FABRICATING AN ONO FLOATING-GATE ELECTRODE IN A TWO BIT EEPROM DEVICE                       |
| 1344221               | AF01073GB                 | United Kingdom | 07/31/2001  | 11/05/2008 | WORD LINE DECODING ARCHITECTURE IN A FLASH MEMORY                                                                                         |
| 1266377               | AF01075GB                 | United Kingdom | 03/12/2001  | 09/12/2007 | MULTIPLE BANK SIMULTANEOUS OPERATION FOR A FLASH MEMORY                                                                                   |
| 1295294               | AF01076GB                 | United Kingdom | 05/21/2001  | 01/25/2005 | BURST ARCHITECTURE FOR A FLASH MEMORY                                                                                                     |
| 1327193               | AF01078GB                 | United Kingdom | 07/17/2001  | 02/21/2007 | BURST READ INCORPORATING OUTPUT BASED REDUNDANCY                                                                                          |
| 1297534               | AF01085GB                 | United Kingdom | 06/04/2001  | 03/14/2007 | METHOD TO REDUCE CAPACITIVE LOADING IN FLASH MEMORY X-DECODER FOR ACCURATE VOLTAGE CONTROL AT WORDLINES AND SELECT LINES                  |
| 1226586               | AF01086GB                 | United Kingdom | 09/29/2000  | 06/18/2003 | A WORD LINE TRACKING STRUCTURE FOR USE IN AN ARRAY OF FLASH EEPROM MEMORY CELLS                                                           |
| 2391985               | AF01090GB                 | United Kingdom | 11/14/2001  | 11/24/2004 | I/O PARTITIONING AND METHODOLOGY TO REDUCE BAND-TO-BAND TUNNELING CURRENT DURING ERASE                                                    |
| 1415302               | AF01096GB                 | United Kingdom | 12/12/2001  | 12/07/2005 | SOFT PROGRAM AND SOFT PROGRAM VERIFY OF THE CORE CELLS IN FLASH MEMORY ARRAY                                                              |
| 1338034               | AF01102GB                 | United Kingdom | 08/07/2001  | 01/06/2010 | SIMULTANEOUS FORMATION CHARGE STORAGE AND BITLINE TO WORDLINE ISOLATION                                                                   |
| 1338037               | AF01112GB                 | United Kingdom | 11/15/2001  | 03/30/2011 | NON-VOLATILE SONOS SEMICONDUCTOR MEMORY DEVICE                                                                                            |
| 1495471               | AF01116GB                 | United Kingdom | 03/03/2003  | 10/17/2007 | SYSTEM AND METHOD FOR MULTI-BIT FLASH READS USING DUAL DYNAMIC REFERENCES                                                                 |
| 2407913               | AF01132GB                 | United Kingdom | 01/21/2003  | 10/19/2005 | HARD MASK PROCESS FOR MEMORY DEVICE WITHOUT BITLINE SHORTS                                                                                |
| 1493185               | AF01137GB                 | United Kingdom | 02/14/2003  | 11/11/2009 | MEMORY MANUFACTURING PROCESS WITH BITLINE ISOLATION                                                                                       |
| 1636801               | AF01169GB                 | United Kingdom | 05/21/2004  | 11/02/2006 | MEMORY WITH A CORE-BASED VIRTUAL GROUND AND DYNAMIC REFERENCE SENSING SCHEME                                                              |
| 1665387               | AF01182GB                 | United Kingdom | 05/21/2004  | 08/13/2008 | MEMORY DEVICE AND METHOD OF ERASING THE SAME                                                                                              |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY        | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                                            |
|-----------------------|---------------------------|----------------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2434030               | AF01209GB                 | United Kingdom | 04/13/2004  | 01/09/2008 | METHOD FOR REDUCING SHORT CHANNEL EFFECTS IN MEMORY CELLS AND RELATED STRUCTURE                                                                                                                  |
| 2430802               | AF01232GB                 | United Kingdom | 04/29/2005  | 01/14/2009 | BOND PAD STRUCTURE FOR COPPER METALLIZATION HAVING INCREASED RELIABILITY AND METHOD FOR FABRICATING SAME                                                                                         |
| 2427494               | AF01241GB                 | United Kingdom | 04/13/2004  | 01/16/2008 | NEW COMMAND FOR SECTOR PROTECTION                                                                                                                                                                |
| 2427731               | AF01248GB                 | United Kingdom | 04/21/2004  | 10/21/2008 | NON-VOLATILE SEMICONDUCTOR DEVICE AND METHOD FOR AUTOMATICALLY RECOVERING ERASE FAILURE IN THE DEVICE                                                                                            |
| 0701432.7             | AF01306GB                 | United Kingdom | 06/30/2005  |            | SWITCHABLE MEMORY DIODE- A NEW MEMORY DEVICE                                                                                                                                                     |
| 2432245               | AF01320GB                 | United Kingdom | 08/08/2005  | 03/19/2008 | SYSTEMS AND METHODS FOR ADJUSTING PROGRAMMING THRESHOLDS OF POLYMER MEMORY CELLS                                                                                                                 |
| 2432700               | AF01321DE                 | United Kingdom | 08/08/2005  | 06/04/2008 | POLYMER MEMORY DEVICE WITH VARIABLE PERIOD OF RETENTION TIME                                                                                                                                     |
| 1788582               | AF01329GB                 | United Kingdom | 08/30/2004  | 04/28/2010 | ERASE METHOD OF A NON-VOLATILE MEMORY DEVICE AND A NON-VOLATILE MEMORY DEVICE                                                                                                                    |
| 2434674               | AF01338GB                 | United Kingdom | 10/26/2004  | 12/16/2009 | METHOD OF SETTING INFORMATION OF NON-VOLATILE MEMORY AND NON-VOLATILE MEMORY                                                                                                                     |
| 2431027               | AF01361GB                 | United Kingdom | 06/30/2005  | 12/24/2008 | METHOD OF IMPROVING ERASE VOLTAGE DISTRIBUTION FOR A FLASH MEMORY ARRAY HAVING DUMMY WORDLINES                                                                                                   |
| 1774530               | AF01365GB                 | United Kingdom | 04/29/2005  | 01/23/2008 | FLASH MEMORY UNIT AND METHOD OF PROGRAMMING A FLASH MEMORY DEVICE                                                                                                                                |
| 1717816               | AF01372GB                 | United Kingdom | 02/19/2004  | 12/24/2008 | CURRENT-VOLTAGE CONVERTER CIRCUIT AND CONTROL METHOD THEREOF                                                                                                                                     |
| 1720172               | AF01377GB                 | United Kingdom | 02/20/2004  | 06/06/2012 | A SEMICONDUCTOR MEMORY STORAGE DEVICE AND ITS REDUNDANCY CONTROL METHOD                                                                                                                          |
| 1782460               | AF01379GB                 | United Kingdom | 04/29/2005  | 06/01/2011 | METHOD FOR FABRICATING A FLOATING GATE MEMORY CELL                                                                                                                                               |
| 1717814               | AF01380GB                 | United Kingdom | 02/20/2004  | 09/19/2012 | SEMICONDUCTOR STORAGE DEVICE AND SEMICONDUCTOR STORAGE DEVICE CONTROL METHOD                                                                                                                     |
| 2432699               | AF01383GB                 | United Kingdom | 09/20/2005  | 05/14/2008 | READ APPROACH FOR MULTI-LEVEL VIRTUAL GROUND MEMORY                                                                                                                                              |
| 2436055               | AF01390GB                 | United Kingdom | 12/20/2005  | 08/11/2010 | MULTI-LEVEL ONO FLASH PROGRAM ALGORITHM FOR THRESHOLD WIDTH CONTROL                                                                                                                              |
| 2432024               | AF01402GB                 | United Kingdom | 07/30/2004  | 05/07/2008 | NEW CASCADE AND SENSE-AMPLIFIER                                                                                                                                                                  |
| 2431026               | AF01403GB                 | United Kingdom | 07/30/2004  | 05/07/2008 | SEMICONDUCTOR DEVICE AND WRITING METHOD                                                                                                                                                          |
| 2429315               | AF01416GB                 | United Kingdom | 05/12/2004  | 03/19/2008 | SEMICONDUCTOR DEVICE AND ITS CONTROL METHOD                                                                                                                                                      |
| 2443105               | AF01416GB DIV             | United Kingdom | 12/14/2007  | 09/03/2008 | SEMICONDUCTOR DEVICE AND ITS CONTROL METHOD                                                                                                                                                      |
| 2427948               | AF01417GB                 | United Kingdom | 05/11/2004  | 11/14/2007 | NONVOLATILE SEMICONDUCTOR MEMORY, SEMICONDUCTOR DEVICE AND CHARGE PUMP UNIT                                                                                                                      |
| 2442831               | AF01417GB DIV             | United Kingdom | 05/11/2004  | 06/18/2008 | NONVOLATILE SEMICONDUCTOR MEMORY, SEMICONDUCTOR DEVICE AND CHARGE PUMP UNIT                                                                                                                      |
| 2432698               | AF01422GB                 | United Kingdom | 05/11/2004  | 11/28/2007 | DUMMY CELL ARRAY BETWEEN CORE AND REFERENCE ARRAYS                                                                                                                                               |
| 2430522               | AF01423GB                 | United Kingdom | 05/11/2004  | 02/13/2008 | MULTI BIT PROGRAMMING FOR VIRTUAL GROUND ARRAY                                                                                                                                                   |
| 2427949               | AF01425GB                 | United Kingdom | 05/11/2004  | 06/04/2008 | IMPROVED APPARATUS FOR ADVANCED SECTOR PROTECTION (1)                                                                                                                                            |
| 2444178               | AF01425GB DIV             | United Kingdom | 11/28/2007  | 08/13/2008 | IMPROVED APPARATUS FOR ADVANCED SECTOR PROTECTION (1)                                                                                                                                            |
| 2428121               | AF01427GB                 | United Kingdom | 05/12/2004  | 12/24/2008 | IMPROVED SLATCH AND THE LAYOUT                                                                                                                                                                   |
| 2451592               | AF01427GB DIV             | United Kingdom | 11/26/2008  | 11/25/2009 | IMPROVED SLATCH AND THE LAYOUT                                                                                                                                                                   |
| 2460213               | AF01427GB DIV2            | United Kingdom | 11/26/2008  | 12/30/2009 | IMPROVED SLATCH AND THE LAYOUT                                                                                                                                                                   |
| 1788578               | AF01432GB                 | United Kingdom | 08/31/2004  | 05/11/2011 | THE SEMICONDUCTOR MEMORY STORAGE DEVICE WHICH CARRIED THE NEGATIVE VOLTAGE GENERATING CIRCUIT                                                                                                    |
| 1830366               | AF01438GB                 | United Kingdom | 12/24/2004  | 07/13/2011 | BIAS APPLICATION METHOD OF STORAGE AND STORAGE                                                                                                                                                   |
| 2434676               | AF01439GB                 | United Kingdom | 11/30/2004  | 11/18/2009 | NON-VOLATILE SELECT GATE IN NAND FLASH MEMORY                                                                                                                                                    |
| 2431025               | AF01441GB                 | United Kingdom | 07/29/2004  | 04/29/2009 | A NON-VOLATILE MEMORY APPARATUS AND ITS CONTROL METHOD                                                                                                                                           |
| 2429582               | AF01443GB                 | United Kingdom | 05/11/2004  | 02/11/2009 | CARRIER FOR SEMICONDUCTOR DEVICES TO BE STACKED AND FABRICATION METHOD OF THE DEVICE                                                                                                             |
| 2429842               | AF01446GB                 | United Kingdom | 05/20/2004  | 01/28/2009 | SEMICONDUCTOR CHIP ASSEMBLY AND FABRICATION METHOD OF THE SAME                                                                                                                                   |
| 2427947               | AF01453GB                 | United Kingdom | 02/11/2005  | 07/10/2007 | METHODS AND SYSTEMS FOR HIGH WRITE PERFORMANCE IN MULTI-BIT FLASH MEMORY DEVICES                                                                                                                 |
| 2436234               | AF01454GB                 | United Kingdom | 11/30/2004  | 04/28/2010 | NEW MEMORY CELL STRUCTURE IN WHICH HIGH-SPEED WRITING IS POSSIBLE                                                                                                                                |
| 2434919               | AF01455GB                 | United Kingdom | 11/30/2004  | 05/05/2010 | NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                         |
| 2434901               | AF01463GB                 | United Kingdom | 09/30/2004  | 05/07/2008 | SEMICONDUCTOR DEVICE AND DATA WRITING METHOD                                                                                                                                                     |
| 2437447               | AF01467GB                 | United Kingdom | 01/12/2006  | 07/16/2008 | MEMORY DEVICE HAVING TRAPEZOIDAL BITLINES AND METHOD OF FABRICATING SAME                                                                                                                         |
| 2434917               | AF01468GB                 | United Kingdom | 10/29/2004  | 05/26/2010 | SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME                                                                                                                                          |
| 2434675               | AF01470GB                 | United Kingdom | 11/30/2004  | 01/06/2010 | SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE CONTROL METHOD                                                                                                                                     |
| 2462959               | AF01470GB DIV             | United Kingdom | 11/30/2004  | 01/06/2010 | SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE CONTROL METHOD                                                                                                                                     |
| 1829048               | AF01485GB                 | United Kingdom | 12/20/2005  | 06/15/2011 | METHOD OF PROGRAMMING, READING AND ERASING MEMORY-DIODE IN A MEMORY-DIODE ARRAY                                                                                                                  |
| 2434694               | AF01491GB                 | United Kingdom | 11/10/2005  | 03/31/2010 | DIODE ARRAYS ARCHITECTURE FOR ADDRESSING NANOSCALE RESISTIVE MEMORY ARRAYS                                                                                                                       |
| 0713428.1             | AF01523GB                 | United Kingdom | 12/20/2005  |            | SENSE AMPLIFIER WIHT HIGH VOLTAGE SWING                                                                                                                                                          |
| 2433815               | AF01645GB                 | United Kingdom | 10/26/2004  | 02/25/2009 | NON-VOLATILE STORAGE DEVICE                                                                                                                                                                      |
| 2436271               | AF01653GB                 | United Kingdom | 01/24/2005  | 06/16/2010 | SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME                                                                                                                                          |
| 2436272               | AF01698GB                 | United Kingdom | 01/27/2005  | 01/19/2011 | A NON-VOLATILE MEMORY STORAGE DEVICE AND ITS CONTROL METHOD (PLACEMENT FORMATION (STRUCTURE) OF "AN INFORMATION MEMORY CELL OF OPERATION", AND ITS READ/WRITE APPARATUS, AND ITS CONTROL METHOD) |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY        | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                                            |
|-----------------------|---------------------------|----------------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2468051               | AF01698GB DIV             | United Kingdom | 01/27/2005  | 02/09/2011 | A NON-VOLATILE MEMORY STORAGE DEVICE AND ITS CONTROL METHOD (PLACEMENT FORMATION (STRUCTURE) OF "AN INFORMATION MEMORY CELL OF OPERATION", AND ITS READ/WRITE APPARATUS, AND ITS CONTROL METHOD) |
| 2438128               | AF01709GB                 | United Kingdom | 03/22/2006  | 03/22/2006 | VARIABLE BREAKDOWN CHARACTERISTIC DIODE                                                                                                                                                          |
| 1898460               | AF01792GB                 | United Kingdom | 06/28/2005  | 01/04/2012 | MIRRORBIT DEVICE HAVING STI AND DUAL POLY FILMS                                                                                                                                                  |
| 1907868               | AF01852GB                 | United Kingdom | 07/07/2006  | 08/25/2010 | INTEGRATED CIRCUIT TEST SOCKET                                                                                                                                                                   |
| 1103980               | AF02178GB                 | United Kingdom | 11/24/2000  | 01/16/2008 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                          |
| 1223586               | AF02182GB                 | United Kingdom | 08/18/2000  | 08/03/2005 | NONVOLATILE MEMORY CIRCUIT STORAGE MULTI-                                                                                                                                                        |
| 1310994               | AF02184GB                 | United Kingdom | 07/17/2000  | 02/13/2013 | NONVOLATILE MEMORY DEVICE AND                                                                                                                                                                    |
| 1310963               | AF02186GB                 | United Kingdom | 06/29/2000  | 12/27/2006 | SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                                      |
| 1286359               | AF02200GB                 | United Kingdom | 03/18/2002  | 01/17/2007 | MEMORY CONTROLLER FOR MULTI LEVEL                                                                                                                                                                |
| 1574867               | AF02230GB                 | United Kingdom | 12/17/2003  | 08/08/2007 | SEMICONDUCTOR DEVICE AND TEST METHOD                                                                                                                                                             |
| 1575056               | AF02233GB                 | United Kingdom | 12/17/2003  | 06/06/2007 | NONVOLATILE MEMORY AND METHOD AND WRITE METHOD OF THE SAME                                                                                                                                       |
| 0792516               | B011/2097GB               | United Kingdom | 11/08/1995  | 03/10/1999 | NITRIDE ETCH PROCESS WITH CRITICAL DIMENSION (CD) GAIN                                                                                                                                           |
| 0799497               | B047GB                    | United Kingdom | 11/22/1995  | 01/19/2000 | NOVEL PROCESSING TECHNIQUES FOR ACHIEVING PRODUCTION WORTHY LOW DIELECTRIC LOW INTERCONNECT RESISTANCE AND HIGH PERFORMANCE                                                                      |
| 0784867               | B100GB                    | United Kingdom | 07/31/1996  | 12/05/2007 | THREE-DIMENSIONAL NON-VOLATILE MEMORY                                                                                                                                                            |
| 0780023               | B111GB                    | United Kingdom | 06/21/1996  | 04/10/2002 | PROCESS FOR SELF-ALIGNED SOURCE FOR HIGH DENSITY MEMORY                                                                                                                                          |
| 0856188               | B128GB                    | United Kingdom | 08/30/1996  | 10/27/1999 | A FLASH EEPROM MEMORY WITH SEPARATE REFERENCE ARRAY                                                                                                                                              |
| 0835509               | B132GB                    | United Kingdom | 06/18/1996  | 08/11/1999 | CHANNEL HOT CARRIER PAGE WRITE                                                                                                                                                                   |
| 0880783               | B257GB                    | United Kingdom | 08/15/1996  | 10/13/1999 | LOW SUPPLY VOLTAGE NEGATIVE CHARGE PUMP                                                                                                                                                          |
| 0861517               | B258GB                    | United Kingdom | 07/23/1996  | 10/13/1999 | A FAST 3 STATE BOOSTER CIRCUIT                                                                                                                                                                   |
| 0858661               | B260GB                    | United Kingdom | 07/19/1996  | 12/15/1999 | A NEW PROGRAM ALGORITHM FOR LOW VOLTAGE (3V) SINGLE POWER SUPPLY FLASH MEMORIES                                                                                                                  |
| 0857346               | B261GB                    | United Kingdom | 06/21/1996  | 08/11/1999 | A PROGRAM ERASE ALGORITHM THAT GREATLY REDUCES UNDER ERASE IN FLASH MEMORIES                                                                                                                     |
| 0858660               | B262GB                    | United Kingdom | 07/19/1996  | 09/15/1999 | TEMPERATURE COMPENSATED REFERENCE FOR OVER ERASE CORRECTION CIRCUITRY                                                                                                                            |
| 97917648.4            | B277GB                    | United Kingdom | 03/25/1997  | 07/09/2008 | A NOVEL PROCESS FOR RELIABLE ULTRATHIN OXYNITRIDE FORMATION                                                                                                                                      |
| 0907956               | C072296GB                 | United Kingdom | 03/28/1997  | 05/31/2000 | USING FLOATING GATE DEVICES AS SELECT GATE DEVICES FOR NAND FLASH MEMORY AND ITS BIAS SCHEME                                                                                                     |
| 1019914               | C141496GB                 | United Kingdom | 04/10/1998  | 03/06/2002 | A DUAL SOURCE SIDE POLYSILICON SELECT GATE STUCTURE AND PROGRAMMING METHOD UTILIZING SINGLE TUNNEL OXIDE FOR NAND ARRAY FLASH MEMORY                                                             |
| 0944907               | C196596GB                 | United Kingdom | 11/13/1997  | 10/17/2001 | BANK ARCHITECTURE FOR A NON-VOLATILE MEMORY ENABLING SIMULTANEOUS READING AND WRITING                                                                                                            |
| 1040486               | C369297GB                 | United Kingdom | 12/18/1998  | 02/27/2002 | BIASING METHOD AND STRUCTURE FOR REDUCING BAND-TO-BAND AND/OR AVALANCHE CURRENTS DURING THE ERASE OF FLASH MEMORY DEVICE                                                                         |
| 1012878               | C526397GB                 | United Kingdom | 08/25/1998  | 07/28/2004 | REDUCTION OF CHARGE LOSS IN NONVOLATILE MEMORY CELLS BY PHOSPHOROUS IMPLANTATION INTO PECVD NITRIDE/OXYNITRIDE FILMS                                                                             |
| 1042810               | C627497GB                 | United Kingdom | 12/18/1998  | 05/20/2010 | METHODS AND ARRANGEMENTS FOR IMPROVED FORMATION OF CONTROL AND FLOATING GATES IN NON-VOLATILE MEMORY SEMICONDUCTOR DEVICES                                                                       |
| 1247299               | C656497GB                 | United Kingdom | 08/31/2000  | 04/11/2007 | TUNGSTEN GATE MOS TRANSISTOR AND MEMORY CELL AND METHOD OF MAKING SAME                                                                                                                           |
| 1204989               | C695497GB                 | United Kingdom | 06/29/2000  | 04/02/2014 | THIN FLOATING GATE AND CONDUCTIVE SELECT GATE IN SITU                                                                                                                                            |
| 1116240               | C715497GB                 | United Kingdom | 09/21/1999  | 11/13/2002 | WORDLINE DRIVER FOR FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EEPROM)                                                                                                           |
| 1203378               | C725497GB                 | United Kingdom | 08/01/2000  | 03/05/2003 | CIRCUIT IMPLEMENTATION TO QUENCH BIT LINE LEAKAGE CURRENT IN PROGRAM AND AUTO PROGRAM DISTURB MODE IN FLASH EPROM USING RESISTOR SOURCE LOAD                                                     |
| 1123547               | D016GB                    | United Kingdom | 10/05/1999  | 08/06/2003 | BIT LINE BIASING METHOD TO ELIMINATE PROGRAM DISTURBANCE IN A NON-VOLATILE MEMORY DEVICE AND MEMORY DEVICE EMPLOYING THE SAME                                                                    |
| 1125302               | D138GB                    | United Kingdom | 10/05/1999  | 01/08/2003 | SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON-VOLATILE MEMORY ARRAY                                                                                                                            |
| 1116238               | D139GB                    | United Kingdom | 08/16/1999  | 02/26/2003 | BANK SELECTOR CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITETURE                                                                                |
| 1116239               | D168GB                    | United Kingdom | 08/16/1999  | 05/15/2002 | SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                                                                                    |
| 1116236               | D169GB                    | United Kingdom | 08/16/1999  | 05/15/2002 | METHOD OF MAKING FLEXIBLY PARTITIONED METAL LINE SEGMENTS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                                           |
| 1125301               | D170GB                    | United Kingdom | 08/16/1999  | 10/16/2002 | MEMORY ADDRESS DECODING CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                                                                     |
| 1142014               | D802GB                    | United Kingdom | 10/27/1999  | 09/03/2008 | METHOD FOR IMPROVING ELECTROSTATIC DISCHARGE (ESD) ROBUSTNESS                                                                                                                                    |
| 1175680               | D832GB                    | United Kingdom | 05/05/2000  | 02/26/2003 | RAMPED OR STEPPED GATE CHANNEL ERASE FOR FLASH MEMORY APPLICATION                                                                                                                                |
| 1214715               | D833GB                    | United Kingdom | 08/29/2000  | 10/15/2009 | 1 TRANSISTOR FOR EEPROM APPLICATION                                                                                                                                                              |
| 1224696               | D838GB                    | United Kingdom | 10/24/2000  | 08/30/2006 | SOLID-SOURCE DOPING FOR SOURCE/DRAIN OF FLASH MEMORY                                                                                                                                             |
| 1218941               | D877GB                    | United Kingdom | 07/17/2000  | 04/02/2014 | NON-VOLATILE MEMORY HAVING HIGH GATE COUPLING CAPACITANCE                                                                                                                                        |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY        | FILING DATE | ISSUE DATE | TITLE                                                                                                                     |
|-----------------------|---------------------------|----------------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------|
| 1222690               | D894GB                    | United Kingdom | 09/29/2000  | 01/23/2008 | METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITH REDUCED ARC LOSS IN PERIPHERAL CIRCUITRY REGION                       |
| 1218938               | DA01016GB                 | United Kingdom | 07/14/2000  | 12/19/2007 | METHOD FOR PROVIDING A DOPANT LEVEL FOR POLYSILICON FOR FLASH MEMORY DEVICES                                              |
| 0221924.4             | DA01025GB                 | United Kingdom | 04/03/2001  |            | FLASH MEMORY ARRAY AND A METHOD AND SYSTEM OF FABRICATION THEREOF                                                         |
| 1256116               | E0251GB                   | United Kingdom | 07/14/2000  | 09/03/2003 | FLASH MEMORY ARCHITECTURE EMPLOYING THREE LAYER METAL INTERCONNECT                                                        |
| 1290559               | E0462GB                   | United Kingdom | 05/21/2001  | 03/24/2004 | DUAL PORTED CAMS FOR SIMULTANEOUS OPERATION FLASH MEMORY                                                                  |
| 1350253               | F0257GB                   | United Kingdom | 08/07/2001  | 09/22/2010 | METHOD AND SYSTEM FOR EMBEDDED CHIP ERASE VERIFICATION                                                                    |
| 2400708               | F0258GB                   | United Kingdom | 12/17/2002  | 08/17/2005 | METHOD AND APPARATUS FOR SOFT PROGRAM VERIFICATION IN A MEMORY DEVICE                                                     |
| 1468424               | F0262GB                   | United Kingdom | 12/17/2002  | 06/08/2005 | METHOD AND APPARATUS FOR SOFT PROGRAM VERIFICATION IN A MEMORY DEVICE                                                     |
| 2400709               | F0272GB                   | United Kingdom | 12/17/2002  | 12/28/2005 | CHARGE INJECTION                                                                                                          |
| 1366497               | F0274GB                   | United Kingdom | 11/01/2001  | 06/04/2014 | HIGHER PROGRAM VT AND FASTER PROGRAMMING RATES BASED ON IMPROVED ERASE METHODS                                            |
| 1435114               | F0283GB                   | United Kingdom | 09/27/2002  | 12/08/2010 | SALICIDED GATE FOR VIRTUAL GROUND ARRAYS                                                                                  |
| 1386323               | F1067GB                   | United Kingdom | 02/19/2002  | 06/17/2009 | THRESHOLD VOLTAGE COMPACTING FOR NON-VOLATILE SEMICONDUCTOR MEMORY DESIGNS                                                |
| 69412360              | FMA13-0015FR              | United Kingdom | 05/26/1994  | 08/12/1998 | POWER LINE CONNECTION CIRCUIT AND POWER LINES SWITCH IC FOR THE SAME                                                      |
| 0915231.5             | FMA13-00335GB             | United Kingdom | 03/14/2007  |            | OUTPUT CIRCUIT                                                                                                            |
| 2345148               | FMA13-00472FR             | United Kingdom | 11/11/2008  | 09/03/2014 | METHOD OF DETECTING AN OPERATING CONDITION OF AN ELECTRIC STEPPER MOTOR                                                   |
| 2381450               | FMA13-00503FR             | United Kingdom | 02/03/2011  | 07/16/2014 | SEMICONDUCTOR MEMORY                                                                                                      |
| 2308026               | FMA13-0102GB              | United Kingdom | 08/30/1995  | 02/10/1999 | ELECTRONIC APPARATUS HAVING A BATTERY PACK                                                                                |
| 2308025               | FMA13-0102GB DIV          | United Kingdom | 08/30/1995  | 02/10/1999 | CHARGING DEVICE                                                                                                           |
| 2308024               | FMA13-0102GB DIV1         | United Kingdom | 08/30/1995  | 02/10/1999 | CHARGING AND DISCHARGING DEVICE                                                                                           |
| 2292845               | FMA13-0102US CON          | United Kingdom | 08/30/1995  | 02/10/1999 | ELECTRONIC APPARATUS                                                                                                      |
| 1435694               | FMA13-0177FR-2            | United Kingdom | 12/23/2003  | 08/30/2006 | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT JITTER GENERATION CIRCUIT AND SEMICONDUCTOR DEVICE                               |
| 1641124               | FMA13-0177GB              | United Kingdom | 12/23/2003  | 06/03/2009 | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT                                                                                  |
| 1672800               | FMA13-0177GB1             | United Kingdom | 12/23/2003  | 08/19/2009 | JITTERY GENERATION CIRCUIT                                                                                                |
| 1553636               | FMA13-0178FR              | United Kingdom | 03/03/2003  | 05/01/2013 | MOS TYPE VARIABLE CAPACITANCE DEVICE                                                                                      |
| 1857826               | FMA13-0211EP DIV          | United Kingdom | 04/04/2005  | 08/07/2013 | CAPACITANCE DIFFERENCE DETECTING CIRCUIT AND MEMS SENSOR                                                                  |
| 1906312               | FMA13-0227FR              | United Kingdom | 01/26/2005  | 07/25/2012 | DYNAMIC MEMORY CONFIGURATION                                                                                              |
| 1748562               | FMA13-0266FR              | United Kingdom | 11/01/2005  | 05/07/2008 | CLOCK GENERATING CIRCUIT AND CLOCK GENERATING METHOD                                                                      |
| 2436406               | FMA13-0299US              | United Kingdom | 03/23/2006  | 09/15/2009 | DELAY CONTROL CIRCUIT                                                                                                     |
| 1399965               | G0074GB                   | United Kingdom | 12/14/2001  | 01/12/2011 | SOURCE DRAIN IMPLANT DURING ONO FORMATION FOR IMPROVED ISOLATION OF SONOS DEVICES                                         |
| 1529293               | G0391GB                   | United Kingdom | 06/10/2003  | 11/23/2005 | BUILT-IN-SELF-TEST (BIST) OF FLASH MEMORY CELLS AND IMPLEMENTATION OF BIST INTERFACE                                      |
| 1459374               | G0689GB                   | United Kingdom | 12/11/2002  | 03/17/2010 | SHALLOW TRENCH ISOLATION APPROACH FOR IMPROVED STI CORNER ROUNDING                                                        |
| 0509151.7             | G0730-PCT                 | United Kingdom | 09/24/2003  |            | METHOD FOR REDUCING CONTACT DEFECTS IN SEMICONDUCTOR CELLS                                                                |
| 1497833               | G0861GB                   | United Kingdom | 02/14/2003  | 12/08/2008 | IMPROVED ERASE METHOD FOR SINGLE SIDED MIRROR OPERATION                                                                   |
| 1493159               | G0862GB                   | United Kingdom | 02/14/2003  | 10/01/2009 | REFRESH SCHEME FOR DYNAMIC PAGE PROGRAMMING                                                                               |
| 1568045               | G0865GB                   | United Kingdom | 07/10/2003  | 12/09/2009 | METHOD AND SYSTEM FOR DEFINING A REDUNDANCY WINDOW AROUND A PARTICULAR COLUMN IN A MEMORY ARRAY                           |
| 1518247               | G0866GB                   | United Kingdom | 04/22/2003  | 02/08/2006 | STEPPED PRE-ERASE VOLTAGE FOR MIRRORBIT ERASE                                                                             |
| 0417907.3             | G1255GB                   | United Kingdom | 02/05/2003  |            | PARTIAL PAGE PROGRAMMING OF MULTI LEVEL FLASH                                                                             |
| 1559110               | H0297GB                   | United Kingdom | 07/10/2003  | 01/20/2010 | CONTROL OF MEMORY ARRAYS UTILIZING ZENER DIODE-LIKE DEVICES                                                               |
| 2432701               | H0325GB                   | United Kingdom | 09/19/2005  | 04/09/2008 | CONTROL OF MEMORY DEVICES POSSESSING VARIABLE RESISTANCE CHARACTERISTICS                                                  |
| 2419231               | H0422GB                   | United Kingdom | 05/11/2004  | 01/17/2007 | METHOD AND SYSTEM FOR MANUFACTURING POLYMER MEMORY DEVICE IN VIA OPENING                                                  |
| 2423174               | H0423GB                   | United Kingdom | 09/16/2004  | 04/02/2008 | SELF ASSEMBLY OF CONDUCTING POLYMER FOR FORMATION OF POLYMER MEMORY CELL                                                  |
| 1559109               | H0434GB                   | United Kingdom | 07/10/2003  | 02/24/2010 | STACKED ORGANIC MEMORY DEVICES AND METHODS OF OPERATING AND FABRICATING                                                   |
| 1629535               | H0437GB                   | United Kingdom | 05/11/2004  | 03/14/2007 | PLANAR POLYMER MEMORY DEVICE                                                                                              |
| 1556887               | H0514GB                   | United Kingdom | 06/10/2003  | 04/16/2008 | NITROGEN OXIDATION TO REDUCE ENCROACHMENT                                                                                 |
| GB2419044             | H0541GB                   | United Kingdom | 07/15/2004  | 09/13/2006 | LOW POWER CHARGE PUMP                                                                                                     |
| 1568043               | H0570GB                   | United Kingdom | 07/24/2003  | 12/05/2007 | IMPROVED SYSTEM FOR PROGRAMMING A NON-VOLATILE MEMORY CELL                                                                |
| 1568037               | H0575GB                   | United Kingdom | 07/24/2003  | 06/18/2008 | IMPROVED PRE-CHARGE METHOD FOR READING A NON-VOLATILE MEMORY CELL ARRAY WITH STAGGERED LOCAL INTERCONNECT STRUCTURE       |
| 1673781               | H0576GB                   | United Kingdom | 09/16/2004  | 07/25/2007 | RECESS CHANNEL FLASH ARCHITECTURE FOR REDUCED SHORT CHANNEL EFFECT                                                        |
| 2422955               | H0577GB                   | United Kingdom | 09/16/2004  | 04/11/2007 | RECESS CHANNEL FLASH ARCHITECTURE FOR REDUCED SHORT CHANNEL EFFECT                                                        |
| 1590810               | H0625GB                   | United Kingdom | 01/08/2004  | 07/27/2011 | IMPROVED METHOD FOR READING A NON-VOLATILE MEMORY CELL ADJACENT TO AN INACTIVE REGION OF A NON-VOLATILE MEMORY CELL ARRAY |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY        | FILING DATE | ISSUE DATE | TITLE                                                                                                                           |
|-----------------------|---------------------------|----------------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------|
| 2425201               | H0626GB                   | United Kingdom | 09/16/2004  | 04/25/2007 | MEMORY DEVICE AND METHOD USING POSITIVE GATE STRESS TO RECOVER OVERERASED CELL                                                  |
| 1563507               | H1203GB                   | United Kingdom | 07/10/2003  | 04/15/2009 | CASCADE AMPLIFIER CIRCUIT FOR PRODUCING A FAST, STABLE AND ACCURATE BITLINE VOLTAGE                                             |
| 1573746               | H1205GB                   | United Kingdom | 07/24/2003  | 12/24/2008 | CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS                                                                                     |
| 1644974               | H1368GB                   | United Kingdom | 06/18/2004  | 06/15/2011 | PECVD SILICON-RICH OXIDE LAYER FOR REDUCED UV CHARGING                                                                          |
| 2418535               | H1414GB                   | United Kingdom | 06/05/2004  | 11/07/2007 | NON-VOLATILE MEMORY DEVICE                                                                                                      |
| 2424518               | H1415GB                   | United Kingdom | 10/26/2004  | 07/04/2007 | FLASH MEMORY DEVICE                                                                                                             |
| 1602109               | H1513GB                   | United Kingdom | 03/01/2004  | 10/15/2008 | CIRCUIT FOR FAST AND ACCURATE MEMORY READ OPERATIONS                                                                            |
| 2420226               | H1862GB                   | United Kingdom | 08/31/2004  | 01/17/2007 | MEMORY CELL STRUCTURE HAVING NITRIDE LAYER WITH REDUCED CHARGE LOSS AND METHOD FOR FABRICATING SAME                             |
| 1434232               | H1979GB                   | United Kingdom | 08/13/2001  | 09/19/2007 | MEMORY CELL                                                                                                                     |
| 0621481.1             | H1984GB                   | United Kingdom | 02/11/2005  |            | METHODS AND APPARATUS FOR WORDLINE PROTECTION IN FLASH MEMORY DEVICES                                                           |
| 2431291               | H1990GB                   | United Kingdom | 04/29/2005  | 12/27/2007 | METHOD OF FORMING NARROWLY SPACED FLASH MEMORY CONTACT OPENINGS                                                                 |
| 1745511               | H1993GB                   | United Kingdom | 02/11/2005  | 03/31/2010 | BITLINE IMPLANT UTILIZING DUAL POLY                                                                                             |
| 1872399               | H1998GB                   | United Kingdom | 04/04/2006  | 06/18/2014 | A NON-CRITICAL COMPLEMENTARY MASKING METHOD FOR POLY-1 DEFINITION IN FLASH MEMORY DEVICE FABRICATION                            |
| 0801083.7             | H2114GB                   | United Kingdom | 06/23/2006  |            | USE OF SUPERCRITICAL FLUID TO DRY WAFER AND CLEAN LANS IN IMMERSION LITHOGRAPHY                                                 |
| 1459374               | P116WO-GB                 | United Kingdom | 12/11/2002  | 03/17/2010 | A SHALLOW TRENCH ISOLATION APPROACH FOR IMPROVED STI CORNER ROUNDING                                                            |
| 1168363               | P-2505GB                  | United Kingdom | 06/15/2001  | 08/09/2006 | METHOD FOR PROGRAMMING OF A SEMICONDUCTOR MEMORY CELL                                                                           |
| 1527458               | SE0002GB                  | United Kingdom | 03/11/2003  | 01/16/2008 | A SYSTEM AND METHOD OF ERASE VOLTAGE CONTROL DURING MULTIPLE SECTOR ERASE OF A FLASH MEMORY DEVICE                              |
| 1502677.6             | SP09-0058GB               | United Kingdom | 07/31/2013  |            | POWER SAVINGS APPARATUS AND METHOD FOR MEMORY DEVICE USING DELAY LOCKED LOOP                                                    |
| 1305446.5             | SP11-0021GB               | United Kingdom | 03/26/2013  |            | APPARATUS AND METHOD FOR A REDUCED PIN COUNT (RPC) MEMORY BUS INTERFACE INCLUDING A READ DATA STROBE SIGNAL                     |
| 1415401.7             | SP11-0027 GB              | United Kingdom | 02/08/2013  |            | IMPROVING REDUNDANCY LOADING EFFICIENCY                                                                                         |
| 2500082               | SP11-0034CN               | United Kingdom | 01/02/2013  | 03/19/2014 | CONTINUOUS READ BURST SUPPORT AT HIGH CLOCK RATES                                                                               |
| 1501977.1             | SP12-0021GB               | United Kingdom | 07/29/2013  |            | BITLINE VOLTAGE REGULATION IN NON-VOLATILE MEMORY                                                                               |
| 1502853.3             | SP13-0036GB               | United Kingdom | 02/20/2015  |            | MEMORY SUBSYSTEM WITH WRAPPED-TO-CONTINUOUS READ                                                                                |
| 0729187               | TT0497FR                  | United Kingdom | 01/30/1996  | 04/03/2002 | A NON-VOLATILE MEMORY DEVICES HAVING A FLOATING GATE WITH ENHANCED CHANGE RETENTION                                             |
| 0929898               | TT1997GB                  | United Kingdom | 09/29/1997  | 11/28/2001 | MEMORY BLOCK SELECT USING MULTIPLE WORD LINES TO ADDRESS A SINGLE MEMORY CELL ROW                                               |
| 6,180,538             | 9076/434-AMD              | United States  | 10/25/1999  | 01/30/2001 | PROCESS FOR FABRICATING AN ONO FLOATING-GATE ELECTRODE IN A TWO-BIT EEPROM DEVICE USING RAPID-THERMAL-CHEMICAL-VAPOR-DEPOSITION |
| 4,716,552             | A328/1235US               | United States  | 03/29/1985  | 12/29/1987 | METHOD AND APPARATUS FOR NON-DESTRUCTIVE ACCESS OF VOLATILE AND NONVOLATILE DATE IN A SHADOW MEMORY ARRAY                       |
| 4,672,580             | A332/1315US               | United States  | 04/30/1985  | 06/09/1987 | MEMORY CELL PROVIDING SIMULTANEOUS NON-DESTRUCTIVE ACCESS TO VOLATILE AND NON-VOLATILE DATA                                     |
| 4,672,241             | A342/1324US               | United States  | 05/29/1985  | 06/09/1987 | HIGH VOLTAGE ISOLATION ON CMOS NETWORKS                                                                                         |
| 4,789,883             | A413/1408US               | United States  | 12/17/1985  | 12/06/1988 | INTEGRATED CIRCUIT STRUCTURE HAVING GATE ELECTRODE AND UNDERLYING OXIDE AND METHOD OF MAKING SAME                               |
| 4,774,197             | A496/1525US               | United States  | 06/17/1986  | 09/27/1988 | METHOD OF IMPROVING SILICON DIOXIDE                                                                                             |
| 07/162,822            | A628/1701US               | United States  | 03/02/1988  |            | EPROM ELEMENT EMPLOYING SELF-ALIGNING PROCESS                                                                                   |
| 4,964,143             | A628US CIP                | United States  | 11/23/1988  | 10/16/1990 | EPROM ELEMENT EMPLOYING SELF-ALIGNING PROCESS                                                                                   |
| 5,091,326             | A628US DIV                | United States  | 09/12/1990  | 02/25/1992 | EPROM ELEMENT EMPLOYING SELF-ALIGNING PROCESS                                                                                   |
| 4,894,353             | A629/1703US               | United States  | 04/29/1988  | 01/16/1990 | METHOD OF FABRICATING PASSIVATED TUNNEL OXIDE                                                                                   |
| 4,958,321             | A674/1751US               | United States  | 09/22/1988  | 09/18/1990 | ONE TRANSISTOR FLASH EPROM CELL                                                                                                 |
| 5,013,675             | A719/1812US               | United States  | 05/23/1989  | 05/07/1991 | METHOD OF FORMING AND REMOVING POLYSILICON LIGHTLY DOPED DRAIN SPACERS                                                          |
| 4,992,391             | A738/1820US               | United States  | 11/29/1989  | 02/12/1991 | PROCESS FOR FABRICATING A CONTROL GATE FOR A FLOATING GATE FET                                                                  |
| 5,107,465             | A747/1841US               | United States  | 09/13/1989  | 04/21/1992 | ASYNCHRONOUS/SYNCHRONOUS PIPELINE DUAL MODE MEMORY ACCESS CIRCUIT                                                               |
| 4,914,055             | A750/1853US               | United States  | 08/24/1989  | 04/03/1990 | SEMICONDUCTOR ANTIFUSE STRUCTURE AND METHOD                                                                                     |
| 5,126,808             | A754/1863US               | United States  | 10/23/1989  | 06/30/1992 | FLASH EEPROM ARRAY WITH PAGED ERASE ARCHITECTURE                                                                                |
| 5,077,691             | A755/1866US               | United States  | 10/23/1989  | 12/31/1991 | FLASH EEPROM ARRAY WITH NEGATIVE GATE VOLTAGE ERASE OPERATION                                                                   |
| 5,008,799             | A767/1836US               | United States  | 04/05/1990  | 04/16/1991 | BACK-TO-BACK CAPACITOR CHARGE PUMP                                                                                              |
| 5,059,815             | A768/1837US               | United States  | 04/05/1990  | 10/22/1991 | HIGH VOLTAGE CHARGE PUMP WITH SERIES CAPACITORS                                                                                 |
| 5,113,373             | A807/1897US               | United States  | 08/06/1990  | 05/12/1992 | POWER CONTROL CIRCUIT                                                                                                           |
| 5,191,556             | A808/1864US               | United States  | 03/13/1991  | 03/02/1993 | METHOD OF PAGE-MODE PROGRAMMING FLASH EEPROM CELL ARRAYS                                                                        |
| 5,477,499             | A846/1941US               | United States  | 10/13/1993  | 12/19/1995 | MEMORY ARCHITECTURE FOR A THREE VOLT FLASH EEPROM                                                                               |
| 5,579,274             | A846US DIV                | United States  | 06/06/1995  | 11/26/1996 | MEMORY ARCHITECTURE FOR THREE VOLT FLASH EPROM                                                                                  |
| 5,291,446             | A887US                    | United States  | 10/22/1992  | 03/01/1994 | VPP POWER SUPPLY                                                                                                                |
| 5,263,000             | A888/1987US               | United States  | 10/22/1992  | 11/16/1993 | DRAIN POWER SUPPLY                                                                                                              |
| 5,282,170             | A889/1988US               | United States  | 10/22/1992  | 01/25/1994 | NEGATIVE POWER SUPPLY                                                                                                           |
| 5,376,835             | A890/1989US               | United States  | 10/22/1992  | 12/27/1994 | POWER-ON-RESET                                                                                                                  |
| 5,335,198             | A891/1990US               | United States  | 05/06/1993  | 08/02/1994 | FLASH EEPROM ARRAY WITH HIGH ENDURANCE                                                                                          |
| 5,367,206             | A900/1996US               | United States  | 06/17/1993  | 11/22/1994 | OUTPUT BUFFER CIRCUIT FOR LOW VOLTAGE EPROM                                                                                     |
| 5,357,458             | A901/1997US               | United States  | 06/25/1993  | 10/18/1994 | A SYSTEM FOR ALLOWING A CONTENT ADDRESSABLE MEMORY TO OPERATE WITH MULTIPLE POWER VOLTAGE LEVELS                                |
| 5,406,517             | A927/2024US               | United States  | 08/23/1993  | 04/11/1995 | DISTRIBUTED NEGATIVE GATE POWER SUPPLY                                                                                          |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                             |
|-----------------------|--------------------------|---------------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------|
| 5,365,484             | A928/2025US              | United States | 08/23/1993  | 11/15/1994 | INDEPENDENT ARRAY GROUNDS FOR FLASH EEPROM WITH PAGED<br>ERASE ARCHITECTURE                                                                       |
| 5,349,558             | A931/2028US              | United States | 08/26/1993  | 09/20/1994 | SECTOR-BASED REDUNDANCY ARCHITECTURE                                                                                                              |
| 5,828,601             | A938/2033US              | United States | 12/01/1993  | 10/27/1998 | PROGRAMMED REFERENCE                                                                                                                              |
| 5,511,026             | A939/2034US              | United States | 12/01/1993  | 04/23/1996 | BOOSTED AND REGULATED GATE POWER SUPPLY WITH<br>REFERENCE TRACKING FOR MULTI-DENSITY AND LOW VOLTAGE<br>SUPPLY MEMORIES                           |
| 08/914,871            | A956CIP-D2               | United States | 08/20/1997  |            | METHOD PROTECTING A STACKED GATE EDGE IN A<br>SEMICONDUCTOR DEVICE FROM SELF ALIGNED SOURCE (SAS) ETCH                                            |
| 08/500,422            | A956CIP-DIV              | United States | 07/11/1995  |            | METHOD PROTECTING A STACKED GATE EDGE IN A<br>SEMICONDUCTOR DEVICE FROM SELF ALIGNED SOURCE (SAS) ETCH                                            |
| 5,470,773             | A956US                   | United States | 04/25/1994  | 11/28/1995 | METHOD PROTECTING A STACKED GATE EDGE IN A<br>SEMICONDUCTOR DEVICE FROM SELF AKIGNED SOURCE (SAS) ETCH                                            |
| 5,534,455             | A956US CIP               | United States | 05/02/1995  | 07/09/1996 | METHOD PROTECTING A STACKED GATE EDGE IN A<br>SEMICONDUCTOR DEVICE FROM SELF ALIGNED SOURCE (SAS) ETCH                                            |
| 5,693,972             | A956US CIP DIV           | United States | 12/18/1996  | 12/02/1997 | METHOD PROTECTING A STACKED GATE EDGE IN A<br>SEMICONDUCTOR DEVICE FROM SELF ALIGNED SOURCE (SAS) ETCH                                            |
| 5,517,443             | A956US DIV               | United States | 06/01/1995  | 05/14/1996 | METHOD & SYSTEM FOR PROTECTING A STACKED GATE EDGE IN A<br>SEMICONDUCTOR DEVICE FROM SELF ALIGNED SOURCE (SAS) ETCH<br>IN A SEMI-CONDUCTOR DEVICE |
| 5,955,874             | A957/2052US              | United States | 06/23/1994  | 09/21/1999 | SUPPLY VOLTAGE-INDEPENDENT REFERENCE VOLTAGE CIRCUIT                                                                                              |
| 08/267,726            | A959/2050                | United States | 06/28/1994  |            | FLASH EEPROM ARRAY WITH FLOATING SUBSTRATE ERASE<br>OPERATION                                                                                     |
| 5,561,620             | A959US CON               | United States | 07/31/1995  | 10/01/1996 | FLASH EEPROM ARRAY WITH FLOATING SUBSTRATE ERASE<br>OPERATION                                                                                     |
| 5,598,369             | A959US DIV               | United States | 06/07/1995  | 01/28/1997 | FLASH EEPROM ARRAY WITH FLOATING SUBSTRATE ERASE<br>OPERATION                                                                                     |
| 5,530,803             | A960/2054US              | United States | 04/14/1994  | 06/25/1996 | MEMORY DEVICES AND METHOD FOR CONTROLLING THE<br>PROGRAMMING OF SUCH MEMORY DEVICE                                                                |
| 5,576,991             | A975/2066US              | United States | 07/01/1994  | 11/19/1996 | MULTISTEPED TRESHOLD CONVERGENCE FOR A FLASH MEMORY<br>ARRAY                                                                                      |
| 5,541,875             | A976/2067US              | United States | 07/01/1994  | 07/30/1996 | HIGH ENERGY BURIED LAYER IMPLANT TO PROVIDE A LOW<br>RESISTANCE P-WELL IN A FLASH EPROM ARRAY                                                     |
| 5,457,336             | A998/2089US              | United States | 10/13/1994  | 10/10/1995 | NON-VOLATILE MEMORY STRUCTURE INCLUDING PROTECTION AND<br>STRUCTURE FOR MAINTAINING THRESHOLD STABILITY                                           |
| 6,259,633             | AF01001US                | United States | 10/19/1999  | 07/10/2001 | SENSE AMPLIFIER ARCHITECTURE FOR SLIDING BANKS FOR A<br>SIMULTANEOUS OPERATION FLASH MEMORY                                                       |
| 6,359,808             | AF01002US                | United States | 10/19/1999  | 03/19/2002 | LOW VOLTAGE READ CASCODE FOR 2V/3V AND DIFFERENT BANK<br>COMBINATIONS WITHOUT METAL OPTIONS FOR A SIMULTANEOUS<br>OPERATION FLASH MEMORY DEVICE   |
| 6,327,181             | AF01003US                | United States | 10/19/1999  | 12/04/2001 | REFERENCE CELL BITLINE PATH ARCHITECTURE FOR A<br>SIMULTANEOUS OPERATION FLASH MEMORY DEVICE                                                      |
| 7,072,781             | AF01005US                | United States | 07/06/2004  | 07/04/2006 | ARCHITECTURE FOR GENERATING ADAPTIVE ARBITRARY<br>WAVEFORMS                                                                                       |
| 6,397,313             | AF01006US                | United States | 08/04/2000  | 05/28/2002 | REDUNDANT DUAL BANK ARCHITECTURE FOR A SIMULTANEOUS<br>OPERATION FLASH MEMORY                                                                     |
| 6,550,028             | AF01008US                | United States | 10/19/1999  | 04/15/2003 | ARRAY VT MODE IMPLEMENTATION FOR A SIMULTANEOUS<br>OPERATION FLASH MEMORY DEVICE                                                                  |
| 6,275,421             | AF01009US                | United States | 09/14/2000  | 08/14/2001 | CHIP ENABLE INPUT BUFFER                                                                                                                          |
| 6,463,516             | AF01010US                | United States | 09/18/2000  | 10/08/2002 | VARIABLE SECTOR SIZE FOR A HIGH DENSITY FLASH MEMORY<br>DEVICE                                                                                    |
| 6,285,627             | AF01011US                | United States | 09/18/2000  | 09/04/2001 | ADDRESS TRANSITION DETECTOR (ATD) ARCHITECTURE FOR HIGH<br>DENSITY FLASH MEMORY DEVICE                                                            |
| 6,353,566             | AF01012US                | United States | 09/18/2000  | 03/05/2002 | METHOD FOR TRACKING SENSING SPEED BY AN EQUALIZATION<br>PULSE FOR A HIGH DENSITY FLASH MEMORY DEVICE                                              |
| 6,297,993             | AF01014US                | United States | 11/13/2000  | 10/02/2001 | ACCELERATION VOLTAGE IMPLEMENTATION FOR HIGH DENSITY<br>FLASH MEMORY DEVICE                                                                       |
| 6,327,194             | AF01015US                | United States | 08/23/2000  | 12/04/2001 | PRECISE REFERENCE WORDLINE LOADING COMPENSATION FOR A<br>HIGH DENSITY FLASH MEMORY DEVICE                                                         |
| 6,125,055             | AF01016US                | United States | 10/19/1999  | 09/26/2000 | SECTOR WRITE PROTECT CAMS FOR A SIMULTANEOUS OPERATION<br>FLASH MEMORY                                                                            |
| 6,662,262             | AF01016US CIP            | United States | 10/19/1999  | 12/09/2003 | OTP SECTOR DOUBLE PROTECTION FOR A SIMULTANEOUS<br>OPERATION FLASH MEMORY                                                                         |
| 6,571,307             | AF01018US                | United States | 10/19/1999  | 05/27/2003 | MULTIPLE PURPOSE BUS FOR A SIMULTANEOUS OPERATION FLASH<br>MEMORY DEVICE                                                                          |
| 6,331,950             | AF01019US                | United States | 10/19/1999  | 12/18/2001 | WRITE PROTECT INPUT IMPLEMENTATION FOR A SIMULTANEOUS<br>OPERATION FLASH MEMORY DEVICE                                                            |
| 6,125,058             | AF01020US                | United States | 10/19/1999  | 09/26/2000 | SYSTEM FOR OPTIMIZING THE EQUALIZATION PULSE OF A READ<br>SENSE SMPLIFIER FOR A SIMULTANEOUS OPERATION FLASH<br>MEMORY DEVICE                     |
| 6,201,753             | AF01023US                | United States | 10/19/1999  | 03/13/2001 | LATCH CAM DATA IN A FLASH MEMORY DEVICE                                                                                                           |
| 6,185,128             | AF01024US                | United States | 10/19/1999  | 02/06/2001 | REFERENCE CELL FOUR-WAY SWITCH FOR A SIMULTANEOUS<br>OPERATION FLASH MEMORY DEVICE                                                                |
| 6,111,787             | AF01025US                | United States | 10/19/1999  | 08/29/2000 | ADDRESS TRANSITION DETECT TIMING ARCHITECTURE FOR A<br>SIMULTANEOUS OPERATION FLASH MEMORY DEVICE                                                 |
| 6,208,556             | AF01025US CON1           | United States | 04/12/2000  | 03/27/2001 | ADDRESS TRANSITION DETECT TIMING ARCHITECTURE FOR A<br>SIMULTANEOUS OPERATION FLASH MEMORY DEVICE                                                 |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                    |
|-----------------------|---------------------------|---------------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------|
| 6,285,585             | AF01026US                 | United States | 10/19/1999  | 09/04/2001 | OUTPUT SWITCHING IMPLEMENTATION FOR A FLASH MEMORY DEVICE                                                                |
| 6,118,698             | AF01027US                 | United States | 10/19/1999  | 09/12/2000 | OUTPUT MULTIPLEXING IMPLEMENTATION FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE                                      |
| 6,266,284             | AF01028US                 | United States | 09/14/2000  | 07/24/2001 | OUTPUT BUFFER FOR VCC2                                                                                                   |
| 6,310,805             | AF01029US                 | United States | 10/02/2000  | 10/30/2001 | ARCHITECTURE FOR A DUAL-BANK PAGE MODE MEMORY WITH REDUNDANCY                                                            |
| 6,298,007             | AF01030US                 | United States | 08/31/2000  | 10/02/2001 | METHOD AND APPARATUS FOR ELIMINATING FALSE DATA IN A PAGE MODE MEMORY DEVICE                                             |
| 6,324,108             | AF01032US                 | United States | 09/22/2000  | 11/27/2001 | APPLICATION OF EXTERNAL VOLTAGE DURING ARRAY VT TESTING                                                                  |
| 6,438,041             | AF01033US                 | United States | 09/22/2000  | 08/20/2002 | NEGATIVE VOLTAGE REGULATION                                                                                              |
| 6,400,638             | AF01036US                 | United States | 10/05/2000  | 06/04/2002 | WORDLINE DRIVER FOR FLASH MEMORY READ MODE                                                                               |
| 6,622,230             | AF01041US                 | United States | 11/28/2000  | 09/16/2003 | MULTI-SET BLOCK ERASE                                                                                                    |
| 6,201,737             | AF01042US                 | United States | 04/26/2000  | 03/13/2001 | APPARATUS AND METHOD TO CHARACTERIZE THE THRESHOLD DISTRIBUTION IN AN NROM VIRTUAL GROUND ARRAY                          |
| 6,373,742             | AF01043US                 | United States | 10/12/2000  | 04/16/2002 | TWO SIDE DECODING OF A MEMORY ARRAY                                                                                      |
| 6,813,735             | AF01045US                 | United States | 10/02/2000  | 11/02/2004 | I/O BASED COLUMN REDUNDANCY FOR VIRTUAL GROUND WITH 2-BIT CELL FLASH MEMORY                                              |
| 6,750,103             | AF01047US                 | United States | 02/27/2002  | 06/15/2004 | NROM CELL WITH N-LESS CHANNEL                                                                                            |
| 6,583,479             | AF01050US                 | United States | 10/16/2000  | 06/24/2003 | SIDEWALL NROM AND METHOD OF MANUFACTURE THEREOF FOR NON-VOLATILE MEMORY CELLS                                            |
| 6,218,227             | AF01052US                 | United States | 10/25/1999  | 04/17/2001 | A METHOD TO GENERATE A MONOS TYPE FLASH CELL USING POLYCRYSTALLINE SILICON AS AN ONO TOP LAYER                           |
| 6,265,268             | AF01054US                 | United States | 10/25/1999  | 07/24/2001 | HIGH TEMPERATURE OXIDE DEPOSITION PROCESS FOR FABRICATING AN ONO FLOATING-GATE ELECTRODE IN A TWO BIT EEPROM DEVICE      |
| 6,248,628             | AF01055US                 | United States | 10/25/1999  | 06/19/2001 | METHOD FOR FABRICATING AN ONO DIELECTRIC BY NITRIDATION FOR MNOS MEMORY CELLS                                            |
| 6,248,635             | AF01056US                 | United States | 10/25/1999  | 06/19/2001 | PROCESS FOR FABRICATING A BIT-LINE IN MONOS DEVICE USING A DUAL LAYER HARD MASK                                          |
| 6,528,390             | AF01057US                 | United States | 03/02/2001  | 03/04/2003 | PROCESS FOR FABRICATING A NON-VOLATILE MEMORY DEVICE                                                                     |
| 6,117,730             | AF01058US                 | United States | 10/25/1999  | 09/12/2000 | INTEGRATED METHOD BY USING HTO FOR TOP OXIDE AND PERIPHERY GATE OXIDE                                                    |
| 6,242,305             | AF01059US                 | United States | 10/25/1999  | 06/05/2001 | PROCESS FOR FABRICATING A BIT-LINE USING BURIED DIFFUSION ISOLATION                                                      |
| 60/227,118            | AF01060US PROV            | United States | 08/22/2000  |            | METHOD OF FORMING ZERO MARKS                                                                                             |
| 6,573,140             | AF01063US                 | United States | 03/16/2001  | 06/03/2003 | PROCESS FOR MAKING A DUAL BIT MEMORY DEVICE WITH ISOLATED POLYSILICON FLOATING GATES                                     |
| 60/228,711            | AF01063US PROV            | United States | 08/29/2000  |            | PROCESS FOR MAKING A DUAL BIT MEMORY DEVICE WITH ISOLATED POLYSILICON FLOATING GATES                                     |
| 6,479,411             | AF01064US                 | United States | 03/21/2000  | 11/12/2002 | METHOD FOR FORMING HIGH QUALITY MULTIPLE THICKNESS OXIDE USING HIGH TEMPERATURE DESCUM                                   |
| 6,432,618             | AF01065US                 | United States | 03/23/2000  | 08/13/2002 | METHOD FOR FORMING HIGH QUALITY MULTIPLE THICKNESS OXIDE LAYERS BY REDUCING DESCUM INDUCED DEFECTS                       |
| 6,461,973             | AF01066US                 | United States | 03/23/2000  | 10/08/2002 | METHOD FOR FORMING HIGH QUALITY MULTIPLE THICKNESS OXIDE LAYERS BY REDUCING DESCUM INDUCED DEFECTS                       |
| 6,713,809             | AF01067US                 | United States | 03/16/2001  | 03/30/2004 | DUAL BIT MEMORY DEVICE WITH ISOLATED POLYSILICON FLOATING GATES                                                          |
| 60/228,712            | AF01067US PROV            | United States | 08/29/2000  |            | DUAL BIT MEMORY DEVICE WITH ISOLATED POLYSILICON FLOATING GATES                                                          |
| 6,537,866             | AF01068US                 | United States | 10/18/2000  | 03/25/2003 | METHOD OF FORMING NARROW INSULATING SPACERS FOR USE IN REDUCING MINIMUM COMPONENT SIZE                                   |
| 6,243,316             | AF01071US                 | United States | 02/09/2000  | 06/05/2001 | IMPROVED VOLTAGE BOOST RESET CIRCUIT FOR A FLASH MEMORY                                                                  |
| 6,351,420             | AF01072US                 | United States | 06/16/2000  | 02/26/2002 | VOLTAGE BOOST LEVEL CLAMPING CIRCUIT FOR A FLASH MEMORY                                                                  |
| 6,347,052             | AF01073US                 | United States | 10/17/2000  | 02/12/2002 | WORD LINE DECODING ARCHITECTURE IN A FLASH MEMORY                                                                        |
| 6,463,003             | AF01074US                 | United States | 12/04/2000  | 10/08/2002 | POWER SAVING SCHEME FOR BURST MODE IMPLEMENTATION DURING READING OF DATA FROM A MEMORY DEVICE                            |
| 60/210,134            | AF01074US PROV            | United States | 06/07/2000  |            | POWER SAVING SCHEME FOR BURST MODE IMPLEMENTATION DURING READING OF DATA FROM A MEMORY DEVICE                            |
| 6,240,040             | AF01075US                 | United States | 03/15/2000  | 05/29/2001 | MULTIPLE BANK SIMULTANEOUS OPERATION FOR A FLASH MEMORY                                                                  |
| 6,621,761             | AF01076US                 | United States | 04/09/2001  | 09/16/2003 | BURST ARCHITECTURE FOR A FLASH MEMORY                                                                                    |
| 60/208,652            | AF01076US PROV            | United States | 05/21/2000  |            | BURST ARCHITECTURE FOR A FLASH MEMORY                                                                                    |
| 09/693,809            | AF01077US                 | United States | 10/20/2000  |            | COMMAND-DRIVEN TEST MODES                                                                                                |
| 6,307,787             | AF01078US                 | United States | 11/28/2000  | 10/23/2001 | BURST READ INCORPORATING OUTPUT BASED REDUNDANCY                                                                         |
| 09/741,320            | AF01079US                 | United States | 12/19/2000  |            | INITIAL LATENCY CHECKING FOR BURST MODE READ IN A BURST MODE MEMORY DEVICE                                               |
| 6,507,527             | AF01080US                 | United States | 10/27/2000  | 01/14/2003 | MEMORY LINE DISCHARGE BEFORE SENSING                                                                                     |
| 6,229,735             | AF01081US                 | United States | 07/30/2001  |            | BURST READ WORDLINE BOOSTING                                                                                             |
| 6,400,633             | AF01083US                 | United States | 09/29/2000  | 06/04/2002 | POWER-SAVING MODES FOR MEMORIES                                                                                          |
| 6,611,473             | AF01083US DIV             | United States | 02/01/2002  | 08/26/2003 | POWER-SAVING MODES FOR MEMORIES                                                                                          |
| 10/100,877            | AF01083US DIV2            | United States | 03/18/2002  |            | POWER-SAVING MODES FOR MEMORIES                                                                                          |
| 6,212,108             | AF01084US                 | United States | 01/24/2000  | 04/03/2001 | DISTRIBUTED VOLTAGE CHARGE CIRCUITS TO REDUCE SENSING TIME IN A MEMORY DEVICE                                            |
| 6,208,561             | AF01085US                 | United States | 06/13/2000  | 03/27/2001 | METHOD TO REDUCE CAPACITIVE LOADING IN FLASH MEMORY X-DECODER FOR ACCURATE VOLTAGE CONTROL AT WORDLINES AND SELECT LINES |
| 6,163,481             | AF01086US                 | United States | 10/29/1999  | 12/19/2000 | WORD LINE TRACKING IN WHOLE CHIP                                                                                         |
| 6,417,082             | AF01087US                 | United States | 08/30/2000  | 07/09/2002 | SEMICONDUCTOR STRUCTURE                                                                                                  |
| 6,429,479             | AF01088US                 | United States | 03/09/2000  | 08/06/2002 | NAND FLASH MEMORY WITH SPECIFIED GATE OXIDE THICKNESS                                                                    |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                  |
|-----------------------|--------------------------|---------------|-------------|------------|------------------------------------------------------------------------------------------------------------------------|
| 6,385,093             | AF01090US                | United States | 03/30/2001  | 05/07/2002 | I/O PARTITIONING AND METHODOLOGY TO REDUCE BAND-TO-BAND TUNNELING CURRENT DURING ERASE                                 |
| 6,510,082             | AF01091US                | United States | 10/23/2001  | 01/21/2003 | DRAIN SIDE SENSING SCHEME FOR VIRTUAL GROUND FLASH EPROM ARRAY WITH ADJACENT BIT CHARGE AND HOLD                       |
| 6,525,969             | AF01092US                | United States | 08/10/2001  | 02/25/2003 | DECODER APPARATUS AND METHODS FOR PRE-CHARGING BIT LINES                                                               |
| 6,381,163             | AF01093US                | United States | 06/04/2001  | 04/30/2002 | METHODS AND APPARATUS FOR READING A CAM CELL USING BOOSTED AND REGULATED GATE VOLTAGE                                  |
| 6,535,424             | AF01094US                | United States | 07/25/2001  | 03/18/2003 | VOLTAGE BOOST CIRCUIT USING SUPPLY VOLTAGE DETECTION TO COMPENSATE FOR SUPPLY VOLTAGE VARIATIONS IN READ MODE VOLTAGES |
| 6,493,266             | AF01096US                | United States | 04/09/2001  | 12/10/2002 | SOFT PROGRAM AND SOFT PROGRAM VERIFY OF THE CORE CELLS IN FLASH MEMORY ARRAY                                           |
| 6,370,061             | AF01098US                | United States | 06/19/2001  | 04/09/2002 | CEILING TEST MODE TO CHARACTERIZE THE THRESHOLD VOLTAGE DISTRIBUTION OF OVER PROGRAMMED MEMORY CELLS                   |
| 6,445,030             | AF01099US                | United States | 01/30/2001  | 09/03/2002 | FLASH MEMORY ERASE SPEED BY FLUORINE IMPLANT OR FLUORINATION                                                           |
| 6,707,078             | AF01101US                | United States | 08/29/2002  | 03/16/2004 | DUMMY WORDLINE FOR ERASE AND BITLINE LEAKAGE                                                                           |
| 6,465,306             | AF01102US                | United States | 11/28/2000  | 10/15/2002 | SIMULTANEOUS FORMATION OF CHARGE STORAGE AND BITLINE TO WORDLINE ISOLATION                                             |
| 6,555,436             | AF01102US DIV1           | United States | 08/19/2002  | 04/29/2003 | SIMULTANEOUS FORMATION OF CHARGE STORAGE AND BITLINE TO WORDLINE ISOLATION                                             |
| 6,468,865             | AF01105US                | United States | 11/28/2000  | 10/22/2002 | METHOD OF SIMULTANEOUS FORMATION OF BITLINE ISOLATION AND PERIPHERY OXIDE                                              |
| 6,730,564             | AF01107US                | United States | 08/12/2002  | 05/04/2004 | SALICIDED GATE FOR VIRTUAL GROUND ARRAYS                                                                               |
| 6,362,051             | AF01110US                | United States | 08/25/2000  | 03/26/2002 | METHOD OF FORMING ONO FLASH MEMORY DEVICES USING LOW ENERGY NITROGEN IMPLANTATION                                      |
| 6,395,654             | AF01111US                | United States | 08/25/2000  | 05/28/2002 | METHOD OF FORMING ONO FLASH MEMORY DEVICES USING RAPID THERMAL OXIDATION                                               |
| 6,541,816             | AF01112US                | United States | 06/27/2001  | 04/01/2003 | PLANAR STRUCTURE FOR NON-VOLITALE MEMORY DEVICES                                                                       |
| 60/372,361            | AF01116                  | United States | 04/12/2002  |            | METHOD FOR MULTI-BIT FLASH READS USING DUAL DYNAMIC REFERENCES                                                         |
| 6,799,256             | AF01116US                | United States | 05/01/2002  | 09/28/2004 | SYSTEM AND METHOD FOR MULTI-BIT FLASH READS USING DUAL DYNAMIC REFERENCES                                              |
| 7,103,706             | AF01116US CON            | United States | 09/03/2004  | 09/05/2006 | SYSTEM AND METHOD FOR MULTI-BIT FLASH READS USING DUAL DYNAMIC REFERENCES                                              |
| 10/223,775            | AF01118US                | United States | 08/19/2002  |            | HIGH-K SEMICONDUCTOR DEVICE HAVING A P-TYPE POLYSILICON GATE TO INCREASE BARRIER HEIGHT FOR ELECTRON TUNNELING         |
| 10/023,548            | AF01120US                | United States | 12/17/2001  |            | INTEGRATED ONO PROCESSING FOR SEMICONDUCTOR DEVICES USING IN-SITU STEAM GENERATION (ISSG) PROCESS                      |
| 7,115,469             | AF01120US DIV            | United States | 01/08/2004  | 10/03/2006 | INTEGRATED ONO PROCESSING FOR SEMICONDUCTOR DEVICES USING IN-SITU STEAM GENERATION (ISSG) PROCESS                      |
| 10/298,667            | AF01122                  | United States | 11/19/2002  |            | A BURIED SILICIDE LOCAL INTERCONNECT AND METHOD FOR MAKING THE SAME                                                    |
| 6,828,199             | AF01124US                | United States | 12/20/2001  | 12/07/2004 | MONOS DEVICE HAVING BURIED METAL SILICIDE BIT LINE                                                                     |
| 7,786,003             | AF01125US                | United States | 05/25/2005  | 08/31/2010 | A BURIED SILICIDE LOCAL INTERCONNECT WITH SIDEWALL SPACERS AND METHOD FOR MAKING THE SAME                              |
| 8,049,334             | AF01125US DIV            | United States | 07/26/2010  | 11/01/2011 | BURIED SILICIDE LOCAL INTERCONNECT WITH SIDEWALL SPACERS AND METHOD FOR MAKING THE SAME                                |
| 8,368,219             | AF01125US DIV CON        | United States | 10/26/2011  | 02/05/2013 | BURIED SILICIDE LOCAL INTERCONNECT WITH SIDEWALL SPACERS AND METHOD FOR MAKING THE SAME                                |
| 10/165,836            | AF01129                  | United States | 06/06/2002  |            | METHOD AND SYSTEM FOR PROVIDING SOURCE CONNECTIONS USING POLYSILICON FOR NONVOLATILE MEMORY CELLS                      |
| 6,808,992             | AF01131US                | United States | 05/15/2002  | 10/26/2004 | METHOD AND SYSTEM FOR TAILORING CORE AND PERIPHERY CELLS IN A NONVOLATILE MEMORY                                       |
| 6,706,595             | AF01132US                | United States | 03/14/2002  | 03/16/2004 | HARD MASK PROCESS FOR MEMORY DEVICE WITHOUT BITLINE SHORTS                                                             |
| 6,617,215             | AF01133US                | United States | 03/27/2002  | 09/09/2003 | MEMORY WORDLINE HARD MASK                                                                                              |
| 6,479,348             | AF01134US                | United States | 03/27/2002  | 11/12/2002 | METHOD OF MAKING MEMORY WORDLINE HARD MASK EXTENSION                                                                   |
| 6,720,133             | AF01135US                | United States | 04/19/2002  | 04/13/2004 | MEMORY MANUFACTURING PROCESS USING DISPOSABLE ARC FOR WORDLINE FORMATION                                               |
| 10/109,527            | AF01136                  | United States | 03/27/2002  |            | SEMICONDUCTOR MEMORY WITH DATA RETENTION LINER                                                                         |
| 7,297,592             | AF01136US CIP            | United States | 08/01/2005  | 11/20/2007 | SEMICONDUCTOR MEMORY WITH DATA RETENTION LINER                                                                         |
| 8,673,716             | AF01137US                | United States | 04/08/2002  | 03/18/2014 | MEMORY MANUFACTURING PROCESS WITH BITLINE ISOLATION                                                                    |
| 7,074,677             | AF01138US                | United States | 11/29/2002  | 07/11/2006 | MEMORY WITH IMPROVED CHARGE-TRAPPING DIELECTRIC LAYER                                                                  |
| 6,670,241             | AF01139US                | United States | 04/22/2002  | 12/30/2003 | SEMICONDUCTOR MEMORY WITH DEUTERATED MATERIALS                                                                         |
| 6,884,681             | AF01139US DIV            | United States | 09/26/2003  | 04/26/2005 | METHOD OF MANUFACTURING SEMICONDUCTOR MEMORY WITH DEUTERATED MATERIALS                                                 |
| 6,803,265             | AF01140US                | United States | 03/27/2002  | 10/12/2004 | LINER FOR SEMICONDUCTOR MEMORIES AND MANUFACTURING METHODS THEREFOR                                                    |
| 6,653,191             | AF01141US                | United States | 05/16/2002  | 11/25/2003 | MEMORY MANUFACTURING PROCESS USING BITLINE RAPID THERMAL ANNEAL                                                        |
| 6,791,880             | AF01154US                | United States | 05/06/2003  | 09/14/2004 | NON-VOLATILE MEMORY READ CIRCUIT WITH END OF LIFE SIMULATION                                                           |
| 6,566,736             | AF01157US                | United States | 11/30/2001  | 05/20/2003 | DIE SEAL SEMICONDUCTOR DEVICE MOISTURE PROTECTION                                                                      |
| 7,265,014             | AF01158US                | United States | 03/12/2004  | 09/04/2007 | AVOIDING FIELD OXIDE GOUGING IN SHALLOW TRENCH ISOLATION (STI) REGIONS                                                 |
| 11/781,551            | AF01158US DIV            | United States | 07/23/2007  |            | DEVICE HAVING A PROTECTIVE CAP FORMED OVER AN ANTI-REFLECTIVE COATING LAYER AND OVER AN INSULATING MATERIAL            |
| 6,809,033             | AF01159US                | United States | 11/07/2001  | 10/26/2004 | INNOVATIVE METHOD OF HARD MASK REMOVAL                                                                                 |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                                                                                       |
|-----------------------|---------------------------|---------------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6,642,148             | AF01162US                 | United States | 04/19/2002  | 11/04/2003 | RELACS SHRINK METHOD APPLIED FOR SINGLE PRINT RESIST MASK FOR LLD OR BURIED BITLINE IMPLANTS USNG CHEMICALLY AMPLIFIED DUV TYPE PHOTORESIST                                                                                                 |
| 6,744,666             | AF01164US                 | United States | 09/12/2002  | 06/01/2004 | METHOD AND SYSTEM TO MINIMIZE PAGE PROGRAMMING TIME FOR FLASH MEMORY DEVICES                                                                                                                                                                |
| 7,142,454             | AF01165US                 | United States | 09/12/2002  | 11/28/2006 | SYSTEM AND METHOD FOR Y-DECODEING IN A FLASH MEMORY DEVICE                                                                                                                                                                                  |
| 6,859,393             | AF01166US                 | United States | 10/04/2002  | 02/22/2005 | GROUND STRUCTURE FOR PAGE READ AND PAGE WRITE FOR FLASH MEMORY                                                                                                                                                                              |
| 6,728,160             | AF01167US                 | United States | 09/12/2002  | 04/27/2004 | PATH GATE DRIVER CIRCUIT                                                                                                                                                                                                                    |
| 6,944,057             | AF01168US                 | United States | 05/06/2003  | 09/13/2005 | METHOD TO OBTAIN TEMPERATURE INDEPENDENT PROGRAM THRESHOLD VOLTAGE DISTRIBUTION USING TEMPERATURE DEPENDENT VOLTAGE REFERENCE                                                                                                               |
| 7,324,374             | AF01169US                 | United States | 06/20/2003  | 01/29/2008 | MEMORY WITH A CORE-BASED VIRTUAL GROUND AND DYNAMIC REFERENCE SENSING SCHEME                                                                                                                                                                |
| 7,606,068             | AF01169US                 | United States | 01/22/2008  | 10/20/2009 | MEMORY WITH A CORE-BASED VIRTUAL GROUND AND DYNAMIC REFERENCE SENSING SCHEME                                                                                                                                                                |
| 6,754,105             | AF01170US                 | United States | 05/06/2003  | 06/22/2004 | TRENCH SIDE WALL CHARGE TRAPPING DIELECTRIC FLASH MEMORY DEVICE                                                                                                                                                                             |
| 6,974,995             | AF01171US                 | United States | 12/27/2001  | 12/13/2005 | METHOD AND SYSTEM FOR FORMING DUAL GATE STRUCTURES IN A NONVOLATILE MEMORY USING A PROTECTIVE LAYER                                                                                                                                         |
| 10/032,755            | AF01172                   | United States | 12/27/2001  |            | METHOD AND SYSTEM FOR PERFORMING A REVERSE SELF-ALIGNED SOURCE ETCH USING NITRIDE SPACERS                                                                                                                                                   |
| 6,936,515             | AF01174US                 | United States | 03/12/2003  | 08/30/2005 | MEMORY DEVICE HAVING REVERSE LDD METHOD                                                                                                                                                                                                     |
| 7,163,860             | AF01181US                 | United States | 05/06/2003  | 01/16/2007 | METHOD OF FORMATION OF GATE STACK SPACER AND CHARGE STORAGE MATERIALS HAVING REDUCED HYDROGEN CONTENT IN CHARGE TRAPPING DIELECTRIC FLASH MEMORY DEVICE                                                                                     |
| 6,912,163             | AF01182US CIP             | United States | 09/09/2003  | 06/28/2005 | MEMORY DEVICE HAVING HIGH WORK FUNCTION GATE AND METHOD OF ERASING SAME                                                                                                                                                                     |
| 6,794,764             | AF01186US                 | United States | 03/05/2003  | 09/21/2004 | CHARGE-TRAPPING MEMORY ARRAYS RESISTANT TO DAMAGE FROM CONTACT HOLE FORMATION                                                                                                                                                               |
| 6,667,212             | AF01187US                 | United States | 03/21/2003  | 12/23/2003 | ALIGNMENT SYSTEM FOR PLANAR CHARGE TRAPPING DIELECTRIC MEMORY CELL LITHOGRAPHY                                                                                                                                                              |
| 7,033,957             | AF01188US                 | United States | 02/05/2003  | 04/25/2006 | ONO FABRICATION PROCESS FOR INCREASING OXYGEN CONTENT AT BOTTOM OXIDE-SUBSTRATE INTERFACE IN FLASH MEMORY DEVICES                                                                                                                           |
| 6,803,275             | AF01189US                 | United States | 12/03/2002  | 10/12/2004 | ONO FABRICATION PROCESS FOR REDUCING OXYGEN VACANCY CONTENT IN BOTTOM OXIDE LAYER IN FLASH MEMORY DEVICES                                                                                                                                   |
| 6,969,886             | AF01189US DIV             | United States | 07/12/2004  | 11/29/2005 | ONO FABRICATION PROCESS FOR REDUCING OXYGEN VACANCY CONTENT IN BOTTOM OXIDE LAYER IN FLASH MEMORY DEVICES                                                                                                                                   |
| 6,958,511             | AF01191US                 | United States | 10/06/2003  | 10/25/2005 | FLASH MEMORY DEVICE AND METHOD OF FABRICATION THEREOF                                                                                                                                                                                       |
| 6,949,481             | AF01194US                 | United States | 12/09/2003  | 09/27/2005 | IMPROVED PROCESS FOR FABRICATION OF SPACER LAYER WITH REDUCED HYDROGEN CONTENT IN SEMICONDUCTOR DEVICE                                                                                                                                      |
| 6,955,965             | AF01196US                 | United States | 12/09/2003  | 10/18/2005 | PROCESS FOR FABRICATION OF NITRIDE LAYER WITH REDUCED HYDROGEN CONTENT IN ONO STRUCTURE IN SEMICONDUCTOR DEVICE                                                                                                                             |
| 10/430,601            | AF01197US                 | United States | 05/06/2003  |            | PROCESS FOR REDUCING HYDROGEN CONTENT IN ETCH STOP LAYER INFLASH MEMORY DEVICES                                                                                                                                                             |
| 11/532,917            | AF01197US DIV             | United States | 09/19/2006  |            | PROCESS FOR REDUCING HYDROGEN CONTENT IN ETCH STOP LAYER INFLASH MEMORY DEVICES                                                                                                                                                             |
| 6,949,433             | AF01200US                 | United States | 02/07/2003  | 09/27/2005 | METHOD OF FORMATION OF SEMICONDUCTOR RESISTANT TO HOT CARRIER INJECTION STRESS                                                                                                                                                              |
| 6,740,605             | AF01201US                 | United States | 05/05/2003  | 05/25/2004 | PROCESS FOR REDUCING HYDROGEN CONTAMINATION DIELECTRIC MATERIALS IN MEMORY DEVICES                                                                                                                                                          |
| 6,819,591             | AF01202US                 | United States | 01/20/2004  | 11/16/2004 | METHOD FOR ERASING A MEMORY SECTOR IN VIRTUAL GROUND ARCHITECTURE WITH REDUCED LEAKAGE CURRENT                                                                                                                                              |
| 6,765,254             | AF01203US                 | United States | 06/12/2003  | 07/20/2004 | STRUCTURE AND METHOD FOR PREVENTING UV RADIATION DAMAGE AND INCREASING DATA RETENTION IN MEMORY CELLS                                                                                                                                       |
| 6,833,581             | AF01204US                 | United States | 06/12/2003  | 12/21/2004 | STRUCTURE AND METHOD FOR PREVENTING PROCESS-INDUCED UV RADIATION DAMAGE IN A MEMORY CELL                                                                                                                                                    |
| 6,894,342             | AF01207US                 | United States | 06/12/2003  | 05/17/2005 | STRUCTURE AND METHOD FOR PREVENTING UV RADIATION DAMAGE IN A MEMORY CELL AND IMPROVING CONTACT CD CONTROL                                                                                                                                   |
| 6,773,990             | AF01209US                 | United States | 05/03/2003  | 08/10/2004 | METHOD FOR REDUCING SHORT CHANNEL EFFECTS IN MEMORY CELLS AND RELATED STRUCTURE                                                                                                                                                             |
| 6,963,106             | AF01209US DIV             | United States | 05/04/2004  | 11/08/2005 | METHOD FOR REDUCING SHORT CHANNEL EFFECTS IN MEMORY CELLS AND RELATED STRUCTURE                                                                                                                                                             |
| 7,019,366             | AF01210US                 | United States | 01/14/2004  | 03/28/2006 | ELECTROSTATIC DISCHARGE PERFORMANCE OF A SILICON STRUCTURE AND EFFICIENT USE OF AREA WITH ELECTROSTATIC DISCHARGE PROTECTIVE DEVICE UNDER THE PAD APPROACH AND ADJUSTMENT OF VIA CONFIGURATION THERETO TO CONTROL DRAIN JUNCTION RESISTANCE |
| 10/823,971            | AF01211                   | United States | 04/13/2004  |            | SEMICONDUCTOR DEVICE HAVING A PAD METAL LAYER AND A LOWER METAL LAYER THAT ARE ELECTRICALLY COUPLED WITH VIAS FORMED BELOW A PERIMETER AREA OF THE PAD METAL LAYER                                                                          |
| 7,423,312             | AF01212US                 | United States | 07/20/2004  | 09/09/2008 | APPARATUS AND METHOD FOR A MEMORY ARRAY WITH SHALLOW TRENCH ISOLATION REGIONS BETWEEN BIT LINES FOR INCREASED PROCESS MARGINS                                                                                                               |
| 8,507,971             | AF01212US DIV             | United States | 08/06/2008  | 08/13/2013 | APPARATUS AND METHOD FOR A MEMORY ARRAY WITH SHALLOW TRENCH ISOLATION REGIONS BETWEEN BIT LINES FOR INCREASED PROCESS MARGINS                                                                                                               |
| 7,092,297             | AF01213US                 | United States | 07/26/2004  | 08/15/2006 | METHOD FOR PULSE ERASE IN DUAL BIT MEMORY DEVICES                                                                                                                                                                                           |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                                                 |
|-----------------------|--------------------------|---------------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10/758,148            | AF01214US                | United States | 01/14/2004  |            | EFFICIENT USE OF WAFER AREA WITH DEVICE UNDER THE PAD APPROACH                                                                                                                                        |
| 7,632,749             | AF01215US                | United States | 04/13/2004  | 12/15/2009 | SEMICONDUCTOR DEVICE HAVING A PAD METAL LAYER AND A LOWER METAL LAYER THAT ARE ELECTRICALLY COUPLED, WHEREAS APERTURES ARE FORMED IN THE LOWER METAL LAYER BELOW A CENTER AREA OF THE PAD METAL LAYER |
| 7,026,211             | AF01216US                | United States | 03/08/2004  | 04/11/2006 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE                                                                                                                                                     |
| 7,301,193             | AF01220US                | United States | 01/22/2004  | 11/27/2007 | STRUCTURE AND METHOD FOR LOW VSS RESISTANCE AND REDUCED DIBL IN A FLOATING GATE MEMORY CELL                                                                                                           |
| 7,067,377             | AF01221US                | United States | 03/30/2004  | 06/27/2006 | RECESSED CHANNEL WITH SEPARATED ONO MEMORY DEVICE                                                                                                                                                     |
| 7,394,125             | AF01221US DIV            | United States | 02/24/2006  | 07/01/2008 | RECESSED CHANNEL WITH SEPARATED ONO MEMORY DEVICE                                                                                                                                                     |
| 7,098,546             | AF01222US                | United States | 06/16/2004  | 08/29/2006 | ALIGNMENT MARKS WITH SALICIDED SPACERS BETWEEN BITLINES FOR ALIGNMENT SIGNAL IMPROVEMENT                                                                                                              |
| 10/877,701            | AF01223                  | United States | 06/26/2004  |            | ALIGNMENT MARK ON OXIDE                                                                                                                                                                               |
| 7,157,335             | AF01224US                | United States | 08/13/2004  | 01/02/2007 | USING THIN UNDOPED TEOS WITH BPTEOS ILD OR BPTEOS ILD ALONE TO IMPROVE CHARGE LOSS AND CONTACT RESISTANCE IN MULTI BIT MEMORY DEVICES                                                                 |
| 11/546,688            | AF01224US DIV            | United States | 10/12/2006  |            | USING THIN UNDOPED TEOS WITH BPTEOS ILD OR BPTEOS ILD ALONE TO IMPROVE CHARGE LOSS AND CONTACT RESISTANCE IN MULTI-BIT MEMORY DEVICES                                                                 |
| 7,283,398             | AF01225US                | United States | 05/04/2004  | 10/16/2007 | METHOD FOR MINIMIZING FALSE DETECTION OF STATES IN FLASH MEMORY DEVICES                                                                                                                               |
| 8,896,048             | AF01226US                | United States | 06/04/2004  | 11/25/2014 | APPARATUS AND METHOD FOR SOURCE SIDE IMPLANTATION AFTER SPACER FORMATION TO REDUCE SHORT CHANNEL EFFECTS IN METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS                                        |
| 8,237,210             | AF01227US                | United States | 02/08/2006  | 08/07/2012 | ARRAY TYPE CAM CELL FOR SIMPLIFYING PROCESSES                                                                                                                                                         |
| 7,226,839             | AF01228US                | United States | 06/04/2004  | 06/05/2007 | METHOD AND SYSTEM FOR IMPROVING THE TOPOGRAPHY OF A MEMORY ARRAY                                                                                                                                      |
| 7,151,027             | AF01229US                | United States | 06/01/2004  | 12/19/2006 | METHOD AND DEVICE FOR REDUCING INTERFACE AREA OF A MEMORY DEVICE                                                                                                                                      |
| 10/861,574            | AF01230                  | United States | 06/04/2004  |            | DIELECTRIC STRUCTURE HAVING A HIGH-K DIELECTRIC LAYER FOR A SEMICONDUCTOR DEVICE                                                                                                                      |
| 7,242,102             | AF01232US                | United States | 07/08/2004  | 07/10/2007 | BOND PAD STRUCTURE FOR COPPER METALLIZATION HAVING INCREASED RELIABILITY AND METHOD FOR FABRICATING SAME                                                                                              |
| 10/953,228            | AF01233                  | United States | 09/29/2004  |            | A METHOD OF IMPROVING LINE-TO-LINE BREAKDOWN VOLTAGES IN Cu INTERCONNECTS                                                                                                                             |
| 6,974,989             | AF01234US                | United States | 05/06/2004  | 12/13/2005 | STRUCTURE AND METHOD FOR PROTECTING MEMORY CELLS FROM UV RADIATION DAMAGE AND UV RADIATION-INDUCED CHARGING DURING BACKEND PROCESSING                                                                 |
| 10/938,790            | AF01235                  | United States | 09/10/2004  |            | MEMORY ARRAY HAVING REDUCED BIT LINE TO BIT LINE AND WORD LINE TO WORD LINE LEAKAGE                                                                                                                   |
| 10/949,083            | AF01236                  | United States | 09/24/2004  |            | INTERCONNECT STRUCTURE FOR COPPER METALLIZATION HAVING A TOP ALUMINUM INTERCONNECT LAYER                                                                                                              |
| 7,158,417             | AF01240US                | United States | 03/25/2005  | 01/02/2007 | SEMICONDUCTOR DEVICE AND METHOD FOR WRITING DATE INTO THE SEMICONDUCTOR DEVICE                                                                                                                        |
| 11/103,960            | AF01241US                | United States | 04/12/2005  |            | SECTOR PROTECTION CIRCUIT FOR A NON-VOLATILE SEMICONDUCTOR MEMORY, SECTOR PROTECTION METHOD AND A NON-VOLATILE SEMICONDUCTOR MEMORY                                                                   |
| 7,352,620             | AF01248US                | United States | 04/20/2005  | 04/01/2008 | NON-VOLATILE SEMICONDUCTOR DEVICE AND METHOD FOR AUTOMATICALLY RECOVERING ERASE FAILURE IN THE DEVICE                                                                                                 |
| 7,079,423             | AF01272US                | United States | 07/20/2004  | 07/18/2006 | METHOD FOR PROGRAMMING DUAL BIT MEMORY DEVICES TO REDUCE COMPLEMENTARY BIT DISTURBANCE                                                                                                                |
| 7,281,180             | AF01273US                | United States | 07/01/2005  | 10/09/2007 | MEMORY SYSTEM AND TEST METHOD THEREOF                                                                                                                                                                 |
| 7,286,219             | AF01274US                | United States | 08/30/2005  | 10/23/2007 | EXPOSURE SYSTEM, SEMICONDUCTOR DEVICE, AND METHOD FOR FABRICATING THE SEMICONDUCTOR DEVICE                                                                                                            |
| 8,274,107             | AF01274US DIV            | United States | 08/22/2007  | 09/25/2012 | EXPOSURE SYSTEM, SEMICONDUCTOR DEVICE, AND METHOD FOR FABRICATING THE SEMICONDUCTOR DEVICE                                                                                                            |
| 7,479,427             | AF01276US                | United States | 09/27/2005  | 01/20/2009 | SEMICONDUCTOR DEVICE AND METHOD OF FABRICATION                                                                                                                                                        |
| 8,952,536             | AF01276US DIV            | United States | 08/27/2008  | 02/10/2015 | SEMICONDUCTOR DEVICE AND METHOD OF FABRICATION                                                                                                                                                        |
| 7,145,824             | AF01278US                | United States | 03/22/2005  | 12/05/2006 | TEMPERATURE COMPENSATION OF THIN FILM DIODE VOLTAGE THRESHOLD IN MEMORY SENSING CIRCUIT                                                                                                               |
| 10/935,301            | AF01279                  | United States | 09/07/2004  |            | VERTICAL JFET AS USED FOR SELECTIVE COMPONENT IN MEMORY ARRAY                                                                                                                                         |
| 7,474,579             | AF01281US                | United States | 12/21/2006  | 01/06/2009 | USE OF PERIODIC REFRESH IN MEDIUM RETENTION MEMORY ARRAYS                                                                                                                                             |
| 11/191,126            | AF01285                  | United States | 07/27/2005  |            | PROGRAM/ERASE WAVESHAPING CONTROL TO INCREASE DATA RETENTION OF A MEMORY CELL                                                                                                                         |
| 7,579,631             | AF01286US                | United States | 03/22/2005  | 08/25/2009 | VARIABLE BREAKDOWN CHARACTERISTIC DIODE                                                                                                                                                               |
| 6,441,418             | AF01287                  | United States | 11/01/1999  | 08/27/2002 | SPACER NARROWED, DUAL WIDTH CONTACT FOR CHARGE GAIN REDUCTION                                                                                                                                         |
| 7,564,720             | AF01287US                | United States | 07/18/2007  | 07/21/2009 | NONVOLATILE STORAGE AND ERASE CONTROL                                                                                                                                                                 |
| 7,902,086             | AF01288US                | United States | 12/08/2006  | 03/08/2011 | PREVENTION OF OXIDATION OF CARRIER IONS TO IMPROVE MEMORY RETENTION PROPERTIES OF POLYMER MEMORY CELL                                                                                                 |
| 7,129,133             | AF01291US                | United States | 09/13/2004  | 10/31/2006 | METHOD AND STRUCTURE OF MEMORY ELEMENT PLUG WITH CONDUCTIVE TA REMOVED FROM SIDEWALL AT REGION OF MEMORY ELEMENT FILMS                                                                                |
| 7,361,586             | AF01293US                | United States | 07/01/2005  | 04/22/2008 | PREAMORPHIZATION TO MINIMIZE VOID FORMATION                                                                                                                                                           |
| 7,232,765             | AF01296                  | United States | 11/12/2004  | 06/19/2007 | UTILIZATION OF A TA-CONTAINING CAP OVER COPPER TO FACILITATE CONCURRENT FORMATION OF COPPER VIAS AND MEMORY ELEMENT STRUCTURES                                                                        |
| 7,391,064             | AF01300US                | United States | 12/01/2004  | 06/24/2008 | MEMORY DEVICE WITH A SELECTION ELEMENT AND A CONTROL LINE IN A SUBSTANTIALLY SIMILAR LAYER                                                                                                            |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                       |
|-----------------------|--------------------------|---------------|-------------|------------|-------------------------------------------------------------------------------------------------------------|
| 7,696,017             | AF01300US DIV            | United States | 06/18/2008  | 04/13/2010 | MEMORY DEVICE WITH A SELECTION ELEMENT AND A CONTROL LINE<br>IN A SUBSTANTIALLY SIMILAR LAYER               |
| 7,288,487             | AF01301US                | United States | 12/01/2004  | 10/30/2007 | METAL/OXIDE ETCH AFTER POLISH TO PREVENT BRIDGING BETWEEN<br>ADJACENT FEATURES OF A SEMICONDUCTOR STRUCTURE |
| 11/135,957            | AF01303US                | United States | 05/24/2005  |            | A LATERAL ORGANIC MEMORY CELL AND METHOD TO PRODUCE A<br>LATERAL MEMORY CELL STRUCTURE                      |
| 7,157,732             | AF01306US                | United States | 07/01/2004  | 01/02/2007 | SWITCHABLE MEMORY DIODE- A NEW MEMORY DEVICE                                                                |
| 7,550,761             | AF01306US DIV            | United States | 12/26/2006  | 06/23/2009 | SWITCHABLE MEMORY DIODE- A NEW MEMORY DEVICE                                                                |
| 7,981,773             | AF01306US DIV2           | United States | 05/22/2009  | 07/19/2011 | SWITCHABLE MEMORY DIODE- A NEW MEMORY DEVICE                                                                |
| 7,105,374             | AF01308US                | United States | 01/12/2005  | 09/12/2006 | MEMORY CELL CONTAINING COPOLYMER CONTAINING<br>DAIRYLACETYLENE PORTION                                      |
| 7,777,218             | AF01308US DIV            | United States | 08/04/2006  | 08/17/2010 | MEMORY CELL CONTAINING COPOLYMER CONTAINING<br>DAIRYLACETYLENE PORTION                                      |
| 10/882,949            | AF01309US                | United States | 07/01/2004  |            | POLYMER MEMORY DEVICE AND FABRICATION PROCESS                                                               |
| 7,582,893             | AF01310US                | United States | 09/15/2005  | 09/01/2009 | SEMICONDUCTOR MEMORY DEVICE COMPRISING ONE OR MORE<br>INJECTING BILAYER ELECTRODES                          |
| 60/609,513            | AF01311                  | United States | 09/13/2004  |            | METHOD OF FORMING COPPER SULFIDE LAYER OVER SUBSTRATE                                                       |
| 11/224,196            | AF01311US                | United States | 09/12/2005  |            | METHOD OF FORMING COPPER SULFIDE LAYER OVER SUBSTRATE                                                       |
| 7,344,913             | AF01312US                | United States | 04/06/2005  | 03/18/2008 | SPIN ON MEMORY CELL ACTIVE LAYER DOPED WITH METAL IONS                                                      |
| 7,122,853             | AF01313US                | United States | 08/17/2004  | 10/17/2006 | METHOD TO IMPROVE YIELD AND SIMPLIFY OPERATION OF POLYMER<br>MEMORY CELLS                                   |
| 7,232,750             | AF01315US                | United States | 01/12/2005  | 06/19/2007 | METHODS INVOLVING SPIN-ON POLYMERS THAT REVERSIBLY BIND<br>CHARGE CARRIERS                                  |
| 7,776,682             | AF01316US                | United States | 04/20/2005  | 08/17/2010 | ORDERED POROSITY TO DIRECT MEMORY ELEMENT FORMATION                                                         |
| 7,067,349             | AF01318US                | United States | 10/19/2004  | 06/27/2006 | ION PATH POLYMERS FOR ION-MOTION MEMORY                                                                     |
| 7,289,353             | AF01320US                | United States | 08/17/2004  | 10/30/2007 | SYSTEMS AND METHODS FOR ADJUSTING PROGRAMMING<br>THRESHOLDS OF POLYMER MEMORY CELLS                         |
| 10/978,622            | AF01321TW                | United States | 11/01/2004  |            | CONTROLLED VOID MEMORY DEVICE                                                                               |
| 7,307,338             | AF01322US                | United States | 07/26/2004  | 12/11/2007 | THREE DIMENSIONAL POLYMER MEMORY CELL SYSTEMS                                                               |
| 7,309,893             | AF01327US                | United States | 06/14/2005  | 12/18/2007 | SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME                                                     |
| 7,387,936             | AF01327US DIV            | United States | 10/23/2007  | 06/17/2008 | SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME                                                     |
| 7,141,844             | AF01328US                | United States | 12/01/2004  | 11/28/2006 | SELECTIVE POLYMER GROWTH FOR MEMORY CELL FABRICATION                                                        |
| 7,266,019             | AF01329US CON            | United States | 08/30/2005  | 09/04/2007 | NON-VOLATILE MEMORY DEVICE AND ERASING METHOD THEREFOR                                                      |
| 6,984,563             | AF01333US                | United States | 07/01/2004  | 01/10/2006 | FLOATING GATE SEMICONDUCTOR COMPONENT AND METHOD OF<br>MANUFACTURE                                          |
| 7,120,050             | AF01338US CON            | United States | 10/26/2005  | 10/10/2006 | METHOD AND APPARATUS FOR SETTING OPERATIONAL<br>INFORMATION OF A NON-VOLATILE MEMORY                        |
| 6,977,195             | AF01340US                | United States | 08/16/2004  | 12/20/2005 | TEST STRUCTURE FOR CHARACTERIZING JUNCTION LEAKAGE<br>CURRENT                                               |
| 10/909,904            | AF01341                  | United States | 08/02/2004  |            | TEST STRUCTURE FOR CHARACTERIZING DIELECTRIC BREAKDOWN                                                      |
| 11/214,633            | AF01342US                | United States | 08/30/2004  |            | SEMICONDUCTOR DEVICE AND METHOD FOR BOOSTING WORD LINE                                                      |
| 7,525,853             | AF01342US CIP            | United States | 08/12/2005  | 04/28/2009 | SEMICONDUCTOR DEVICE AND METHOD FOR BOOSTING WORD LINE                                                      |
| 7,791,961             | AF01342US CON            | United States | 03/18/2009  | 09/07/2010 | SEMICONDUCTOR DEVICE AND METHOD FOR BOOSTING WORD LINE                                                      |
| 7,450,460             | AF01343US                | United States | 06/25/2004  | 11/11/2008 | VOLTAGE CONTROL CIRCUIT AND SEMICONDUCTOR DEVICE                                                            |
| 7,307,893             | AF01346US                | United States | 09/16/2005  | 12/11/2007 | SEMICONDUCTOR DEVICE AND METHOD FOR CONTROLLING THE<br>SAME                                                 |
| 7,558,904             | AF01349US                | United States | 07/22/2005  | 07/07/2009 | FILE MANAGEMENT FOR RECOVERING FROM SUDDEN POWER OFF                                                        |
| 11/261,174            | AF01351US CON            | United States | 10/29/2004  |            | MULTI-CHIP PACKAGE AND METHOD OF FABRICATING THE SAME                                                       |
| 7,400,013             | AF01353US                | United States | 12/03/2004  | 07/15/2008 | HIGH-VOLTAGE TRANSISTOR HAVING A U-SHAPED GATE AND<br>METHOD FOR FORMING SAME                               |
| 7,068,204             | AF01355US                | United States | 09/28/2004  | 06/27/2006 | SYSTEM THAT FACILITATES READING MULTI-LEVEL DATA IN NON-<br>VOLATILE MEMORY                                 |
| 11/201,042            | AF01360                  | United States | 08/10/2005  |            | METHOD OF FORMING GATE ELECTRODE STRUCTURES                                                                 |
| 6,987,696             | AF01361US                | United States | 07/06/2004  | 01/17/2006 | ERASE DISTRIBUTION IMPROVEMENT WITH ENHANCED DUMMY<br>WORDLINES IN FLASH MEMORY                             |
| 7,042,766             | AF01362US                | United States | 07/22/2004  | 05/09/2006 | METHOD OF PROGRAMMING A FLASH MEMORY DEVICE USING<br>MULTILEVEL CHARGE STORAGE                              |
| 7,042,767             | AF01365US                | United States | 08/02/2004  | 05/09/2006 | FLASH MEMORY UNIT AND METHOD OF PROGRAMMING A FLASH<br>MEMORY DEVICE                                        |
| 11/228,840            | AF01370US                | United States | 09/16/2005  |            | SEMICONDUCTOR DEVICE AND DATA READING METHOD                                                                |
| 7,206,232             | AF01371US                | United States | 06/23/2005  | 04/17/2007 | SEMICONDUCTOR DEVICE AND SOURCE VOLTAGE CONTROL<br>METHOD                                                   |
| 7,046,043             | AF01372US                | United States | 02/18/2005  | 05/16/2006 | CURRENT-VOLTAGE CONVERTER CIRCUIT AND CONTROL METHOD<br>THEREOF                                             |
| 7,061,816             | AF01376US                | United States | 02/18/2005  | 06/13/2006 | SEMICONDUCTOR MEMORY STORAGE DEVICE AND ITS REDUNDANT<br>METHOD                                             |
| 7,068,555             | AF01377US                | United States | 02/18/2005  | 06/22/2006 | SEMICONDUCTOR MEMORY STORAGE DEVICE AND A REDUNDANCY<br>CONTROL METHOD THEREFOR                             |
| 7,170,130             | AF01379US                | United States | 08/11/2004  | 01/30/2007 | MEMORY CELL WITH REDUCED DIBL AND VSS RESISTANCE                                                            |
| 7,154,807             | AF01380US                | United States | 02/22/2005  | 12/26/2006 | SEMICONDUCTOR MEMORY STORAGE DEVICE AND ITS CONTROL<br>METHOD                                               |
| 7,415,646             | AF01381US                | United States | 09/22/2004  | 08/19/2008 | PAGE EXE ERASE ALGORITHM FOR FLASH MEMORY                                                                   |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                         |
|-----------------------|---------------------------|---------------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------|
| 7,009,887             | AF01382US                 | United States | 06/03/2004  | 03/07/2006 | METHOD OF DETERMINING VOLTAGE COMPENSATION FOR FLASH MEMORY DEVICES                                                           |
| 7,440,333             | AF01382US DIV             | United States | 01/27/2006  | 10/21/2008 | METHOD OF DETERMINING VOLTAGE COMPENSATION FOR FLASH MEMORY DEVICES                                                           |
| 7,038,948             | AF01383US                 | United States | 09/22/2004  | 05/02/2006 | READ APPROACH FOR MULTI-LEVEL VIRTUAL GROUND MEMORY                                                                           |
| 7,113,431             | AF01385US                 | United States | 03/29/2005  | 09/26/2006 | QUAD BIT USING HOT HOLE ERASE FOR CBD CONTROL                                                                                 |
| 7,251,158             | AF01386US                 | United States | 06/10/2004  | 07/31/2007 | ERASE ALGORITHM FOR MULTI-LEVEL BIT FLASH MEMORY                                                                              |
| 7,672,803             | AF01387US                 | United States | 12/07/2004  | 03/02/2010 | INPUT OF TEST CONDITIONS AND OUTPUT GENERATION FOR BUILT-IN SELF TEST                                                         |
| 7,038,950             | AF01388US                 | United States | 11/05/2004  | 05/02/2006 | IMPROVED MULTI BIT PROGRAM ALGORITHM                                                                                          |
| 7,284,167             | AF01389US                 | United States | 01/24/2005  | 10/16/2007 | AUTOMATED TESTS FOR BUILT IN SELF TEST                                                                                        |
| 7,130,210             | AF01390US                 | United States | 01/13/2005  | 10/31/2006 | MULTI-LEVEL ONO FLASH PROGRAM ALGORITHM FOR THRESHOLD WIDTH CONTROL                                                           |
| 7,306,988             | AF01393                   | United States | 02/22/2005  | 12/11/2007 | MEMORY CELL AND METHOD OF MAKING THE MEMORY CELL                                                                              |
| 7,148,144             | AF01395US                 | United States | 09/13/2004  | 12/12/2006 | METHOD OF FORMING COPPER SULFIDE LAYER OVER SUBSTRATE                                                                         |
| 8,039,391             | AF01396                   | United States | 03/27/2006  | 10/18/2011 | A METHOD OF FORMING A CONTACT IN A SEMICONDUCTOR DEVICE WITH ENGINEERED PLASMA TREATMENT PROFILE OF BARRIER METAL LAYER       |
| 7,675,104             | AF01396US                 | United States | 07/31/2006  | 03/09/2010 | INTEGRATED CIRCUIT MEMORY SYSTEM EMPLOYING SILICON RICH LAYERS                                                                |
| 10/935,344            | AF01397US                 | United States | 09/07/2004  |            | SYSTEMS AND METHODS TO REDUCE LINE EDGE ROUGHNESS (LER)                                                                       |
| 7,084,062             | AF01398US                 | United States | 01/12/2005  | 08/01/2006 | USE OF TA-CAPPED METAL LINE TO IMPROVE FORMATION OF MEMORY ELEMENT FILMS                                                      |
| 7,288,782             | AF01398US DIV             | United States | 10/14/2005  | 10/30/2007 | USE OF Ta-CAPPED METAL LINE TO IMPROVE FORMATION OF MEMORY ELEMENT FILMS                                                      |
| 8,274,073             | AF01400US                 | United States | 03/11/2005  | 09/25/2012 | MEMORY DEVICE WITH IMPROVED SWITCHING SPEED AND DATA RETENTION                                                                |
| 7,221,595             | AF01402US                 | United States | 07/29/2005  | 05/22/2007 | SEMICONDUCTOR DEVICE AND METHOD OF GENERATING SENSE SIGNAL                                                                    |
| 7,227,778             | AF01403US                 | United States | 07/29/2005  | 06/05/2007 | SEMICONDUCTOR DEVICE AND WRITING METHOD                                                                                       |
| 7,184,338             | AF01404US                 | United States | 08/30/2005  | 02/27/2007 | SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE TESTING METHOD, AND PROGRAMMING METHOD                                             |
| 11/389,095            | AF01407US                 | United States | 03/27/2006  |            | METHOD OF FORMING A CONTACT WITH IMPROVED CONTACT FILL INCLUDING MULTIPLE CYCLE BARRIER METAL DEPOSITION AND PLASMA TREATMENT |
| 11/388,975            | AF01408US                 | United States | 03/27/2006  |            | A METHOD OF FORMING IMPROVED CONTACT METAL BOTTOM COVERAGE WITH REDUCED OVERHANG IN A CONTACT HOLE                            |
| 7,450,416             | AF01409US                 | United States | 12/23/2004  | 11/11/2008 | UTILIZATION OF MEMORY-DIODE WHICH MAY HAVE EACH OF A PLURALITY OF DIFFERENT MEMORY STATES                                     |
| 10/928,354            | AF01411                   | United States | 08/27/2004  |            | DEPOSITION OF HARD-MASK WITH MINIMIZED HILLOCKS AND BUBBLES                                                                   |
| 7,490,192             | AF01412US CON             | United States | 07/29/2004  | 02/10/2009 | METHOD AND APPARATUS FOR INFORMATION SETTING IN A NON-VOLATILE MEMORY DEVICE                                                  |
| 7,221,594             | AF01413US                 | United States | 07/29/2005  | 05/22/2007 | SEMICONDUCTOR DEVICE AND METHOD FOR WRITING DATA INTO SEMICONDUCTOR DEVICE                                                    |
| 7,450,434             | AF01416US                 | United States | 05/12/2005  | 11/11/2008 | SEMICONDUCTOR DEVICE AND ITS CONTROL METHOD                                                                                   |
| 7,729,170             | AF01416US DIV             | United States | 09/15/2008  | 06/01/2010 | SEMICONDUCTOR DEVICE AND ITS CONTROL METHOD                                                                                   |
| 7,821,833             | AF01416US DIV2            | United States | 09/15/2008  | 10/26/2010 | SEMICONDUCTOR DEVICE AND ITS CONTROL METHOD                                                                                   |
| 7,113,442             | AF01417US                 | United States | 05/11/2005  | 09/26/2006 | NON-VOLATILE SEMICONDUCTOR MEMORY, SEMICONDUCTOR DEVICE AND CHARGE PUMP CIRCUIT                                               |
| 7,206,241             | AF01422US                 | United States | 05/11/2005  | 04/17/2007 | SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD                                                                                   |
| 7,221,587             | AF01423US                 | United States | 05/11/2005  | 05/22/2007 | SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD                                                                                   |
| 7,224,602             | AF01425US                 | United States | 05/11/2005  | 05/29/2007 | SEMICONDUCTOR DEVICE AND CONTROL METHOD HAVING DATA PROTECTION FEATURE                                                        |
| 7,307,894             | AF01427US                 | United States | 05/12/2005  | 12/11/2007 | SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME                                                                           |
| 7,280,414             | AF01432US                 | United States | 08/30/2005  | 10/09/2007 | NON-VOLATILE MEMORY DEVICE, AND CONTROL METHOD THEREFOR                                                                       |
| 7,651,826             | AF01434US                 | United States | 11/30/2005  | 01/26/2010 | SEMICONDUCTOR DEVICE, FABRICATING METHOD THEREOF, AND PHOTOMASK                                                               |
| 12/575,122            | AF01434US DIV             | United States | 10/07/2009  |            | SEMICONDUCTOR DEVICE, FABRICATING METHOD THEREOF, AND PHOTOMASK                                                               |
| 7,239,548             | AF01438US                 | United States | 12/21/2005  | 07/03/2007 | METHOD AND APPARATUS FOR APPLYING BIAS TO A STORAGE DEVICE                                                                    |
| 7,251,161             | AF01439US                 | United States | 11/30/2005  | 07/31/2007 | SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING SAID SEMICONDUCTOR DEVICE                                                      |
| 7,415,568             | AF01441US CON             | United States | 07/28/2005  | 08/19/2008 | METHOD AND APPARATUS FOR INITIALIZATION CONTROL IN A NON-VOLATILE MEMORY DEVICE                                               |
| 7,285,848             | AF01443US                 | United States | 05/11/2005  | 10/23/2007 | CARRIER FOR STACKED TYPE SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME                                              |
| 7,642,637             | AF01443US DIV             | United States | 08/22/2007  | 01/05/2010 | CARRIER FOR STACKED TYPE SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME                                              |
| 7,675,107             | AF01445US                 | United States | 12/27/2005  | 03/09/2010 | SONOS WITH USE OF SWITCH GATE, WITHOUT BURIED DIFFUSION LAYER BITLINE                                                         |
| 7,888,209             | AF01445US DIV             | United States | 10/07/2009  | 02/15/2011 | NON-VOLATILE SONOS-TYPE MEMORY DEVICE                                                                                         |
| 11/133,966            | AF01446US                 | United States | 05/20/2005  |            | METHOD FOR FABRICATING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE                                                          |
| 7,488,657             | AF01447US                 | United States | 06/16/2005  | 02/10/2009 | METHOD AND SYSTEM FOR FORMING STRAIGHT WORD LINES IN A FLASH MEMORY ARRAY                                                     |
| 7,851,306             | AF01447US DIV             | United States | 12/03/2008  | 12/14/2010 | METHOD FOR FORMING A FLASH MEMORY DEVICE WITH STRAIGHT WORD LINES                                                             |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                                      |
|-----------------------|---------------------------|---------------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7,151,028             | AF01449US                 | United States | 11/04/2004  | 12/19/2006 | MEMORY CELL WITH PLASMA-GROWN OXIDE SPACER FOR REDUCED DIBL AND VSS RESISTANCE AND INCREASED RELIABILITY                                                                                   |
| 7,238,569             | AF01451US                 | United States | 04/25/2005  | 07/03/2007 | THE FORMATION METHOD OF AN ARRAY SOURCE LINE IN NAND FLASH MEMORY                                                                                                                          |
| 7,505,328             | AF01452US                 | United States | 08/14/2006  | 03/17/2009 | METHOD AND ARCHITECTURE FOR FAST FLASH MEMORY PROGRAMMING                                                                                                                                  |
| 7,764,546             | AF01452US DIV             | United States | 03/17/2009  | 07/27/2010 | METHOD AND ARCHITECTURE FOR FAST FLASH MEMORY PROGRAMMING                                                                                                                                  |
| 7,206,224             | AF01453US                 | United States | 01/18/2005  | 04/17/2007 | METHOD AND SYSTEMS FOR HIGH WRITE PERFORMANCE IN MULTI-BIT FLASH MEMORY DEVICES                                                                                                            |
| 60/563,046            | AF01453US                 | United States | 04/16/2004  |            | METHOD AND SYSTEMS FOR HIGH WRITE PERFORMANCE IN MULTI-BIT FLASH MEMORY DEVICES                                                                                                            |
| 7,283,402             | AF01453US DIV             | United States | 01/16/2007  | 10/16/2007 | METHODS AND SYSTEMS FOR HIGH WRITE PERFORMANCE IN MULTI-BIT FLASH MEMORY DEVICES                                                                                                           |
| 7,307,879             | AF01454US                 | United States | 11/29/2005  | 12/11/2007 | NONVOLATILE MEMORY DEVICE, AND ITS MANUFACTURING METHOD                                                                                                                                    |
| 7,736,953             | AF01455US                 | United States | 11/30/2005  | 06/15/2010 | SEMICONDUCTOR MEMORY AND METHOD OF FABRICATING THE SAME                                                                                                                                    |
| 7,232,724             | AF01458US                 | United States | 04/25/2005  | 06/19/2007 | RADICAL OXIDATION FOR BITLINE OXIDE OF SONOS                                                                                                                                               |
| 7,303,964             | AF01459US                 | United States | 04/25/2005  | 12/04/2007 | SELF-ALIGNED STI SONOS                                                                                                                                                                     |
| 7,196,008             | AF01461                   | United States | 03/23/2005  | 03/27/2007 | ALUMINUM OXIDE AS LINER OR COVER LAYER TO SPACERS IN MEMORY DEVICE                                                                                                                         |
| 7,286,398             | AF01462US                 | United States | 11/30/2004  | 10/23/2007 | SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING SAID SEMICONDUCTOR DEVICE                                                                                                                   |
| 7,263,007             | AF01463US                 | United States | 09/16/2005  | 08/28/2007 | SEMICONDUCTOR MEMORY DEVICE USING READ DATA BUS FOR WRITING DATA DURING HIGH-SPEED WRITING                                                                                                 |
| 7,151,293             | AF01464US                 | United States | 08/27/2004  | 12/19/2006 | SONOS MEMORY WITH INVERSION BIT-LINES                                                                                                                                                      |
| 7,501,677             | AF01464US DIV             | United States | 11/10/2006  | 03/10/2009 | SONOS MEMORY WITH INVERSION BIT-LINES                                                                                                                                                      |
| 8,125,018             | AF01467US                 | United States | 01/12/2005  | 02/28/2012 | MEMORY DEVICE HAVING TRAPEZOIDAL BITLINES AND METHOD OF FABRICATING SAME                                                                                                                   |
| 8,957,472             | AF01467US DIV             | United States | 01/24/2012  | 02/17/2015 | MEMORY DEVICE HAVING TRAPEZOIDAL BITLINES AND METHOD OF FABRICATING SAME                                                                                                                   |
| 11/257,825            | AF01468US CON             | United States | 10/24/2005  |            | SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME                                                                                                                                    |
| 7,227,780             | AF01470US                 | United States | 11/30/2005  | 06/05/2007 | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREOF                                                                                                                                            |
| 7,286,407             | AF01472US                 | United States | 10/28/2005  | 10/23/2007 | SEMICONDUCTOR DEVICE AND METHOD FOR CONTROLLING THE SAME                                                                                                                                   |
| 11/215,184            | AF01473US                 | United States | 08/29/2005  |            | ONE STEP REACTIVE ION ETCH TO REMOVE MULTIPLE OXIDE AND NITRIDE LAYERS                                                                                                                     |
| 7,362,620             | AF01475US                 | United States | 03/31/2006  | 04/22/2008 | SEMICONDUCTOR DEVBICE AND METHOD OF CONTROLLING THE SAME                                                                                                                                   |
| 7,910,974             | AF01477US                 | United States | 10/28/2005  | 03/22/2011 | SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THEREOF                                                                                                                                    |
| 8,389,361             | AF01477US DIV             | United States | 03/22/2011  | 03/05/2013 | SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THEREOF                                                                                                                                    |
| 13/786,252            | AF01477US DIV2            | United States | 03/05/2013  |            | SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THEREOF                                                                                                                                    |
| 7,321,511             | AF01479US                 | United States | 12/22/2005  | 01/22/2008 | SEMICONDUCTOR DEVICE AND METHOD FOR CONTROLLING OPERATION THEREOF                                                                                                                          |
| 11/139,228            | AF01480US                 | United States | 05/27/2005  |            | VERIFY AND READ CIRCUIT FOR NANO SCALE RESISTIVE MEMORY                                                                                                                                    |
| 11/446,611            | AF01481US                 | United States | 06/05/2006  |            | WET ETCH CHEMISTRIES AND PROCESSES FOR ELECTRONIC DEVICES                                                                                                                                  |
| 7,259,983             | AF01482US                 | United States | 05/27/2005  | 08/21/2007 | PAGE BUFFER ARCHITECTURE FOR PROGRAMMING, ERASING AND READING NANOSCALE RESISTIVE MEMORY DEVICES                                                                                           |
| 7,378,682             | AF01484US                 | United States | 02/07/2005  | 05/27/2008 | MEMORY ELEMENT USING ACTIVE LAYERS OF BLENDED MATERIALS                                                                                                                                    |
| 7,379,317             | AF01485US                 | United States | 12/23/2004  | 05/27/2008 | METHOD OF PROGRAMMING, READING AND ERASING MEMORY-DIODE IN A MEMORY-DIODE ARRAY                                                                                                            |
| 7,154,769             | AF01486US                 | United States | 02/07/2005  | 12/26/2006 | MEMORY DEVICE INCLUDING BARRIER LAYER FOR IMPROVED SWITCHING SPEED AND DATA RETENTION                                                                                                      |
| 7,269,050             | AF01488US                 | United States | 06/07/2005  | 09/11/2007 | METHOD OF PROGRAMMING A MEMORY DEVICE                                                                                                                                                      |
| 8,098,521             | AF01490US                 | United States | 03/31/2005  | 01/17/2012 | METHOD OF PROVIDING AN ERASE ACTIVATION ENERGY OF A MEMORY DEVICE                                                                                                                          |
| 13/324,310            | AF01490US DIV             | United States | 12/13/2011  |            | SYSTEM FOR PROGRAMMING A PHASE CHANGE MEMORY DEVICE INCLUDING PROVIDING A SECOND ERASE ACTIVATION ENERGY GREATER THAN A FIRST ERASE ACTIVATION ENERGY THAT CORRESPONDS TO A PROGRAM ENERGY |
| 7,035,141             | AF01491US                 | United States | 11/17/2004  | 04/25/2006 | DIODE ARRAY ARCHITECTURE FOR ADDRESSING NANOSCALE RESISTIVE MEMORY ARRAYS                                                                                                                  |
| 7,830,015             | AF01492US                 | United States | 03/25/2005  | 11/09/2010 | MEMORY DEVICE WITH IMPROVED DATA RETENTION                                                                                                                                                 |
| 7,968,464             | AF01492US DIV             | United States | 10/05/2010  | 06/28/2011 | Memory device with improved data retention                                                                                                                                                 |
| 7,994,007             | AF01493US                 | United States | 12/17/2008  | 08/09/2011 | SEMICONDUCTOR DVICE AND METHOD FOR MANUFACTURING DIODES USING ORGANIC MATERIAL                                                                                                             |
| 11/021,734            | AF01495US                 | United States | 12/23/2004  |            | MEMORY ELEMENTS USING ORGANIC ACTIVE LAYER                                                                                                                                                 |
| 7,102,156             | AF01496US                 | United States | 12/23/2004  | 09/05/2006 | MEMORY ELEMENT WITH NITROGEN-CONTAINING ACTIVE LAYER                                                                                                                                       |
| 7,208,757             | AF01497US                 | United States | 12/23/2004  | 04/24/2007 | MEMORY ELEMENT WITH IMPROVED PERFORMANCE                                                                                                                                                   |
| 11/147,059            | AF01498US                 | United States | 06/07/2005  |            | PROTECTION OF ACTIVE LAYERS OF MEMORY CELLS DURING PROCESSING OF OTHER ELEMENTS                                                                                                            |
| 7,220,642             | AF01500US                 | United States | 11/12/2004  | 05/22/2007 | MEMORY DEVICE WITH IMPROVED DATA RETENTION                                                                                                                                                 |
| 11/174,861            | AF01501US                 | United States | 07/05/2005  |            | MEMORY DEVICE WITH IMPROVED DATA RETENTION                                                                                                                                                 |
| 7,449,742             | AF01502US                 | United States | 12/20/2006  | 11/11/2008 | MEMORY DEVICES WITH ACTIVE AND PASSIVE LAYERS HAVING MULTIPLE SELF-ASSEMBLED SUBLAYERS                                                                                                     |
| 7,633,129             | AF01503US                 | United States | 09/16/2005  | 12/15/2009 |                                                                                                                                                                                            |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                |
|-----------------------|--------------------------|---------------|-------------|------------|----------------------------------------------------------------------------------------------------------------------|
| 7,468,296             | AF01504US                | United States | 11/30/2005  | 12/23/2008 | THIN FILM GERMANIUM DIODE WITH LOW REVERSE BREAKDOWN                                                                 |
| 7,307,321             | AF01506US                | United States | 03/25/2005  | 12/11/2007 | MEMORY DEVICE WITH IMPROVED DATA RETENTION                                                                           |
| 7,307,280             | AF01511US                | United States | 09/16/2005  | 12/11/2007 | MEMORY DEVICES WITH ACTIVE AND PASSIVE DOPED SOL-GEL<br>LAYERS                                                       |
| 11/228,839            | AF01512US                | United States | 09/16/2005  |            | MEMORY DEVICES WITH ACTIVE AND PASSIVE LAYERS HAVING<br>MULTIPLE SPIN-ON SUBLAYERS                                   |
| 11/174,881            | AF01514US                | United States | 07/05/2005  |            | STACKABLE MEMORY DEVICE AND ORGANIC TRANSISTOR<br>STRUCTURE                                                          |
| 7,312,641             | AF01523US                | United States | 12/28/2004  | 12/25/2007 | SENSE AMPLIFIER WITH HIGH VOLTAGE SWING                                                                              |
| 7,498,849             | AF01523US DIV            | United States | 11/15/2007  | 03/03/2009 | SENSE AMPLIFIERS WITH HIGH VOLTAGE SWING                                                                             |
| 7,126,862             | AF01524US                | United States | 03/08/2005  | 10/24/2006 | DECODER FOR MEMORY DEVICE                                                                                            |
| 10/975,629            | AF01527                  | United States | 10/28/2004  |            | SYSTEM AND METHOD FOR IMPROVED MEMORY PERFORMANCE IN A<br>MOBILE DEVICE                                              |
| 7,319,623             | AF01528US                | United States | 11/04/2004  | 01/15/2008 | METHOD FOR ISOLATING A FAILURE SITE IN A WORDLINE IN A<br>MEMORY ARRAY                                               |
| 7,274,592             | AF01530US CON            | United States | 01/30/2006  | 09/25/2007 | NON-VOLATILE MEMORY AND METHOD OF CONTROLLING THE SAME                                                               |
| 7,158,442             | AF01531US                | United States | 05/23/2005  | 01/02/2007 | FLEXIBLE LATENCY IN FLASH MEMORY                                                                                     |
| 10/987,678            | AF01532                  | United States | 11/12/2004  |            | INTEGRATED CIRCUIT PACKAGE AND MANUFACTURING METHOD                                                                  |
| 7,446,369             | AF01535US                | United States | 08/04/2005  | 11/04/2008 | SONOS MEMORY CELL HAVING HIGH-K DIELECTRIC                                                                           |
| 7,320,914             | AF01536US                | United States | 02/23/2005  | 01/22/2008 | SYSTEM AND METHOD FOR GATE FORMATION IN A SEMICONDUCTOR<br>DEVICE                                                    |
| 7,927,723             | AF01537US                | United States | 03/29/2005  | 04/19/2011 | FILM STACKS TO PREVENT UV-INDUCED DEVICE DAMAGE                                                                      |
| 7,238,571             | AF01539US                | United States | 02/24/2005  | 07/03/2007 | NON-VOLATILE MEMORY DEVICE WITH INCREASED RELIABILITY                                                                |
| 8,022,468             | AF01540US                | United States | 03/29/2005  | 09/20/2011 | ULTRAVIOLET RADIATION BLOCKING INTERLAYER DIELECTRIC                                                                 |
| 11/062,628            | AF01541US                | United States | 02/23/2005  |            | LITHOGRAPHIC MARK ISOLATION FOR OVERLAY ALIGNMENT                                                                    |
| 7,476,604             | AF01542US                | United States | 05/13/2005  | 01/13/2009 | AGGRESSIVE CLEANING PROCESS FOR SEMICONDUCTOR DEVICE<br>CONTACT FORMATION                                            |
| 7,432,178             | AF01543US                | United States | 10/21/2005  | 10/07/2008 | BIT LINE IMPLANT                                                                                                     |
| 11/380,971            | AF01544US                | United States | 05/01/2006  |            | BIT LINES FOR SEMICONDUCTOR DEVICES                                                                                  |
| 7,972,948             | AF01544US CON            | United States | 09/13/2010  | 07/05/2011 | METHOD FOR FORMING BIT LINES FOR SEMICONDUCTOR DEVICES                                                               |
| 7,811,915             | AF01544US DIV            | United States | 03/14/2008  | 10/12/2010 | METHOD FOR FORMING BIT LINES FOR SEMICONDUCTOR DEVICES                                                               |
| 7,285,499             | AF01545US                | United States | 05/12/2005  | 10/23/2007 | POLYMER SPACERS FOR CREATING SUB-LITHOGRAPHIC SPACES                                                                 |
| 7,341,956             | AF01546US                | United States | 04/07/2005  | 03/11/2008 | DISPOSABLE HARD MASK FOR FORMING BIT LINES                                                                           |
| 7,220,643             | AF01547US                | United States | 06/08/2005  | 05/22/2007 | SYSTEM AND METHOD FOR GATE FORMATION IN A SEMICONDUCTOR<br>DEVICE                                                    |
| 7,888,269             | AF01548US                | United States | 10/24/2005  | 02/15/2011 | TRIPLE LAYER ANTI-REFLECTIVE HARD MASK                                                                               |
| 7,307,027             | AF01549US                | United States | 08/11/2005  | 12/11/2007 | VOID FREE INTERLAYER DIELECTRIC                                                                                      |
| 11/380,973            | AF01550US                | United States | 05/01/2006  |            | CONDUCTIVE SPACERS FOR DEVICE ELECTRICAL CONTACT                                                                     |
| 7,256,141             | AF01551US                | United States | 05/24/2005  | 08/14/2007 | INTERFACE LAYER BETWEEN DUAL POLYCRYSTALLINE SILICON<br>LAYERS                                                       |
| 7,300,886             | AF01552US                | United States | 06/08/2005  | 11/27/2007 | INTERLAYER DIELECTRIC FOR CHARGE LOSS IMPROVEMENT                                                                    |
| 7,704,878             | AF01553US                | United States | 10/03/2005  | 04/27/2010 | CONTACT SPACER FORMATION USING ATOMIC LAYER DEPOSITION                                                               |
| 7,561,457             | AF01577US                | United States | 08/18/2006  | 07/14/2009 | SELECT TRANSISTOR USING BURIED BITLINE (FROM CORE) AS<br>SOURCE AND DRAIN                                            |
| 7,402,868             | AF01578US                | United States | 11/01/2004  | 07/22/2008 | SYSTEM AND METHOD FOR PROTECTING SEMICONDUCTOR DEVICES                                                               |
| 7,167,398             | AF01579US                | United States | 02/23/2005  | 01/23/2007 | SYSTEM AND METHOD FOR ERASING A MEMORY CELL                                                                          |
| 10/989,254            | AF01580US                | United States | 11/17/2004  |            | MEMORY CELL HAVING N-TYPE SUBSTRATE                                                                                  |
| 11/100,562            | AF01581US                | United States | 04/07/2005  |            | METHOD FOR ERASING A MEMORY DEVICE                                                                                   |
| 7,750,407             | AF01582US                | United States | 12/18/2006  | 07/06/2010 | STRAPPING CONTACT FOR CHARGE PROTECTION                                                                              |
| 8,404,541             | AF01582US DIV            | United States | 05/28/2010  | 03/26/2013 | STRAPPING CONTACT FOR CHARGE PROTECTION                                                                              |
| 7,285,827             | AF01583US                | United States | 08/02/2005  | 10/23/2007 | BACK-TO-BACK NPN/PNP PROTECTION DIODES                                                                               |
| 7,573,103             | AF01583US CON            | United States | 09/14/2007  | 08/11/2009 | BACK-TO-BACK NPN/PNP PROTECTION DIODES                                                                               |
| 8,148,770             | AF01584US                | United States | 06/24/2005  | 04/03/2012 | MEMORY DEVICE WITH BURIED BIT LINE STRUCTURE                                                                         |
| 7,269,067             | AF01586US                | United States | 07/06/2005  | 09/11/2007 | PROGRAMMING A MEMORY DEVICE                                                                                          |
| 8,912,014             | AF01587US                | United States | 01/18/2006  | 12/16/2014 | CONTROLLING THE LATCHUP EFFECT                                                                                       |
| 14/570,801            | AF01587US DIV            | United States | 12/15/2014  |            | CONTROLLING THE LATCHUP EFFECT                                                                                       |
| 7,170,796             | AF01588US                | United States | 08/01/2005  | 01/30/2007 | METHODS AND SYSTEMS FOR REDUCING THE THRESHOLD VOLTAGE<br>DISTRIBUTION FOLLOWING A MEMORY CELL ERASE                 |
| 7,678,674             | AF01589US                | United States | 08/26/2005  | 03/16/2010 | MEMORY CELL DUAL POCKET IMPLANT                                                                                      |
| 7,262,095             | AF01600US                | United States | 06/07/2005  | 08/28/2007 | SYSTEM AND METHOD FOR REDUCING PROCESS-INDUCED<br>CHARGING                                                           |
| 8,203,178             | AF01600US CON            | United States | 08/20/2010  | 06/19/2012 | SYSTEM AND METHOD FOR REDUCING PROCESS-INDUCED<br>CHARGING                                                           |
| 7,804,125             | AF01600US DIV            | United States | 07/24/2007  | 09/28/2010 | SYSTEM AND METHOD FOR REDUCING PROCESS-INDUCED<br>CHARGING                                                           |
| 7,679,129             | AF01601US                | United States | 05/13/2005  | 03/16/2010 | SYSTEM AND METHOD FOR IMPROVING OXIDE-NITRIDE-OXIDE (ONO)<br>COUPLING IN A SEMICONDUCTOR DEVICE                      |
| 7,842,618             | AF01602US                | United States | 08/01/2005  | 11/30/2010 | SYSTEM AND METHOD FOR IMPROVING MESA WIDTH IN A<br>SEMICONDUCTOR DEVICE                                              |
| 8,598,645             | AF01602US DIV            | United States | 10/22/2010  | 12/03/2013 | SYSTEM AND METHOD FOR IMPROVING MESA WIDTH IN A<br>SEMICONDUCTOR DEVICE                                              |
| 7,079,424             | AF01603US                | United States | 09/22/2004  | 07/18/2006 | METHODS AND SYSTEMS FOR REDUCING ERASE TIMES IN FLASH<br>MEMORY DEVICES                                              |
| 7,599,228             | AF01604US                | United States | 11/01/2004  | 10/06/2009 | FLASH MEMORY DEVICE HAVING INCREASED OVER-ERASE<br>CORRECTION EFFICIENCY AND ROBUSTNESS AGAINST DEVICE<br>VARIATIONS |
| 8,319,266             | AF01605US                | United States | 12/10/2004  | 11/27/2012 | ETCH STOP LAYER FOR MEMORY CELL RELIABILITY IMPROVEMENT                                                              |
| 8,658,496             | AF01605US DIV            | United States | 09/14/2012  | 02/25/2014 | ETCH STOP LAYER FOR MEMORY CELL RELIABILITY IMPROVEMENT                                                              |
| 7,939,440             | AF01606US                | United States | 06/15/2005  | 05/10/2011 | JUNCTION LEAKAGE SUPPRESSION IN MEMORY DEVICES                                                                       |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                              |
|-----------------------|--------------------------|---------------|-------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------|
| 8,536,011             | AF01606US CON            | United States | 03/29/2011  | 09/17/2013 | JUNCTION LEAKAGE SUPPRESSION IN MEMORY DEVICES                                                                                                     |
| 7,985,687             | AF01607US                | United States | 07/22/2005  | 07/26/2011 | SYSTEMS AND METHOD FOR IMPROVING RELIABILITY IN A SEMICONDUCTOR DEVICE                                                                             |
| 8,564,041             | AF01608US                | United States | 10/20/2006  | 10/22/2013 | CONTACTS FOR SEMICONDUCTOR DEVICES                                                                                                                 |
| 14/059,077            | AF01608US CON            | United States | 10/21/2013  |            | CONTACTS FOR SEMICONDUCTOR DEVICES                                                                                                                 |
| 8,802,537             | AF01609US                | United States | 07/27/2005  | 08/12/2014 | SYSTEM AND METHOD FOR IMPROVING RELIABILITY IN A SEMICONDUCTOR DEVICE                                                                              |
| 8,759,894             | AF01610US                | United States | 07/27/2005  | 06/24/2014 | SYSTEM AND METHOD FOR REDUCING CROSS-COUPPLING NOISE BETWEEN CHARGE STORAGE ELEMENTS IN A SEMICONDUCTOR DEVICE                                     |
| 8,367,493             | AF01612US                | United States | 04/20/2005  | 02/05/2013 | VOID FREE INTERLAYER DIELECTRIC                                                                                                                    |
| 8,614,475             | AF01612US CON            | United States | 12/31/2012  | 12/24/2013 | VOID FREE INTERLAYER DIELECTRIC                                                                                                                    |
| 8,133,801             | AF01613US                | United States | 07/27/2005  | 03/13/2012 | METHOD FOR FORMING A SEMICONDUCTOR LAYER WITH IMPROVED GAP FILLING PROPERTIES                                                                      |
| 8,647,899             | AF01613US CON            | United States | 01/31/2012  | 02/11/2014 | METHOD FOR FORMING A SEMICONDUCTOR LAYER WITH IMPROVED GAP FILLING PROPERTIES                                                                      |
| 7,492,001             | AF01625US                | United States | 03/23/2005  | 02/17/2009 | HIGH K STACK FOR NON-VOLATILE MEMORY                                                                                                               |
| 7,855,114             | AF01625US DIV            | United States | 01/09/2009  | 12/21/2010 | HIGH K STACK FOR NON-VOLATILE MEMORY                                                                                                               |
| 7,071,538             | AF01626US                | United States | 12/10/2004  | 07/04/2006 | ONO STACK WITH STEAM OXIDE FOR CHARGE RETENTION                                                                                                    |
| 7,863,128             | AF01627US                | United States | 02/04/2005  | 01/04/2011 | NON-VOLATILE MEMORY DEVICE WITH IMPROVED ERASE SPEED                                                                                               |
| 7,365,389             | AF01628US                | United States | 12/10/2004  | 04/29/2008 | MEMORY CELL HAVING ENHANCED HIGH-K DIELECTRIC                                                                                                      |
| 7,671,403             | AF01630US                | United States | 12/06/2006  | 03/02/2010 | P-CHANNEL NAND IN ISOLATED N-WELL                                                                                                                  |
| 7,381,620             | AF01631US                | United States | 03/09/2006  | 06/03/2008 | OXYGEN ELIMINATION FOR DEVICE PROCESSING                                                                                                           |
| 7,498,222             | AF01632US                | United States | 03/09/2006  | 03/03/2009 | ENHANCED ETCHING OF A HIGH DIELECTRIC CONSTANT LAYER                                                                                               |
| 7,879,718             | AF01634US                | United States | 12/27/2006  | 02/01/2011 | LOCAL INTERCONNECT HAVING INCREASED MISALIGNMENT TOLERANCE                                                                                         |
| 8,283,249             | AF01634US CON            | United States | 12/16/2010  | 10/09/2012 | LOCAL INTERCONNECT HAVING INCREASED MISALIGNMENT TOLERANCE                                                                                         |
| 8,314,454             | AF01634US DIV            | United States | 12/16/2010  | 11/20/2012 | LOCAL INTERCONNECT HAVING INCREASED MISALIGNMENT TOLERANCE                                                                                         |
| 13/616,719            | AF01634US DIV CON        | United States | 09/14/2012  |            | LOCAL INTERCONNECT HAVING INCREASED MISALIGNMENT TOLERANCE                                                                                         |
| 11/371,025            | AF01635US                | United States | 03/09/2006  |            | SALICIDED LOCAL INTERCONNECT FOR SOURCE LINE                                                                                                       |
| 7,202,128             | AF01636US                | United States | 06/24/2005  | 04/10/2007 | METHOD OF FORMING A MEMORY DEVICE HAVING IMPROVED ERASE SPEED                                                                                      |
| 7,465,644             | AF01637US                | United States | 10/26/2005  | 12/16/2008 | ISOLATION REGION BIRD'S BEAK SUPPRESSION                                                                                                           |
| 7,053,445             | AF01638US                | United States | 08/02/2005  | 05/30/2006 | MEMORY DEVICE WITH BARRIER LAYER                                                                                                                   |
| 7,816,724             | AF01638US                | United States | 07/21/2006  | 10/19/2010 | MEMORY DEVICE WITH BARRIER LAYER                                                                                                                   |
| 7,573,091             | AF01642US CON            | United States | 02/23/2006  | 08/11/2009 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME                                                                                          |
| 7,977,189             | AF01642US DIV            | United States | 07/14/2009  | 07/12/2011 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME                                                                                          |
| 7,323,744             | AF01643US CON            | United States | 02/24/2006  | 01/29/2008 | SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR                                                                                               |
| 7,489,029             | AF01644US                | United States | 08/30/2005  | 02/10/2009 | CARRIER STRUCTURE FOR STACKED-TYPE SEMICONDUCTOR DEVICE, METHOD OF PRODUCING THE SAME, AND METHOD OF FABRICATING STACKED-TYPE SEMICONDUCTOR DEVICE |
| 12/315,417            | AF01644US DIV            | United States | 12/03/2008  |            | CARRIER STRUCTURE FOR STACKED-TYPE SEMICONDUCTOR DEVICE, METHOD OF PRODUCING THE SAME, AND METHOD OF FABRICATING STACKED-TYPE SEMICONDUCTOR DEVICE |
| 8,443,131             | AF01645US                | United States | 10/26/2005  | 05/14/2013 | NON-VOLATILE MEMORY DEVICE                                                                                                                         |
| 7,737,019             | AF01646US                | United States | 03/08/2005  | 06/15/2010 | METHOD FOR CONTAINING A SILICIDED GATE WITHIN A SIDEWALL SPACER IN INTEGRATED CIRCUIT TECHNOLOGY                                                   |
| 8,252,676             | AF01646US CON            | United States | 04/30/2010  | 08/28/2012 | METHOD FOR CONTAINING A SILICIDED GATE WITHIN A SIDEWALL SPACER IN INTEGRATED CIRCUIT TECHNOLOGY                                                   |
| 10/993,253            | AF01647                  | United States | 11/19/2004  |            | SYSTEM AND METHOD FOR IN-PACKAGE MEMORY PROCESSING                                                                                                 |
| 7,679,150             | AF01650US                | United States | 04/27/2006  | 03/16/2010 | SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD THEREFOR                                                                                               |
| 7,052,961             | AF01652                  | United States | 12/03/2004  | 05/30/2006 | METHOD FOR FORMING WORDLINES HAVING IRREGULAR SPACING IN A MEMORY ARRAY                                                                            |
| 8,901,637             | AF01653US CON            | United States | 01/24/2006  | 12/02/2014 | SEMICONDUCTOR MEMORY DEVICE HAVING LOWERED BIT LINE RESISTANCE                                                                                     |
| 14/540,803            | AF01653US DIV            | United States | 11/13/2014  |            | SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME                                                                                            |
| 11/341,932            | AF01654US CON            | United States | 01/26/2006  |            | SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME                                                                                            |
| 7,622,067             | AF01657US                | United States | 05/26/2006  | 11/24/2009 | RESIN-SEALING METHOD USING INTERMEDIATE PLATE                                                                                                      |
| 7,414,277             | AF01658US                | United States | 04/22/2005  | 08/19/2008 | MEMORY CELL HAVING COMBINATION RAISED SOURCE AND DRAIN AND METHOD OF FABRICATING SAME                                                              |
| 11/363,792            | AF01661US CON            | United States | 02/28/2006  |            | SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREOF                                                                                                |
| 7,968,404             | AF01662US CON            | United States | 02/24/2006  | 06/28/2011 | SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR                                                                                               |
| 7,414,305             | AF01663US CON            | United States | 01/27/2006  | 08/19/2008 | CARRIER FOR STACKED TYPE SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING STACKED TYPE SEMICONDUCTOR DEVICE                                          |
| 7,846,771             | AF01663US DIV            | United States | 07/01/2008  | 12/07/2010 | CARRIER FOR STACKED TYPE SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING STACKED TYPE SEMICONDUCTOR DEVICE                                          |
| 7,312,495             | AF01665US                | United States | 04/07/2005  | 12/25/2007 | SPLIT GATE MULTI-BIT MEMORY CELL                                                                                                                   |
| 8,445,972             | AF01666US                | United States | 03/31/2006  | 05/21/2013 | SEMICONDUCTOR DEVICE WITH RECONFIGURABLE LOGIC                                                                                                     |
| 7,443,732             | AF01668US                | United States | 09/20/2005  | 10/28/2008 | HIGH PERFORMANCE FLASH MEMORY DEVICE CAPABLE OF HIGH DENSITY DATA STORAGE                                                                          |
| 7,433,228             | AF01669US                | United States | 09/20/2005  | 10/07/2008 | MULTI-BIT FLASH MEMORY DEVICE HAVING IMPROVED PROGRAM RATE                                                                                         |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                   |
|-----------------------|---------------------------|---------------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------|
| 7,295,475             | AF01673US                 | United States | 09/20/2005  | 11/13/2007 | FLASH MEMORY PROGRAMMING USING AN INDICATION BIT TO INTERPRET STATE                                                     |
| 8,358,543             | AF01674US                 | United States | 09/20/2005  | 01/22/2013 | FLASH MEMORY PROGRAMMING WITH DATA DEPENDENT CONTROL OF SOURCE LINES                                                    |
| 7,352,626             | AF01675US                 | United States | 08/29/2005  | 04/01/2008 | VOLTAGE REGULATOR WITH LESS OVERSHOOT AND FASTER SETTLING TIME                                                          |
| 7,706,183             | AF01676US                 | United States | 07/27/2005  | 04/27/2010 | IMPROVED READ MODE FOR FLASH MEMORY                                                                                     |
| 8,107,294             | AF01676US DIV             | United States | 03/24/2010  | 01/31/2012 | IMPROVED READ MODE FOR FLASH MEMORY                                                                                     |
| 7,342,830             | AF01677US                 | United States | 01/17/2006  | 03/11/2008 | IMPROVED PROGRAM AND PROGRAM VERIFY OPERATIONS FOR FLASH MEMORY                                                         |
| 7,196,938             | AF01681US                 | United States | 09/20/2005  | 03/27/2007 | CHARGE SHARING TECHNIQUE DURING FLASH MEMORY PROGRAMMING                                                                |
| 7,423,915             | AF01682US                 | United States | 01/17/2006  | 09/09/2008 | RANDOM CACHE READ USING A DOUBLE MEMORY                                                                                 |
| 7,307,878             | AF01684US                 | United States | 08/29/2005  | 12/11/2007 | FLASH MEMORY DEVICE HAVING IMPROVED PROGRAM RATE                                                                        |
| 7,453,724             | AF01684US DIV             | United States | 10/31/2007  | 11/18/2008 | FLASH MEMORY DEVICE HAVING IMPROVED PROGRAM RATE                                                                        |
| 7,957,204             | AF01686US                 | United States | 09/20/2005  | 06/07/2011 | FLASH MEMORY PROGRAMMING POWER REDUCTION                                                                                |
| 8,462,564             | AF01686US CON             | United States | 04/20/2011  | 06/11/2013 | FLASH MEMORY PROGRAMMING POWER REDUCTION                                                                                |
| 11/258,823            | AF01688US                 | United States | 10/25/2005  |            | SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME                                                                 |
| 11/317,083            | AF01689US                 | United States | 12/21/2005  |            | FABRICATION METHOD FOR A SEMICONDUCTOR DEVICE                                                                           |
| 7,239,576             | AF01690US CON             | United States | 01/27/2006  | 07/03/2007 | MEMORY DEVICE AND METHOD OF CONTROLLING THE SAME                                                                        |
| 7,239,574             | AF01691US                 | United States | 12/21/2005  | 07/03/2007 | SYNCHRONOUS STORAGE DEVICE AND CONTROLLING METHOD THEREOF                                                               |
| 8,089,110             | AF01693US                 | United States | 02/09/2006  | 01/03/2012 | SWITCHABLE MEMORY DIODES BASED ON FERROELECTRIC/CONJUGATED POLYMER HETEROSTRUCTURES AND/OR THEIR COMPOSITES             |
| 8,710,628             | AF01693US DIV             | United States | 12/09/2011  | 04/29/2014 | SWITCHABLE MEMORY DIODES BASED ON FERROELECTRIC/CONJUGATED POLYMER HETEROSTRUCTURES AND/OR THEIR COMPOSITES             |
| 14/222,258            | AF01693US DIV2            | United States | 03/21/2014  |            | SWITCHABLE MEMORY DIODES BASED ON FERROELECTRIC/CONJUGATED POLYMER HETEROSTRUCTURES AND/OR THEIR COMPOSITES             |
| 7,645,693             | AF01694US                 | United States | 04/27/2006  | 01/12/2010 | SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD THEREFOR                                                                    |
| 8,586,413             | AF01695US                 | United States | 05/04/2005  | 11/19/2013 | MULTI-CHIP MODULE HAVING A SUPPORT STRUCTURE AND METHOD OF MANUFACTURE                                                  |
| 14/076,706            | AF01695US DIV             | United States | 11/11/2013  |            | MULTI-CHIP MODULE AND METHOD OF MANUFACTURE                                                                             |
| 7,696,616             | AF01696US                 | United States | 01/25/2006  | 04/13/2010 | STACKED TYPE SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING STACKED TYPE SEMICONDUCTOR DEVICE                           |
| 7,433,219             | AF01698US CON             | United States | 01/27/2006  | 10/07/2008 | METHOD AND APPARATUS FOR ADDRESS ALLOTING AND VERIFICATION IN A SEMICONDUCTOR DEVICE                                    |
| 7,813,154             | AF01698US DIV             | United States | 09/18/2008  | 10/12/2010 | METHOD AND APPARATUS FOR ADDRESS ALLOTING AND VERIFICATION IN A SEMICONDUCTOR DEVICE                                    |
| 8,023,341             | AF01698US DIV2            | United States | 10/12/2010  | 09/20/2011 | METHOD AND APPARATUS FOR ADDRESS ALLOTING AND VERIFICATION IN A SEMICONDUCTOR DEVICE                                    |
| 7,692,236             | AF01700US                 | United States | 02/15/2005  | 04/06/2010 | MULTIPLE DUAL BIT MEMORY INTEGRATED CIRCUIT SYSTEM                                                                      |
| 11/045,450            | AF01705US                 | United States | 01/28/2005  |            | DIODE STRUCTURE AND METHOD OF MANUFACTURE                                                                               |
| 11/394,986            | AF01707US                 | United States | 03/30/2006  |            | STACKED-TYPE SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME                                                  |
| 7,397,696             | AF01708US                 | United States | 12/28/2004  | 07/08/2008 | CURRENT SENSING ARCHITECTURE FOR HIGH BITLINE VOLTAGE, RAIL TO RAIL OUTPUT SWING AND V <sub>CC</sub> NOISE CANCELLATION |
| 7,099,204             | AF01709US                 | United States | 03/23/2005  | 08/29/2006 | CURRENT SENSING CIRCUIT WITH A CURRENT-COMPENSATED DRAIN VOLTAGE REGULATION                                             |
| 7,327,186             | AF01710US                 | United States | 05/24/2005  | 02/05/2008 | FAST WIDE OUTPUT RANGE CMOS VOLTAGE REFERENCE                                                                           |
| 7,321,513             | AF01713US                 | United States | 03/28/2006  | 01/22/2008 | SEMICONDUCTOR DEVICE AND METHOD OF GENERATING A REFERENCE VOLTAGE THEREFOR                                              |
| 7,354,826             | AF01715US                 | United States | 04/22/2005  | 04/08/2008 | METHOD FOR FORMING MEMORY ARRAY BITLINES COMPRISING EPITAXIALLY GROWN SILICON AND RELATED STRUCTURE                     |
| 7,236,843             | AF01716US                 | United States | 07/20/2005  | 06/26/2007 | METHOD AND APPARATUS FOR SCHEDULING WORK IN A FABRICATION FACILITY                                                      |
| 7,141,838             | AF01720US                 | United States | 01/27/2005  | 11/28/2006 | BURIED WORD LINE MEMORY INTEGRATED CIRCUIT SYSTEM                                                                       |
| 8,508,047             | AF01720US DIV             | United States | 10/17/2006  | 08/13/2013 | BURIED WORD LINE MEMORY INTEGRATED CIRCUIT SYSTEM                                                                       |
| 7,466,605             | AF01721US CON             | United States | 02/22/2006  | 12/16/2008 | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREFOR                                                                        |
| 11/361,223            | AF01723US CON             | United States | 02/23/2006  |            | METHOD AND APPARATUS FOR REDUNDANCY SETTING IN A STORAGE DEVICE                                                         |
| 7,352,638             | AF01724US CON             | United States | 02/23/2006  | 04/01/2008 | METHOD AND APPARATUS FOR TESTING A MEMORY DEVICE                                                                        |
| 7,239,553             | AF01725US CON             | United States | 01/31/2006  | 07/03/2007 | METHOD AND APPARATUS FOR REFERENCE CELL ADJUSTING IN A STORAGE DEVICE                                                   |
| 7,626,227             | AF01728US                 | United States | 04/27/2006  | 12/01/2009 | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR                                                                  |
| 11/441,771            | AF01729US                 | United States | 05/26/2006  |            | SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME                                                                |
| 7,163,839             | AF01730US                 | United States | 04/27/2005  | 01/16/2007 | MULTI CHIP MODULE AND METHOD OF MANUFACTURE                                                                             |
| 11/165,629            | AF01731                   | United States | 06/23/2005  |            | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE                                                                       |
| 7,385,844             | AF01733US CIP             | United States | 07/27/2006  | 06/10/2008 | SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME                                                                 |
| 7,825,457             | AF01735US                 | United States | 04/27/2006  | 11/02/2010 | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR                                                                  |
| 8,097,518             | AF01735US DIV             | United States | 10/06/2010  | 01/17/2012 | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR                                                                  |
| 13/323,579            | AF01735US DIV2            | United States | 12/12/2011  |            | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR                                                                  |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                              |
|-----------------------|---------------------------|---------------|-------------|------------|----------------------------------------------------------------------------------------------------|
| 7,739,559             | AF01739US                 | United States | 05/30/2006  | 06/15/2010 | MEMORY DEVICE COMPRISING A PROGRAM ERROR RECOVERY FUNCTION                                         |
| 11/136,981            | AF01741                   | United States | 05/25/2005  |            | READ-ONLY MEMORY ARRAY WITH DIELECTRIC BREAKDOWN PROGRAMMABILITY                                   |
| 8,076,753             | AF01742US CIP             | United States | 06/30/2006  | 12/13/2011 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME                                          |
| 8,698,280             | AF01742US CON             | United States | 12/08/2011  | 04/15/2014 | CAPACITIVE ELEMENT USING MOS TRANSISTORS                                                           |
| 8,642,422             | AF01742US DIV             | United States | 12/08/2011  | 02/04/2014 | METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE                                                       |
| 7,321,515             | AF01743US                 | United States | 03/16/2006  | 01/22/2008 | MEMORY DEVICE AND CONTROL METHOD THEREFOR                                                          |
| 7,943,982             | AF01744US                 | United States | 05/30/2005  | 05/17/2011 | SEMICONDUCTOR DVICE HAVING LAMINATED ELECTRONIC CONDUCTOR ON BIT LINE                              |
| 8,278,171             | AF01744US DIV             | United States | 04/07/2011  | 10/02/2012 | SEMICONDUCTOR DVICE HAVING LAMINATED ELECTRONIC CONDUCTOR ON BIT LINE                              |
| 7,376,033             | AF01745US CON             | United States | 05/30/2006  | 05/20/2008 | SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD THEREFOR                                               |
| 11/227,749            | AF01746                   | United States | 09/11/2006  |            | METHOD FOR FORMING SPACERS BETWEEN BITLINES IN A VIRTUAL GROUND MEMORY ARRAY AND REALTED STRUCTURE |
| 7,273,775             | AF01747US                 | United States | 10/04/2005  | 09/25/2007 | RELIABLE AND SCALABLE VIRTUAL GROUND MEMORY ARRAYS FORMED WITH REDUCED THERMAL CYCLE               |
| 5,815,438             | AF01757TW                 | United States | 02/28/1997  | 09/29/1998 | OPTIMIZED BIASING SCHEME FOR NAND READ AND HOT-CARRIER WRITE OPERATIONS                            |
| 7,274,602             | AF01758US CON             | United States | 05/30/2006  | 09/25/2007 | STORAGE DEVICE AND CONTROL METHOD THEREFOR                                                         |
| 11/158,510            | AF01759                   | United States | 06/22/2005  |            | AUTOMATIC RESOURCE ASSIGNMENT IN DEVICES HAVING STACKED MODULES                                    |
| 60/655,269            | AF01759                   | United States | 02/21/2005  |            | DEVICE HAVING STACKED MODULES                                                                      |
| 60/655,271            | AF01759                   | United States | 02/22/2005  |            | DEVICE HAVING STACKED MODULES                                                                      |
| 7,286,384             | AF01760US                 | United States | 06/22/2005  | 10/23/2007 | AUTOMATIC RESOURCE ASSIGNMENT IN STACKED MODULE DEVICES                                            |
| 7,691,668             | AF01761US                 | United States | 12/19/2006  | 04/06/2010 | METHOD AND APPARATUS FOR MULTI-CHIP PACKAGING                                                      |
| 8,324,716             | AF01761US DIV             | United States | 03/09/2010  | 12/04/2012 | METHOD AND APPARATUS FOR MULTI-CHIP PACKAGING                                                      |
| 7,227,768             | AF01762US                 | United States | 07/01/2005  | 06/05/2007 | POWER INTERCONNECT STRUCTURE FOR BALANCED BITLINE CAPACITANCE IN A MEMORY ARRAY                    |
| 7,260,014             | AF01763US                 | United States | 10/14/2005  | 08/21/2007 | VOLTAGE SUPPLY CIRCUIT FOR MEMORY ARRAY PROGRAMMING                                                |
| 7,462,903             | AF01765US                 | United States | 09/14/2005  | 12/09/2008 | METHODS FOR FABRICATING SEMICONDUCTOR DEVICES AND CONTACTS TO SEMICONDUCTOR DEVICES                |
| 8,803,216             | AF01766US                 | United States | 03/20/2006  | 08/12/2014 | MEMORY CELL SYSTEM USING SILICON-RICH NITRIDE                                                      |
| 7,372,743             | AF01770US CIP             | United States | 12/13/2006  | 05/13/2008 | A NON VOLATILE MEMORY DEVICE AND ITS CONTROL METHOD                                                |
| 7,928,005             | AF01772US                 | United States | 09/27/2005  | 04/19/2011 | METHOD FOR FORMING NARROW STRUCTURES IN A SEMICONDUCTOR DEVICE                                     |
| 8,901,720             | AF01772US CON             | United States | 03/09/2011  | 12/02/2014 | METHOD OF FORMING NARROW STRUCTURES IN A SEMICONDUCTOR DEVICE                                      |
| 7,639,768             | AF01773US                 | United States | 05/01/2006  | 12/29/2009 | METHOD FOR IMPROVING PERFORMANCE IN A MOBILE DEVICE                                                |
| 11/126,800            | AF01775US                 | United States | 05/11/2005  |            | RESISTIVE MEMORY DEVICE WITH IMPROVED DATA RETENTION AND REDUCED POWER                             |
| 11/203,359            | AF01776                   | United States | 08/12/2005  |            | CONTROL OF THRESHOLD VOLTAGE DISTRIBUTION IN MEMORY ARRAY                                          |
| 7,244,660             | AF01777US                 | United States | 10/31/2005  | 07/17/2007 | METHOD FOR MANUFACTURING A SEMICONDUCTOR COMPONENT                                                 |
| 7,163,862             | AF01778US                 | United States | 10/04/2005  | 01/16/2007 | SEMICONDUCTOR MEMORY DEVICES AND METHODS FOR FABRICATING THE SAME                                  |
| 7,835,183             | AF01780US CIP             | United States | 11/20/2007  | 11/16/2010 | NONVOLATILE STORAGE DEVICE AND CONTROL METHOD THEREOF                                              |
| 7,573,743             | AF01781US CIP             | United States | 08/30/2006  | 08/11/2009 | SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME                                                |
| 7,903,473             | AF01781US CON             | United States | 07/23/2009  | 03/08/2011 | SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME                                                |
| 7,889,577             | AF01781US DIV             | United States | 06/25/2009  | 02/15/2011 | SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME                                                |
| 7,286,388             | AF01782US                 | United States | 06/23/2005  | 10/23/2007 | RESISTIVE MEMORY DEVICE WITH IMPROVED DATA RETENTION                                               |
| 8,008,778             | AF01783US CIP             | United States | 06/30/2006  | 08/30/2011 | NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD OF NON-VOLATILE MEMORY DEVICE                        |
| 13/217,172            | AF01783US CIP DIV         | United States | 08/24/2011  |            | METHOD OF FORMING A DAMASCENE INTERCONNECT ON A BARRIER LAYER (as amended)                         |
| 8,395,959             | AF01784US                 | United States | 08/25/2006  | 03/12/2013 | STORAGE DEVICE, CONTROL METHOD OF STORAGE DEVICE, AND CONTROL METHOD OF STORAGE CONTROL DEVICE     |
| 8,811,107             | AF01784US DIV             | United States | 12/21/2012  | 08/19/2014 | STORAGE DEVICE, CONTROL METHOD OF STORAGE DEVICE, AND CONTROL METHOD OF STORAGE CONTROL DEVICE     |
| 7,706,197             | AF01785US CIP             | United States | 08/25/2006  | 04/27/2010 | MEMORY DEVICE AND CONTROL METHOD OF MEMORY DEVICE                                                  |
| 7,436,715             | AF01789US CIP             | United States | 06/30/2006  | 10/14/2008 | NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD OF NON-VOLATILE MEMORY DEVICE                        |
| 7,880,218             | AF01792US CIP             | United States | 06/28/2006  | 02/01/2011 | SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR                                               |
| 8,530,307             | AF01792US DIV             | United States | 12/21/2010  | 09/10/2013 | SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR                                               |
| 8,222,147             | AF01793US CIP             | United States | 06/29/2006  | 07/17/2012 | SEMICONDUCTOR DEVICE WITH STOP LAYERS AND FABRICATION METHOD USING CERIA SLURRY                    |
| 13/523,568            | AF01793US DIV             | United States | 06/14/2012  |            | SEMICONDUCTOR DEVICE WITH STOP LAYERS AND FABRICATION METHOD USING CERIA SLURRY                    |
| 7,635,994             | AF01796US                 | United States | 01/20/2006  | 12/22/2009 | FAST RAIL-TO-RAIL VOLTAGE COMPARATOR AND METHOD FOR RAIL-TO-RAIL VOLTAGE COMPARISON                |
| 7,632,689             | AF01797US                 | United States | 10/03/2006  | 12/15/2009 | METHODS FOR CONTROLLING THE PROFILE OF A TRENCH OF A SEMICONDUCTOR STRUCTURE                       |
| 7,596,032             | AF01802US CIP             | United States | 06/28/2006  | 09/29/2009 | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREFOR                                                   |
| 7,978,523             | AF01802US CON             | United States | 07/30/2009  | 07/12/2011 | SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME                                                |
| 8,130,584             | AF01802US CON2            | United States | 10/15/2010  | 03/06/2012 | SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME                                                |
| 8,705,303             | AF01802US CON3            | United States | 03/06/2012  | 04/22/2014 | SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME                                                |
| 7,969,787             | AF01802US DIV             | United States | 07/30/2009  | 06/28/2011 | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREFOR                                                   |
| 8,264,901             | AF01802US DIV CON         | United States | 10/11/2010  | 09/11/2012 | SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME                                                |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO.  | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                 |
|-----------------------|---------------------------|---------------|-------------|------------|-------------------------------------------------------------------------------------------------------|
| 8,611,167             | AF01802US DIV CON<br>DIV  | United States | 09/11/2012  | 12/17/2013 | SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME                                                   |
| 14/081,987            | AF01802US DIV CON<br>DIV2 | United States | 11/15/2013  |            | SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME                                                   |
| 8,045,388             | AF01802US DIV2            | United States | 06/18/2010  | 10/25/2011 | SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME                                                   |
| 8,351,268             | AF01802US DIV3            | United States | 10/05/2011  | 01/08/2013 | SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME                                                   |
| 7,724,071             | AF01803US CIP             | United States | 07/25/2006  | 05/25/2010 | SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE<br>SAME                                            |
| 11/243,078            | AF01806                   | United States | 10/04/2005  |            | DECODER FOR MEMORY DEVICE WITH LOADING CAPACITOR                                                      |
| 11/243,064            | AF01807                   | United States | 10/04/2005  |            | VOLTAGE BOOSTING FOR MEMORY DEVICE                                                                    |
| 7,859,026             | AF01810US                 | United States | 03/16/2006  | 12/28/2010 | VERTICAL SEMICONDUCTOR DEVICE                                                                         |
| 7,339,222             | AF01811US                 | United States | 05/03/2006  | 03/04/2008 | METHOD FOR DETERMINING WORDLINE CRITICAL DIMENSION IN A<br>MEMORY ARRAY AND RELATED STRUCTURE         |
| 11/529,805            | AF01812US CIP             | United States | 09/29/2006  |            | SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR                                                  |
| 7,915,663             | AF01813US CIP             | United States | 07/25/2006  | 03/29/2011 | FABRICATION AND METHOD OF OPERATION OF MULTI-LEVEL<br>MEMORY CELL ON SOI SUBSTRATE                    |
| 8,369,161             | AF01813US CIP DIV         | United States | 02/11/2011  | 02/05/2013 | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREFOR                                                      |
| 7,589,371             | AF01814US CIP             | United States | 12/15/2008  | 09/15/2009 | SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR                                                  |
| 7,915,661             | AF01814US CON             | United States | 08/18/2009  | 03/29/2011 | SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR                                                  |
| 7,443,746             | AF01816US                 | United States | 10/18/2005  | 10/28/2008 | MEMORY ARRAY TESTER INFORMATION PROCESSING SYSTEM                                                     |
| 7,289,351             | AF01817US                 | United States | 06/24/2005  | 10/30/2007 | METHOD OF PROGRAMMING A RESISTIVE MEMORY DEVICE                                                       |
| 8,183,622             | AF01818US CIP             | United States | 07/27/2006  | 05/22/2012 | SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR                                                  |
| 13/323,538            | AF01818US DIV             | United States | 12/12/2011  |            | SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR                                                  |
| 7,606,085             | AF01819US CIP             | United States | 08/08/2006  | 10/20/2009 | SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME                                                   |
| 7,898,879             | AF01819US CON             | United States | 10/06/2009  | 03/01/2011 | SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME                                                   |
| 7,957,205             | AF01819US DIV             | United States | 10/06/2009  | 06/07/2011 | SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME                                                   |
| 8,379,472             | AF01819US DIV2            | United States | 06/07/2011  | 02/19/2013 | SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME                                                   |
| 8,699,283             | AF01819US DIV3            | United States | 02/19/2013  | 04/15/2014 | SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME                                                   |
| 11/423,643            | AF01823US                 | United States | 06/12/2006  |            | METHOD AND APPARATUS FOR VERSATILE HIGH VOLTAGE LEVEL<br>DETECTION WITH RELATIVE NOISE IMMUNITY       |
| 7,345,916             | AF01826US                 | United States | 06/12/2006  | 03/18/2008 | METHOD AND APPARATUS FOR HIGH VOLTAGE OPERATION FOR A<br>HIGH PERFORMANCE SEMICONDUCTOR MEMORY DEVICE |
| 7,613,044             | AF01826US DIV             | United States | 12/05/2007  | 11/03/2009 | METHOD AND APPARATUS FOR HIGH VOLTAGE OPERATION FOR A<br>HIGH PERFORMANCE SEMICONDUCTOR MEMORY DEVICE |
| 7,813,459             | AF01828US                 | United States | 10/03/2005  | 10/12/2010 | DIGITAL DATA TRANSFER BETWEEN DIFFERENT CLOCK DOMAINS                                                 |
| 7,683,473             | AF01829US CIP             | United States | 09/28/2006  | 03/23/2010 | SEMICONDUCTOR DEVICE, FABRICATION METHOD THEREFOR, AND<br>FILM FABRICATION METHOD                     |
| 7,538,383             | AF01831US                 | United States | 05/03/2006  | 05/26/2009 | TWO-BIT MEMORY CELL HAVING CONDUCTIVE CHARGE STORAGE<br>SEGMENTS AND METHOD FOR FABRICATING SAME      |
| 7,462,907             | AF01832US                 | United States | 11/07/2005  | 12/09/2008 | METHOD OF INCREASING ERASE SPEED IN MEMORY ARRAYS                                                     |
| 7,626,253             | AF01833US CIP             | United States | 08/30/2006  | 12/01/2009 | SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR                                                  |
| 7,859,096             | AF01833US DIV             | United States | 11/23/2009  | 12/28/2010 | SEMICONDUCTOR DEVICE                                                                                  |
| 8,330,263             | AF01833US DIV2            | United States | 12/10/2010  | 12/11/2012 | SEMICONDUCTOR DEVICE                                                                                  |
| 8,329,562             | AF01833US DIV3            | United States | 12/10/2010  | 12/11/2012 | METHODS OF MAKING A SEMICONDUCTOR DEVICE                                                              |
| 13/711,443            | AF01833US DIV4            | United States | 12/11/2012  |            | SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR                                                  |
| 7,470,614             | AF01834US                 | United States | 02/15/2006  | 12/30/2008 | METHODS FOR FABRICATING SEMICONDUCTOR DEVICES AND<br>CONTACTS TO SEMICONDUCTOR DEVICES                |
| 8,064,264             | AF01836US CIP             | United States | 10/11/2007  | 11/22/2011 | ORNAND FLASH MEMORY AND METHOD FOR CONTROLLING THE<br>SAME                                            |
| 7,902,590             | AF01839US                 | United States | 12/21/2007  | 03/08/2011 | SEMICONDUCTOR DEVICE, METHOD OF CONTROLLING THE SAME,<br>AND METHOD OF MANUFACTURING THE SAME         |
| 8,716,082             | AF01839US DIV             | United States | 01/24/2011  | 05/06/2014 | SEMICONDUCTOR DEVICE, METHOD OF CONTROLLING THE SAME,<br>AND METHOD OF MANUFACTURING THE SAME         |
| 14/222,399            | AF01839US DIV2            | United States | 03/21/2014  |            | SEMICONDUCTOR DEVICE, METHOD OF CONTROLLING THE SAME,<br>AND METHOD OF MANUFACTURING THE SAME         |
| 7,630,245             | AF01840US CIP             | United States | 10/04/2006  | 12/08/2009 | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREFOR                                                      |
| 7,416,940             | AF01842US                 | United States | 05/03/2006  | 08/26/2008 | METHODS FOR FABRICATING FLASH MEMEORY DEVICES                                                         |
| 7,910,980             | AF01843US                 | United States | 09/22/2008  | 03/22/2011 | SONOS DEVICE WITH INSULATING STORAGE LAYER AND P-N<br>JUNCTION ISOLATION                              |
| 7,534,732             | AF01844US                 | United States | 02/17/2006  | 05/19/2009 | SEMICONDUCTOR DEVICES WITH COPPER INTERCONNECTS AND<br>COMPOSITE SILICON NITRIDE CAPPING LAYERS       |
| 11/582,442            | AF01845US                 | United States | 10/18/2006  |            | CONFORMAL LINER FOR GAP-FILLING                                                                       |
| 7,355,904             | AF01849US                 | United States | 06/12/2006  | 04/08/2008 | METHOD AND APPARATUS FOR DRAIN PUM OPERATION                                                          |
| 11/423,649            | AF01850US                 | United States | 06/12/2006  |            | METHOD AND APPARATUS FOR DRAIN PUMP POWER CONSERVATION                                                |
| 7,108,535             | AF01852US                 | United States | 07/12/2005  | 09/19/2006 | INTEGRATED CIRCUIT TEST SOCKET                                                                        |
| 7,260,019             | AF01853US                 | United States | 10/31/2005  | 08/21/2007 | MEMORY ARRAY                                                                                          |
| 7,502,271             | AF01854US CIP             | United States | 04/25/2007  | 03/10/2009 | SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD                                                           |
| 7,639,543             | AF01860US CIP             | United States | 11/20/2007  | 12/29/2009 | NONVOLATILE MEMORY DEVICE                                                                             |
| 7,848,154             | AF01860US DIV             | United States | 12/29/2009  | 12/07/2010 | NONVOLATILE MEMORY DEVICE                                                                             |
| 7,468,909             | AF01862US CIP             | United States | 12/11/2006  | 12/23/2008 | SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE<br>SAME                                            |
| 8,018,767             | AF01862US DIV             | United States | 11/20/2008  | 09/13/2011 | SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE<br>SAME                                            |
| 8,325,523             | AF01862US DIV2            | United States | 08/01/2011  | 12/04/2012 | SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE<br>SAME                                            |
| 8,787,089             | AF01862US DIV3            | United States | 12/03/2012  | 07/22/2014 | SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE<br>SAME                                            |
| 11/359,122            | AF01863                   | United States | 02/21/2006  |            | METHOD FOR REGULATING VOLTAGE AND CIRCUIT THEREFOR                                                    |
| 11/551,535            | AF01867US                 | United States | 10/20/2006  |            | METHOD FOR MANUFACTURING A MEMORY DEVICE                                                              |
| 8,264,029             | AF01869US CIP             | United States | 12/17/2007  | 09/11/2012 | CONVEX SHAPED THIN-FILM TRANSISTOR DEVICE                                                             |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                            |
|-----------------------|--------------------------|---------------|-------------|------------|------------------------------------------------------------------------------------------------------------------|
| 8,691,645             | AF01869US DIV            | United States | 08/10/2012  | 04/08/2014 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME                                                        |
| 14/215,468            | AF01869US DIV CON        | United States | 03/17/2014  |            | METHOD OF MANUFACTURING CONVEX SHAPED THIN-FILM TRANSISTOR DEVICE HAVING ELONGATED CHANNEL OVER INSULATING LAYER |
| 7,908,025             | AF01870US CIP            | United States | 12/06/2006  | 03/15/2011 | REAL-TIME EQUIPMENT CONTROL TO MAINTAIN YIELD                                                                    |
| 8,577,494             | AF01870US CIP DIV        | United States | 02/03/2011  | 11/05/2013 | SEMICONDUCTOR MANUFACTURING APPARATUS AND CONTROL SYSTEM AND CONTROL METHOD THEREFOR                             |
| 8,531,019             | AF01872US                | United States | 12/20/2007  | 09/10/2013 | HEAT DISSIPATION METHODS AND STRUCTURES FOR SEMICONDUCTOR DEVICE                                                 |
| 8,759,157             | AF01872US DIV            | United States | 08/13/2013  | 06/24/2014 | HEAT DISSIPATION METHODS AND STRUCTURES FOR SEMICONDUCTOR DEVICE                                                 |
| 8,749,012             | AF01873US                | United States | 12/20/2007  | 06/10/2014 | METHODS AND STRUCTURES FOR DISCHARGING PLASMA FORMED DURING THE FABRICATION OF SEMICONDUCTOR DEVICE              |
| 8,819,326             | AF01875US                | United States | 12/12/2006  | 08/26/2014 | A HOST/CLIENT SYSTEM HAVING A SCALABLE SERIAL BUS INTERFACE                                                      |
| 14/453,306            | AF01875US DIV            | United States | 08/06/2014  |            | HOST/CLIENT SYSTEM HAVING A SCALABLE SERIAL BUS INTERFACE                                                        |
| 60/869,723            | AF01876                  | United States | 12/12/2006  |            | REPROGRAMMABLE READ-ONLY-TYPE MEMORY SYSTEM                                                                      |
| 60/869,724            | AF01877                  | United States | 12/12/2006  |            | DEDICATED REPROGRAMMABLE READ-ONLY-TYPE MEMORY SYSTEM                                                            |
| 60/869,725            | AF01878                  | United States | 12/12/2006  |            | COMPUTER SYSTEM FOR AUTOMATED PROGRAMMING OF MEMORY SYSTEMS                                                      |
| 7,847,340             | AF01879US                | United States | 12/21/2007  | 12/07/2010 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME                                                       |
| 12/126,600            | AF01881US                | United States | 05/23/2008  |            | METHOD FOR BALL GRID ARRAY (BGA) SOLDER ATTACH FOR SURFACE MOUNT                                                 |
| 7,940,563             | AF01882US                | United States | 04/24/2008  | 05/10/2011 | NONVOLATILE STORAGE DEVICE AND BIAS CONTROL METHOD THEREOF                                                       |
| 7,378,836             | AF01886US                | United States | 06/19/2006  | 05/27/2008 | AUTOMATED LOADING/UNLOADING OF DEVICES FOR BURN-IN TESTING                                                       |
| 13/538,646            | AF01886US CON            | United States | 06/29/2012  |            | AUTOMATED LOADING/UNLOADING OF DEVICES FOR BURN-IN TESTING                                                       |
| 7,567,076             | AF01886US DIV            | United States | 03/25/2008  | 07/28/2009 | AUTOMATED LOADING/UNLOADING OF DEVICES FOR BURN-IN TESTING                                                       |
| 8,228,082             | AF01886US DIV2           | United States | 06/26/2009  | 07/24/2012 | AUTOMATED LOADING/UNLOADING OF DEVICES FOR BURN-IN TESTING                                                       |
| 8,105,098             | AF01886US DIV3           | United States | 06/26/2009  | 01/31/2012 | AUTOMATED LOADING/UNLOADING OF DEVICES FOR BURN-IN TESTING                                                       |
| 60/766,316            | AF01886US PROV           | United States | 01/10/2006  |            | AUTOMATED LOADING/UNLOADING OF DEVICES FOR BURN-IN TESTING                                                       |
| 7,892,984             | AF01887US                | United States | 12/20/2007  | 02/22/2011 | REDUCTION OF DEFECTS FORMED ON THE SURFACE OF A SILICON OXYNITRIDE FILM                                          |
| 8,158,534             | AF01887US DIV            | United States | 02/22/2011  | 04/17/2012 | REDUCTION OF DEFECTS FORMED ON THE SURFACE OF A SILICON OXYNITRIDE FILM                                          |
| 7,895,406             | AF01889US CIP            | United States | 11/20/2007  | 02/22/2011 | MEMORY DEVICE AND PASSWORD STORING METHOD THEREOF                                                                |
| 12/005,870            | AF01890US                | United States | 12/28/2007  |            | PACKAGE-ON-PACKAGE SEMICONDUCTOR DEVICE                                                                          |
| 8,637,997             | AF01891US CIP            | United States | 11/20/2007  | 01/28/2014 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME                                                        |
| 14/109,464            | AF01891US DIV            | United States | 12/17/2013  |            | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME                                                        |
| 7,619,934             | AF01893US                | United States | 12/20/2006  | 11/17/2009 | METHOD AND APPARTATUS FOR ADAPTIVE MEMORY CELL OVERERASE COMPENSATION                                            |
| 7,929,353             | AF01893US DIV            | United States | 10/06/2009  | 04/19/2011 | METHOD AND APPARTATUS FOR ADAPTIVE MEMORY CELL OVERERASE COMPENSATION                                            |
| 7,660,148             | AF01894US                | United States | 04/01/2008  | 02/09/2010 | NONVOLATILE MEMORY DEVICE AND METHOD TO CONTROL THE SAME                                                         |
| 7,566,978             | AF01895US CIP            | United States | 01/17/2007  | 07/28/2009 | SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD                                                                      |
| 8,772,953             | AF01895US CON            | United States | 03/13/2009  | 07/08/2014 | SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD                                                                      |
| 7,834,470             | AF01895US DIV            | United States | 06/24/2009  | 11/16/2010 | SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD                                                                      |
| 8,530,282             | AF01895US DIV CON        | United States | 10/07/2010  | 09/10/2013 | SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD                                                                      |
| 8,900,923             | AF01895US DIV CON2       | United States | 08/16/2013  | 12/02/2014 | SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD                                                                      |
| 7,643,371             | AF01897US CIP            | United States | 11/20/2007  | 01/05/2010 | SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME                                                          |
| 8,598,717             | AF01898US                | United States | 12/21/2007  | 12/03/2013 | SEMICONDUCTOR DEVICE AN METHOD FOR MANUFACTURING THE SAME                                                        |
| 8,765,529             | AF01898US DIV            | United States | 10/30/2013  | 07/01/2014 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME                                                       |
| 7,644,226             | AF01899US                | United States | 12/19/2006  | 01/05/2010 | SYSTEM AND METHOD FOR MAINTAINING RAM COMMAND TIMING ACROSS PHASE-SHIFTED TIME DOMAINS                           |
| 7,565,477             | AF01900US                | United States | 12/22/2006  | 07/21/2009 | SEMICONDUCTOR DEVICE AND METHOD FOR CONTROLLING THE SAME                                                         |
| 7,574,576             | AF01902US                | United States | 12/22/2006  | 08/11/2009 | SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME                                                          |
| 12/026,421            | AF01903US                | United States | 02/05/2008  |            | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME                                                       |
| 7,626,882             | AF01905US                | United States | 12/20/2006  | 12/01/2009 | FLASH MEMORY DEVICE WITH EXTERNAL HIGH VOLTAGE SUPPLY                                                            |
| 8,357,965             | AF01906US                | United States | 12/28/2007  | 01/22/2013 | SEMICONDUCTOR DEVICE HAVING MULTIPLE STORAGE REGIONS                                                             |
| 7,404,026             | AF01907US                | United States | 04/10/2006  | 07/22/2008 | MULTI MEDIA CARD WITH HIGH STORAGE CAPACITY                                                                      |
| 7,605,457             | AF01908US CIP            | United States | 12/07/2006  | 10/20/2009 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME                                                        |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                  |
|-----------------------|---------------------------|---------------|-------------|------------|--------------------------------------------------------------------------------------------------------|
| 8,030,179             | AF01908US DIV             | United States | 09/09/2009  | 10/04/2011 | SEMICONDUCTOR DIVICE AND METHOD OF MANUFACTURING THE SAME                                              |
| 13/252,714            | AF01908US DIV2            | United States | 10/04/2011  |            | SEMICONDUCTOR DIVICE AND METHOD OF MANUFACTURING THE SAME                                              |
| 7,355,886             | AF01910US                 | United States | 12/05/2006  | 04/08/2008 | METHOD OF PROGRAMMING, ERASING AND READING MEMORY CELLS IN A RESISTIVE MEMORY ARRAY                    |
| 7,916,523             | AF01911US                 | United States | 12/05/2006  | 03/29/2011 | METHOD OF ERASING A RESISTIVE MEMORY DEVICE                                                            |
| 8,077,495             | AF01912US                 | United States | 12/05/2006  | 12/13/2011 | METHOD OF PROGRAMMING, ERASING AND REPAIRING A MEMORY DEVICE                                           |
| 8,482,959             | AF01912US DIV             | United States | 12/13/2011  | 07/09/2013 | METHOD OF PROGRAMMING, ERASING AND REPAIRING A MEMORY DEVICE                                           |
| 7,564,708             | AF01916US                 | United States | 12/05/2006  | 07/21/2009 | METHOD OF PROGRAMMING MEMORY DEVICE                                                                    |
| 11/521,205            | AF01923US                 | United States | 09/14/2006  |            | METHOD OF FORMING INSULATING LAYER IN A METAL-INSULATOR-METAL MEMORY DEVICE                            |
| 8,791,018             | AF01925US                 | United States | 12/19/2006  | 07/29/2014 | METHOD OF DEPOSITING COPPER USING PHYSICAL VAPOR DEPOSITION                                            |
| 14/313,751            | AF01925US DIV             | United States | 06/24/2014  |            | METHOD OF DEPOSITING COPPER USING PHYSICAL VAPOR DEPOSITION                                            |
| 14/315,003            | AF01925US DIV2            | United States | 06/25/2014  |            | METHOD OF DEPOSITING COPPER USING PHYSICAL VAPOR DEPOSITION                                            |
| 7,790,497             | AF01926US                 | United States | 12/20/2007  | 09/07/2010 | METHOD TO PREVENT ALLOY FORMATION WHEN FORMING LAYERED METAL OXIDES BY METAL OXIDATION                 |
| 6,542,403             | AF01927US                 | United States | 02/08/2001  | 04/01/2003 | PIGGYBACK PROGRAMMING USING VOLTAGE CONTROL FOR MULTI-LEVEL CELL FLASH MEMORY DESIGNS                  |
| 8,373,148             | AF01929US                 | United States | 04/26/2007  | 02/12/2013 | MEMORY DEVICE WITH IMPROVED PERFORMANCE                                                                |
| 8,093,680             | AF01930US                 | United States | 09/14/2006  | 01/10/2012 | METAL-INSULATOR-METAL-INSULATOR-METAL (MIM) MEMORY DEVICE                                              |
| 8,717,803             | AF01930US DIV             | United States | 12/09/2011  | 05/06/2014 | METAL-INSULATOR-METAL-INSULATOR-METAL (MIM) MEMORY DEVICE                                              |
| 8,093,698             | AF01935US                 | United States | 12/05/2006  | 01/10/2012 | GETTERING/STOP LAYER FOR PREVENTION OF REDUCTION OF INSULATING OXIDE IN A METAL-INSULATOR-METAL DEVICE |
| 8,035,099             | AF01936US                 | United States | 02/27/2008  | 10/11/2011 | DIODE AND RESISTIVE MEMORY DEVICE STRUCTURES                                                           |
| 8,803,120             | AF01936US DIV             | United States | 10/11/2011  | 08/12/2014 | DIODE AND RESISTIVE MEMORY DEVICE STRUCTURES                                                           |
| 8,089,113             | AF01937US                 | United States | 12/05/2006  | 01/03/2012 | DAMASCENE METAL-INSULATOR-METAL (MIM) DEVICE                                                           |
| 8,232,175             | AF01938US                 | United States | 09/14/2006  | 07/31/2012 | DAMASCENE METAL-INSULATOR-METAL (MIM) DEVICE WITH IMPROVED SCALEABILITY                                |
| 13/529,284            | AF01938US DIV             | United States | 06/21/2012  |            | DAMASCENE METAL-INSULATOR-METAL (MIM) DEVICE WITH IMPROVED SCALEABILITY                                |
| 7,468,525             | AF01941US                 | United States | 12/05/2006  | 12/23/2008 | TEST STRUCTURES FOR DEVELOPMENT OF METAL-INSULATOR-METAL (MIM) DEVICES                                 |
| 8,084,770             | AF01941US DIV             | United States | 11/17/2008  | 12/27/2011 | TEST STRUCTURES FOR DEVELOPMENT OF METAL-INSULATOR-METAL (MIM) DEVICES                                 |
| 7,894,243             | AF01944US                 | United States | 12/05/2006  | 02/22/2011 | METHODS OF PROGRARMING AND ERASING RESISTIVE MEMORY DEVICES                                            |
| 7,495,951             | AF01946US                 | United States | 04/27/2006  | 02/24/2009 | RESISTIVE MEMORY CELL ARRAY WITH COMMON PLATE                                                          |
| 7,839,671             | AF01946US DIV             | United States | 10/28/2008  | 11/23/2010 | RESISTIVE MEMORY CELL ARRAY WITH COMMON PLATE                                                          |
| 7,450,419             | AF01949US CIP             | United States | 12/07/2006  | 11/11/2008 | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREFOR                                                       |
| 7,968,990             | AF01953US CIP             | United States | 01/17/2007  | 06/28/2011 | SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME                                                |
| 7,692,253             | AF01954US                 | United States | 04/27/2006  | 04/06/2010 | MEMORY CELL ARRAY WITH LOW RESISTANCE COMMON SOURCE AND HIGH CURRENT DRIVABILITY                       |
| 8,008,645             | AF01954US DIV1            | United States | 11/13/2007  | 08/30/2011 | MEMORY CELL ARRAY WITH LOW RESISTANCE COMMON SOURCE AND HIGH CURRENT DRIVABILITY                       |
| 7,724,563             | AF01954US DIV2            | United States | 11/13/2007  | 05/25/2010 | MEMORY CELL ARRAY WITH LOW RESISTANCE COMMON SOURCE AND HIGH CURRENT DRIVABILITY                       |
| 7,319,615             | AF01955US                 | United States | 08/02/2006  | 01/15/2008 | RAMP GATE ERASE FOR DUAL BIT FLASH MEMORY                                                              |
| 7,671,405             | AF01957US                 | United States | 12/26/2006  | 03/02/2010 | DEEP BITLINE IMPLANT TO AVOID PROGRAM DISTURB                                                          |
| 7,561,471             | AF01961US                 | United States | 03/16/2007  | 07/14/2009 | CYCLING IMPROVEMENT USING HIGHER ERASE BIAS                                                            |
| 60/877,192            | AF01961US                 | United States | 12/26/2006  |            | CYCLING IMPROVEMENT USING HIGHER ERASE BIAS                                                            |
| 7,888,218             | AF01964US                 | United States | 03/16/2007  | 02/15/2011 | USING THICK SPACER FOR BITLINE IMPLANT THEN REMOVE                                                     |
| 60/876,181            | AF01964US                 | United States | 12/20/2006  |            | USE THICK SPACER FOR BL IMPLANT THEN REMOVE                                                            |
| 11/634,777            | AF01965US                 | United States | 12/06/2006  |            | BARRIER REGION FOR MEMORY DEVICES                                                                      |
| 7,713,875             | AF01974US                 | United States | 05/14/2007  | 05/11/2010 | VARIABLE SALICIDE BLOCK FOR RESISTANCE EQUALIZATION IN AN ARRAY                                        |
| 60/875,905            | AF01974US                 | United States | 12/20/2006  |            | VARIABLE SALICIDE BLOCK FOR RESISTANCE EQUALIZATION IN AN ARRAY                                        |
| 7,977,218             | AF01975US                 | United States | 12/26/2006  | 07/12/2011 | THIN OXIDE DUMMY TILING AS CHARGE PROTECTION                                                           |
| 7,553,727             | AF01976US                 | United States | 03/16/2007  | 06/30/2009 | USING IMPLANTED POLY-I TO IMPROVE CHARGING PROTECTION IN DUAL-POLY PROCESS                             |
| 60/876,180            | AF01976US                 | United States | 12/20/2006  |            | USING IMPLANTED POLY-I TO IMPROVE CHARGING PROTECTION IN DUAL-POLY PROCESS                             |
| 11/724,725            | AF01978US                 | United States | 03/16/2007  |            | DIELECTRIC EXTENSION TO MITIGATE SHORT CHANNEL EFFECTS                                                 |
| 60/877,300            | AF01978US PROV            | United States | 12/27/2006  |            | DIELECTRIC EXTENSION TO MITIGATE SHORT CHANNEL EFFECTS                                                 |
| 7,696,094             | AF01982US                 | United States | 12/27/2006  | 04/13/2010 | METHOD FOR IMPROVED PLANARIZATION IN SEMICONDUCTOR DEVICES                                             |
| 7,829,464             | AF01988US                 | United States | 10/20/2006  | 11/09/2010 | PLANARIZATION METHOD USING OXIDE AND POLYSILICON CMP                                                   |
| 7,972,962             | AF01988US CON             | United States | 09/21/2010  | 07/05/2011 | PLANARIZATION METHOD USING HYBRID OXIDE AND POLYSILICON CMP                                            |
| 8,415,734             | AF01989US                 | United States | 12/07/2006  | 04/09/2013 | MEMORY DEVICE PROTECTION LAYER                                                                         |
| 13/858,229            | AF01989US DIV             | United States | 04/08/2013  |            | MEMORY DEVICE PROTECTION LAYER                                                                         |
| 7,670,959             | AF01990US                 | United States | 12/26/2006  | 03/02/2010 | MEORY DEVICE ETCH METHODS                                                                              |
| 7,972,951             | AF01990US CON             | United States | 01/15/2010  | 07/05/2011 | MEORY DEVICE ETCH METHODS                                                                              |
| 11/461,998            | AF02039US                 | United States | 08/02/2006  |            | MEMORY CELL SYSTEM WITH NITRIDE CHARGE ISOLATION                                                       |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                     |
|-----------------------|---------------------------|---------------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------|
| 11/462,009            | AF02040US                 | United States | 08/02/2006  |            | MEMORY CELL SYSTEM WITH GRADIENT CHARGE ISOLATION                                                                         |
| 8,587,049             | AF02041US                 | United States | 07/17/2006  | 11/19/2013 | MEMORY CELL SYSTEM WITH CHARGE TRAP                                                                                       |
| 14/076,415            | AF02041US DIV             | United States | 11/11/2013  |            | MEMORY DEVICE WITH CHARGE TRAP                                                                                            |
| 8,143,661             | AF02042US                 | United States | 10/10/2006  | 03/27/2012 | MEMORY CELL SYSTEM WITH CHARGE TRAP                                                                                       |
| 8,809,936             | AF02044US                 | United States | 07/31/2006  | 08/19/2014 | MEMORY CELL SYSTEM WITH MULTIPLE NITRIDE LAYERS                                                                           |
| 11/958,646            | AF02049US                 | United States | 12/18/2007  |            | INTEGRATED CIRCUIT SYSTEM WITH MEMORY SYSTEM                                                                              |
| 60/871,432            | AF02049US PROV            | United States | 12/21/2006  |            | INTEGRATED CIRCUIT SYSTEM WITH MEMORY SYSTEM                                                                              |
| 8,283,718             | AF02052US                 | United States | 12/16/2006  | 10/09/2012 | INTEGRATED CIRCUIT SYSTEM WITH METAL AND SEMI-CONDUCTING GATE                                                             |
| 8,815,727             | AF02052US DIV             | United States | 10/04/2012  | 08/26/2014 | INTEGRATED CIRCUIT WITH METAL AND SEMI-CONDUCTING GATE                                                                    |
| 11/611,860            | AF02053US                 | United States | 12/16/2006  |            | INTEGRATED CIRCUIT SYSTEM WITH IMPLANT OXIDE                                                                              |
| 8,119,477             | AF02054US                 | United States | 08/31/2006  | 02/21/2012 | MEMORY SYSTEM WITH PROTECTION LAYER                                                                                       |
| 8,114,736             | AF02055US                 | United States | 12/17/2007  | 02/14/2012 | INTEGRATED CIRCUIT SYSTEM WITH MEMORY SYSTEM                                                                              |
| 60/871,434            | AF02055US PROV            | United States | 12/21/2006  |            | INTEGRATED CIRCUIT SYSTEM WITH MEMORY SYSTEM                                                                              |
| 11/735,229            | AF02056                   | United States | 04/13/2007  |            | INTEGRATED CIRCUIT SYSTEM WITH MEMORY SYSTEM                                                                              |
| 60/871,436            | AF02056US                 | United States | 12/21/2006  |            | INTEGRATED CIRCUIT SYSTEM WITH MEMORY SYSTEM                                                                              |
| 8,785,268             | AF02057US                 | United States | 12/21/2006  | 07/22/2014 | MEMORY SYSTEM WITH FIN FET TECHNOLOGY                                                                                     |
| 11/694,089            | AF02059                   | United States | 03/30/2007  |            | MEMORY SYSTEM WITH DEPLETION GATE                                                                                         |
| 60/871,431            | AF02059                   | United States | 12/21/2006  |            | MEMORY SYSTEM WITH DEPLETION GATE                                                                                         |
| 11/614,839            | AF02060                   | United States | 12/21/2006  |            | MEMORY SYSTEM WITH SELECT GATE ERASE                                                                                      |
| 11/735,241            | AF02062US                 | United States | 04/13/2007  |            | MEMORY SYSTEM WITH POLY METAL GATE                                                                                        |
| 60/871,421            | AF02062US PROV            | United States | 12/21/2006  |            | MEMORY SYSTEM WITH POLY METAL GATE                                                                                        |
| 7,443,712             | AF02067US                 | United States | 09/07/2006  | 10/28/2008 | MEMORY ERASE MANAGEMENT SYSTEM                                                                                            |
| 8,014,199             | AF02071US                 | United States | 05/22/2006  | 09/06/2011 | MEMORY SYSTEM WITH SWITCH ELEMENT                                                                                         |
| 7,781,806             | AF02073US                 | United States | 04/18/2008  | 08/24/2010 | OPTICAL ERASE MEMORY STRUCTURE                                                                                            |
| 8,895,405             | AF02075US                 | United States | 12/21/2007  | 11/25/2014 | METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE                                                                           |
| 14/184,191            | AF02075US CON             | United States | 02/19/2014  |            | METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE                                                                           |
| 7,808,830             | AF02076US                 | United States | 02/05/2008  | 10/05/2010 | SEMICONDUCTOR DEVICE AND METHOD FOR ADJUSTING REFERENCE LEVELS OF REFERENCE CELLS                                         |
| 8,031,527             | AF02076US CON             | United States | 08/30/2010  | 10/04/2011 | SEMICONDUCTOR DEVICE AND METHOD FOR ADJUSTING REFERENCE LEVELS OF REFERENCE CELLS                                         |
| 12/180,306            | AF02077US                 | United States | 07/25/2008  |            | MIRRORBIT DEVICE HAVING THE CHARGE STORAGE REGION ON BOTH SIDES OF ONE WORD LINE                                          |
| 8,801,895             | AF02078US                 | United States | 02/05/2008  | 08/12/2014 | SEMICONDUCTOR MANUFACTURING EQUIPMENT AND MANUFACTURING METHOD OF THE SAME                                                |
| 12/039,511            | AF02080US                 | United States | 02/28/2008  |            | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME                                                                |
| 8,202,790             | AF02081US                 | United States | 02/05/2008  | 06/19/2012 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME                                                                 |
| 13/526,321            | AF02081US DIV             | United States | 06/18/2012  |            | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME                                                                 |
| 8,143,664             | AF02083US CIP             | United States | 02/27/2007  | 03/27/2012 | MIRROR BIT MEMORY DEVICE HAVING BOTH PSG SPACER AND SILICIDE LAYER ON THE BIT LINE                                        |
| 8,536,638             | AF02083US DIV             | United States | 12/14/2011  | 09/17/2013 | METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE HAVING LOWER LEAKAGE CURRENT BETWEEN SEMICONDUCTOR SUBSTRATE AND BIT LINES |
| 7,901,954             | AF02084US                 | United States | 09/29/2008  | 03/08/2011 | METHOD FOR DETECTING A VOID                                                                                               |
| 8,344,510             | AF02084US DIV             | United States | 03/08/2011  | 01/01/2013 | SEMICONDUCTOR DEVICE WITH VOID DETECTION MONITOR                                                                          |
| 7,825,448             | AF02085US                 | United States | 08/15/2008  | 11/02/2010 | U-SHAPED SONOS MEMORY HAVING AN ELEVATED SOURCE AND DRAIN                                                                 |
| 7,633,824             | AF02086US                 | United States | 02/01/2008  | 12/15/2009 | CHARGE PUMP TO SUPPLY VOLTAGE BANDS                                                                                       |
| 8,815,652             | AF02087US                 | United States | 05/30/2008  | 08/26/2014 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME AND SEMICONDUCTOR MANUFACTURING DEVICE                          |
| 8,445,966             | AF02088US                 | United States | 12/20/2006  | 05/21/2013 | METHOD AND APPARATUS FOR PROTECTION AGAINST PROCESS-INDUCED CHARGING                                                      |
| 13/866,915            | AF02088US DIV             | United States | 04/19/2013  |            | METHOD AND APPARATUS FOR PROTECTION AGAINST PROCESS-INDUCED CHARGING                                                      |
| 11/529,166            | AF02089US                 | United States | 09/28/2006  |            | FLASH MEMORY CELL STRUCTURE FOR INCREASED PROGRAM SPEED AND ERASE SPEED                                                   |
| 7,384,800             | AF02090US                 | United States | 12/05/2006  | 06/10/2008 | METHOD OF FABRICATING METAL-INSULATOR-METAL (MIM) DEVICE WITH STABLE DATA RETENTION                                       |
| 7,902,056             | AF02093US                 | United States | 08/20/2008  | 03/08/2011 | PLASMA TREATED METAL SILICIDE LAYER FORMATION                                                                             |
| 7,846,780             | AF02096US                 | United States | 02/01/2008  | 12/07/2010 | FLIP-CHIP PACKAGE COVERED WITH TAPE                                                                                       |
| 12/962,479            | AF02096US DIV             | United States | 12/07/2010  |            | FLIP-CHIP PACKAGE COVERED WITH TAPE                                                                                       |
| 12/032,444            | AF02097US                 | United States | 02/15/2008  |            | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME                                                                |
| 8,230,154             | AF02100US                 | United States | 01/19/2007  | 07/24/2012 | FULLY ASSOCIATIVE BANKING FOR MEMORY                                                                                      |
| 8,239,637             | AF02101US                 | United States | 01/19/2007  | 08/07/2012 | BYTE MASK COMMAND FOR MEMORIES                                                                                            |
| 12/049,089            | AF02102US                 | United States | 03/14/2008  |            | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THEREOF                                                                 |
| 14/628,939            | AF02102US DIV             | United States | 02/23/2015  |            | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THEREOF                                                                 |
| 8,076,206             | AF02103US                 | United States | 08/18/2008  | 12/13/2011 | METHOD FOR MANUFACTURING SONOS FLASH MEMORY                                                                               |
| 13/275,989            | AF02103US CIP             | United States | 10/18/2011  |            | SONOS FLASH MEMORY DEVICE                                                                                                 |
| 8,110,412             | AF02109US                 | United States | 12/22/2006  | 02/07/2012 | INTEGRATED CIRCUIT WAFER SYSTEM WITH CONTROL STRATEGY                                                                     |
| 7,432,156             | AF02113US                 | United States | 04/21/2006  | 10/07/2008 | MEMORY DEVICE AND METHODS FOR ITS FABRICATION                                                                             |
| 7,564,091             | AF02113US DIV             | United States | 08/27/2008  | 07/21/2009 | MEMORY DEVICE AND METHODS FOR ITS FABRICATION                                                                             |
| 7,767,517             | AF02117US                 | United States | 12/20/2006  | 08/03/2010 | A SEMICONDUCTOR MEMORY COMPRISING DUAL CHARGE STORAGE NODES AND METHODS FOR ITS FABRICATION                               |
| 8,076,712             | AF02117US DIV             | United States | 07/20/2010  | 12/13/2011 | SEMICONDUCTOR MEMORY COMPRISING DUAL CHARGE STORAGE NODES AND METHODS FOR ITS FABRICATION                                 |
| 7,915,123             | AF02118US                 | United States | 04/20/2006  | 03/29/2011 | DUAL CHARGE STORAGE NODE MEMORY DEVICE AND METHODS FOR FABRICATING SUCH DEVICE                                            |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                        |
|-----------------------|--------------------------|---------------|-------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| 8,183,623             | AF02118US DIV            | United States | 03/29/2011  | 05/22/2012 | DUAL CHARGE STORAGE NODE MEMORY DEVICE AND METHODS FOR FABRICATING SUCH DEVICE                                                               |
| 7,732,281             | AF02119US                | United States | 04/24/2006  | 06/08/2010 | METHODS FOR FABRICATING DUAL BIT FLASH MEMORY DEVICES                                                                                        |
| 7,867,848             | AF02119US DIV            | United States | 04/22/2010  | 01/11/2011 | METHODS FOR FABRICATING DUAL BIT FLASH MEMORY DEVICES                                                                                        |
| 7,666,739             | AF02120US                | United States | 12/20/2006  | 02/23/2010 | METHODS FOR FABRICATING A SPLIT CHARGE STORAGE NODE SEMICONDUCTOR MEMORY                                                                     |
| 7,368,347             | AF02121US                | United States | 10/03/2006  | 05/06/2008 | DUAL BIT FLASH MEMORY DEVICES AND METHODS FOR FABRICATING THE SAME                                                                           |
| 7,705,390             | AF02121US DIV            | United States | 03/24/2008  | 04/27/2010 | DUAL BIT FLASH MEMORY DEVICES AND METHODS FOR FABRICATING THE SAME                                                                           |
| 7,622,389             | AF02122US                | United States | 04/25/2006  | 11/24/2009 | SELECTIVE CONTACT FORMATION USING MASKING AND RESIST PATTERNING                                                                              |
| 7,687,360             | AF02124US                | United States | 12/22/2006  | 03/30/2010 | SEMICONDUCTOR MEMORY DEVICES AND METHODS FOR FABRICATING THE SAME                                                                            |
| 12/696,409            | AF02124US DIV            | United States | 01/29/2010  |            | SEMICONDUCTOR MEMORY DEVICES AND METHODS FOR FABRICATING THE SAME                                                                            |
| 7,785,965             | AF02127US                | United States | 09/08/2006  | 08/31/2010 | DUAL STORAGE NODE MEMORY DEVICES AND METHODS FOR FABRICATING THE SAME                                                                        |
| 11/615,425            | AF02129US                | United States | 12/22/2006  |            | FLASH MEMORY DEVICES AND METHODS FOR FABRICATING THE SAME                                                                                    |
| 8,486,782             | AF02131US                | United States | 12/22/2006  | 07/16/2013 | FLASH MEMORY DEVICES AND METHODS FOR FABRICATING THE SAME                                                                                    |
| 8,748,972             | AF02131US DIV            | United States | 06/18/2013  | 06/10/2014 | FLASH MEMORY DEVICES AND METHODS FOR FABRICATING THE SAME                                                                                    |
| 7,635,627             | AF02132US                | United States | 12/20/2006  | 12/22/2009 | METHODS FOR FABRICATING A MEMORY DEVICE INCLUDING A DUAL BIT MEMORY CELL                                                                     |
| 7,696,038             | AF02133US                | United States | 04/26/2006  | 04/13/2010 | METHODS FOR FABRICATING FLASH MEMORY DEVICES                                                                                                 |
| 7,385,851             | AF02134US                | United States | 12/22/2006  | 06/10/2008 | REPETITIVE ERASE VERIFY TECHNIQUE FOR FLASH MEMORY DEVICES                                                                                   |
| 7,463,525             | AF02135US                | United States | 12/22/2006  | 12/09/2008 | NEGATIVE WORDLINE BIAS FOR REDUCTION OF LEAKAGE CURRENT DURING FLASH MEMORY OPERATION                                                        |
| 7,489,560             | AF02136US                | United States | 04/05/2006  | 02/10/2009 | REDUCTION OF LEAKAGE CURRENT AND PROGRAM DISTURBS IN FLASH MEMORY DEVICES                                                                    |
| 7,394,702             | AF02137US                | United States | 04/05/2006  | 07/01/2008 | METHODS FOR ERASING AND PROGRAMMING MEMORY DEVICES                                                                                           |
| 11/399,158            | AF02138US                | United States | 04/06/2006  |            | METHODS FOR ERASING MEMORY DEVICES AND MULTI-LEVEL PROGRAMMING MEMORY DEVICE                                                                 |
| 7,778,088             | AF02139US                | United States | 12/19/2006  | 08/17/2010 | ERASING FLASH MEMORY USING ADAPTIVE DRAIN AND/OR GATE BIAS                                                                                   |
| 8,144,522             | AF02139US CON            | United States | 07/06/2010  | 03/27/2012 | ERASING FLASH MEMORY USING ADAPTIVE DRAIN AND/OR GATE BIAS                                                                                   |
| 7,382,650             | AF02140US                | United States | 10/03/2006  | 06/03/2008 | METHOD AND APPARATUS FOR SECTOR ERASE OPERATION IN A FLASH MEMORY ARRAY                                                                      |
| 7,948,052             | AF02141US                | United States | 12/18/2006  | 05/24/2011 | DUAL-BIT MEMORY DEVICE HAVING TRENCH ISOLATION MATERIAL DISPOSED NEAR BIT LINE CONTACT AREAS                                                 |
| 7,622,373             | AF02144US                | United States | 12/22/2006  | 11/24/2009 | MEMORY DEVICE HAVING IMPLANTED OXIDE TO BLOCK ELECTRON DRIFT, AND METHOD OF MANUFACTURING THE SAME                                           |
| 8,076,715             | AF02145US                | United States | 12/27/2006  | 12/13/2011 | DUAL-BIT MEMORY DEVICE HAVING ISOLATION MATERIAL DISPOSED UNDERNEATH A BIT LINE SHARED BY ADJACENT DUAL-BIT MEMORY CELLS                     |
| 7,630,253             | AF02146US                | United States | 04/05/2006  | 12/08/2009 | FLASH MEMORY PROGRAMMING AND VERIFICATION WIHT REDUCED LEAKAGE CURRENT                                                                       |
| 8,031,528             | AF02146US DIV1           | United States | 09/11/2009  | 10/04/2011 | FLASH MEMORY PROGRAMMING AND VERIFICATION WITH REDUCED LEAKAGE CURRENT                                                                       |
| 8,064,262             | AF02148US                | United States | 09/18/2008  | 11/22/2011 | SEMICONDUCTOR DEVICE AND METHOD USING STRESS INFORMATION                                                                                     |
| 11/616,384            | AF02149                  | United States | 12/27/2006  |            | METHOD TO ACHIEVE A LOW COST TRANSISTOR ISOLATION DIELECTRIC PROCESS MODULE WITH IMPROVED PROCESS CONTROL, PROCESS COST, AND YIELD POTENTIAL |
| 8,225,172             | AF02150US                | United States | 06/16/2008  | 07/17/2012 | ERROR CORRECTION SCHEME FOR NON-VOLATILE MEMORY                                                                                              |
| 8,438,460             | AF02150US DIV            | United States | 06/22/2012  | 05/07/2013 | ERROR CORRECTION SCHEME FOR NON-VOLATILE MEMORY                                                                                              |
| 8,769,377             | AF02150US DIV CON        | United States | 05/03/2013  | 07/01/2014 | ERROR CORRECTION SCHEME FOR NON-VOLATILE MEMORY                                                                                              |
| 11/829,135            | AF02152US                | United States | 07/27/2007  |            | FUEL CELL USING DEUTERIUM                                                                                                                    |
| 8,486,756             | AF02153US                | United States | 12/23/2008  | 07/16/2013 | FLIP CHIP PACKAGE WITH SHELF AND METHOD OF MANUFACTURING THE SAME                                                                            |
| 8,796,864             | AF02153US DIV            | United States | 06/14/2013  | 08/05/2014 | FLIP CHIP PACKAGE WITH SHELF AND METHOD OF MANUFACTURING THEREOF                                                                             |
| 7,871,896             | AF02155US                | United States | 06/05/2008  | 01/18/2011 | PRECISION TRENCH FORMATION THROUGH OXIDE REGION FORMATION FOR A SEMICONDUCTOR DEVICE                                                         |
| 8,354,326             | AF02155US DIV            | United States | 12/06/2010  | 01/15/2013 | PRECISION TRENCH FORMATION THROUGH OXIDE REGION FORMATION FOR A SEMICONDUCTOR DEVICE                                                         |
| 8,004,901             | AF02156US                | United States | 12/22/2008  | 08/23/2011 | METHOD OF INHIBITING FRINGE CURRENT IN MIRROR BITMEMORY DEVICE                                                                               |
| 8,537,622             | AF02156US CON            | United States | 08/23/2011  | 09/17/2013 | SEMICONDUCTOR DEVICE AND METHOD FOR CONTROLLING                                                                                              |
| 7,682,974             | AF02159US                | United States | 05/30/2008  | 03/23/2010 | METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE                                                                                                |
| 11/804,170            | AF02160US                | United States | 05/16/2007  |            | SELF REFERENCE SENSING SYSTEM AND METHOD                                                                                                     |
| 12/133,689            | AF02161US                | United States | 06/05/2008  |            | ULTRAVIOLET BLOCKING STRUCTURE AND METHOD FOR SEMICONDUCTOR DEVICE                                                                           |
| 7,791,946             | AF02162US                | United States | 07/01/2008  | 09/07/2010 | SEMICONDUCTOR DEVICE AND METHOD FOR CONTROLLING A SEMICONDUCTOR DEVICE                                                                       |
| 7,863,175             | AF02163US                | United States | 12/21/2006  | 01/04/2011 | ZERO INTERFACE POLYSILICON TO POLYSILICON GATE FOR FLASH MEMORY                                                                              |
| 8,564,042             | AF02164US                | United States | 02/05/2007  | 10/22/2013 | DUAL STORAGE NODE MEMORY                                                                                                                     |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                   |
|-----------------------|--------------------------|---------------|-------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 14/033,170            | AF02164US DIV            | United States | 09/20/2013  |            | DUAL STORAGE NODE MEMORY                                                                                                                |
| 60/765,227            | AF02164US PROV           | United States | 02/03/2006  |            | METHOD OF FABRICATING DUAL STORAGE NODES MEMORY USING SPACER MASKS                                                                      |
| 8,742,486             | AF02165US                | United States | 02/05/2007  | 06/03/2014 | FLASH MEMORY CELLS HAVING TRENCHED STORAGE ELEMENTS                                                                                     |
| 14/254,237            | AF02165US DIV            | United States | 04/16/2014  |            | FLASH MEMORY CELLS HAVING TRENCHED STORAGE ELEMENTS                                                                                     |
| 60/765,111            | AF02165US PROV           | United States | 02/04/2006  |            | APPARATUS AND METHOD FOR FABRICATING FLASH MEMORY CELLS HAVING TRENCHED STORAGE ELEMENTS                                                |
| 11/702,847            | AF02166US                | United States | 02/05/2007  |            | DUAL CHARGE STORAGE NODE WITH UNDERCUT GATE OXIDE FOR DEEP SUB-MICRON MEMORY CELL                                                       |
| 60/765,351            | AF02166US PROV           | United States | 02/04/2006  |            | PROCESS FOR FABRICATING DUAL CHARGE STORAGE NODE WITH UNDERCUT GATE OXIDE FOR DEEP SUB-MICRON MEMORY CELL AND RESULTING STRUCTURE       |
| 11/639,666            | AF02167US                | United States | 12/15/2006  |            | MEMORY CELLS HAVING SPLIT CHARGE STORAGE NODES AND METHODS FOR FABRICATING MEMORY CELLS HAVING SPLIT CHARGE STORAGE NODES               |
| 60/764,847            | AF02167US PROV           | United States | 02/04/2006  |            | APPARATUS AND METHOD FOR FABRICATING FLASH MEMORY VCELLS HAVING TRENCHED STORAGE ELEMENTS AND A PUNCH THROUGH BARRIER REGION            |
| 7,970,129             | AF02168US                | United States | 04/19/2007  | 06/28/2011 | SELECTION OF A LOOKUP TABLE WITH DATA MASKED WITH A COMBINATION OF AN ADDITIVE AND MULTIPLICATIVE MASK                                  |
| 8,705,731             | AF02168US CON            | United States | 05/19/2011  | 04/22/2014 | SELECTION OF A LOOKUP TABLE WITH DATA MASKED WITH A COMBINATION OF AN ADDITIVE AND MULTIPLICATIVE MASK                                  |
| 8,422,668             | AF02169US                | United States | 12/15/2006  | 04/16/2013 | TABLE LOOKUP OPERATION ON MASKED DATA                                                                                                   |
| 8,855,298             | AF02169US CON            | United States | 01/10/2013  | 10/07/2014 | TABLE LOOKUP OPERATION ON MASKED DATA                                                                                                   |
| 7,781,320             | AF02170US                | United States | 10/16/2008  | 08/24/2010 | FABRICATING METHOD OF ETCHING THE INTERLAYER INSULATING FILM BY CONSIDERING THE EXTINCTION COEFFICIENT                                  |
| 8,440,557             | AF02170US CON            | United States | 07/20/2010  | 05/14/2013 | METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE BY CONSIDERING THE EXTINCTION COEFFICIENT DURING ETCHING OF AN INTERLAYER INSULATING FILM |
| 5,950,086             | AF02173US                | United States | 06/18/1997  | 09/07/1999 | MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE                                                                                            |
| 09/573,965            | AF02175US                | United States | 05/19/2000  |            | NONVOLATILE MEMORY ALLOW ENCRYPTED                                                                                                      |
| 6,368,916             | AF02176US                | United States | 03/24/2000  | 04/09/2002 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                 |
| 6,670,669             | AF02177US                | United States | 02/28/2000  | 12/30/2003 | MULTI-LEVEL NONVOLATILE MEMORY USING                                                                                                    |
| 6,324,099             | AF02178US                | United States | 11/27/2000  | 11/27/2001 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                 |
| 6,750,520             | AF02180US CON            | United States | 05/30/2000  | 06/15/2004 | SEMICONDUCTOR MEMORY DEVICE AND METHOD OF MANUFACTURE THEREOF                                                                           |
| 6,574,149             | AF02181US CON            | United States | 03/15/2002  | 06/03/2003 | SEMICONDUCTOR MEMORY DEVICE AND USING                                                                                                   |
| 6,614,686             | AF02182US                | United States | 08/18/2000  | 09/02/2003 | NONVOLATILE MEMORY CIRCUIT FOR RECORDING MULTIPLE BIT INFORMATION                                                                       |
| 10/194,317            | AF02183US                | United States | 07/15/2002  |            | NONVOLATILE MEMORY                                                                                                                      |
| 7,057,229             | AF02184US                | United States | 01/14/2003  | 06/06/2006 | NONVOLATILE MEMORY DEVICE AND                                                                                                           |
| 7,462,529             | AF02184US DIV            | United States | 03/23/2006  | 12/09/2008 | NONVOLATILE MEMORY DEVICE AND                                                                                                           |
| 6,765,828             | AF02185US CON            | United States | 08/03/2000  | 07/20/2004 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                 |
| 7,102,928             | AF02186US                | United States | 06/29/2000  | 09/05/2006 | SEMICONDUCTOR MEMORY DEVICE                                                                                                             |
| 6,480,420             | AF02187US                | United States | 03/28/2001  | 11/12/2002 | SEMICONDUCTOR MEMORY DEVICE AND METHOD OF                                                                                               |
| 6,788,580             | AF02188US                | United States | 12/21/2000  | 09/07/2004 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                 |
| 6,468,861             | AF02189US                | United States | 12/18/2000  | 10/22/2002 | METHOD FOR MANUFACTURING NON-VOLATILE SEMICONDUCTOR MEMORY AND NON-VOLATILE SEMICONDUCTOR MEMORY MANUFACTURED THEREBY                   |
| 6,765,271             | AF02189US DIV            | United States | 09/10/2002  | 07/20/2004 | MANUFACTURING METHOD OF NONVOLATILE                                                                                                     |
| 6,496,414             | AF02190US                | United States | 01/14/2002  | 12/17/2002 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                                                        |
| 6,492,677             | AF02191US                | United States | 09/27/2001  | 12/10/2002 | NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE AND FABRICATION PROCESS THEREOF                                                                |
| 6,642,586             | AF02192US                | United States | 10/11/2001  | 11/04/2003 | SEMICONDUCTOR MEMORY CAPABLE OF BEING DRIVEN AT LOW VOLTAGE AND ITS MANUFACTURE METHOD                                                  |
| 6,927,133             | AF02192US DIV            | United States | 08/28/2003  | 08/09/2005 | SEMICONDUCTOR MEMORY CAPABLE OF BEING DRIVEN AT LOW VOLTAGE AND ITS MANUFACTURE METHOD                                                  |
| 6,950,343             | AF02193US                | United States | 05/25/2001  | 09/27/2005 | NONVOLATILE SEMICONDUCTOR DEVICE                                                                                                        |
| 6,574,139             | AF02194                  | United States | 01/18/2002  | 06/03/2003 | READ METHOD FOR DUAL BIT MEMORY CELL                                                                                                    |
| 60/300,916            | AF02194                  | United States | 06/20/2001  |            | READ METHOD FOR DUAL BIT MEMORY CELL                                                                                                    |
| 09/922,786            | AF02195                  | United States | 08/07/2001  |            | SEMICONDUCTOR DEVICE AND MANUFACTURING                                                                                                  |
| 7,084,037             | AF02195US DIV            | United States | 11/12/2004  | 08/01/2006 | SEMICONDUCTOR DEVICE AND MANUFACTURING                                                                                                  |
| 6,621,742             | AF02196US                | United States | 04/29/2002  | 09/16/2003 | SYSTEM FOR PROGRAMMING A FLASH MEMORY DEVICE                                                                                            |
| 6,594,181             | AF02197US                | United States | 05/10/2002  | 07/15/2003 | READ METHOD FOR TWO BIT MEMORY CELL A                                                                                                   |
| 6,559,500             | AF02198                  | United States | 08/13/2001  | 05/06/2003 | SEMICONDUCTOR MEMORY DEVICE AND DRIVING                                                                                                 |
| 6,735,127             | AF02198US DIV            | United States | 06/04/2002  | 05/11/2004 | SEMICONDUCTOR MEMORY DEVICE AND DRIVING                                                                                                 |
| 6,856,552             | AF02199US                | United States | 07/30/2002  | 02/15/2005 | SEMICONDUCTOR MEMORY DEVICE AND DRIVING                                                                                                 |
| 7,096,406             | AF02200US                | United States | 03/15/2002  | 08/22/2006 | MEMORY CONTROLLER FOR MULTI LEVEL                                                                                                       |
| 7,159,124             | AF02201US                | United States | 11/19/2002  | 01/02/2007 | NONVOLATILE SEMICONDUCTOR MEMORY WITH A FUNCTION FOR PREVENTING UNAUTHORIZED READING                                                    |
| 6,990,623             | AF02202US CIP            | United States | 05/16/2002  | 01/24/2006 | METHOD FOR ERROR DETECTION/CORRECTION OF MULTILEVEL CELL MEMORY AND MULTILEVEL CELL MEMORY HAVING ERROR DETECTION/CORRECTION FUNCTION   |
| 10/199,071            | AF02203US                | United States | 07/22/2002  |            | NONVOLATILE SEMICONDUCTOR MEMORY AND                                                                                                    |
| 6,781,884             | AF02204US                | United States | 03/11/2002  | 08/24/2004 | SETTING SYSTEM FOR THRESHOLD VOLTAGE OF                                                                                                 |
| 6,970,007             | AF02205US                | United States | 04/02/2003  | 11/29/2005 | EQUIPMENT FOR LOW TEMPERATURE                                                                                                           |
| 6,813,189             | AF02206US                | United States | 07/16/2002  | 11/02/2004 | SYSTEM USING DYNAMIC REFERENCE BY                                                                                                       |
| 7,266,664             | AF02207US                | United States | 02/20/2002  | 09/04/2007 | MEMORY DEVICE FOR CONTROLLING NONVOLATILE AND VOLATILE MEMORIES                                                                         |
| 7,026,687             | AF02208US                | United States | 03/14/2003  | 04/11/2006 | NONVOLATILE SEMICONDUCTOR MEMORY AND METHOD OF MANUFACTURING THE SAME                                                                   |
| 11/480,553            | AF02208US CON            | United States | 07/05/2006  |            | NONVOLATILE SEMICONDUCTOR MEMORY AND METHOD OF MANUFACTURING THE SAME                                                                   |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                        |
|-----------------------|---------------------------|---------------|-------------|------------|--------------------------------------------------------------------------------------------------------------|
| 11/080,652            | AF02208US DIV             | United States | 03/16/2005  |            | NONVOLATILE SEMICONDUCTOR MEMORY AND METHOD OF MANUFACTURING THE SAME                                        |
| 6,639,849             | AF02209US                 | United States | 02/03/2003  | 10/28/2003 | NONVOLATILE SEMICONDUCTOR DEVICE                                                                             |
| 10/435,373            | AF02210                   | United States | 05/12/2003  |            | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                      |
| 6,816,423             | AF02211US                 | United States | 04/29/2002  | 11/09/2004 | CONTROL SYSTEM FOR PRECHARGE LEVEL ON                                                                        |
| 6,940,120             | AF02212US                 | United States | 05/15/2003  | 09/06/2005 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND METHOD OF FABRICATING THEREOF                                    |
| 11/183,840            | AF02212US DIV             | United States | 07/19/2005  |            | NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE AND METHOD OF FABRICATING THEREOF                                   |
| 6,969,663             | AF02213US                 | United States | 08/28/2003  | 11/29/2005 | MEMORY INTEGRATED CIRCUIT DEVICE                                                                             |
| 6,914,824             | AF02214US                 | United States | 03/21/2003  | 07/05/2005 | SEMICONDUCTOR MEMORY DEVICE                                                                                  |
| 6,934,194             | AF02215US                 | United States | 08/01/2003  | 08/23/2005 | NONVOLATILE MEMORY HAVING TRANSLAYER                                                                         |
| 6,912,160             | AF02216US                 | United States | 03/11/2003  | 06/28/2005 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                             |
| 7,082,077             | AF02217US                 | United States | 08/07/2003  | 07/25/2006 | SEMICONDUCTOR MEMORY DEVICE THE                                                                              |
| 6,839,279             | AF02218US                 | United States | 06/06/2003  | 01/04/2005 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                             |
| 6,853,596             | AF02219US                 | United States | 09/10/2003  | 02/08/2005 | SEMICONDUCTOR MEMORY FOR FUNCTION WELL                                                                       |
| 7,012,838             | AF02220US                 | United States | 08/01/2003  | 03/14/2006 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                             |
| 6,865,133             | AF02221US                 | United States | 09/02/2003  | 03/08/2005 | MEMORY CIRCUIT HAVING                                                                                        |
| 7,061,809             | AF02222US                 | United States | 08/05/2003  | 06/13/2006 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                             |
| 7,081,776             | AF02223US                 | United States | 02/24/2003  | 07/25/2006 | VOLTAGE DETECTION CIRCUIT, SEMICONDUCTOR DEVICE, METHOD FOR CONTROLLING VOLTAGE DETECTION CIRCUIT            |
| 7,358,778             | AF02223US DIV             | United States | 07/07/2006  | 04/15/2008 | VOLTAGE DETECTION CIRCUIT, SEMICONDUCTOR DEVICE, METHOD FOR CONTROLLING VOLTAGE DETECTION CIRCUIT            |
| 7,106,651             | AF02224US                 | United States | 02/18/2003  | 09/12/2006 | SEMICONDUCTOR MEMORY DEVICE AND DATA READ                                                                    |
| 6,987,297             | AF02225US                 | United States | 02/02/2004  | 01/17/2006 | SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD THEREOF                                                 |
| 7,132,332             | AF02225US DIV             | United States | 10/12/2005  | 11/07/2006 | SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD THEREOF                                                 |
| 7,280,404             | AF02226US CON             | United States | 02/27/2003  | 10/09/2007 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                             |
| 7,487,286             | AF02229US CON             | United States | 02/28/2003  | 02/03/2009 | FLASH MEMORY AND MEMORY CONTROL                                                                              |
| 11/030,129            | AF02230US                 | United States | 12/17/2003  |            | SEMICONDUCTOR DEVICE AND TEST METHOD                                                                         |
| 6,995,423             | AF02230US DIV             | United States | 06/28/2004  | 02/07/2006 | MEMORY DEVICE HAVING A P+ GATE AND THIN BOTTOM OXIDE AND METHOD OF ERASING SAME                              |
| 7,082,066             | AF02231US                 | United States | 04/30/2003  | 07/25/2006 | FLASH MEMORY WITH SPARE SECTOR QUICKEN                                                                       |
| 11/110,700            | AF02232US CON             | United States | 03/11/2003  |            | MEMORY DEVICE                                                                                                |
| 7,212,443             | AF02233US                 | United States | 12/17/2003  | 05/01/2007 | NONVOLATILE MEMORY AND METHOD AND WRITE METHOD OF THE SAME                                                   |
| 6,965,530             | AF02234US                 | United States | 11/19/2003  | 11/15/2005 | SEMICONDUCTOR MEMORY DEVICE AND CONTROL                                                                      |
| 7,185,140             | AF02235US                 | United States | 12/05/2003  | 02/27/2007 | METHOD FOR STORING IN NONVOLATILE MEMORY AND STORAGE UNIT                                                    |
| 6,970,381             | AF02236US                 | United States | 12/30/2003  | 11/29/2005 | SEMICONDUCTOR MEMORY DEVICE                                                                                  |
| 6,975,543             | AF02237US                 | United States | 04/28/2003  | 12/13/2005 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                      |
| 7,280,413             | AF02238US                 | United States | 04/24/2003  | 10/09/2007 | NONVOLATILE SEMICONDUCTOR MEMORY                                                                             |
| 7,180,785             | AF02239US                 | United States | 04/17/2003  | 02/20/2007 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE WITH A PLURALITY OF SECTORS                                          |
| 6,804,151             | AF02240US                 | United States | 05/14/2003  | 10/12/2004 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                      |
| 7,190,630             | AF02241US CON             | United States | 06/06/2003  | 03/13/2007 | SEMICONDUCTOR MEMORY DEVICE AND SELECT                                                                       |
| 7,605,616             | AF02243US CIP             | United States | 10/16/2007  | 10/20/2009 | VOLTAGE DETECTOR CIRCUIT                                                                                     |
| 7,532,518             | AF02246US                 | United States | 06/25/2007  | 05/12/2009 | COMPENSATION METHOD TO ACHIEVE UNIFORM PROGRAMMING SPEED OF FLASH MEMORY DEVICES                             |
| 8,560,756             | AF02247US                 | United States | 10/17/2007  | 10/15/2013 | HYBRID FLASH MEMORY DEVICE                                                                                   |
| 8,367,537             | AF02248US                 | United States | 05/10/2007  | 02/05/2013 | FLASH MEMORY CELL WITH A FLAIR GATE                                                                          |
| 13/725,654            | AF02248US DIV             | United States | 12/21/2012  |            | FLASH MEMORY CELL WITH A FLAIR GATE                                                                          |
| 11/652,785            | AF02249US                 | United States | 01/11/2007  |            | A SHALLOW BIPOLAR JUNCTION TRANSISTOR                                                                        |
| 7,691,737             | AF02250US                 | United States | 12/21/2006  | 04/06/2010 | COPPER PROCESS METHODOLOGY                                                                                   |
| 7,745,236             | AF02251US                 | United States | 12/21/2006  | 06/29/2010 | A FLOATING GATE PROCESS METHODOLOGY                                                                          |
| 12/110,181            | AF02253US                 | United States | 04/25/2008  |            | STRUCTURES AND METHODS FOR STACK TYPE SEMICONDUCTOR PACKAGING                                                |
| 7,808,808             | AF02254US                 | United States | 07/21/2008  | 10/05/2010 | NONVOLATILE MEMORY DEVICE HAVING A PLURALITY OF MEMORY BLOCKS                                                |
| 8,094,478             | AF02254US CON             | United States | 09/09/2010  | 01/10/2012 | NONVOLATILE MEMORY DEVICE HAVING A PLURALITY OF MEMORY BLOCKS                                                |
| 8,638,931             | AF02255US                 | United States | 10/30/2007  | 01/28/2014 | SIGNAL DESCRAMBLING DETECTOR                                                                                 |
| 7,956,424             | AF02256US                 | United States | 08/15/2008  | 06/07/2011 | MIRROR BIT MEMORY DEVICE APPLYING A GATE VOLTAGE ALTERNATELY TO GATE                                         |
| 7,820,547             | AF02257US                 | United States | 07/24/2008  | 10/26/2010 | FLASH MEMORY DEVICE WITH WORD LINES OF UNIFORM WIDTH AND METHOD FOR MANUFACTURING THEREOF                    |
| 8,304,914             | AF02257US CON             | United States | 10/26/2010  | 11/06/2012 | FLASH MEMORY DEVICE WITH WORD LINES OF UNIFORM WIDTH AND METHOD FOR MANUFACTURING THEREOF                    |
| 13/657,047            | AF02257US CON2            | United States | 10/22/2012  |            | FLASH MEMORY DEVICE WITH WORD LINES OF UNIFORM WIDTH AND METHOD FOR MANUFACTURING THEREOF                    |
| 7,934,051             | AF02259US                 | United States | 02/01/2008  | 04/26/2011 | PROGRAM AND ERASE DISABLING CONTROL OF WPCAM BY DOUBLE CONTROLS                                              |
| 8,219,743             | AF02259US CON             | United States | 03/21/2011  | 07/10/2012 | PROGRAM AND ERASE DISABLING CONTROL OF WPCAM BY DOUBLE CONTROLS                                              |
| 7,859,914             | AF02261US                 | United States | 03/28/2008  | 12/28/2010 | NON-VOLATILE MEMORY DEVICE, NON-VOLATILE MEMORY SYSTEM AND CONTROL METHOD FOR THE NON-VOLATILE MEMORY DEVICE |
| 8,003,468             | AF02262US                 | United States | 08/20/2008  | 08/23/2011 | SEPARATION METHODS FOR SEMICONDUCTOR CHARGE OF ACCUMULATION LAYERS AND STRUCTURES THEREOF                    |
| 8,318,566             | AF02262US DIV             | United States | 06/08/2011  | 11/27/2012 | METHOD TO SEPERATE STORAGE REGIONS IN THE MIRROR BIT DEVICE                                                  |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                  |
|-----------------------|---------------------------|---------------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8,642,441             | AF02264US                 | United States | 12/15/2006  | 02/04/2014 | SELF-ALIGNED STI WITH SINGLE POLY FOR MANUFACTURING A FLASH MEMORY DEVICE                                                                              |
| 14/167,845            | AF02264US DIV             | United States | 01/29/2014  |            | SYSTEM AND METHOD FOR MANUFACTURING SELF-ALIGNED STI WITH SINGLE POLY                                                                                  |
| 12/166,290            | AF02266US                 | United States | 07/01/2008  |            | METHOD AND APPRATUS FOR MANUFACTURING SEMICONDUCTOR DEVICE                                                                                             |
| 60/882,707            | AF02267                   | United States | 12/29/2006  |            | MULTI-LEVEL BIT OPERATION IN DUAL BIT CELLS USING A SUPPLEMENTAL PROGRAMMING LEVEL                                                                     |
| 7,652,919             | AF02267US                 | United States | 06/29/2007  | 01/26/2010 | MULTI-LEVEL BIT OPERATION IN DUAL ELEMENT CELLS USING A SUPPLEMENTAL PROGRAMMING LEVEL                                                                 |
| 7,561,465             | AF02269US                 | United States | 03/16/2007  | 07/14/2009 | METHODS AND SYSTEMS FOR MEMORY DEVICES                                                                                                                 |
| 60/877,478            | AF02269US                 | United States | 12/28/2006  |            | METHODS AND SYSTEMS FOR MEMORY DEVICES                                                                                                                 |
| 7,989,328             | AF02271US                 | United States | 12/19/2006  | 08/02/2011 | RESISTIVE MEMORY ARRAY USING P-I-N DIODE SELECT DEVICE AND METHODS OF FABRICATION THEREOF                                                              |
| 13/165,652            | AF02271US DIV             | United States | 06/21/2011  |            | RESISTIVE MEMORY ARRAY USING P-I-N DIODE SELECT DEVICE AND METHODS OF FABRICATION THEREOF                                                              |
| 7,646,624             | AF02272US                 | United States | 10/31/2006  | 01/12/2010 | METHOD OF SELECTING OPERATING CHARACTERISTICS OF A RESISTIVE MEMORY DEVICE                                                                             |
| 7,932,125             | AF02274US                 | United States | 07/31/2008  | 04/26/2011 | SELF-ALIGNED CHARGE STORAGE REGION FORMATION FOR SEMICONDUCTOR DEVICE                                                                                  |
| 8,319,273             | AF02274US DIV             | United States | 04/26/2011  | 11/27/2012 | SELF-ALIGNED CHARGE STORAGE REGION FORMATION FOR SEMICONDUCTOR DEVICE                                                                                  |
| 8,946,020             | AF02279US                 | United States | 09/06/2007  | 02/03/2015 | METHOD OF FORMING CONTROLLABLY CONDUCTIVE OXIDE                                                                                                        |
| 14/612,083            | AF02279US DIV             | United States | 02/02/2015  |            | METHOD OF FORMING CONTROLLABLY CONDUCTIVE OXIDE                                                                                                        |
| 8,156,272             | AF02282US                 | United States | 09/01/2006  | 04/10/2012 | MULTIPLE COMUNICATION CHANNELS ON MMC OR SD CMD LINE                                                                                                   |
| 8,386,681             | AF02282US CON             | United States | 03/02/2012  | 02/26/2013 | MULTIPLE COMUNICATION CHANNELS ON MMC OR SD CMD LINE                                                                                                   |
| 11/641,506            | AF02283US                 | United States | 12/19/2006  |            | STRESS MANAGEMENT IN BGA PACKAGING                                                                                                                     |
| 7,724,075             | AF02284US                 | United States | 12/06/2006  | 05/25/2010 | A NEW METHOD TO PROVIDE A HIGHER REFERENCE VOLTAGE AT A LOWER POWER SUPPLY IN FLASH MEMORY DEVICES                                                     |
| 7,460,415             | AF02285US                 | United States | 12/15/2006  | 12/02/2008 | DRAIN VOLTAGE REGULATOR                                                                                                                                |
| 7,746,706             | AF02286US                 | United States | 12/15/2006  | 06/29/2010 | METHODS AND SYSTEMS FOR MEMORY DEVICES                                                                                                                 |
| 7,964,446             | AF02287US                 | United States | 03/07/2008  | 06/21/2011 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME                                                                                              |
| 8,466,552             | AF02287US DIV             | United States | 06/21/2011  | 06/18/2013 | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME                                                                                              |
| 8,492,890             | AF02288US                 | United States | 03/17/2008  | 07/23/2013 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THEREOF                                                                                              |
| 8,586,412             | AF02288US DIV             | United States | 06/19/2013  | 11/19/2013 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THEREOF                                                                                              |
| 7,816,788             | AF02291US                 | United States | 05/16/2008  | 10/19/2010 | STRUCTURE, METHOD AND SYSTEM FOR ASSESSING BONDING OF ELECTRODES IN FCB PACKAGING                                                                      |
| 8,274,158             | AF02291US DIV             | United States | 09/08/2010  | 09/25/2012 | STRUCTURE, METHOD AND SYSTEM FOR ASSESSING BONDING OF ELECTRODES IN FCB PACKAGING                                                                      |
| 7,932,616             | AF02293US                 | United States | 04/04/2008  | 04/26/2011 | SEMICONDUCTOR DEVICE SEALED IN A RESIN SECTION AND METHOD FOR MANUFACTURING THE SAME                                                                   |
| 8,900,993             | AF02293US DIV             | United States | 03/21/2011  | 12/02/2014 | SEMICONDUCTOR DEVICE SEALED IN RESIN SECTION AND METHOD FOR MANUFACTURING THE SAME                                                                     |
| 14/521,181            | AF02293US DIV2            | United States | 10/22/2014  |            | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME                                                                                             |
| 11/899,575            | AF02299US                 | United States | 09/06/2007  |            | TA-LINED TUNGSTEM PLUGS FOR TRANSISTOR-LOCAL HYDROGEN GATHERING                                                                                        |
| 7,558,907             | AF02301US                 | United States | 10/13/2006  | 07/07/2009 | VIRTUAL MEMORY CARD CONTROLLER                                                                                                                         |
| 7,901,955             | AF02302US                 | United States | 06/25/2007  | 03/08/2011 | METHOD OF CONSTRUCTING A STACKED-DIE SEMICONDUCTOR STRUCTURE                                                                                           |
| 11/650,907            | AF02305                   | United States | 01/08/2007  |            | STRUCTURE AND METHOD FOR WIRE BOND INTEGRITY CHECK ON BGA SUBSTRATES USING INDIRECT ELECTRICAL INTERCONNECTIVITY PATHWAY BETWEEN WIRE BONDS AND GROUND |
| 7,948,820             | AF02306US                 | United States | 12/05/2007  | 05/24/2011 | CIRCUIT PRE-CHARGE TO SENSE A MEMORY LINE                                                                                                              |
| 7,505,298             | AF02307US                 | United States | 04/30/2007  | 03/17/2009 | TRANSFER OF NON-ASSOCIATED INFORMATION ON FLASH MEMORY DEVICES                                                                                         |
| 7,729,169             | AF02312US                 | United States | 05/23/2008  | 06/01/2010 | MULTIPLE PROGRAMMING OF SPARE MEMORY REGION FOR NONVOLATILE MEMORY                                                                                     |
| 8,269,343             | AF02313US                 | United States | 09/19/2008  | 09/18/2012 | SEMICONDUCTOR DEVICE INCLUDING A PRESSURE- CONTACT SECTION                                                                                             |
| 8,421,241             | AF02314US                 | United States | 10/27/2008  | 04/16/2013 | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD                                                                                                          |
| 13/725,637            | AF02314US CON             | United States | 12/21/2012  |            | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THEREOF                                                                                              |
| 7,706,186             | AF02315US CIP             | United States | 11/05/2007  | 04/27/2010 | CONTROLLING A SEMICONDUCTOR DEVICE                                                                                                                     |
| 60/856,545            | AF02315US PROV            | United States | 11/03/2006  |            | ERASURE SUSPENSION FEATURE                                                                                                                             |
| 7,892,892             | AF02316US                 | United States | 06/30/2008  | 02/22/2011 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THEREOF                                                                                              |
| 8,446,015             | AF02316US DIV             | United States | 01/27/2011  | 05/21/2013 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THEREOF                                                                                              |
| 7,743,203             | AF02317US                 | United States | 05/11/2007  | 06/22/2010 | MANAGING MEMORY PROGRAM AND ERASE CYCLES IN THE TIME DOMAIN                                                                                            |
| 7,939,925             | AF02320US                 | United States | 10/24/2008  | 05/10/2011 | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF                                                                                                  |
| 7,803,680             | AF02322US                 | United States | 01/12/2007  | 09/28/2010 | METHODS FOR FORMING A MEMORY CELL HAVING A TOP OXIDE SPACER                                                                                            |
| 7,906,395             | AF02322US CON             | United States | 09/27/2010  | 03/15/2011 | A SELF-ALIGNED PATTERNING METHOD BY USING NON-CONFORMAL FILM AND ETCH BACK FOR FLASH MEMORY AND OTHER SEMICONDUCTOR APPLICATIONS                       |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL NO. | SPANION REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                               |
|--------------------|-----------------------|---------------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------|
| 8,367,466          | AF02326US             | United States | 09/12/2008  | 02/05/2013 | MANUFACTURING STACKED SEMICONDUCTOR DEVICE                                                                                          |
| 8,190,919          | AF02329US             | United States | 12/20/2006  | 05/29/2012 | MULTIPLE STAKEHOLDER SECURE MEMORY PARTITIONING AND ACCESS CONTROL                                                                  |
| 60/864,682         | AF02329US PROV        | United States | 11/07/2006  |            | MULTIPLE STAKEHOLDER SECURE MEMORY PARTITIONING AND ACCESS CONTROL                                                                  |
| 8,117,445          | AF02330US             | United States | 12/20/2006  | 02/14/2012 | NEAR FIELD COMMUNICATION, SECURITY AND NON-VOLATILE MEMORY INTEGRATED SUB-SYSTEM FOR EMBEDDED PORTABLE APPLICATIONS                 |
| 8,261,091          | AF02331US             | United States | 12/21/2006  | 09/04/2012 | SOLID-STATE MEMORY-BASED GENERATION AND HANDLING OF SECURITY AUTHENTICATION TOKENS                                                  |
| 8,190,908          | AF02332US             | United States | 12/20/2006  | 05/29/2012 | SECURE DATA VERIFICATION VIA BIOMETRIC INPUT                                                                                        |
| 8,190,885          | AF02333US             | United States | 12/21/2006  | 05/29/2012 | NON-VOLATILE MEMORY SUB-SYSTEM INTEGRATED WITH SECURITY FOR STORING NEAR FIELD TRANSACTIONS                                         |
| 7,836,269          | AF02334US             | United States | 12/29/2006  | 11/16/2010 | SYSTEMS AND METHODS FOR ACCESS VIOLATION MANAGEMENT OF SECURED MEMORY                                                               |
| 8,356,361          | AF02335US             | United States | 12/21/2006  | 01/15/2013 | SECURE CO-PROCESSING MEMORY CONTROLLER INTEGRATED INTO AN EMBEDDED MEMORY SUBSYSTEM                                                 |
| 60/864,730         | AF02335US PROV        | United States | 11/07/2006  |            | SECURE CO-PROCESSING MEMORY CONTROLLER INTEGRATED INTO AN EMBEDDED MEMORY SUBSYSTEM                                                 |
| 11/612,874         | AF02336US             | United States | 12/19/2006  |            | PORTABLE DIGITAL RIGHTS MANAGEMENT (DRM)                                                                                            |
| 7,512,743          | AF02337US             | United States | 11/07/2006  | 03/31/2009 | USING SHARED MEMORY WITH AN EXECUTE-IN-PLACE PROCESSOR AND A CO-PROCESSOR                                                           |
| 7,882,365          | AF02338US             | United States | 12/22/2006  | 02/01/2011 | SYSTEMS AND METHODS FOR DISTINGUISHING BETWEEN ACTUAL DATA AND RELEASED/BLANK MEMORY WITH REGARD TO ENCRYPTED DATA                  |
| 11/616,385         | AF02339US             | United States | 12/27/2006  |            | PERSONAL DIGITAL RIGHTS MANAGEMENT AGENT-SERVER                                                                                     |
| 8,039,943          | AF02340US             | United States | 09/26/2008  | 10/18/2011 | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR                                                                              |
| 8,481,366          | AF02340US DIV         | United States | 04/26/2011  | 07/09/2013 | SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR                                                                              |
| 7,759,171          | AF02403US             | United States | 08/28/2007  | 07/20/2010 | METHOD AND STRUCTURE OF MINIMIZING MOLD BLEEDING ON A SUBSTRATE SURFACE OF SEMICONDUCTOR PACKAGE                                    |
| 8,546,936          | AF02403US DIV         | United States | 06/18/2010  | 10/01/2013 | METHOD AND STRUCTURE OF MINIMIZING MOLD BLEEDING ON A SUBSTRATE SURFACE OF SEMICONDUCTOR PACKAGE                                    |
| 7,554,204          | AF02404US             | United States | 06/19/2007  | 06/30/2009 | DIE OFFSET DIE TO DIE BONDING                                                                                                       |
| 7,750,481          | AF02404US DIV1        | United States | 12/09/2008  | 07/06/2010 | DIE OFFSET DIE TO DIE BONDING                                                                                                       |
| 7,674,653          | AF02404US DIV2        | United States | 12/09/2008  | 03/09/2010 | DIE OFFSET DIE TO DIE BONDING                                                                                                       |
| 11/842,655         | AF02405US             | United States | 08/21/2007  |            | DIE STACKING IN MULTI-DIE STACKS USING DIE SUPPORT MECHANISMS                                                                       |
| 8,708,710          | AF02406US             | United States | 07/30/2007  | 04/29/2014 | CONTACT CONFIGURATION FOR UNDERTAKING TESTS ON CIRCUIT BOARD                                                                        |
| 14/222,446         | AF02406US CON         | United States | 03/21/2014  |            | CONTACT CONFIGURATION FOR UNDERTAKING TESTS ON CIRCUIT BOARD                                                                        |
| 7,633,815          | AF02417US             | United States | 12/05/2007  | 12/15/2009 | FLEXIBLE WORD LINE BOOSTING ACROSS VCC SUPPLY                                                                                       |
| 7,760,558          | AF02418US             | United States | 01/15/2008  | 07/20/2010 | IMPROVED VOLTAGE BOOSTER BY ISOLATION AND DELAYED SEQUENTIAL DISCHARGE                                                              |
| 7,915,907          | AF02419US             | United States | 06/25/2007  | 03/29/2011 | FAULTY DANGLING METAL ROUTE DETECTION                                                                                               |
| 7,768,856          | AF02420US             | United States | 10/30/2007  | 08/03/2010 | CONTROL OF TEMPERATURE SLOPE FOR BAND GAP REFERENCE VOLTAGE IN A MEMORY DEVICE                                                      |
| 7,558,123          | AF02421US             | United States | 08/13/2007  | 07/07/2009 | EFFICIENT AND SYSTEMATIC MEASUREMENT FLOW ON DRAIN VOLTAGE FOR DIFFERENT TRIMMING IN FLASH SILICON CHARACTERIZATION                 |
| 8,219,738          | AF02422US             | United States | 12/03/2007  | 07/10/2012 | DIRECT INTERCONNECTION BETWEEN PROCESSOR AND MEMORY COMPONENT                                                                       |
| 7,558,116          | AF02423US             | United States | 08/13/2007  | 07/07/2009 | REGULATION OF BOOST-STRAP NODE RAMP RATE USING CAPACITANCE TO COUNTER PARASITIC ELEMENTS IN CHANNEL                                 |
| 7,755,922          | AF02435US             | United States | 03/16/2007  | 07/13/2010 | NON-VOLATILE RESISTIVE SWITCHING FOR ADVANCED MEMORY APPLICATIONS                                                                   |
| 60/877,887         | AF02435US             | United States | 12/29/2006  |            | NON-VOLATILE RESISTIVE SWITCHING FOR ADVANCED MEMORY APPLICATIONS                                                                   |
| 60/877,876         | AF02436               | United States | 12/29/2006  |            | RESISTIVE- SWITCHING MEMORY CELL ARCHITECTURE                                                                                       |
| 8,085,615          | AF02436US             | United States | 03/16/2007  | 12/27/2011 | MULTI-STATE RESISTANCE CHANGING MEMORY WITH A WORD LINE DRIVER FOR APPLYING A SAME PROGRAM VOLTAGE TO THE WORD LINE                 |
| 13/289,553         | AF02436US DIV         | United States | 11/04/2011  |            | RESISTIVE CHANGING MEMORY CELL ARCHITECTURE HAVING A SELECT TRANSISTOR COUPLED TO A RESISTANCE CHANGING MEMORY ELEMENT (as amended) |
| 7,672,161          | AF02437US             | United States | 04/30/2007  | 03/02/2010 | ADAPTIVE DETECTION OF THRESHOLD LEVELS IN MEMORY                                                                                    |
| 8,301,963          | AF02438US             | United States | 10/23/2007  | 10/30/2012 | LOW-DENSITY PARITY-CHECK CODE BASED ERROR CORRECTION FOR MEMORY DEVICE                                                              |
| 7,566,628          | AF02447US             | United States | 06/15/2007  | 07/28/2009 | STRUCTURE AND PROCESS FOR A RESISTIVE MEMORY CELL WITH SEPARATELY PATTERNED ELECTRODES                                              |
| 7,626,869          | AF02450US             | United States | 05/07/2007  | 12/01/2009 | MULTI-PHASE WORDLINE ERASING FOR FLASH MEMORY                                                                                       |
| 7,776,696          | AF02451US             | United States | 04/30/2007  | 08/17/2010 | METHOD TO OBTAIN MULTIPLE GATE THICKNESSES USING IN-SITU GATE ETCH MASK APPROACH                                                    |
| 7,682,905          | AF02453US             | United States | 05/09/2007  | 03/23/2010 | SELF ALIGNED NARROW STORAGE ELEMENTS FOR ADVANCED MEMORY DEVICE                                                                     |
| 8,476,695          | AF02453US DIV         | United States | 02/01/2010  | 07/02/2013 | SELF ALIGNED NARROW STORAGE ELEMENTS FOR ADVANCED MEMORY DEVICE                                                                     |
| 7,846,829          | AF02455US             | United States | 08/21/2008  | 12/07/2010 | STACKED SOLDER BALLS FOR INTEGRATED CIRCUIT DEVICE PACKAGING AND ASSEMBLY                                                           |
| 8,946,663          | AF02460JP DIV         | United States | 05/15/2012  | 02/03/2015 | SOFT ERROR RESISTANT CIRCUITRY                                                                                                      |
| 8,552,523          | AF02460US             | United States | 08/09/2011  | 10/08/2013 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING                                                                                   |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                 |
|-----------------------|--------------------------|---------------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------------|
| 7,902,592             | AF02463US                | United States | 12/17/2008  | 03/08/2011 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING                                                                                     |
| 7,821,842             | AF02465US                | United States | 07/21/2008  | 10/26/2010 | SYNCHRONOUS MEMORY DEVICES AND CONTROL METHODS FOR<br>PERFORMING BURST WRITE OPERATIONS                                               |
| 7,889,573             | AF02466US                | United States | 12/22/2008  | 02/15/2011 | TIME REDUCTION OF ADDRESS SETUP/HOLD TIME FOR<br>SEMICONDUCTOR MEMORY                                                                 |
| 8,031,537             | AF02466US DIV            | United States | 01/10/2011  | 10/04/2011 | TIME REDUCTION OF ADDRESS SETUP/HOLD TIME FOR<br>SEMICONDUCTOR MEMORY                                                                 |
| 7,808,827             | AF02470US                | United States | 11/06/2007  | 10/05/2010 | CONTROLLED BIT LINE DISCHARGE FOR CHANNEL ERASES IN<br>NONVOLATILE MEMORY                                                             |
| 7,679,972             | AF02471US                | United States | 11/26/2007  | 03/16/2010 | HIGH RELIABILITY AND LOW POWER STATIC RANDOM ACCESS<br>MEMORY                                                                         |
| 11/687,479            | AF02472                  | United States | 03/16/2007  |            | MEMORY STORAGE VIA AN INTERNAL COMPRESSION ALGORITHM                                                                                  |
| 7,852,669             | AF02477US                | United States | 03/16/2007  | 12/14/2010 | DIVISION-BASED SENSING AND PARTITIONING OF ELECTRONIC<br>MEMORY                                                                       |
| 8,116,151             | AF02479US                | United States | 08/11/2008  | 02/14/2012 | MULTI-LEVEL PROGRAM ALGORITHM EMPHASIZE DISTURB<br>CONDITION                                                                          |
| 7,802,114             | AF02480US                | United States | 03/16/2007  | 09/21/2010 | STATE CHANGE SENSING                                                                                                                  |
| 7,835,189             | AF02481US                | United States | 03/16/2007  | 11/16/2010 | HIGH ACCURACY ADAPTIVE PROGRAMMING                                                                                                    |
| 7,746,698             | AF02495US                | United States | 12/13/2007  | 06/29/2010 | PROGRAMMING IN MEMORY DEVICES USING SOURCE BITLINE<br>VOLTAGE BIAS                                                                    |
| 7,692,962             | AF02496US                | United States | 12/18/2007  | 04/06/2010 | REDUCED STATE QUADBIT                                                                                                                 |
| 7,659,569             | AF02498US                | United States | 12/10/2007  | 02/09/2010 | WORK FUNCTION ENGINEERING FOR FN ERASE OF A MEMORY<br>DEVICE WITH MULTIPLE CHARGE STORAGE ELEMENTS IN AN<br>UNDERCUT REGION           |
| 7,656,705             | AF02499US                | United States | 10/17/2007  | 02/02/2010 | FAST SINGLE PHASE PROGRAM ALGORITHM FOR QUADBIT                                                                                       |
| 7,679,967             | AF02503US                | United States | 12/21/2007  | 03/16/2010 | CONTROLLING AC DISTURBANCE WHILE PROGRAMMING                                                                                          |
| 8,559,255             | AF02503US CON3           | United States | 08/08/2012  | 10/15/2013 | CONTROLLING AC DISTURBANCE WHILE PROGRAMMING                                                                                          |
| 7,986,562             | AF02503US DIV            | United States | 12/30/2009  | 07/26/2011 | CONTROLLING AC DISTURBANCE WHILE PROGRAMMING                                                                                          |
| 8,264,898             | AF02503US DIV2           | United States | 06/09/2011  | 09/11/2012 | CONTROLLING AC DISTURBANCE WHILE PROGRAMMING                                                                                          |
| 7,746,705             | AF02504US                | United States | 12/10/2007  | 06/29/2010 | SELECTIVE APPLICATION OF WORD LINE BIAS TO MINIMIZE FRINGE<br>EFFECTS IN ELECTROMAGNETIC FIELDS DURING ERASE OF<br>NONVOLATILE MEMORY |
| 7,952,938             | AF02504US DIV            | United States | 05/04/2010  | 05/31/2011 | SELECTIVE APPLICATION OF WORD LINE BIAS TO MINIMIZE FRINGE<br>EFFECTS IN ELECTROMAGNETIC FIELDS DURING ERASE OF<br>NONVOLATILE MEMORY |
| 7,981,745             | AF02517US                | United States | 08/30/2007  | 07/19/2011 | SACRIFICIAL NITRIDE AND GATE REPLACEMENT                                                                                              |
| 8,329,598             | AF02517US DIV            | United States | 06/06/2011  | 12/11/2012 | SACRIFICIAL NITRIDE AND GATE REPLACEMENT                                                                                              |
| 8,455,268             | AF02518US                | United States | 08/31/2007  | 06/04/2013 | GATE REPLACEMENT WITH TOP OXIDE REGROWTH FOR THE TOP<br>OXIDE IMPROVEMENT                                                             |
| 7,807,580             | AF02520US                | United States | 04/30/2007  | 10/05/2010 | TRIPLE POLY-SI REPLACEMENT SCHEME FOR MEMORY DEVICES                                                                                  |
| 7,776,688             | AF02523US                | United States | 08/08/2007  | 08/17/2010 | USE OF A POLYMER SPACER AND SI TRENCH IN A BITLINE JUNCTION<br>OF A FLASH MEMORY CELL TO IMPROVE TPD CHARACTERISTICS                  |
| 7,906,807             | AF02523US DIV            | United States | 06/30/2010  | 03/15/2011 | USE OF A POLYMER SPACER AND SI TRENCH IN A BITLINE JUNCTION<br>OF A FLASH MEMORY CELL TO IMPROVE TPD CHARACTERISTICS                  |
| 7,883,963             | AF02525US                | United States | 10/25/2007  | 02/08/2011 | SPLIT CHARGE STORAGE NODE OUTER SPACER PROCESS                                                                                        |
| 8,039,891             | AF02525US DIV            | United States | 12/29/2010  | 10/18/2011 | SPLIT CHARGE STORAGE NODE OUTER SPACER PROCESS                                                                                        |
| 7,829,936             | AF02526US                | United States | 10/17/2007  | 11/09/2010 | SPLIT CHARGE STORAGE NODE INNER SPACER PROCESS                                                                                        |
| 8,012,830             | AF02527US                | United States | 08/08/2007  | 09/06/2011 | ORO AND ORPRO WITH BITLINE TRENCH TO SUPPRESS TRANSPORT<br>PROGRAM DISTURB                                                            |
| 13/190,565            | AF02527US DIV            | United States | 07/26/2011  |            | ORO AND ORPRO WITH BITLINE TRENCH TO SUPPRESS TRANSPORT<br>PROGRAM DISTURB                                                            |
| 7,951,675             | AF02529US                | United States | 12/17/2007  | 05/31/2011 | SI TRENCH BETWEEN BITLINE HDP FOR BVDSS IMPROVEMENT                                                                                   |
| 7,691,751             | AF02531US                | United States | 10/26/2007  | 04/06/2010 | SELECTIVE SILICIDE FORMATION USING RESIST ETCHBACK                                                                                    |
| 8,445,372             | AF02531US DIV            | United States | 12/22/2009  | 05/21/2013 | SELECTIVE SILICIDE FORMATION USING RESIST ETCHBACK                                                                                    |
| 8,637,986             | AF02536US                | United States | 10/22/2008  | 01/28/2014 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING<br>THEREOF                                                                          |
| 14/136,977            | AF02536US DIV            | United States | 12/20/2013  |            | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING<br>THEREOF                                                                          |
| 8,380,917             | AF02539US                | United States | 06/12/2008  | 02/19/2013 | COMMAND CONTROL FOR SYNCHRONOUS MEMORY DEVICE                                                                                         |
| 8,122,204             | AF02541US                | United States | 06/11/2008  | 02/21/2012 | SHADOW WRITE AND TRANSFER SCHEMES FOR MEMORY DEVICES                                                                                  |
| 7,981,746             | AF02545US                | United States | 12/22/2008  | 07/19/2011 | SEMICONDUCTOR DVICE AND METHOD FOR MANUFACTURING<br>THEREOF                                                                           |
| 8,669,606             | AF02545US DIV            | United States | 06/09/2011  | 03/11/2014 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING<br>THEREOF                                                                          |
| 7,535,767             | AF02548US                | United States | 08/06/2007  | 05/19/2009 | READING MULTI-CELL MEMORY DEVICES UTILIZING<br>COMPLEMENTARY BIT INFORMATION                                                          |
| 7,602,639             | AF02550US                | United States | 12/14/2007  | 10/13/2009 | READING ELECTRONIC MEMORY UTILIZING RELATIONSHIPS<br>BETWEEN CELL STATE DISTRIBUTIONS                                                 |
| 7,869,281             | AF02550US CON            | United States | 08/31/2009  | 01/11/2011 | READING ELECTRONIC MEMORY UTILIZING RELATIONSHIPS<br>BETWEEN CELL STATE DISTRIBUTIONS                                                 |
| 7,799,612             | AF02553US                | United States | 06/25/2007  | 09/21/2010 | PROCESS APPLYING DIE ATTACH FILM TO SINGULATED DIE                                                                                    |
| 8,174,107             | AF02554US                | United States | 12/17/2008  | 05/08/2012 | STACKED SEMICONDUCTOR DEVICES AND METHOD FOR<br>FABRICATING THE SAME                                                                  |
| 7,851,260             | AF02556US                | United States | 12/10/2008  | 12/14/2010 | METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE                                                                                       |
| 8,749,039             | AF02557US                | United States | 08/21/2008  | 06/10/2014 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING<br>THEREOF                                                                          |
| 14/271,115            | AF02557US DIV            | United States | 05/06/2014  |            | SEMICONDUCTOR DEVICE HAVING CHIP MOUNTED ON AN<br>INTERPOSER (as amended)                                                             |
| 7,786,587             | AF02559US                | United States | 07/01/2008  | 08/31/2010 | STRUCTURE AND MANUFACTURING METHOD FOR A CHIP WHICH HAS<br>A THROUGH-HOLE ELECTRODE                                                   |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL NO. | SPANSON REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                                |
|--------------------|-----------------------|---------------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8,148,771          | AF02559US CON         | United States | 07/15/2010  | 04/03/2012 | SEMICONDUCTOR DEVICE AND METHOD TO MANUFACTURE THEREOF                                                                                                                               |
| 60/958,084         | AF02559US PROV        | United States | 07/02/2007  |            | STRUCTURE AND MANUFACTURING METHOD FOR A CHIP WHICH HAS A THROUGH-HOLE ELECTRODE                                                                                                     |
| 11/770,239         | AF02560US             | United States | 06/28/2007  |            | DIE ATTACHMENT, DIE STACKING, AND WIRE EMBEDDING USING FILM                                                                                                                          |
| 7,482,217          | AF02562US             | United States | 12/03/2007  | 01/27/2009 | FORMING METAL-SEMICONDUCTOR FILMS HAVING DIFFERENT THICKNESSES WITHIN DIFFERENT REGIONS OF AN ELECTRONIC DEVICE                                                                      |
| 7,880,221          | AF02562US DIV         | United States | 12/19/2008  | 02/01/2011 | FORMING METAL-SEMICONDUCTOR FILMS HAVING DIFFERENT THICKNESSES WITHIN DIFFERENT REGIONS OF AN ELECTRONIC DEVICE                                                                      |
| 8,832,408          | AF02563US             | United States | 10/30/2007  | 09/09/2014 | NON-VOLATILE MEMORY ARRAY PARTITIONING ARCHITECTURE AND METHOD TO UTILIZE SINGLE LEVEL CELLS AND MULTI-LEVEL CELLS WITHIN THE SAME MEMORY                                            |
| 8,650,399          | AF02565US             | United States | 02/29/2008  | 02/11/2014 | MEMORY DEVICE AND CHIP SET PROCESSOR PAIRING                                                                                                                                         |
| 7,945,792          | AF02566               | United States | 10/17/2008  |            | TAMPER REACTIVE MEMORY DEVICE TO SECURE DATA FROM TAMPER ATTACKS                                                                                                                     |
| 8,201,258          | AF02567US             | United States | 10/17/2007  | 06/12/2012 | SECURE PERSONALIZATION OF MEMORY-BASED ELECTRONIC DEVICES                                                                                                                            |
| 8,140,746          | AF02568US             | United States | 12/14/2007  | 03/20/2012 | INTELLIGENT MEMORY DATA MANAGEMENT                                                                                                                                                   |
| 8,694,776          | AF02570US             | United States | 12/21/2007  | 04/08/2014 | AUTHENTICATED MEMORY AND CONTROLLER SLAVE                                                                                                                                            |
| 14/180,444         | AF02570US CON         | United States | 02/14/2014  |            | AUTHENTICATED MEMORY AND CONTROLLER SLAVE                                                                                                                                            |
| 8,130,955          | AF02571US             | United States | 12/21/2007  | 03/06/2012 | RANDOM NUMBER GENERATION THROUGH USE OF MEMORY CELL ACTIVITY                                                                                                                         |
| 8,670,557          | AF02572US             | United States | 09/10/2007  | 03/11/2014 | CRYPTOGRAPHIC SYSTEM WITH MODULAR RANDOMIZATION OF EXPONENTIATION                                                                                                                    |
| 8,202,810          | AF02583US             | United States | 01/09/2008  | 06/19/2012 | LOW-H PLASMA TREATMENT FOR ELECTRONIC MEMORY DEVICES                                                                                                                                 |
| 7,787,312          | AF02585US             | United States | 05/30/2008  | 08/31/2010 | SEMICONDUCTOR DEVICE AND CONTROLLING METHOD FOR THE SAME                                                                                                                             |
| 7,679,968          | AF02586US             | United States | 05/29/2008  | 03/16/2010 | ENHANCED ERASING OPERATION FOR NON-VOLATILE MEMORY SEMICONDUCTOR DEVICE AND METHOD FOR CONTROLLING THEREOF                                                                           |
| 8,423,705          | AF02587US             | United States | 06/13/2008  | 04/16/2013 |                                                                                                                                                                                      |
| 60/152,151         | AF02589               | United States | 08/31/1999  |            | MULTI-PROCESSOR TECHNIQUES                                                                                                                                                           |
| 09/652,815         | AF02589US CIP         | United States | 08/31/2000  |            | HIGH-AVAILABILITY SHARED-MEMORY CLUSTER                                                                                                                                              |
| 09/653,183         | AF02589US CIP2        | United States | 08/31/2000  |            | MULTI-PROCESSOR TECHNIQUES                                                                                                                                                           |
| 09/653,189         | AF02589US CIP3        | United States | 08/31/2000  |            | MULTI-PROCESSOR TECHNIQUES                                                                                                                                                           |
| 09/653,421         | AF02589US CIP4        | United States | 08/31/2000  |            | EFFICIENT PAGE OWNERSHIP CONTROL                                                                                                                                                     |
| 09/653,425         | AF02589US CIP5        | United States | 08/31/2000  |            | MULTI-PROCESSOR TECHNIQUES                                                                                                                                                           |
| 09/653,429         | AF02589US CIP6        | United States | 08/31/2000  |            | MULTI-PROCESSOR TECHNIQUES                                                                                                                                                           |
| 09/653,475         | AF02589US CIP7        | United States | 08/31/2000  |            | SHARED MEMORY DISK                                                                                                                                                                   |
| 09/653,502         | AF02589US CIP8        | United States | 08/31/2000  |            | MULTI-PROCESSOR TECHNIQUES                                                                                                                                                           |
| 09/653,557         | AF02589US CIP9        | United States | 08/31/2000  |            | MULTI-PROCESSOR TECHNIQUES                                                                                                                                                           |
| 09/672,909         | AF02590               | United States | 09/28/2000  |            | LOW LATENCY, HIGH BANDWIDTH MULTI-COMPUTER SYSTEM INTERCONNECT                                                                                                                       |
| 60/159,086         | AF02590               | United States | 10/13/1999  |            | LOW LATENCY, HIGH BANDWIDTH MULTI-COMPUTER SYSTEM INTERCONNECT                                                                                                                       |
| 60/220,748         | AF02591               | United States | 07/26/2000  |            | TECHNIQUE FOR PROVIDING GLOBALLY-AVAILABLE SYNCHRONIZATION PRIMITIVES IN A DISTRIBUTED COMPUTING ENVIRONMENT WHERE NODES WITHIN THAT ENVIRONMENT SHARE AT LEAST ONE STORAGE RESOURCE |
| 60/220,974         | AF02592               | United States | 07/26/2000  |            | EFFICIENT EVENT WRITING                                                                                                                                                              |
| 6,675,277          | AF02592US             | United States | 07/25/2001  | 01/06/2004 | DEMAND USABLE ADAPTER MEMORY ACCESS MANAGEMENT                                                                                                                                       |
| 6,665,777          | AF02592US CIP         | United States | 07/25/2001  | 12/15/2003 | MULTIPLE BLOCK SEQUENTIAL MEMORY MANAGEMENT                                                                                                                                          |
| 09/912,833         | AF02592US CIP         | United States | 07/25/2001  |            | METHOD AND APPARATUS FOR DEMAND USABLE ADAPTER MEMORY ACCESS MANAGEMENT                                                                                                              |
| 09/912,856         | AF02592US CIP3        | United States | 07/25/2001  |            | EFFICIENT EVENT WRITING                                                                                                                                                              |
| 6,782,440          | AF02592US CIP4        | United States | 07/25/2001  | 08/24/2004 | RESOURCE LOCKING AND THREAD SYNCHRONIZATION IN A MULTIPROCESSOR ENVIRONMENT                                                                                                          |
| 09/912,872         | AF02592US CIP5        | United States | 07/25/2001  |            | EFFICIENT EVENT WRITING                                                                                                                                                              |
| 6,715,059          | AF02592US CIP6        | United States | 07/25/2001  | 03/30/2004 | METHODS AND SYSTEMS FOR A SHARED MEMORY UNIT WITH EXTENDABLE FUNCTIONS                                                                                                               |
| 09/915,002         | AF02592US CIP8        | United States | 07/25/2001  |            | EFFICIENT EVENT WRITING                                                                                                                                                              |
| 6,892,298          | AF02592US CIP9        | United States | 07/25/2001  | 05/10/2005 | LOAD/STORE MICROPACKET HANDLING SYSTEM                                                                                                                                               |
| 6,295,571          | AF02593US             | United States | 03/19/1999  | 09/25/2001 | SHARED MEMORY APPARATUS AND METHOD FOR MULTIPROCESSOR SYSTEMS                                                                                                                        |
| 6,467,011          | AF02593US CON         | United States | 05/15/2001  | 10/15/2002 | SHARED MEMORY APPARATUS AND METHOD FOR MULTIPROCESSOR SYSTEMS                                                                                                                        |
| 6,519,672          | AF02593US DIV         | United States | 05/10/2001  | 02/11/2003 | SHARED MEMORY APPARATUS AND METHOD FOR MULTIPROCESSOR SYSTEMS                                                                                                                        |
| 7,749,855          | AF02597US             | United States | 08/14/2007  | 07/06/2010 | CAPACITOR STRUCTURE USED FOR FLASH MEMORY                                                                                                                                            |
| 11/957,028         | AF02598US             | United States | 12/14/2007  |            | REDUCING NOISE AND DISTURBANCE BETWEEN MEMORY STORAGE ELEMENTS USING ANGLED WORDLINES                                                                                                |
| 11/835,545         | AF02599               | United States | 08/08/2007  |            | SINGULATED BARE DIE TESTING                                                                                                                                                          |
| 60/895,920         | AF02599               | United States | 03/20/2007  |            | SINGULATED BARE DIE TESTING                                                                                                                                                          |
| 12/038,059         | AF02600US             | United States | 02/27/2008  |            | SECURE DATA TRANSFER AFTER AUTHENTICATION BETWEEN MEMORY AND A REQUESTOR                                                                                                             |
| 7,979,658          | AF02601US             | United States | 03/25/2008  | 07/12/2011 | SECURE MANAGEMENT OF MEMORY REGIONS IN A MEMORY                                                                                                                                      |
| 8,239,732          | AF02602US             | United States | 10/30/2007  | 08/07/2012 | ERROR CORRECTION CODING IN FLASH MEMORY DEVICES                                                                                                                                      |
| 7,921,322          | AF02603US             | United States | 10/17/2007  | 04/05/2011 | OPTIMIZE PERSONALIZATION CONDITIONS FOR ELECTRONIC DEVICE TRANSMISSION RATES WITH INCREASED TRANSMITTING FREQUENCY                                                                   |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                                                  |
|-----------------------|--------------------------|---------------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8,139,763             | AF02635US                | United States | 10/10/2007  | 03/20/2012 | RANDOMIZED RSA-BASED CRYPTOGRAPHIC EXPONENTIATION<br>RESISTANT TO SIDE CHANNEL AND FAULT ATTACKS                                                                                                       |
| 7,838,406             | AF02636US                | United States | 12/31/2008  | 11/23/2010 | SONOS-NAND DEVICE HAVING THE STORAGE REGION SEPARATED<br>BETWEEN CELLS                                                                                                                                 |
| 7,979,667             | AF02637US                | United States | 12/10/2007  | 07/12/2011 | MEMORY ARRAY SEARCH ENGINE                                                                                                                                                                             |
| 7,949,851             | AF02638US                | United States | 12/28/2007  | 05/24/2011 | TRANSLATION MANAGEMENT OF LOGICAL BLOCK ADDRESSES AND<br>PHYSICAL BLOCK ADDRESSES                                                                                                                      |
| 8,464,021             | AF02639US                | United States | 05/28/2008  | 06/11/2013 | ADDRESS CACHING STORED TRANSLATION                                                                                                                                                                     |
| 8,239,611             | AF02640US                | United States | 12/28/2007  | 08/07/2012 | RELOCATING DATA IN A MEMORY DEVICE                                                                                                                                                                     |
| 13/539,688            | AF02640US DIV            | United States | 07/02/2012  |            | RELOCATING DATA IN A MEMORY DEVICE                                                                                                                                                                     |
| 8,239,875             | AF02641US                | United States | 12/21/2007  | 08/07/2012 | COMMAND QUEUING FOR NEXT OPERATIONS OF MEMORY DEVICES                                                                                                                                                  |
| 7,675,776             | AF02643US                | United States | 12/21/2007  | 03/09/2010 | BIT MAP CONTROL OF ERASE BLOCK DEFECT LIST IN A MEMORY                                                                                                                                                 |
| 7,953,919             | AF02644                  | United States | 12/21/2007  | 05/31/2011 | PHYSICAL BLOCK ADDRESSING OF ELECTRONIC MEMORY DEVICES                                                                                                                                                 |
| 8,788,740             | AF02645US                | United States | 12/21/2007  | 07/22/2014 | DATA COMMIT ON MULTICYCLE PASS COMPLETE WITHOUT ERROR                                                                                                                                                  |
| 6,567,312             | AF02649US                | United States | 10/13/2000  | 05/20/2003 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                                |
| 8,898,350             | AF02651US                | United States | 11/27/2007  | 11/25/2014 | MULTI-BUS ARCHITECTURE FOR MASS STORAGE SYSTEM-ON-CHIP<br>CONTROLLERS                                                                                                                                  |
| 8,239,182             | AF02652US                | United States | 12/04/2007  | 08/07/2012 | DATA TRANSMISSION SYSTEM-ON-CHIP MEMORY MODEL BASED<br>VALIDATION                                                                                                                                      |
| 11/963,466            | AF02653US                | United States | 12/21/2007  |            | HIGH PERFORMANCE FLASH CHANNEL INTERFACE                                                                                                                                                               |
| 11/963,241            | AF02654US                | United States | 12/21/2007  |            | FLEXIBLE FLASH INTERFACE                                                                                                                                                                               |
| 8,261,124             | AF02657US                | United States | 12/21/2007  | 09/04/2012 | SYSTEM AND METHOD FOR OPTIMIZED ERROR CORRECTION IN<br>FLASH MEMORY ARRAYS                                                                                                                             |
| 7,827,359             | AF02658US                | United States | 12/14/2007  | 11/02/2010 | CLOCK ENCODED PRE-FETCH TO ACCESS MEMORY DATA IN<br>CLUSTERING NETWORK ENVIRONMENT                                                                                                                     |
| 8,175,528             | AF02659US                | United States | 03/18/2008  | 05/08/2012 | WIRELESS MASS STORAGE FLASH MEMORY                                                                                                                                                                     |
| 8,440,357             | AF02660.DIV              | United States | 06/09/2011  | 05/14/2013 | FUEL CELL CATALYST REGENERATION                                                                                                                                                                        |
| 7,981,825             | AF02660US                | United States | 03/27/2008  | 07/19/2011 | FUEL CELL CATALYST REGENERATION                                                                                                                                                                        |
| 8,793,992             | AF02663US                | United States | 07/28/2008  | 08/05/2014 | THERMOELECTRIC DEVICE FOR USE WITH STIRLING ENGINE                                                                                                                                                     |
| 8,017,859             | AF02666US                | United States | 10/17/2007  | 09/13/2011 | PHOTOVOLTAIC THIN COATING FOR COLLECTOR GENERATOR                                                                                                                                                      |
| 7,842,880             | AF02667US                | United States | 11/29/2007  | 11/30/2010 | WEAVABLE FIBER PHOTOVOLTAIC COLLECTORS                                                                                                                                                                 |
| 12/206,117            | AF02674US                | United States | 09/08/2008  |            | SOI SUBSTRATE USING DIC                                                                                                                                                                                |
| 7,645,993             | AF02681US                | United States | 12/28/2007  | 01/12/2010 | ARRAYED NEUTRON DETECTOR WITH MULTI SHIELDING ALLOWING<br>FOR DISCRIMINATION BETWEEN RADIATION TYPES                                                                                                   |
| 7,732,276             | AF02691US                | United States | 04/26/2007  | 06/08/2010 | SELF-ALIGNED PATTERNING METHOD BY USING NON-CONFORMAL<br>FILM AND ETCH BACK FOR FLASH MEMORY AND OTHER<br>SEMICONDUCTOR APPLICATIONS                                                                   |
| 8,035,153             | AF02691US DIV            | United States | 05/26/2010  | 10/11/2011 | SELF-ALIGNED PATTERNING METHOD BY USING NON-CONFORMAL<br>FILM AND ETCH FOR FLASH MEMORY AND OTHER SEMICONDUCTOR<br>APPLICATIONS                                                                        |
| 7,948,035             | AF02693US                | United States | 02/20/2008  | 05/24/2011 | DECODING SYSTEM CAPABLE OF CHARGING PROTECTION FOR<br>FLASH MEMORY DEVICES                                                                                                                             |
| 13/183,373            | AF02694.DIV              | United States | 07/14/2011  |            | A 3-D INTEGRATED CIRCUIT SYATEM AND MENTHOD                                                                                                                                                            |
| 7,998,846             | AF02694US                | United States | 09/12/2008  | 08/16/2011 | A 3-D INTEGRATED CIRCUIT SYATEM AND MENTHOD                                                                                                                                                            |
| 7,907,448             | AF02695                  | United States | 10/07/2008  | 03/15/2011 | SCALED DOWN SELECT GATES OF NAND FLASH MEMORY CELL<br>STRINGS AND METHOD OF FORMING SAME                                                                                                               |
| 12/105,208            | AF02696US                | United States | 04/17/2008  |            | USE OF SILICON RICH SILICON NITRIDE IN A MEMORY DEVICE                                                                                                                                                 |
| 7,848,146             | AF02697US                | United States | 03/19/2009  | 12/07/2010 | PARTIAL LOCAL SELF-BOOSTING OF A MEMORY CELL CHANNEL                                                                                                                                                   |
| 8,692,310             | AF02698US                | United States | 02/09/2009  | 04/08/2014 | GATE FRINGING EFFECT BASED CHANNEL FORMATION FOR<br>SEMICONDUCTOR DEVICE                                                                                                                               |
| 14/179,316            | AF02698US DIV            | United States | 02/12/2014  |            | GATE FRINGING EFFECT BASED CHANNEL FORMATION FOR<br>SEMICONDUCTOR DEVICE                                                                                                                               |
| 8,638,609             | AF02699US                | United States | 05/19/2010  | 01/28/2014 | PARTIAL LOCAL SELF BOOSTING FOR NAND                                                                                                                                                                   |
| 14/132,430            | AF02699US CON            | United States | 12/18/2013  |            | PARTIAL LOCAL SELF BOOSTING FOR NAND                                                                                                                                                                   |
| 12/240,627            | AF02700US                | United States | 09/29/2008  |            | MECHANICAL ENHANCEMENT OF NANO-POROUS ULTRA LOW<br>DIELECTRIC FILMS AS INTER LAYER DIELECTRIC MATERIALS FOR<br>40NM AND BEYOND NAND BACK-END-OF-LINE APPLICATION TO<br>REDUCE RC OR INTERCONNECT DELAY |
| 7,867,899             | AF02701US                | United States | 04/29/2008  | 01/11/2011 | WORDLINE RESISTANCE REDUCTION METHOD AND STRUCTURE IN<br>AN INTEGRATED CIRCUIT MEMORY DEVICE                                                                                                           |
| 12/961,379            | AF02701US DIV            | United States | 12/06/2010  |            | WORDLINE RESISTANCE REDUCTION METHOD AND STRUCTURE IN<br>AN INTEGRATED CIRCUIT MEMORY DEVICE                                                                                                           |
| 8,669,597             | AF02703US                | United States | 05/06/2008  | 03/11/2014 | MEMORY DEVICE INTERCONNECTS AND METHOD OF<br>MANUFACTURING                                                                                                                                             |
| 14/102,446            | AF02703US CON1           | United States | 12/10/2013  |            | MEMORY DEVICE INTERCONNECTS AND METHOD OF MANUFACTURE                                                                                                                                                  |
| 14/102,450            | AF02703US CON2           | United States | 12/10/2013  |            | MEMORY DEVICE INTERCONNECTS AND METHOD OF MANUFACTURE                                                                                                                                                  |
| 8,171,627             | AF02708US                | United States | 12/21/2007  | 05/08/2012 | METHOD OF FORMING AN ELECTRONIC DEVICE                                                                                                                                                                 |
| 8,643,083             | AF02708US DIV            | United States | 05/07/2012  | 02/04/2014 | ELECTRONIC DEVICES WITH ULTRAVIOLET BLOCKING LAYERS (as<br>amended)                                                                                                                                    |
| 8,003,306             | AF02718US                | United States | 12/17/2007  | 08/23/2011 | METHODS OF FORMING ELECTRONIC DEVICES BY ION IMPLANTING                                                                                                                                                |
| 12/879,936            | AF02722US                | United States | 09/10/2010  |            | APPARATUS AND METHOD FOR PROGRAMMABLE READ PREAMBLE                                                                                                                                                    |
| 7,915,169             | AF02731US                | United States | 11/02/2007  | 03/29/2011 | PROCESSES FOR FORMING ELECTRONIC DEVICES INCLUDING<br>POLISHING METAL-CONTAINING LAYERS                                                                                                                |
| 8,232,209             | AF02731US CON            | United States | 02/11/2011  | 07/31/2012 | PROCESSES FOR FORMING ELECTRONIC DEVICES INCLUDING<br>POLISHING METAL-CONTAINING LAYERS                                                                                                                |
| 8,179,153             | AF02739US                | United States | 07/17/2008  | 05/15/2012 | PROBE APPARATUS, A PROCESS OF FORMING A PROBE HEAD, AND A<br>PROCES OD FORMING AN ELECTRONIC DEVICE                                                                                                    |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                  |
|-----------------------|--------------------------|---------------|-------------|------------|----------------------------------------------------------------------------------------------------------------------------------------|
| 7,986,579             | AF02763US                | United States | 02/13/2008  | 07/26/2011 | MEMORY DEVICE AND METHOD THEREOF                                                                                                       |
| 7,791,947             | AF02764US                | United States | 01/10/2008  | 09/07/2010 | NON-VOLATILE MEMORY DEVICE AND METHODS OF USING                                                                                        |
| 12/366,519            | AF02765US                | United States | 02/05/2009  |            | FRACTURED ERASE SYSTEM AND METHOD                                                                                                      |
| 14/630,238            | AF02765US DIV            | United States | 02/24/2015  |            | FRACTURED ERASE SYSTEM AND METHOD                                                                                                      |
| 8,386,736             | AF02766US                | United States | 12/18/2008  | 02/26/2013 | NAND PROGRAM SEQUENCE REORDERING                                                                                                       |
| 13/764,602            | AF02766US CON            | United States | 02/11/2013  |            | RAPID MEMORY BUFFER WRITE STORAGE SYSTEM AND METHOD                                                                                    |
| 8,273,627             | AF02767US                | United States | 12/17/2008  | 09/25/2012 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING<br>THEREOF                                                                           |
| 7,835,172             | AF02770US                | United States | 10/01/2008  | 11/16/2010 | SYSTEM AND METHOD OF OPERATION FOR RESISTIVE CHANGE<br>MEMORY                                                                          |
| 10/449,414            | AF02801                  | United States | 06/02/2003  |            | NONVOLATILE SEMICONDUCT MEMORY DEVICE AND METHOD FOR<br>FABRICATING THE SAME                                                           |
| 6,507,068             | AF02806US                | United States | 09/25/1998  | 01/14/2003 | FLASH MEMORY DEVICE AND A FABRICATION PROCESS THEREOF                                                                                  |
| 7,894,238             | AF02812US                | United States | 10/17/2008  | 02/22/2011 | SEMICONDUCTOR MEMORY DEVICE WITH STACKED MEMORY CELL<br>STRUCTURE                                                                      |
| 8,289,750             | AF02812US CON            | United States | 01/12/2011  | 10/16/2012 | SEMICONDUCTOR MEMORY DEVICE FEATURING SELECTIVE DATA<br>STORAGE IN A STACKED MEMORY CELL                                               |
| 8,773,885             | AF02812US CON2           | United States | 09/19/2012  | 07/08/2014 | SEMICONDUCTOR MEMORY DEVICE FEATURING SELECTIVE DATA<br>STORAGE IN A STACKED MEMORY CELL STRUCTURE                                     |
| 8,938,655             | AF02814US                | United States | 12/20/2007  | 01/20/2015 | EXTENDING FLASH MEMORY DATA RETENTION VIA REWRITE<br>REFRESH                                                                           |
| 8,004,888             | AF02816US                | United States | 09/22/2008  | 08/23/2011 | FLASH MIRROR BIT ARCHITECTURE USING SINGLE PROGRAM AND<br>ERASE ENTITY AS LOGICAL CELL                                                 |
| 7,864,596             | AF02817US                | United States | 09/22/2008  | 01/04/2011 | SECTOR CONFIGURE REGISTERS FOR A FLASH DEVICE GENERATING<br>MULTIPLE VIRTUAL GROUND DECODING SCHEMES                                   |
| 7,881,105             | AF02818US                | United States | 09/22/2008  | 02/01/2011 | QUAD + BIT STORAGE IN TRAP BASED FLASH DESIGN USING SINGLE<br>PROGRAM AND ERASE ENTITY AS LOGICAL CELL                                 |
| 7,907,455             | AF02819US                | United States | 09/22/2008  | 03/15/2011 | HIGH VT STATE USED AS ERASE CONDITION IN TRAP BASED NOR<br>FLASH CELL DESIGN                                                           |
| 7,804,713             | AF02820US                | United States | 09/22/2008  | 09/28/2010 | EEPROM EMULATION IN FLASH DEVICE                                                                                                       |
| 7,791,954             | AF02821US                | United States | 09/22/2008  | 09/07/2010 | DYNAMIC ERASE STATE IN FLASH DEVICE                                                                                                    |
| 12/258,131            | AF02822US                | United States | 10/24/2008  |            | PACKAGE HAVING DUMMY METAL FOR LESS CURVE                                                                                              |
| 11/961,757            | AF02823US                | United States | 12/20/2007  |            | ELECTRONIC DEVICE INCLUDING A SILICON NITRIDE LAYER AND A<br>PROCESS OF FORMING THE SAME                                               |
| 8,700,830             | AF02824US                | United States | 11/20/2007  | 04/15/2014 | A MEMORY BUFFERING SYSTEM THAT IMPROVES READ/WRITE<br>PERFORMANCE AND PROVIDES LOW LATENCY FOR MOBILE<br>SYSTEMS                       |
| 14/250,113            | AF02824US CON            | United States | 04/10/2014  |            | MEMORY BUFFERING SYSTEM THAT IMPROVES READ/WRITE<br>PERFORMANCE AND PROVIDES LOW LATENCY FOR MOBILE<br>SYSTEMS                         |
| 7,840,900             | AF02833US                | United States | 04/30/2009  | 11/23/2010 | REPLACING RESET PIN IN BUSES WHILE GUARANTEEING SYSTEM<br>RECOVERY                                                                     |
| 8,359,423             | AF02834US                | United States | 03/14/2008  | 01/22/2013 | USING LPDDR1 BUS AS TRANSPORT LAYER TO COMMUNICATE TO<br>FLASH                                                                         |
| 7,630,250             | AF02850US                | United States | 10/16/2007  | 12/08/2009 | CONTROLLED RAMP RATES FOR METAL BITLINES DURING WRITE<br>OPERATIONS FROM HIGH VOLTAGE DRIVER FOR MEMORY<br>APPLICATIONS                |
| 7,619,932             | AF02851US                | United States | 12/18/2007  | 11/17/2009 | ALGORITHM FOR CHARGE LOSS REDUCTION AND VT DISTRIBUTION<br>IMPROVEMENT                                                                 |
| 7,785,973             | AF02853US                | United States | 01/25/2008  | 08/31/2010 | ELECTRONIC DEVICE INCLUDING A GATE ELECTRODE HAVING<br>PORTIONS WITH DIFFERENT CONDUCTIVITY TYPES AND A PROCESS<br>OF FORMING THE SAME |
| 8,310,008             | AF02853US DIV            | United States | 07/27/2010  | 11/13/2012 | ELECTRONIC DEVICE INCLUDING A GATE ELECTRODE HAVING<br>PORTIONS WITH DIFFERENT CONDUCTIVITY TYPES                                      |
| 7,830,716             | AF02854US                | United States | 06/06/2008  | 11/09/2010 | NON VOLATILE MEMORY STRING MODULE WITH BUFFER AND<br>METHOD                                                                            |
| 11/950,339            | AF02855US                | United States | 12/04/2007  |            | METHOD OF OPERATING A PROCESSING CHAMBER USED IN<br>FORMING ELECTRONIC DEVICES                                                         |
| 7,613,042             | AF02856US                | United States | 11/05/2007  | 11/03/2009 | DECODING SYSTEM CAPABLE OF REDUCING SECTOR SELECT AREA<br>OVERHEAD FOR FLASH MEMORY                                                    |
| 8,117,521             | AF02857US                | United States | 08/26/2008  | 02/14/2012 | IMPLEMENTATION OF RECYCLING UNUSED ECC PARITY BITS DURING<br>FLASH MEMORY PROGRAMING                                                   |
| 7,944,746             | AF02858US                | United States | 11/27/2007  | 05/17/2011 | ROOM TEMPERATURE DRIFT SUPPRESSION VIA SOFT PROGRAM<br>AFTER ERASE                                                                     |
| 8,445,913             | AF02861US                | United States | 10/30/2007  | 05/21/2013 | METAL-INSULATOR-METAL (MIM) DEVICE AND METHOD OF<br>FORMATION THEREOF                                                                  |
| 8,828,837             | AF02861US DIV            | United States | 04/19/2013  | 09/09/2014 | METAL-INSULATOR-METAL (MIM) DEVICE AND METHOD OF<br>FORMATION THEREOF                                                                  |
| 14/460,205            | AF02861US DIV2           | United States | 08/14/2014  |            | METAL-INSULATOR-METAL (MIM) DEVICE AND METHOD OF<br>FORMATION THEREOF                                                                  |
| 7,602,067             | AF02862US                | United States | 12/17/2007  | 10/13/2009 | HETERO-STRUCTURE VARIABLE SILICON RICHNESS NITRIDE FOR<br>MLC FLASH MEMORY DEVICE                                                      |
| 7,706,168             | AF02864US                | United States | 10/30/2007  | 04/27/2010 | IMPROVEMENT OF ERASE, PROGRAMMING AND LEAKAGE<br>CHARACTERISTICS OF A RESISTIVE MEMORY DEVICE                                          |
| 11/844,518            | AF02865US                | United States | 08/24/2007  |            | PROCESS OF FORMING AN ELECTRONIC DEVICE INCLUDING<br>DEPOSITING LAYERS WITHIN OPENINGS                                                 |
| 7,979,625             | AF02866US                | United States | 11/27/2007  | 07/12/2011 | SPI BANK ADDRESSING SCHEME FOR MEMORY DENSITIES ABOVE<br>128MB                                                                         |
| 7,984,284             | AF02867US                | United States | 11/27/2007  | 07/19/2011 | SPI AUTO-BOOT MODE                                                                                                                     |
| 7,932,131             | AF02868US                | United States | 11/05/2007  | 04/26/2011 | REDUCTION OF PACKAGE HEIGHT IN A STACKED DIE<br>CONFIGURATION                                                                          |
| 7,893,681             | AF02869US                | United States | 12/12/2008  | 02/22/2011 | ELECTRONIC CIRCUIT                                                                                                                     |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                     |
|-----------------------|---------------------------|---------------|-------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7,567,457             | AF02871US                 | United States | 10/30/2007  | 07/28/2009 | NONVOLATILE MEMORY ARRAY PARTITIONING ARCHITECTURE AND METHOD TO UTILIZE SINGLE LEVEL CELL, AND MULTI LEVEL CELLS WITHIN THE SAME MEMORY ARRAY            |
| 8,874,810             | AF02873US                 | United States | 11/21/2008  | 10/28/2014 | SYSTEM AND METHOD FOR READ DATA BUFFERING WHEREIN ANALYZING POLICY DETERMINES WHETHER TO DECREMENT OR INCREMENT THE COUNT OF INTERNAL OR EXTERNAL BUFFERS |
| 14/520,016            | AF02873US DIV             | United States | 10/21/2014  |            | STORAGE SYSTEM AND METHOD                                                                                                                                 |
| 61/004,434            | AF02873US PROV            | United States | 11/26/2007  |            | STORAGE SYSTEM AND METHOD                                                                                                                                 |
| 8,732,360             | AF02874US                 | United States | 11/21/2008  | 05/20/2014 | SYSTEM AND METHOD FOR ACCESSING MEMORY                                                                                                                    |
| 61/004,362            | AF02874US PROV            | United States | 11/26/2007  |            | SYSTEM AND METHOD FOR ACCESSING MEMORY                                                                                                                    |
| 61/004,412            | AF02875PROV               | United States | 11/26/2007  |            | A METHOD FOR SETTING PARAMETERS AND DETERMINING LATENCY IN A CHAINED DEVICE SYSTEM                                                                        |
| 8,930,593             | AF02875US                 | United States | 11/21/2008  | 01/06/2015 | METHOD FOR SETTING PARAMETERS AND DETERMINING LATENCY IN A CHAINED DEVICE SYSTEM                                                                          |
| 8,601,181             | AF02876US                 | United States | 11/21/2008  | 12/03/2013 | SYSTEM AND METHOD FOR READ DATA BUFFERING WHEREIN AN ARBITRATION POLICY DETERMINES WHETHER INTERNAL OR EXTERNAL BUFFERS ARE GIVEN PREFERENCE              |
| 61/004,361            | AF02876US PROV            | United States | 11/26/2007  |            | SYSTEMS AND METHODS FOR READ DATA BUFFERING                                                                                                               |
| 7,894,267             | AF02879                   | United States | 10/30/2007  | 02/22/2011 | DETERMINISTIC PROGRAMMING ALGORITHM THAT PROVIDES TIGHTER CELL DISTRIBUTIONS WITH A REDUCED NUMBER OF PROGRAMMING PULSES                                  |
| 7,995,385             | AF02880US                 | United States | 10/30/2007  | 08/09/2011 | MEMORY ARRAY OF PAIRS OF NONVOLATILE MEMORY CELLS USING FOWLER-NORDHEIM PROGRAMMING AND ERASING                                                           |
| 7,558,101             | AF02881US                 | United States | 12/14/2007  | 07/07/2009 | SCAN SENSING METHOD THAT IMPROVES SENSING MARGINS                                                                                                         |
| 8,040,738             | AF02882US                 | United States | 12/30/2008  | 10/18/2011 | MTHOD AND APPARATUS FOR PERFORMING SEMICONDUCTOR MEMORY OPERATIONS                                                                                        |
| 7,561,484             | AF02883US                 | United States | 12/13/2007  | 07/14/2009 | REFERENCE-FREE SAMPLED SENSING                                                                                                                            |
| 7,804,715             | AF02884US                 | United States | 05/05/2008  | 09/28/2010 | BITCELL CURRENT SENSE DEVICE AND METHOD THEREOF                                                                                                           |
| 7,787,313             | AF02885US                 | United States | 03/27/2008  | 08/31/2010 | A BITLINE VOLTAGE DRIVER                                                                                                                                  |
| 8,295,102             | AF02885US CON             | United States | 07/23/2010  | 10/23/2012 | A BITLINE VOLTAGE DRIVER                                                                                                                                  |
| 8,003,545             | AF02886US                 | United States | 02/14/2008  | 08/23/2011 | METHOD OF FORMING AN ELECTRONIC DEVICE INCLUDING FORMING FEATURES WITHIN A MASK AND A SELECTIVE REMOVAL PROCESS                                           |
| 8,409,952             | AF02887US                 | United States | 04/14/2008  | 04/02/2013 | METHOD OF FORMING AN ELECTRONIC DEVICE INCLUDING FORMING A CHARGE STORAGE ELEMENT IN A TRENCH OF A WORKPIECE                                              |
| 8,097,961             | AF02888US                 | United States | 12/22/2008  | 01/17/2012 | SEMICONDUCTOR DVICE HAVING A SIMPLIFIED STACK AND METHOD FOR MANUFACTURING THEREOF                                                                        |
| 8,361,857             | AF02888US DIV             | United States | 12/12/2011  | 01/29/2013 | SEMICONDUCTOR DEVICE HAVING A SIMPLIFIED STACK AND METHOD FOR MANUFACTURING THEREOF                                                                       |
| 7,675,805             | AF02892US                 | United States | 01/04/2008  | 03/09/2010 | TABLE LOOKUP VOLTAGE COMPENSATION FOR MEMORY CELLS                                                                                                        |
| 7,965,574             | AF02892US CON             | United States | 02/22/2010  | 06/21/2011 | TABLE LOOKUP VOLTAGE COMPENSATION FOR MEMORY CELLS                                                                                                        |
| 8,189,421             | AF02892US CON3            | United States | 05/13/2011  | 05/29/2012 | TABLE LOOKUP VOLTAGE COMPENSATION FOR MEMORY CELLS                                                                                                        |
| 8,456,941             | AF02892US CON3            | United States | 05/25/2012  | 06/04/2013 | TABLE LOOKUP VOLTAGE COMPENSATION FOR MEMORY CELLS                                                                                                        |
| 12/022,795            | AF02897US                 | United States | 01/30/2008  |            | ELECTRONIC DEVICE HAVING A DOPED REGION WITH A GROUP 13 ATOM                                                                                              |
| 7,761,740             | AF02898US                 | United States | 12/13/2007  | 07/20/2010 | POWER SAFE TRANSLATION TABLE OPERATION IN FLASH MEMORY                                                                                                    |
| 8,041,895             | AF02899US                 | United States | 01/28/2008  | 10/18/2011 | TRANSLATION TABLE CACHE COHERENCY MECHANISM USING CACHE WAY SET INDEX WRITE BUFFER                                                                        |
| 8,656,083             | AF02900US                 | United States | 12/21/2007  | 02/18/2014 | FREQUENCY DISTRIBUTED FLASH MEMORY ALLOCATION BASED ON FREE PAGE TABLES                                                                                   |
| 8,694,714             | AF02901US                 | United States | 01/18/2008  | 04/08/2014 | RETARGETING OF A WRITE OPERATION RETRY IN THE EVENT OF A WRITE OPERATION FAILURE                                                                          |
| 8,010,776             | AF02902US                 | United States | 12/17/2007  | 08/30/2011 | ADAPTIVE SYSTEM BOOT ACCELERATOR FOR COMPUTING SYSTEMS                                                                                                    |
| 8,261,006             | AF02903US                 | United States | 12/19/2007  | 09/04/2012 | EFFICIENT MEMORY HIERARCHY IN SOLID STATE DRIVE DESIGN                                                                                                    |
| 12/206,310            | AF02905US                 | United States | 09/08/2008  |            | PROCESS OF FABRICATING A WORKPIECE USING A TEST MASK                                                                                                      |
| 61/093,646            | AF02905US PROV            | United States | 09/02/2008  |            | PROCESS FOR FABRICATING A WORKPIECE USING A TEST MASK                                                                                                     |
| 8,774,400             | AF02907US                 | United States | 01/03/2008  | 07/08/2014 | METHOD FOR PROTECTING DATA AGAINST DIFFERENTIAL FAULT ANALYSIS INVOLVED IN RIVEST, SHAMIR AND ADELMAN CRYPTOGRAPHY USING THE CHINESE REMAINDER THEOREM    |
| 6,643,178             | AF02911US                 | United States | 07/31/2001  | 11/04/2003 | SYSTEM FOR SOURCE SIDE SENSING                                                                                                                            |
| 8,275,945             | AF02912US                 | United States | 02/05/2008  | 09/25/2012 | MITIGATION OF FLASH MEMORY LATENCY AND BANDWIDTH LIMITATIONS VIA A WRITE ACTIVITY LOG AND BUFFER                                                          |
| 14/269,299            | AF02912US CON             | United States | 05/05/2014  |            | MITIGATE FLASH WRITE LATENCY AND BANDWIDTH LIMITATION                                                                                                     |
| 8,756,376             | AF02912US DIV             | United States | 08/21/2012  | 06/17/2014 | MITIGATE FLASH WRITE LATENCY AND BANDWIDTH LIMITATION VIA CACHING AND DATA CAPACITY OF A BUFFER                                                           |
| 8,352,671             | AF02913US                 | United States | 02/05/2008  | 01/08/2013 | PARTIAL ALLOCATE PAGING MECHANISM USING A CONTROLLER AND A BUFFER                                                                                         |
| 13/709,479            | AF02913US CON             | United States | 12/10/2012  |            | PARTIAL ALLOCATE PAGING MECHANISM USING A CONTROLLER AND A BUFFER                                                                                         |
| 8,209,463             | AF02914US                 | United States | 02/05/2008  | 06/26/2012 | EXPANSION SLOTS FOR FLASH MEMORY BASED RANDOM ACCESS MEMORY SUBSYSTEM                                                                                     |
| 8,332,572             | AF02915US                 | United States | 02/05/2008  | 12/11/2012 | WEAR LEVELING MECHANISM USING A DRAM BUFFER                                                                                                               |
| 8,719,489             | AF02915US CON             | United States | 11/07/2012  | 05/06/2014 | HARDWARE BASED WEAR LEVELING MECHANISM                                                                                                                    |
| 8,228,679             | AF02918US                 | United States | 04/02/2008  | 07/24/2012 | CONNECTIONS FOR ELECTRONIC DEVICES ON DOUBLE-SIDED CIRCUIT BOARD                                                                                          |
| 7,902,520             | AF02921US                 | United States | 12/19/2008  | 03/08/2011 | RADIATION DETECTING ELECTRONIC DEVICE AND METHODS OF OPERATING                                                                                            |
| 8,738,840             | AF02922US                 | United States | 03/31/2008  | 05/27/2014 | OPERATING SYSTEM BASED DRAM AND FLASH MANAGEMENT                                                                                                          |
| 14/253,056            | AF02922US CON             | United States | 04/15/2014  |            | OPERATING SYSTEM BASED DRAM AND FLASH MANAGEMENT                                                                                                          |
| 7,838,342             | AF02932US                 | United States | 06/06/2008  | 11/23/2010 | MEMORY DEVICE AND METHOD                                                                                                                                  |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                  |
|-----------------------|--------------------------|---------------|-------------|------------|----------------------------------------------------------------------------------------------------------------------------------------|
| 7,983,089             | AF02933US                | United States | 06/06/2008  | 07/19/2011 | SENSE AMPLIFIER WITH CAPACITANCE-COUPLED DIFFERENTIAL SENSE AMPLIFIER                                                                  |
| 8,514,631             | AF02933US DIV            | United States | 06/07/2011  | 08/20/2013 | DETERMINING A LOGIC STATE BASED ON CURRENTS RECEIVED BY A SENSE AMPLIFIER                                                              |
| 8,563,441             | AF02937US                | United States | 04/28/2008  | 10/22/2013 | METHODS FOR FABRICATING MEMORY CELLS HAVING FIN STRUCTURES WITH SMOOTH SIDEWALLS AND ROUNDED TOP CORNERS AND EDGES                     |
| 8,404,549             | AF02944US                | United States | 11/06/2008  | 03/26/2013 | FABRICATING METHOD OF MIRROR BIT MEMORY DEVICE HAVING SPLIT ONO FILM WITH TOP OXIDE FILM FORMED BY OXIDATION PROCESS                   |
| 8,669,161             | AF02944US CON            | United States | 02/25/2013  | 03/11/2014 | FABRICATING METHOD OF MIRROR BIT MEMORY DEVICE HAVING SPLIT ONO FILM WITH TOP OXIDE FILM FORMED BY OXIDATION PROCESS                   |
| 8,610,199             | AF02944US DIV            | United States | 02/25/2013  | 12/17/2013 | FABRICATING METHOD OF MIRROR BIT MEMORY DEVICE HAVING SPLIT ONO FILM WITH TOP OXIDE FILM FORMED BY OXIDATION PROCESS                   |
| 8,370,644             | AF02946US                | United States | 05/30/2008  | 02/05/2013 | INSTANT HARDWARE ERASE MECHANISM FOR CONTENT RESET AND PSEUDO-RANDOM NUMBER GENERATION                                                 |
| 12/180,185            | AF02948US                | United States | 07/25/2008  |            | STACKED DIE PACKAGE HAVING REDUCED HEIGHT AND METHOD OF MAKING SAME                                                                    |
| 8,072,802             | AF02949US                | United States | 12/05/2008  | 12/06/2011 | MEMORY EMPLOYING REDUNDANT CELL ARRAY OF MULTI-BIT CELLS                                                                               |
| 7,849,229             | AF02953US                | United States | 11/25/2008  | 12/07/2010 | SPI ADDRESSING BEYOND 24-BITS                                                                                                          |
| 12/273,289            | AF02956US                | United States | 11/18/2008  |            | ELECTROPLATING APPARATUS AND METHOD WITH UNIFORMITY IMPROVEMENT                                                                        |
| 7,940,570             | AF02962US                | United States | 06/29/2009  | 05/10/2011 | EMPLOYING SEPARATE DYNAMIC REFERENCE AREAS                                                                                             |
| 7,961,519             | AF02966US                | United States | 06/29/2009  | 06/14/2011 | MEMORY EMPLOYING INDEPENDENT DYNAMIC REFERENCE AREAS                                                                                   |
| 12/489,226            | AF02968US                | United States | 06/22/2009  |            | NAND MEMORY CELL STRING HAVING A STACKED SELECT GATE STRUCTURE AND PROCESS FOR FORMING THE SAME                                        |
| 8,487,373             | AF02970US                | United States | 04/29/2009  | 07/16/2013 | SONOS MEMORY CELLS HAVING NON-UNIFORM TUNNEL OXIDE AND METHODS FOR FABRICATING SAME                                                    |
| 8,742,496             | AF02970US DIV            | United States | 06/17/2013  | 06/03/2014 | SONOS MEMORY CELLS HAVING NON-UNIFORM TUNNEL OXIDE AND METHODS FOR FABRICATING SAME                                                    |
| 8,790,751             | AF02974US                | United States | 04/16/2008  | 07/29/2014 | METHOD OF IMPROVING ADHESION OF DIELECTRIC CAP TO COPPER                                                                               |
| 8,271,737             | AF02975US                | United States | 05/27/2009  | 09/18/2012 | CACHE AUTO-FLUSH IN A SOLID STATE MEMORY DEVICE                                                                                        |
| 8,581,595             | AF02978US                | United States | 08/15/2008  | 11/12/2013 | METHOD FOR MEASURING FLASH MEMORY CELL CURRENT                                                                                         |
| 8,122,181             | AF02989US                | United States | 11/13/2008  | 02/21/2012 | SYSTEMS AND METHODS FOR ENHANCING A DATA STORE FOR HANDLING SEMANTIC INFORMATION                                                       |
| 7,969,816             | AF02990US                | United States | 08/26/2009  | 06/28/2011 | MEMORY DEVICE                                                                                                                          |
| 8,299,439             | AF02992US                | United States | 05/19/2009  | 10/30/2012 | RADIATION DETECTING DEVICE AND METHOD OF OPERATING                                                                                     |
| 8,581,203             | AF02992US DIV            | United States | 09/13/2012  | 11/12/2013 | RADIATION DETECTING DEVICE AND METHOD OF OPERATING                                                                                     |
| 12/110,974            | AF02993US                | United States | 04/28/2008  |            | METHODS FOR FABRICATING MEMORY CELLS HAVING FIN STRUCTURES WITH SEMICIRCULAR TOP SURFACES AND ROUNDED TOP CORNERS AND EDGES            |
| 12/340,295            | AF02994                  | United States | 12/19/2008  |            | NEUTRON DETECTOR FOR UBIQUITOUS MONITORING                                                                                             |
| 8,560,761             | AF02995US                | United States | 03/31/2008  | 10/15/2013 | MEMORY RESOURCE MANAGEMENT FOR A FLASH AWARE KERNEL                                                                                    |
| 8,745,311             | AF02996US                | United States | 03/31/2008  | 06/03/2014 | FLASH MEMORY USABILITY ENHANCEMENTS IN MAIN MEMORY APPLICATION                                                                         |
| 8,458,393             | AF02997US                | United States | 03/31/2008  | 06/04/2013 | FLASH MEMORY AND OPERATING SYSTEM KERNEL                                                                                               |
| 7,916,529             | AF02998US                | United States | 02/13/2009  | 03/29/2011 | PIN DIODE DEVICE AND ARCHITECTURE                                                                                                      |
| 7,848,167             | AF03000US                | United States | 10/21/2008  | 12/07/2010 | APPARATUS AND METHOD FOR GENERATING WIDE-RANGE REGULATED SUPPLY VOLTAGES FOR A FLASH MEMORY                                            |
| 12/556,199            | AF03004US                | United States | 09/09/2009  |            | VARIED SILICON RICHNESS SILICON NITRIDE FORMATION WITH ATOMIC LAYER DEPOSITION FOR NON-VOLATILE MEMORY DEVICES                         |
| 12/249,261            | AF03005US                | United States | 10/10/2008  |            | MULTI-LAYER GLOBAL BIT LINE APPROACH TO REDUCE RC                                                                                      |
| 8,085,588             | AF03012US                | United States | 04/30/2009  | 12/27/2011 | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREOF                                                                                        |
| 8,094,509             | AF03014US                | United States | 10/30/2008  | 01/10/2012 | APPARATUS AND METHOD FOR PLACEMENT OF BOOSTING CELL WITH ADAPTIVE BOOSTER SCHEME                                                       |
| 8,379,443             | AF03016US                | United States | 05/27/2009  | 02/19/2013 | CHARGE RETENTION FOR FLASH MEMORY BY MANIPULATING THE PROGRAM DATA METHODOLOGY                                                         |
| 8,255,777             | AF03017US                | United States | 02/10/2009  | 08/28/2012 | SYSTEMS AND METHODS FOR LOCATING ERROR BITS IN ENCODED DATA                                                                            |
| 12/253,207            | AF03018US                | United States | 10/16/2008  |            | SYSTEMS AND METHODS FOR DOWNLOADING CODE AND DATA INTO A SECURE NON-VOLATILE MEMORY                                                    |
| 12/231,369            | AF03019US                | United States | 09/02/2008  |            | NARROW WORD LINE FORMATION BY SIDEWALL NISi FORMATION AND SELECTIVE ETCHING FOR 22NM AND BEYOND                                        |
| 8,633,074             | AF03020US                | United States | 09/17/2008  | 01/21/2014 | ELECTRICALLY PROGRAMMABLE AND ERASABLE MEMORY DEVICE AND METHOD OF FABRICATION THEREOF                                                 |
| 14/153,900            | AF03020US CON            | United States | 01/13/2014  |            | ELECTRICALLY PROGRAMMABLE AND ERASEABLE MEMORY DEVICE                                                                                  |
| 8,735,960             | AF03021US                | United States | 11/17/2008  | 05/27/2014 | HIGH ULTRA VIOLET ABSORBANCE OXYNITRIDE FILM FOR IMPROVED LINE-TO-LINE LEAKAGE, SCALABILITY, AND DATA RETENTION IN FLASH MEMORY DEVICE |
| 12/286,149            | AF03022US                | United States | 09/29/2008  |            | RUTHENIUM INTERCONNECT WITH HIGH ASPECT RATIO CONTACT AND METHOD OF FABRICATION THEREOF                                                |
| 7,985,674             | AF03023US                | United States | 11/05/2008  | 07/26/2011 | SiH4 SOAK FOR LOW HYDROGEN SiN DEPOSITION TO IMPROVE FLASH MEMEORY DEVICE PERFORMANCE                                                  |
| 8,309,455             | AF03023US DIV            | United States | 06/08/1999  |            | SiH4 SOAK FOR LOW HYDROGEN SiN DEPOSITION TO IMPROVE FLASH MEMEORY DEVICE PERFORMANCE                                                  |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                 |
|-----------------------|--------------------------|---------------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------------|
| 09/327,419            | AF03023US DIV            | United States | 06/21/2011  | 11/13/2012 | NON-VOLATILE TRENCH SEMICONDUCTOR DEVICE                                                                                              |
| 8,391,070             | AF03031US                | United States | 12/02/2008  | 03/05/2013 | MOVING VERIFY PROGRAMMING TECHNIQUE FOR FLASH MEMORY DEVICES                                                                          |
| 5,679,599             | AF03032US                | United States | 06/22/1995  | 10/21/1997 | ISOLATION USING SELF ALIGNED TRENCH FORMATION AND CONVENTIONAL LOCOS                                                                  |
| 7,995,386             | AF03034US                | United States | 11/21/2008  | 08/09/2011 | APPLYING NEGATIVE GATE VOLTAGE TO WORDLINES ADJACENT TO WORLDLINE ASSOCIATED WITH READ OR VERIFY TO REDUCE ADJACENT WORLDLINE DISTURB |
| 7,821,840             | AF03035US                | United States | 11/24/2008  | 10/26/2010 | MULTI-PHASE PROGRAMMING OF MULTI-LEVEL MEMORY                                                                                         |
| 7,935,596             | AF03053US                | United States | 12/22/2008  | 05/03/2011 | HTO OFFSET AND BL TRENCH PROCESS FOR MEMORY DEVICE TO IMPROVE DEVICE PERFORMANCE                                                      |
| 8,330,209             | AF03053US DIV            | United States | 03/23/2011  | 12/11/2012 | HTO OFFSET AND BL TRENCH PROCESS FOR MEMORY DEVICE TO IMPROVE DEVICE PERFORMANCE                                                      |
| 8,653,581             | AF03054US                | United States | 12/22/2008  | 02/18/2014 | HTO OFFSET FOR LONG EFFECTIVE BETTER DEVICE PERFORMANCE                                                                               |
| 14/109,157            | AF03054US DIV            | United States | 12/17/2013  |            | HTO OFFSET FOR LONG EFFECTIVE BETTER DEVICE PERFORMANCE                                                                               |
| 7,943,983             | AF03055US                | United States | 12/22/2008  | 05/17/2011 | HTO OFFSET SPACER AND OFF PROCESS TO DEFINE INVENTION                                                                                 |
| 12/390,550            | AF03064US                | United States | 02/23/2009  |            | ADVANCED WORDLINE DISTURB REDUCTION USING BORN/INDIUM IMPLANT                                                                         |
| 8,067,314             | AF03073US                | United States | 04/15/2009  | 11/29/2011 | GATE TRIM PROCESS USING EITHER WET ETCH OR DRY ETCH APPROACH TO TARGET CD FOR SELECTED TRANSISTORS                                    |
| 8,409,994             | AF03073US DIV            | United States | 10/21/2011  | 04/02/2013 | GATE TRIM PROCESS USING EITHER WET ETCH OR DRY ETCH APPROACH TO TARGET CD FOR SELECTED TRANSISTORS                                    |
| 8,296,626             | AF03091US                | United States | 11/07/2008  | 10/23/2012 | ERROR CORRECTION FOR FLASH MEMORY                                                                                                     |
| 13/616,379            | AF03091US CON            | United States | 09/14/2012  |            | ERROR CORRECTION FOR FLASH MEMORY                                                                                                     |
| 12/433,159            | AF03093US                | United States | 04/30/2009  |            | DIRECT POINTER ACCESS AND XIP REDIRECTOR FOR EMULATION OF MEMORY-MAPPED DEVICES                                                       |
| 8,076,199             | AF03099US                | United States | 02/13/2009  | 12/13/2011 | METHOD AND DEVICE EMPLOYING POLYSILICON SCALING                                                                                       |
| 8,637,918             | AF03099US DIV            | United States | 11/10/2011  | 01/28/2014 | METHOD AND DEVICE EMPLOYING POLYSILICON SCALING                                                                                       |
| 7,951,704             | AF03100US CIP            | United States | 07/30/2009  | 05/31/2011 | MEMORY DVICE PERIPHERAL INTERCONNECTS AND METHOD OF MANUFACTURING                                                                     |
| 8,441,041             | AF03100US CIP DIV        | United States | 11/10/2010  | 05/14/2013 | MEMORY DEVICE PERIPHERAL INTERCONNECTS                                                                                                |
| 8,232,515             | AF03113US                | United States | 05/27/2009  | 07/31/2012 | IMAGING DEVICE                                                                                                                        |
| 8,436,289             | AF03113US CIP            | United States | 07/28/2010  | 05/07/2013 | SYSTEM AND METHOD FOR DETECTING PARTICLES WITH A SEMICONDUCTOR DEVICE                                                                 |
| 8,748,800             | AF03113US CIP            | United States | 03/05/2013  | 06/10/2014 | A CHARGE STORAGE DEVICE FOR DETECTING ALPHA PARTICLES (as amended)                                                                    |
| 8,803,066             | AF03113US CON            | United States | 07/24/2012  | 08/12/2014 | IMAGING DEVICE                                                                                                                        |
| 61/060,001            | AF03113US PROV           | United States | 06/09/2008  |            | IMAGING DEVICE                                                                                                                        |
| 61/060,002            | AF03114US                | United States | 06/09/2008  |            | IMAGING DEVICE                                                                                                                        |
| 8,680,671             | AF03135US                | United States | 01/28/2009  | 03/25/2014 | SELF-ALIGNED DOUBLE PATTERNING FOR MEMORY AND OTHER MICROELECTRONIC DEVICES                                                           |
| 14/204,373            | AF03135US CON            | United States | 03/11/2014  |            | SELF-ALIGNED DOUBLE PATTERNING FOR MEMORY AND OTHER MICROELECTRONIC DEVICES                                                           |
| 13/781,396            | AF03137US                | United States | 02/28/2013  |            | NON-VOLATILE MEMORY BASED RAM                                                                                                         |
| 8,357,563             | AF03209US                | United States | 08/10/2010  | 01/22/2013 | STITCH BUMP STACKING DESIGN FOR OVERALL PACKAGE SIZE REDUCTION FOR MULTIPLE STACK                                                     |
| 8,680,686             | AF03219US                | United States | 06/29/2010  | 03/25/2014 | METHOD AND SYSTEM FOR THINK MULTI CHIP STACK PACKAGE WITH FILM ON WIRE AND COPPER WIRE                                                |
| 8,617,983             | AF03634US CON2           | United States | 09/10/2012  | 12/31/2013 | LOCAL INTERCONNECT HAVING INCREASED MISALIGNMENT TOLERANCE                                                                            |
| 6,794,248             | AF04000US                | United States | 10/25/2002  | 09/21/2004 | METHOD OF FABRICATING SEMICONDUCTOR MEMORY DEVICE AND SEMICONDUCTOR MEMORY DEVICE DRIVER                                              |
| 7,189,659             | AF04007US                | United States | 11/13/2003  | 03/13/2007 | Method for fabricating a semiconductor device                                                                                         |
| 7,063,991             | AF04009KR                | United States | 07/28/2004  | 06/20/2006 | METHODS OF DETERMINING CHARACTERISTICS OF DOPED REGIONS ON DEVICE WAFERS, AND SYSTEM FOR ACCOMPLISHING SAME                           |
| 7,410,857             | AF04010US                | United States | 08/29/2003  | 08/12/2008 | SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD THEREOF                                                                          |
| 8,116,142             | AF04010US DIV            | United States | 09/06/2005  | 02/14/2012 | METHOD AND CIRCUIT FOR ERASING A NON-VOLATILE MEMORY CELL                                                                             |
| 6,329,257             | AF04016JP                | United States | 12/19/1997  | 12/11/2001 | METHOD FOR LATERALLY PEAKED SOURCE DURING PROFILES FOR BETTER ERASE CONTROL IN FLASH MEMORY DEVICES                                   |
| 11/595,309            | AF04017US                | United States | 11/09/2006  |            | NROM STORAGE DEVICES BASED ON RESONANT TUNNELING                                                                                      |
| 11/595,426            | AF04018US                | United States | 11/09/2006  |            | NON-VOLATILE MEMORY ON RESONANT TUNNELING DEVICES                                                                                     |
| 11/595,724            | AF04019US                | United States | 11/09/2006  |            | SRAM CIRCUIT HAVING A SONOS-BASED NAND DEVICE                                                                                         |
| 7,515,478             | AF04021US                | United States | 08/20/2007  | 04/07/2009 | CMOS LOGIC COMPATIBLE NON-VOLATILE MEMORY CELL STRUCTURE, OPERATION, AND ARRAY CONFIGURATION                                          |
| 6,477,083             | AF04022US                | United States | 10/11/2000  | 11/05/2002 | BANK SELECTOR CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                    |
| 61/195,743            | AF04023                  | United States | 10/10/2008  |            | SENONE SCORING UNIT FOR SPEECH RECOGNITION                                                                                            |
| 13/123,698            | AF04028US                | United States | 10/07/2009  |            | REAL-TIME DATA PATTERN ANALYSIS SYSTEM AND METHOD OF OPERATION THEREOF                                                                |
| 6,826,107             | AF04029JP                | United States | 08/01/2002  | 11/30/2004 | HIGH VOLTAGE INSERTION IN FLASH MEMORY CARDS                                                                                          |
| 8,327,052             | AF04030TW                | United States | 12/23/2009  | 12/04/2012 | VARIABLE READ LATENCY ON A SERIAL MEMORY BUS                                                                                          |
| 11/251,068            | AF04031US                | United States | 10/14/2005  |            | NON-VOLATILE MEMORY AND SRAM BASED ON RESONANT TUNNELING DEVICES                                                                      |
| 11/595,038            | AF04032US                | United States | 11/09/2006  |            | SONOS-BASED NAND DEVICES BASED ON RESONANT TUNNELING                                                                                  |
| 11/595,237            | AF04033US                | United States | 11/09/2006  |            | SRAM DEVICES BASED ON RESONANT TUNNELING                                                                                              |
| 60/718,089            | AF04034JP                | United States | 09/16/2005  |            | NON-VOLATILE MEMORY AND PSEUDO-SRAM BASED ON RESONANT TUNNELING CONCEPT                                                               |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                   |
|-----------------------|--------------------------|---------------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13/490,124            | AF04035US                | United States | 06/06/2012  |            | ACOUSTIC PROCESSING UNIT INTERFACE                                                                                                                      |
| 8,924,453             | AF04036US                | United States | 06/06/2012  | 12/30/2014 | ARITHMETIC LOGIC UNIT ARCHITECTURE                                                                                                                      |
| 14/048,076            | AF04041JP                | United States | 10/08/2013  |            | METHODS CIRCUITS APPARATUSES AND SYSTEMS FOR PROVIDING CURRENT TO A NON-VOLATILE MEMORY ARRAY AND NON-VOLATILE MEMORY DEVICES PRODUCED ACCORDINGLY      |
| 11/764,736            | AF04042TW                | United States | 06/18/2007  |            | CMOS COMPATIBLE SINGLE-POLY NON-VOLATILE MEMORY                                                                                                         |
| 14/073,914            | AF04045DE                | United States | 11/07/2013  |            | METHODS CIRCUITS APPARATUSES AND SYSTEMS FOR SENSING A LOGICAL STATE OF A NON-VOLATILE MEMORY CELL AND NON-VOLATILE MEMORY DEVICES PRODUCED ACCORDINGLY |
| 8,208,300             | AF04049US                | United States | 01/08/2009  | 08/26/2012 | NON-VOLATILE MEMORY CELL WITH INJECTOR                                                                                                                  |
| 7,415,318             | AF04051JP                | United States | 10/10/2003  | 08/19/2008 | METHOD AND APPARATUS FOR MANUFACTURING SEMICONDUCTOR DEVICE                                                                                             |
| 7,253,046             | AF04052TW                | United States | 08/29/2003  | 08/07/2007 | SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD THEREOF                                                                                            |
| 13/769,403            | AF04053JP                | United States | 02/18/2013  |            | APPARATUS AND METHODS TO REDUCE BIT LINE DISTURBS                                                                                                       |
| 8,236,693             | AF04055US                | United States | 05/15/2007  | 08/07/2012 | METHODS OF FORMING SILICIDES OF DIFFERENT THICKNESSES ON DIFFERENT STRUCTURES                                                                           |
| 8,915,775             | AF04056US                | United States | 04/24/2007  | 12/23/2014 | EXHAUST SYSTEM                                                                                                                                          |
| 7,884,630             | AF04057US                | United States | 03/13/2008  | 02/08/2011 | IC CARRIER, IC SOCKET AND METHOD FOR TESTING IC DEVICE                                                                                                  |
| 8,026,169             | AF04058US                | United States | 11/06/2006  | 09/27/2011 | CU ANNEALING FOR IMPROVED DATA RETENTION IN FLASH MEMORY DEVICES                                                                                        |
| 8,928,397             | AF04059US                | United States | 08/01/2012  | 01/06/2015 | SEMICONDUCTOR DEVICE AND VOLTAGE DIVIDER                                                                                                                |
| 8,345,483             | AF04061US                | United States | 01/21/2011  | 01/01/2013 | SYSTEM AND METHOD FOR ADDRESSING THRESHOLD VOLTAGE SHIFTS OF MEMORY CELLS IN AN ELECTRONIC PRODUCT                                                      |
| 12/034,410            | AF04062US                | United States | 02/20/2008  |            | DEVICE AND METHOD FOR PREVENTING LOST SYNCHRONIZATION                                                                                                   |
| 12/213,871            | AF04063US                | United States | 06/25/2008  |            | SIMULATION OF PROGRAM EXECUTION TO DETECT PROBLEM SUCH AS DEADLOCK                                                                                      |
| 7,125,763             | AMD-E306                 | United States | 06/19/2001  | 10/24/2006 | SILICIDED BURIED BITLINE PROCESS FOR A NON-VOLATILE MEMORY CELL                                                                                         |
| 5,468,981             | B001US                   | United States | 09/01/1994  | 11/21/1995 | A SELF-ALIGNED BURIED CHANNEL/JUNCTION STACKED GATE FLASH MEMORY CELL                                                                                   |
| 08/764,735            | B001US CON               | United States | 12/06/1996  |            | A SELF-ALIGNED BURIED CHANNEL/JUNCTION STACKED GATE FLASH MEMORY CELL                                                                                   |
| 08/451,293            | B001US DIV               | United States | 05/26/1995  |            | A SELF-ALIGNED BURIED CHANNEL/JUNCTION STACKED GATE FLASH MEMORY CELL                                                                                   |
| 5,574,685             | B002US                   | United States | 09/01/1994  | 11/12/1996 | A Self-Aligned Buried Channel/Junction Stacked Gate Flash Memory Cell                                                                                   |
| 08/451,897            | B002US DIV               | United States | 05/22/1995  |            | A SELF-ALIGNED BURIED CHANNEL/JUNCTION STACKED GATE FLASH MEMORY CELL                                                                                   |
| 08/342,174            | B011/2097US              | United States | 11/18/1994  |            | NITRIDE ETCH PROCESS WITH CRITICAL DIMENSION (CD) GAIN                                                                                                  |
| 6,593,245             | B011/2097US CON          | United States | 08/01/1996  | 07/15/2003 | SILICON NITRIDE ETCH PROCESS WITH CRITICAL DIMENSION GAIN                                                                                               |
| 5,485,423             | B012US                   | United States | 10/11/1994  | 01/16/1996 | METHOD FOR ELIMINATION OF CYCLING INDUCED ELECTRON TRAPPING IN THE TUNNELING OXIDE OF 5V ONLY FLASH EPROMS                                              |
| 5,534,731             | B015/2104US              | United States | 10/28/1994  | 07/09/1996 | LAYERED LOW DIELECTRIC CONSTANT TECHNOLOGY                                                                                                              |
| 5,693,566             | B015/2104US DIV          | United States | 06/02/1995  | 12/02/1997 | LAYERED LOW DIELECTRIC CONSTANT TECHNOLOGY                                                                                                              |
| 5,726,920             | B020US                   | United States | 09/29/1995  | 03/10/1998 | WATCHDOG SYSTEM OF HAVING DIFFERENTIATING MEANS FOR USE IN MONITORING OF SEMICONDUCTOR WAFER TESTING LINE                                               |
| 5,656,521             | B023US                   | United States | 01/12/1995  | 08/12/1997 | METHOD OF ERASING UPROM TRANSISTORS                                                                                                                     |
| 5,481,494             | B037US                   | United States | 12/22/1994  | 01/02/1996 | TIGHTENING VT DISTRIBUTION OF 5V ONLY FLASH EPROM BY RECONSTRUCTING CONSTANT ERASE BIAS CONDITION                                                       |
| 5,491,657             | B038US                   | United States | 02/24/1995  | 02/13/1996 | METHODS FOR BULK (OR BYTE) CHARGING & DISCHARGING AN ARRAY OF FLASH EEPROM MEMORY CELLS                                                                 |
| 5,550,405             | B047US                   | United States | 12/21/1994  | 08/27/1996 | NOVEL PROCESSING TECHNIQUES FOR ACHIEVING PRODUCTION WORTHY LOW DIELECTRIC LOW INTERCONNECT RESISTANCE AND HIGH PERFORMANCE                             |
| 5,965,934             | B047US CON               | United States | 07/22/1996  | 10/12/1999 | NOVEL PROCESSING TECHNIQUES FOR ACHIEVING PRODUCTION WORTHY, LOW DIELECTRIC, LOW INTERCONNECT RESISTANCE AND HIGH PERFORMANCE ICS                       |
| 5,679,608             | B047US DIV               | United States | 06/05/1995  | 10/21/1997 | NOVEL PROCESSING TECHNIQUES FOR ACHIEVING PRODUCTION WORTHY LOW DIELECTRIC LOW INTERCONNECT RESISTANCE AND HIGH PERFORMANCE                             |
| 5,482,881             | B052US                   | United States | 03/14/1995  | 01/09/1996 | FLASH EEPROM MEMORY WITH REDUCED COLUMN LEAKAGE CURRENT AND METHOD THEREFOR                                                                             |
| 5,652,447             | B052US CON               | United States | 07/22/1996  | 07/29/1997 | FLASH EEPROM MEMORY WITH REDUCED COLUMN LEAKAGE CURRENT AND METHOD THEREFOR                                                                             |
| 08/465,069            | B052US DIV               | United States | 06/05/1995  |            | FLASH EEPROM MEMORY WITH REDUCED COLUMN LEAKAGE CURRENT AND METHOD THEREFOR                                                                             |
| 5,617,357             | B053/2124US              | United States | 04/07/1995  | 04/01/1997 | FLASH EEPROM MEMORY WITH IMPROVED DISCHARGE SPEED USING SUBSTRATE BIAS AND METHOD THEREFOR                                                              |
| 5,708,588             | B053/2124US DIV          | United States | 06/05/1995  | 01/13/1998 | FLASH EEPROM MEMORY WITH IMPROVED DISCHARGED SPEED USING SUBSTRATE BIAS AND METHOD THEREFOR                                                             |
| 5,680,345             | B055US                   | United States | 06/06/1995  | 10/21/1997 | NONVOLATILE MEMORY CELL WITH VERTICAL GATE OVERLAP AND ZERO BIRDS BEAK                                                                                  |
| 5,661,055             | B055US DIV1              | United States | 06/07/1995  | 08/26/1997 | METHOD OF MAKING NONVOLATILE MEMORY CELL WITH VERTICAL GATE OVERLAP AND ZERO BIRD'S BEAKS                                                               |
| 6,248,629             | B090US                   | United States | 03/18/1998  | 06/19/2001 | PROCESS FOR FABRICATING A FLASH MEMORY DEVICE                                                                                                           |
| 08/480,876            | B091/2143US              | United States | 06/07/1995  |            | SIMPLIFIED PROCESS FOR FABRICATING FLASH EEPROM CELLS                                                                                                   |
| 5,776,811             | B091/2143US DIV          | United States | 01/04/1996  | 07/07/1998 | SIMPLIFIED PROCESS FOR FABRICATING FLASH EEPROM CELLS                                                                                                   |
| 5,945,705             | B100US                   | United States | 08/01/1995  | 08/31/1999 | THREE-DIMENSIONAL NON-VOLATILE MEMORY                                                                                                                   |
| 6,043,122             | B100US DIV               | United States | 08/01/1995  | 03/28/2000 | THREE-DIMENSIONAL NON-VOLATILE MEMORY                                                                                                                   |
| 5,552,331             | B111US                   | United States | 07/11/1995  | 09/03/1996 | PROCESS FOR SELF-ALIGNED SOURCE FOR HIGH DENSITY MEMORY                                                                                                 |
| 08/440,046            | B117US                   | United States | 05/12/1995  |            | SYSTEM FOR A CONSTANT FIELD ERASURE IN A FLASH EPROM                                                                                                    |
| 5,629,893             | B117US CON1              | United States | 04/18/1996  | 05/13/1997 | SYSTEM FOR A CONSTANT FIELD ERASURE IN A FLASH EPROM                                                                                                    |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                 |
|-----------------------|--------------------------|---------------|-------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5,805,502             | B117US CON2              | United States | 02/04/1997  | 09/08/1998 | SYSTEM FOR A CONSTANT FIELD ERASURE IN A FLASH EPROM                                                                                                                  |
| 5,596,531             | B121/2203US              | United States | 05/25/1995  | 01/21/1997 | A METHOD FOR DECREASING THE DISCHARGE TIME OF A FLASH EPROM CELL NORDHEIM DISCHARGED OPERATION                                                                        |
| 5,629,892             | B128US                   | United States | 10/16/1995  | 05/13/1997 | A FLASH EEPROM MEMORY WITH SEPARATE REFERENCE ARRAY                                                                                                                   |
| 5,553,018             | B129/2219US              | United States | 06/07/1995  | 09/03/1996 | NON VOLATILE MEMORY CELL FORMED USING SELF ALIGNED SOURCE IMPLANT                                                                                                     |
| 5,656,513             | B129/2219US DIV          | United States | 06/07/1995  | 08/12/1997 | NONVOLATILE MEMORY CELL FORMED USING SELF-ALIGNED SOURCE IMPLANT                                                                                                      |
| 5,590,076             | B132US                   | United States | 06/21/1995  | 12/31/1996 | CHANNEL HOT CARRIER PAGE WRITE                                                                                                                                        |
| 08/751,455            | B132US CON               | United States | 11/18/1996  |            | CHANNEL HOT CARRIER PAGE WRITE                                                                                                                                        |
| 5,579,261             | B137US                   | United States | 04/21/1995  | 11/26/1996 | REDUCED COLUMN LEAKAGE DURING PROGRAMMING FOR A FLASH MEMORY ARRAY                                                                                                    |
| 5,650,964             | B153/2241US              | United States | 06/07/1995  | 07/22/1997 | METHOD OF INHIBITING DEGRADATION OF ULTRA SHORT CHANNEL CHARGE-CARRYING DEVICES DURING DISCHARGE                                                                      |
| 5,907,561             | B169/2255US              | United States | 12/17/1997  | 05/25/1999 | METHOD TO IMPROVE TESTING SPEED OF MEMORY                                                                                                                             |
| 5,814,853             | B192US                   | United States | 01/22/1996  | 09/29/1998 | SOURCELESS FLOATING GATE MEMORY DEVICE AND METHOD OF STORING DATA                                                                                                     |
| 5,789,295             | B215US                   | United States | 11/17/1995  | 08/04/1998 | METHOD OF ELIMINATING OR REDUCING POLY 1 OXIDATION AT STACKED GATE EDGE IN FLASH EPROM PROCESS                                                                        |
| 5,608,672             | B216US                   | United States | 09/26/1995  | 03/04/1997 | CORRECTION METHOD LEADING TO A UNIFORM THRESHOLD VOLTAGE DISTRIBUTION FOR A FLASH EPROM                                                                               |
| 5,831,901             | B222US                   | United States | 11/08/1996  | 11/03/1998 | A METHOD OF PROGRAMMING A MEMORY CELL TO CONTAIN MULTIPLE VALUES                                                                                                      |
| 5,981,364             | B225US                   | United States | 09/30/1998  | 11/09/1999 | METHOD OF FORMING A SILICON GATE TO PRODUCE SILICON DEVICES WITH IMPROVED PERFORMANCE                                                                                 |
| 5,869,385             | B226US                   | United States | 12/08/1995  | 02/09/1999 | SELECTIVELY OXIDIZED FIELD OXIDE REGION                                                                                                                               |
| 09/196,105            | B226US DIV               | United States | 11/20/1998  |            | SELECTIVELY OXIDIZED FIELD OXIDE REGION                                                                                                                               |
| 5,638,326             | B232US                   | United States | 04/05/1996  | 06/10/1997 | PARALLEL PAGE BUFFER VERIFY OR READ OF CELLS ON A WORD LINE USING A SIGNAL FROM A REFERENCE CELL IN A FLASH MEMORY DEVICE                                             |
| 5,923,063             | B238US                   | United States | 02/19/1998  | 07/13/1999 | DOUBLE DENSITY V NONVOLATILE MEMORY CELL                                                                                                                              |
| 5,724,284             | B247US                   | United States | 06/24/1996  | 03/03/1998 | A MULTI-LEVEL FLASH SHIFT REGISTER PAGE BUFFER                                                                                                                        |
| 08/668,795            | B247US                   | United States | 06/24/1996  |            | A METHOD FOR DOUBLE DENSITY FLASH EPROM WITH PAGE MODE PROGRAM AND READ                                                                                               |
| 5,754,475             | B247US CON               | United States | 06/27/1997  | 05/19/1998 | A BIT LINE DISCHARGE METHOD FOR READING A MULTIPLE BITS-PER-CELL FLASH EPROM                                                                                          |
| 5,712,815             | B248US                   | United States | 04/22/1996  | 01/27/1998 | A METHOD FOR PAGE MODE PROGRAMMING MULTI-DENSITY FLASH EPROM                                                                                                          |
| 5,763,307             | B250US                   | United States | 11/08/1996  | 06/09/1998 | A BLOCK SELECT TRANSISTOR AND METHOD OF FABRICATION                                                                                                                   |
| 5,680,348             | B255US                   | United States | 12/01/1995  | 10/21/1997 | POWER SUPPLY INDEPENDENT CURRENT SOURCE FOR FLASH EPROM ERASE                                                                                                         |
| 08/559,705            | B257US                   | United States | 02/15/1996  |            | LOW SUPPLY VOLTAGE NEGATIVE CHARGE PUMP                                                                                                                               |
| 5,973,979             | B257US CON               | United States | 12/26/1996  | 10/26/1999 | LOW SUPPLY VOLTAGE NEGATIVE CHARGE PUMP                                                                                                                               |
| 5,708,387             | B258US                   | United States | 11/17/1995  | 01/13/1998 | A FAST 3 STATE BOOSTER CIRCUIT                                                                                                                                        |
| 5,644,531             | B260US                   | United States | 11/01/1995  | 07/01/1997 | A NEW PROGRAM ALGORITHM FOR LOW VOLTAGE (3V) SINGLE POWER SUPPLY FLASH MEMORIES                                                                                       |
| 5,642,311             | B261US                   | United States | 10/24/1995  | 06/24/1997 | A PROGRAM ERASE ALGORITHM THAT GREATLY REDUCES UNDER ERASE IN FLASH MEMORIES                                                                                          |
| 5,650,966             | B262US                   | United States | 11/01/1995  | 07/22/1997 | TEMPERATURE COMPENSATED REFERENCE FOR OVER ERASE CORRECTION CIRCUITRY                                                                                                 |
| 5,939,763             | B277US                   | United States | 09/05/1996  | 08/17/1999 | AN IMPROVED ULTRATHIN OXYNITRIDE STRUCTURE AND PROCESS FOR VLSI APPLICATIONS                                                                                          |
| 6,245,689             | B277US DIV               | United States | 09/08/1998  | 06/12/2001 | NOVEL PROCESS FOR RELIABLE ULTRATHIN OXYNITRIDE FORMATION                                                                                                             |
| 5,854,108             | B287US                   | United States | 06/04/1996  | 12/29/1998 | A METHOD AND SYSTEM FOR PROVIDING A DOUBLE DIFFUSE IMPLANT JUNCTION IN A VERY SHORT CHANNEL FLASH DEVICE                                                              |
| 6,492,675             | B291US                   | United States | 01/16/1998  | 12/10/2002 | FLASH MEMORY ARRAY WITH DUAL FUNCTION CONTROL LINES AND ASYMMETRICAL SOURCE AND DRAIN JUNCTIONS                                                                       |
| 6,744,668             | B291US DIV               | United States | 09/03/2002  | 06/01/2004 | FLASH MEMORY ARRAY WITH DUAL FUNCTION CONTROL LINES AND ASYMMETRICAL SOURCE AND DRAIN JUNCTIONS                                                                       |
| 5,675,537             | B315US                   | United States | 08/22/1996  | 10/07/1997 | ERASE METHOD FOR PAGE MODE MULTIPLE-BITS-PER-CELL FLASH EEPROM                                                                                                        |
| 5,859,796             | B319US                   | United States | 12/16/1997  | 01/12/1999 | PROGRAMMING OF MEMORY CELLS USING CONNECTED FLOATING GATE ANALOG REFERENCE CELL                                                                                       |
| 5,747,882             | C018196US                | United States | 11/07/1996  | 05/05/1998 | METHOD OF PREVENTING TUNGSTEN SILICIDE LIFTING FROM UNDERNEATH POLYSILICON FILM                                                                                       |
| 5,818,082             | C019196US                | United States | 03/04/1996  | 10/06/1998 | E2PROM DEVICE HAVING ERASE GATE IN OXIDE ISOLATION REGION IN SHALLOW TRENCH AND METHOD OF MANUFACTURE THEREOF                                                         |
| 5,751,633             | C023196US                | United States | 05/24/1996  | 05/12/1998 | METHOD OF SCREENING HOT TEMPERATURE ERASE REJECTS AT ROOM TEMPERATURE                                                                                                 |
| 5,870,407             | C024196US                | United States | 05/24/1996  | 02/09/1999 | METHOD OF SCREENING MEMORY CELLS AT ROOM TEMPERATURE THAT WOULD BE REJECTED DURING HOT TEMPERATURE PROGRAMMING TESTS                                                  |
| 5,856,946             | C051296US                | United States | 06/17/1998  | 01/05/1999 | MEMORY CELL PROGRAMMING WITH CONTROLLED CURRENT INJECTION                                                                                                             |
| 5,852,582             | C053296US                | United States | 02/18/1997  | 12/22/1998 | NON-VOLATILE STORAGE DEVICE REFRESH TIME DETECTOR METHODS AND SORT FLOW TO ACHIEVE TIGHT FLASH MEMORY ARRAY PROGRAM/ERASE SPEED AND INSENSITIVE TO PROCESS VARIATIONS |
| 5,793,249             | C054296US                | United States | 09/30/1996  | 08/11/1998 | HIGH VOLTAGE CMOS LEVEL SHIFTER                                                                                                                                       |
| 5,821,800             | C061296US                | United States | 02/11/1997  | 10/13/1998 | BIAS SCHEME OF PROGRAM INHIBIT FOR RANDOM PROGRAMMING IN NAND FLASH MEMORY                                                                                            |
| 5,715,194             | C071296US                | United States | 07/24/1996  | 02/03/1998 |                                                                                                                                                                       |

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| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                          |
|-----------------------|--------------------------|---------------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 5,793,677             | C072296US                | United States | 06/17/1996  | 08/11/1998 | USING FLOATING GATE DEVICES AS SELECT GATE DEVICES FOR NAND FLASH MEMORY AND ITS BIAS SCHEME                                                                                   |
| 6,271,151             | C126496US                | United States | 06/30/1997  | 08/07/2001 | METHOD AND APPARATUS FOR CONTROLLING THE THICKNESS OF A GATE OXIDE IN A SEMICONDUCTOR MANUFACTURING PROCESS                                                                    |
| 09/756,123            | C126496US CON            | United States | 01/09/2001  |            | METHOD AND APPARATUS FOR CONTROLLING THE THICKNESS OF A GATE OXIDE IN A SEMICONDUCTOR MANUFACTURING PROCESS                                                                    |
| 6,187,092             | C126496US DIV1           | United States | 03/03/1998  | 02/13/2001 | METHOD AND APPARATUS FOR CONTROLLING THE THICKNESS OF A GATE OXIDE IN A SEMICONDUCTOR MANUFACTURING PROCESS                                                                    |
| 5,912,489             | C141496US                | United States | 09/30/1997  | 06/15/1999 | A DUAL SOURCE SIDE POLYSILICON SELECT GATE STRUCTURE AND PROGRAMMING METHOD UTILIZING SINGLE TUNNEL OXIDE FOR NAND ARRAY FLASH MEMORY                                          |
| 5,999,452             | C141496US DIV1           | United States | 04/21/1998  | 12/07/1999 | A DUAL SOURCE SIDE POLYSILICON SELECT GATE STRUCTURE AND PROGRAMMING METHOD UTILIZING SINGLE TUNNEL OXIDE FOR NAND ARRAY FLASH MEMORY                                          |
| 6,266,275             | C141496US DIV2           | United States | 09/30/1999  | 07/24/2001 | A DUAL SOURCE SIDE POLYSILICON SELECT GATE STRUCTURE AND PROGRAMMING METHOD UTILIZING SINGLE TUNNEL OXIDE FOR NAND ARRAY FLASH MEMORY                                          |
| 5,801,579             | C144496US                | United States | 02/28/1997  | 09/01/1998 | HIGH VOLTAGE NMOS PASS GATE FOR INTEGRATED CIRCUIT WITH HIGH VOLTAGE GENERATOR                                                                                                 |
| 5,852,576             | C144496US CIP1           | United States | 10/06/1997  | 12/22/1998 | HIGH VOLTAGE NMOS PASS GATE FOR INTEGRATED CIRCUIT WITH HIGH VOLTAGE GENERATOR AND FLASH NON-VOLATILE MEMORY DEVICE HAVING THE PASS GATE                                       |
| 5,805,499             | C157596US                | United States | 02/28/1997  | 09/08/1998 | CHANNEL HOT-CARRIER PAGE WRITE FOR NAND APPLICATIONS                                                                                                                           |
| 5,889,697             | C171596US                | United States | 10/08/1997  | 03/30/1999 | MEMORY CELL FOR STORING AT LEAST THREE LOGIC STATES                                                                                                                            |
| 5,796,651             | C184596US                | United States | 05/19/1997  | 08/18/1998 | A MEMORY DEVICE USING A REDUCED WORD LINE VOLTAGE DURING READ OPERATIONS AND A METHOD OF ACCESSING SUCH A MEMORY DEVICE                                                        |
| 6,163,478             | C191596US                | United States | 10/19/1999  | 12/19/2000 | COMMON FLASH INTERFACE IMPLEMENTATION FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE                                                                                         |
| 5,790,456             | C194596US                | United States | 05/09/1997  | 08/04/1998 | MULTIPLE BITS-PER-CELL FLASH EPROM MEMORY CELL WITH WIDE PROGRAM AND ERASE VT WINDOW                                                                                           |
| 5,933,730             | C195596US                | United States | 03/07/1997  | 08/03/1999 | METHOD OF SPACER FORMATION AND SOURCE PROTECTION AFTER SELF-ALIGNED SOURCE FORMED AND A DEVICE PROVIDED BY SUCH A METHOD                                                       |
| 6,160,317             | C195596US DIV1           | United States | 06/18/1999  | 12/12/2000 | METHOD OF SPACER FORMATION AND SOURCE PROTECTION AFTER SELF-ALIGNED SOURCE FORMED AND A DEVICE PROVIDED BY SUCH A METHOD                                                       |
| 5,867,430             | C196596US                | United States | 12/20/1996  | 02/02/1999 | BANK ARCHITECTURE FOR A NON-VOLATILE MEMORY ENABLING SIMULTANEOUS READING AND WRITING                                                                                          |
| 5,795,627             | C250696US                | United States | 02/14/1997  | 08/18/1998 | METHOD FOR ANNEALING DAMAGES SEMICONDUCTOR REGIONS ALLOWING FOR ENHANCED OXIDE GROWTH                                                                                          |
| 5,844,840             | C253696US                | United States | 08/19/1997  | 12/01/1998 | HIGH VOLTAGE NMOS PASS GATE HAVING SUPPLY RANGE, AREA, AND SPEED ADVANTAGES                                                                                                    |
| 5,909,396             | C253696US DIV1           | United States | 08/03/1998  | 06/01/1999 | HIGH VOLTAGE NMOS PASS GATE HAVING SUPPLY RANGE, AREA, AND SPEED ADVANTAGES                                                                                                    |
| 5,889,302             | C264696US                | United States | 04/21/1997  | 03/30/1999 | MULTILAYER FLOATING GATE FIELD EFFECT TRANSISTOR STRUCTURE                                                                                                                     |
| 5,979,660             | C293197US                | United States | 06/05/1997  | 11/09/1999 | TUBE FOR FLASH MINIATURE CARD                                                                                                                                                  |
| 6,185,630             | C350197US                | United States | 12/18/1997  | 02/06/2001 | DEVICE INITIALIZING SYSTEM WITH PROGRAMMABLE ARRAY LOGIC CONFIGURED TO CAUSE NON-VOLATILE MEMORY TO OUTPUT ADDRESS AND DATA INFORMATION TO THE DEVICE IN A PRESCRIBED SEQUENCE |
| 08/993,570            | C369297US                | United States | 12/18/1997  |            | BIASING METHOD AND STRUCTURE FOR REDUCING BAND-TO-BAND AND/OR AVALANCHE CURRENTS DURING THE ERASE OF FLASH MEMORY DEVICES                                                      |
| 6,236,596             | C369297US CON            | United States | 12/15/1999  | 05/22/2001 | BIASING METHOD AND STRUCTURE FOR REDUCING BAND-TO-BAND AND/OR AVALANCHE CURRENTS DURING THE ERASE OF FLASH MEMORY DEVICES                                                      |
| 5,963,824             | C412397US                | United States | 07/09/1997  | 10/05/1999 | METHOD AND APPARATUS FOR A SEMICONDUCTOR DEVICE WITH ADJUSTABLE THRESHOLD VOLTAGE                                                                                              |
| 6,479,858             | C412397US DIV            | United States | 05/07/1999  | 11/12/2002 | METHOD AND APPARATUS FOR A SEMICONDUCTOR DEVICE WITH ADJUSTABLE THRESHOLD VOLTAGE                                                                                              |
| 6,211,020             | C521397US                | United States | 10/22/1998  | 04/03/2001 | PROCESS FOR FABRICATING A COMMON SOURCE REGION IN MEMORY DEVICES                                                                                                               |
| 5,940,735             | C526397US                | United States | 08/25/1997  | 08/17/1999 | REDUCTION OF CHARGE LOSS IN NONVOLATILE MEMORY CELLS BY PHOSPHOROUS IMPLANTATION INTO PECVD NITRIDE/OXYNITRIDE FILMS                                                           |
| 6,285,054             | C553397US                | United States | 03/30/1998  | 09/04/2001 | TRENCHED GATE NON-VOLATILE SEMICONDUCTOR DEVICE WITH THE SOURCE/DRAIN REGIONS SPACED FROM THE TRENCH BY SIDEWALL DOPINGS                                                       |
| 6,764,904             | C553397US DIV1           | United States | 07/31/2000  | 07/20/2004 | TRENCHED GATE NON-VOLATILE SEMICONDUCTOR METHOD WITH THE SOURCE/DRAIN REGIONS SPACED FROM THE TRENCH BY SIDEWALL DOPINGS                                                       |
| 6,225,659             | C554397US                | United States | 03/30/1998  | 05/01/2001 | TRENCHED GATE SEMICONDUCTOR DEVICE AND METHOD FOR LOW POWER APPLICATIONS                                                                                                       |
| 6,303,437             | C554397US DIV1           | United States | 08/04/2000  | 10/16/2001 | TRENCHED GATE NON-VOLATILE SEMICONDUCTOR DEVICE AND METHOD FOR LOW POWER APPLICATIONS WITH CORNER DOPING AND SIDEWALL DOPING                                                   |
| 6,147,377             | C555397US                | United States | 03/30/1998  | 11/14/2000 | FULLY RECESSED SEMICONDUCTOR DEVICE                                                                                                                                            |
| 6,344,393             | C555397US DIV            | United States | 07/20/2000  | 02/05/2002 | FULLY RECESSED SEMICONDUCTOR DEVICE AND METHOD FOR LOW POWER OPERATIONS                                                                                                        |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                     |
|-----------------------|---------------------------|---------------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 6,147,378             | C557397US                 | United States | 03/30/1998  | 11/14/2000 | FULLY RECESSED SEMICONDUCTOR DEVICE AND METHOD FOR LOW POWER APPLICATIONS WITH SINGLE WRAP AROUND BURIED DRAIN REGION                     |
| 6,225,161             | C557397US DIV1            | United States | 12/22/1999  | 05/01/2001 | FULLY RECESSED SEMICONDUCTOR DEVICE AND METHOD FOR LOW POWER APPLICATIONS WITH SINGLE WRAP AROUND BURIED DRAIN REGION                     |
| 5,933,729             | C560497US                 | United States | 12/08/1997  | 08/03/1999 | REDUCTION OF ONO FENCE DURING SELF-ALIGNED ETCH TO ELIMINATE POLY STRINGERS                                                               |
| 6,232,646             | C608497US                 | United States | 05/20/1998  | 05/15/2001 | SHALLOW TRENCH ISOLATION FILLED WITH THERMAL OXIDE                                                                                        |
| 6,444,539             | C608497US DIV1            | United States | 02/15/2001  | 09/03/2002 | METHOD FOR PRODUCING A SHALLOW TRENCH ISOLATION FILLED WITH THERMAL OXIDE                                                                 |
| 6,555,867             | C610497US                 | United States | 12/16/1997  | 04/29/2003 | FLASH MEMORY GATE COUPLING USING HSG POLYSILICON                                                                                          |
| 6,808,988             | C611497US                 | United States | 02/05/1998  | 10/26/2004 | METHOD FOR FORMING ISOLATION IN FLASH MEMORY WAFER                                                                                        |
| 5,981,341             | C612497US                 | United States | 12/05/1997  | 11/09/1999 | SIDEWALL SPACER FOR PROTECTING TUNNEL OXIDE DURING ISOLATION TRENCH FORMATION IN SELF ALIGNED FLASH                                       |
| 09/401,580            | C612497US DIV1            | United States | 09/22/1999  |            | SIDEWALL SPACER FOR PROTECTING TUNNEL OXIDE DURING ISOLATION TRENCH FORMATION IN SELF ALIGNED FLASH MEMORY CORE                           |
| 6,249,036             | C614497US                 | United States | 03/18/1998  | 06/19/2001 | STEPPER ALIGNMENT MARK FORMATION WITH DUAL FIELD OXIDE PROCESS                                                                            |
| 6,420,224             | C614497US DIV             | United States | 04/16/2001  | 07/16/2002 | STEPPER ALIGNMENT MARK FORMATION WITH DUAL FIELD OXIDE PROCESS                                                                            |
| 6,027,998             | C617497US                 | United States | 12/17/1997  | 02/22/2000 | METHOD FOR FULLY PLANARIZED CONDUCTIVE LINE FOR A STACK GATE                                                                              |
| 6,002,160             | C623497US                 | United States | 12/12/1997  | 12/14/1999 | A SEMICONDUCTOR ISOLATION PROCESS TO MINIMIZE WEAK OXIDE PROBLEMS                                                                         |
| 6,309,949             | C623497US DIV1            | United States | 11/16/1999  | 10/30/2001 | SEMICONDUCTOR ISOLATION PROCESS TO MINIMIZE WEAK OXIDE PROBLEMS                                                                           |
| 6,107,169             | C625497US                 | United States | 08/14/1998  | 08/22/2000 | METHOD FOR FABRICATING A DOPED POLYSILICON FEATURE IN A SEMICONDUCTOR DEVICE                                                              |
| 6,100,559             | C626497US                 | United States | 08/14/1998  | 08/08/2000 | MULTIPURPOSE GRADED SILICON OXYNITRIDE CAP LAYER                                                                                          |
| 6,306,758             | C626497US DIV1            | United States | 05/10/2000  | 10/23/2001 | MULTIPURPOSE GRADED SILICON OXYNITRIDE CAP LAYER                                                                                          |
| 6,258,669             | C627497US                 | United States | 12/18/1997  | 07/10/2001 | METHODS AND ARRANGEMENTS FOR IMPROVED FORMATION OF CONTROL AND FLOATING GATES IN NON-VOLATILE MEMORY SEMICONDUCTOR DEVICES                |
| 6,242,773             | C628497US                 | United States | 09/30/1998  | 06/05/2001 | SELF-ALIGNING POLY 1 ONO DIELECTRIC                                                                                                       |
| 6,034,395             | C629497US                 | United States | 06/05/1998  | 03/07/2000 | METHODS AND ARRANGEMENTS FOR REDUCING THE STEP HEIGHT IN STACKED GATE STRUCTURE WITHIN A SEMICONDUCTOR DEVICE                             |
| 09/477,664            | C629497US DIV1            | United States | 01/05/2000  |            | METHODS AND ARRANGEMENTS FOR REDUCING THE STEP HEIGHT IN STACKED GATE STRUCTURE WITHIN A SEMICONDUCTOR DEVICE                             |
| 6,579,778             | C630497US                 | United States | 08/08/2000  | 06/17/2003 | SOURCE BUS FORMATION FOR A FLASH MEMORY USING SILICIDE                                                                                    |
| 6,174,819             | C634497US                 | United States | 07/21/1998  | 01/16/2001 | LOW TEMPERATURE PHOTORESIST REMOVAL FOR REWORK DURING METAL MASK FORMATION                                                                |
| 6,163,049             | C636497US                 | United States | 10/13/1998  | 12/19/2000 | METHOD OF FORMING A COMPOSITE INTERPOLY GATE DIELECTRIC                                                                                   |
| 6,413,820             | C636497US DIV1            | United States | 11/30/2000  | 07/02/2002 | METHOD OF FORMING A COMPOSITE INTERPOLY GATE DIELECTRIC                                                                                   |
| 6,063,662             | C638497US                 | United States | 12/18/1997  | 05/16/2000 | METHODS FOR FORMING A CONTROL GATE APPARATUS IN NON-VOLATILE MEMORY SEMICONDUCTOR DEVICES                                                 |
| 5,972,751             | C640497US                 | United States | 08/28/1998  | 10/26/1999 | METHODS AND ARRANGEMENTS FOR INTRODUCING NITROGEN INTO A TUNNEL OXIDE IN A NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE                       |
| 6,252,276             | C640497US DIV1            | United States | 08/19/1999  | 06/26/2001 | NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE INCLUDING ASSYMETRICALLY NITROGEN DOPED GATE OXIDE                                               |
| 6,001,713             | C641497US                 | United States | 09/16/1998  | 12/14/1999 | METHODS FOR FORMING NITROGEN-RICH REGIONS IN A FLOATING GATE AND INTERPOLY DIELECTRIC LAYER IN A NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE |
| 6,251,717             | C643497US                 | United States | 09/30/1998  | 06/26/2001 | VIAIBLE MEMORY CELL FORMED USING RAPID THERMAL ANNEALING                                                                                  |
| 6,034,394             | C644497US                 | United States | 12/18/1997  | 03/07/2000 | METHODS AND ARRANGEMENTS FOR FORMING A FLATING GATE IN NON-VOLATILE MEMORY SEMICONDUCTOR DEVICES                                          |
| 6,274,433             | C644497US DIV1            | United States | 01/03/2000  | 08/14/2001 | METHODS AND ARRANGEMENTS FOR FORMING A FLATING GATE IN NON-VOLATILE MEMORY SEMICONDUCTOR DEVICES                                          |
| 09/143,089            | C645497US                 | United States | 08/28/1998  |            | METHODS AND ARRANGEMENTS FOR REDUCING FALSE PROGRAMMING IN NON-VOLATILE SEMICONDUCTOR MEMORY DEVICES                                      |
| 6,989,319             | C645497US DIV             | United States | 11/24/2003  | 01/24/2006 | METHODS FOR FORMING NITROGEN-RICH REGIONS IN NON-VOLATILE SEMICONDUCTOR MEMORY DEVICES                                                    |
| 6,433,383             | C646497US                 | United States | 07/20/1999  | 08/13/2002 | METHODS AND ARRANGEMENTS FOR FORMING A SINGLE INTERPOLY DIELECTRIC LAYER IN A SEMICONDUCTOR DEVICE                                        |
| 6,232,630             | C650497US                 | United States | 07/07/1999  | 05/15/2001 | LIGHT FLOATING GATE DOPING TO IMPORVE TUNNEL OXIDE RELIABILITY                                                                            |
| 6,133,619             | C651497US                 | United States | 08/31/1998  | 10/17/2000 | REDUCTION OF SILICON OXYNITRIDE FILM DELAMINATION IN INTEGRATED CIRCUIT INTER-LEVEL DIELECTRICS                                           |
| 6,124,640             | C652497US                 | United States | 08/31/1998  | 09/26/2000 | SCALABLE AND RELIABLE INTEGRATED CIRCUIT INTER-LEVEL DIELECTRIC                                                                           |
| 6,211,074             | C654497US                 | United States | 05/12/1998  | 03/15/2001 | METHODS AND ARRANGEMENTS FOR REDUCING STRESS AND PREVENTING CRACKING IN A SILICIDE LAYER                                                  |
| 6,429,108             | C655497US                 | United States | 08/31/2000  | 08/06/2002 | NON-VOLATILE MEMORY DEVICE WITH ENCAPSULATED TUNGSTEN GATE AND METHOD OF MAKING SAME                                                      |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                   |
|-----------------------|---------------------------|---------------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------|
| 6,346,467             | C656497US                 | United States | 08/28/2000  | 02/12/2002 | METHOD OF MAKING TUNGSTEN GATE MOS TRANSISTOR AND MEMORY CELL BY ENCAPSULATING                                          |
| 10/059,119            | C656497US DIV             | United States | 01/31/2002  |            | METHOD OF MAKING TUNGSTEN GATE MOS TRANSISTOR AND MEMORY CELL BY ENCAPSULATING                                          |
| 6,436,850             | C658497US                 | United States | 08/31/2000  | 08/20/2002 | METHOD OF DEGASSING LOW K DIELECTRIC FOR METAL DEPOSITION                                                               |
| 6,060,741             | C660497US                 | United States | 09/16/1998  | 05/09/2000 | STACKED GATE STRUCTURE FOR FLASH MEMORY APPLICATION                                                                     |
| 6,011,289             | C661497US                 | United States | 09/16/1998  | 01/04/2000 | METAL OXIDE STACK FOR FLASH MEMORY APPLICATION                                                                          |
| 6,080,639             | C663497US                 | United States | 11/25/1998  | 06/27/2000 | SEMICONDUCTOR DEVICE CONTAINING P-HDP INTERDIELECTRIC LAYER                                                             |
| 5,973,353             | C665497US                 | United States | 12/18/1997  | 10/26/1999 | METHODS AND ARRANGEMENTS FOR FORMING A TAPERED FLOATING GATE IN NON-VOLATILE MEMORY SEMICONDUCTOR DEVICES               |
| 6,159,860             | C666497US                 | United States | 07/17/1998  | 12/12/2000 | METHOD FOR ETCHING LAYERS ON A SEMICONDUCTOR WAFER IN A SINGLE ETCHING CHAMBER                                          |
| 5,977,601             | C667497US                 | United States | 07/17/1998  | 11/02/1999 | METHOD FOR ETCHING MEMORY GATE STACK USING THIN RESIST LAYER                                                            |
| 6,383,939             | C667497US DIV1            | United States | 08/17/1999  | 05/07/2002 | METHOD FOR ETCHING MEMORY GATE STACK USING THIN RESIST LAYER                                                            |
| 09/118,374            | C668497US                 | United States | 07/17/1998  |            | METHOD FOR TRIMMING A PHOTORESIST PATTERN LINE FOR MEMORY GATE ETCHING                                                  |
| 6,372,651             | C668497US DIV             | United States | 04/06/1999  | 04/16/2002 | METHOD FOR TRIMMING A PHOTORESIST PATTERN LINE FOR MEMORY GATE ETCHING                                                  |
| 6,515,328             | C672497US                 | United States | 02/04/1999  | 02/04/2003 | METHOD FOR ETCHING SILICON LAYERS ON A SEMICONDUCTOR SUBSTRATE IN A SINGLE STEP                                         |
| 09/684,780            | C672497US DIV1            | United States | 10/10/2000  |            | METHOD FOR ETCHING SILICON LAYERS ON A SEMICONDUCTOR SUBSTRATE IN A SINGLE STEP                                         |
| 6,159,794             | C673497US                 | United States | 05/12/1998  | 12/12/2000 | METHODS FOR REMOVING SILICIDE RESIDUE IN A SEMICONDUCTOR DEVICE                                                         |
| 6,074,956             | C674497US                 | United States | 05/12/1998  | 06/13/2000 | METHODS FOR PREVENTING SILICIDE RESIDUE FORMATION IN A SEMICONDUCTOR DEVICE                                             |
| 6,110,779             | C675497US                 | United States | 07/17/1998  | 08/29/2000 | METHOD AND STRUCTURE OF ETCHING A MEMORY CELL POLYSILICON GATE LAYER USING RESIST MASK AND ETCHED SILICON OXYNITRIDE    |
| 6,452,225             | C675497US DIV1            | United States | 07/17/2000  | 09/17/2002 | METHOD AND STRUCTURE OF ETCHING A MEMORY CELL POLYSILICON GATE LAYER USING RESIST MASK AND ETCHED SILICON OXYNITRIDE    |
| 5,948,703             | C677497US                 | United States | 06/08/1998  | 09/07/1999 | METHOD OF SELF-LANDING GATE ETCHING TO PREVENT GATE OXIDE DAMAGE                                                        |
| 09/168,988            | C678497US                 | United States | 10/09/1998  |            | METHOD OF CONTROLLING THE SLOPE OF SIDEWALLS IN POLYSILICON                                                             |
| 6,534,411             | C679497US                 | United States | 04/13/2000  | 03/18/2003 | METHOD OF HIGH DENSITY PLASMA METAL ETCHING                                                                             |
| 6,072,191             | C680497US                 | United States | 12/16/1997  | 06/06/2000 | INTERLEVEL DIELECTRIC THICKNESS MONITOR FOR COMPLEX SEMICONDUCTOR CHIPS                                                 |
| 6,350,627             | C680497US DIV             | United States | 04/13/2000  | 02/26/2002 | INTERLEVEL DIELECTRIC THICKNESS MONITOR FOR COMPLEX SEMICONDUCTOR CHIPS                                                 |
| 5,972,749             | C686497US                 | United States | 01/05/1998  | 10/26/1999 | METHOD AND APPARATUS FOR PREVENTING P1 PUNCHTHROUGH                                                                     |
| 6,066,873             | C686497US DIV1            | United States | 03/18/1999  | 05/23/2000 | METHOD AND APPARATUS FOR PREVENTING P1 PUNCHTHROUGH                                                                     |
| 5,994,780             | C687497US                 | United States | 12/16/1997  | 11/30/1999 | SEMICONDUCTOR DEVICE WITH MULTIPLE CONTACT SIZES                                                                        |
| 6,211,058             | C687497US DIV1            | United States | 07/15/1999  | 04/03/2001 | SEMICONDUCTOR DEVICE WITH MULTIPLE CONTACT SIZES                                                                        |
| 6,667,511             | C690497US                 | United States | 12/18/1997  | 12/23/2003 | NOVEL NAND TYPE CORE CELL STRUCTURE AND CORRESPONDING PROCESS FOR HIGH DENSITY AND HIGH PERFORMANCE FLASH MEMORY DEVICE |
| 6,316,293             | C690497US DIV             | United States | 03/20/2000  | 11/13/2001 | METHOD OF FORMING A NAND-TYPE FLASH MEMORY DEVICE HAVING A NON-STACKED SELECT GATE TRANSISTOR STRUCTURE                 |
| 6,017,786             | C692497US                 | United States | 12/17/1997  | 01/25/2000 | METHOD FOR FORMING A LOW BARRIER HEIGHT OXIDE LAYER ON A SILICON SUBSTRATE                                              |
| 6,166,439             | C694497US                 | United States | 12/30/1997  | 12/26/2000 | A LOW DIELECTRIC CONSTANT MATERIAL AND METHOD OF APPLICATION TO ISOLATE CONDUCTIVE LINES                                |
| 6,235,586             | C695497US                 | United States | 07/13/1999  | 05/22/2001 | THIN FLOATING GATE AND CONDUCTIVE SELECT GATE IN SITU                                                                   |
| 6,001,688             | C696497US                 | United States | 12/08/1997  | 12/14/1999 | POLY STRINGER CLEAN-UP FOR FLASH MEMORY STRUCTURES                                                                      |
| 6,159,795             | C697497US                 | United States | 07/02/1998  | 12/12/2000 | LOW VOLTAGE JUNCTION AND HIGH VOLTAGE JUNCTION OPTIMIZATION FOR FLASH MEMORY                                            |
| 09/159,413            | C697497US DIV             | United States | 09/23/1998  |            | LOW VOLTAGE JUNCTION AND HIGH VOLTAGE JUNCTION OPTIMIZATION FOR FLASH MEMORY                                            |
| 6,346,737             | C698497US                 | United States | 07/02/1998  | 02/12/2002 | SHALLOW TRENCH ISOLATION PROCESS PARTICULARLY SUITED FOR HIGH VOLTAGE CIRCUITS                                          |
| 6,046,085             | C700497US                 | United States | 12/08/1997  | 04/04/2000 | ELIMINATION OF POLY STRINGER WITH STRAIGHT POLY PROFILE                                                                 |
| 6,509,232             | C701497US                 | United States | 10/01/2001  | 01/21/2003 | FORMATION OF STI (SHALLOW TRENCH ISOLATION) STRUCTURES WITHIN CORE AND PERIPHERY AREAS OF FLASH MEMORY DEVICE           |
| 5,939,750             | C704497US                 | United States | 01/21/1998  | 08/17/1999 | USE OF IMPLANTED IONS TO REDUCE OXIDE-NITRIDE-OXIDE (ONO) ETCH RESIDUE AND POLYSTRINGERS                                |
| 6,221,768             | C704497US DIV             | United States | 02/25/1999  | 04/24/2001 | USE OF IMPLANTED IONS TO REDUCE OXIDE-NITRIDE-OXIDE (ONO) ETCH RESIDUE AND POLYSTRINGERS                                |
| 6,063,666             | C705497US                 | United States | 06/12/1998  | 05/16/2000 | RTCD OXIDE AND N2O ANNEAL FOR TOP OXIDE OF ONO FILM                                                                     |
| 5,981,339             | C706497US                 | United States | 03/20/1998  | 11/09/1999 | NARROWER ERASE DISTRIBUTION FOR FLASH MEMORY BY SMALLER POLY GRAIN SIZE                                                 |
| 6,140,246             | C707497US                 | United States | 12/18/1997  | 10/31/2000 | IN SITU P DOPED AMORPHOUS SILICON BY NH3 TO FORM OXIDATION RESISTANT AND FINER GRAIN FLOATING GATES                     |
| 5,994,239             | C708497US                 | United States | 12/18/1997  | 11/30/1999 | MANUFACTURING PROCESS TO ELIMINATE POLYSTRINGERS IN HIGH DENSITY NAND-TYPE FLASH MEMORY DEVICE                          |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                         |
|-----------------------|---------------------------|---------------|-------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 6,114,230             | C709497US                 | United States | 12/18/1997  | 09/05/2000 | NITROGEN ION IMPLANTED AMORPHOUS SILICON TO PRODUCE OXIDATION RESISTANT AND FINER GRAIN POLYSILICON BASED FLOATING GATES                      |
| 6,281,078             | C710497US                 | United States | 12/18/1997  | 08/28/2001 | MANUFACTURING PROCESS TO ELIMINATE ONO FENCE MATERIAL IN HIGH DENSITY NAND-TYPE FLASH MEMORY DEVICES                                          |
| 6,157,572             | C712497US                 | United States | 05/27/1998  | 12/05/2000 | METHOD FOR ERASING FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EEPROM)                                                         |
| 5,875,130             | C713497US                 | United States | 05/27/1998  | 02/23/1999 | METHOD FOR PROGRAMMING FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EEPROM)                                                     |
| 6,052,310             | C714497US                 | United States | 08/12/1998  | 04/18/2000 | METHOD FOR TIGHTENING ERASE THRESHOLD VOLTAGE DISTRIBUTION IN FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EEPROM)              |
| 6,134,146             | C715497US                 | United States | 10/05/1998  | 10/17/2000 | WORDLINE DRIVER FOR FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EEPROM)                                                        |
| 6,205,059             | C718497US                 | United States | 10/05/1998  | 03/20/2001 | METHOD FOR ERASING FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EEPROM)                                                         |
| 6,011,721             | C719497US                 | United States | 08/12/1998  | 01/04/2000 | METHOD FOR SENSING STATE OF ERASURE OF FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EEPROM)                                     |
| 5,901,090             | C720497US                 | United States | 05/27/1998  | 05/04/1999 | METHOD FOR ERASING FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EEPROM)                                                         |
| 6,275,415             | C721497US                 | United States | 10/11/1999  | 08/14/2001 | MULTIPLE BYTE CHANNEL HOT ELECTRON PORGRAMMING USING RAMPED GATE WITH SOURCE BIAS                                                             |
| 09/872,708            | C721497US DIV             | United States | 06/01/2001  |            | MULTIPLE BYTE CHANNEL HOT ELECTRON PORGRAMMING USING RAMPED GATE AND SOURCE BIAS VOLTAGE                                                      |
| 6,172,914             | C722497US                 | United States | 09/23/1999  | 01/09/2001 | CONCURRENT ERASE VERIFY SCHEME FOR FLASH MEMORY APPLICATIONS                                                                                  |
| 60/148,782            | C723497                   | United States | 08/13/1999  |            | BIT BY BIT APDE VERIFY FOR FLASH MEMORY APPLICATIONS                                                                                          |
| 6,122,198             | C723497US                 | United States | 10/05/1999  | 09/19/2000 | BIT BY BIT APDE VERIFY FOR FLASH MEMORY APPLICATIONS                                                                                          |
| 60/148,779            | C725497                   | United States | 08/01/2000  | 03/05/2003 | CIRCUIT IMPLEMENTATION TO QUENCH BIT LINE LEAKAGE CURRENT IN PROGRAM AND AUTO PROGRAM DISTURB MODE IN FLASH EPROM USING RESISTOR SOURCE LOAD  |
| 6,046,932             | C725497US                 | United States | 10/13/1999  | 04/04/2000 | CIRCUIT IMPLEMENTATION TO QUENCH BIT LINE LEAKAGE CURRENT IN PROGRAM AND AUTO PROGRAM DISTURB MODE IN FLASH EPROM USING RESISTOR SOURCE LOAD  |
| 6,103,602             | C730497US                 | United States | 12/17/1997  | 08/15/2000 | METHOD AND SYSTEM FOR PROVIDING A DRAIN SIDE POCKET IMPLANT                                                                                   |
| 09/542,587            | C730497US DIV             | United States | 04/04/2000  |            | METHOD AND SYSTEM FOR PROVIDING A DRAIN SIDE POCKET IMPLANT                                                                                   |
| 5,949,718             | C731497US                 | United States | 12/17/1997  | 09/07/1999 | METHOD AND SYSTEM FOR SELECTED SOURCE DURING READ AND PROGRAMMING OF FLASH MEMORY                                                             |
| 6,188,101             | C734497US                 | United States | 01/14/1998  | 02/13/2001 | FLASH EPROM CELL WITH REDUCED SHORT CHANNEL EFFECT AND METHOD FOR PROVIDING SAME                                                              |
| 5,888,867             | C735497US                 | United States | 02/13/1998  | 03/30/1999 | NON-UNIFORM THRESHOLD VOLTAGE ADJUSTMENT IN FLASH EPROMS THROUGH GATE WORK FUNCTION ALTERATION                                                |
| 5,940,709             | C737497US                 | United States | 12/18/1997  | 08/17/1999 | METHOD AND SYSTEM FOR SOURCE-ONLY REOXIDATION AFTER JUNCTION IMPLANT FOR FLASH- MEMORY DEVICES                                                |
| 6,127,222             | C738497US                 | United States | 12/16/1997  | 10/03/2000 | NON-SELF-ALIGNED SIDE CHANNEL IMPLANTS FOR FLASH MEMORY CELLS                                                                                 |
| 6,387,755             | C740497US                 | United States | 12/17/1997  | 05/14/2002 | METHOD AND SYSTEM FOR PROVIDING LOCALIZED GATE-EDGE ROUNDING WITH MINIMAL ENCROACHMENT AND GATE LIFTING                                       |
| 6,015,736             | C742497US                 | United States | 12/19/1997  | 01/18/2000 | METHOD AND SYSTEM FOR GATE STACK REOXIDATION CONTROL                                                                                          |
| 6,153,487             | C743497US                 | United States | 03/17/1998  | 11/28/2000 | NEW APPROACH FOR THE FORMATION OF SEMICONDUCTOR DEVICES WHICH REDUCES BAND-TO-BAND TUNNELING CURRENT AND SHORT-CHANNEL EFFECTS                |
| 6,025,240             | C744497US                 | United States | 12/18/1997  | 02/15/2000 | METHOD AND SYSTEM FOR USING A SPACER TO OFFSET IMPLANT DAMAGE AND REDUCE LATERAL DIFFUSION IN FLASH MEMORY DEVICES                            |
| 6,410,956             | C744497US DIV             | United States | 01/07/2000  | 06/25/2002 | METHOD AND SYSTEM FOR USING A SPACER TO OFFSET IMPLANT DAMAGE AND REDUCE LATERAL DIFFUSION IN FLASH MEMORY DEVICES                            |
| 6,137,153             | C748497US                 | United States | 02/13/1998  | 10/24/2000 | FLOATING GATE CAPACITOR FOR USE IN VOLTAGE REGULATORS                                                                                         |
| 6,262,469             | C749497US                 | United States | 03/25/1998  | 07/17/2001 | CAPACITOR FOR USE IN A CAPACITOR DIVIDER THAT HAS A FLOATING GATE TRANSISTOR AS A CORRESPONDING CAPACITOR                                     |
| 6,005,804             | C752497US                 | United States | 12/18/1997  | 12/21/1999 | SPLIT VOLTAGE FOR NAND FLASH                                                                                                                  |
| 6,081,455             | C753497US                 | United States | 01/14/1999  | 06/27/2000 | EEPROM DECODER BLOCK HAVING A P-WELL COUPLED TO A CHARGE PUMP FOR CHARGING THE P-WELL AND METHOD OF PROGRAMMING WITH THE EEPROM DECODER BLOCK |
| 5,991,202             | C756497US                 | United States | 09/24/1998  | 11/23/1999 | METHOD FOR REDUCING PRGRAM DISTURB DURING SELF-BOOSTING IN A NAND FLASH MEMORY                                                                |
| 6,177,322             | C758497US                 | United States | 10/23/1998  | 01/23/2001 | HIGH VOLTAGE TRANSISTOR WITH HIGH GATED DIODE BREAKDOWN VOLTAGE                                                                               |
| 6,369,433             | C760497US                 | United States | 10/30/1998  | 04/09/2002 | HIGH VOLTAGE TRANSISTOR WITH LOW BODY EFFECT AND LOW LEAKAGE                                                                                  |
| 6,133,746             | C762497                   | United States | 09/30/1998  | 10/17/2000 | METHOD FOR DETERMINING A RELIABLE OXIDE THICKNESS                                                                                             |
| 6,175,522             | C762497US CIP             | United States | 09/30/1999  | 01/16/2001 | READ OPERATION SCHEME FOR A HIGH-DENSITY, LOW VOLTAGE, AND SUPERIOR RELIABILITY NAND FLASH MEMORY DEVICE                                      |
| 6,228,782             | C768497US                 | United States | 05/11/1999  | 05/08/2001 | IMPROVED CORE FIELD ISOLATION FOR A NAND FLASH MEMORY                                                                                         |
| 6,235,632             | C775497US                 | United States | 01/13/1998  | 05/22/2001 | TUNGSTEN PLUG FORMATION                                                                                                                       |
| 6,002,151             | C776497US                 | United States | 12/18/1997  | 12/14/1999 | NON-VOLATILE TRENCH SEMICONDUCTOR DEVICE                                                                                                      |
| 6,124,608             | C777497US                 | United States | 12/18/1997  | 09/26/2000 | NON-VOLATILE TRENCH SEMICONDUCTOR DEVICE HAVING A SHALLOW DRAIN REGION                                                                        |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                          |
|-----------------------|---------------------------|---------------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6,020,238             | C808497US                 | United States | 11/25/1997  | 02/01/2000 | METHOD OF FABRICATING A HIGH DIELECTRIC CONSTANT INTERPOLYSILICON DIELECTRIC STRUCTURE FOR A LOW VOLTAGE NON-VOLATILE MEMORY                                                   |
| 6,025,228             | C809597US                 | United States | 11/25/1997  | 02/15/2000 | METHOD OF FABRICATING AN OXYNITRIDE CAPPED-HIGH DIELECTRIC CONSTANT INTERPOLYSILICON DIELECTRIC STRUCTURE FOR A LOW VOLTAGE NON-VOLATILE MEMORY                                |
| 6,228,746             | C814497US CON             | United States | 12/18/1997  | 05/08/2001 | METHODOLOGY FOR ACHIEVING DUAL FIELD OXIDE THICKNESS                                                                                                                           |
| 6,080,682             | C815597US                 | United States | 12/18/1997  | 06/27/2000 | METHODOLOGY FOR ACHIEVING DUAL GATE OXIDE THICKNESSES                                                                                                                          |
| 6,232,244             | C815597US DIV             | United States | 05/01/2000  | 05/15/2001 | METHODOLOGY FOR ACHIEVING DUAL GATE OXIDE THICKNESSES                                                                                                                          |
| 6,091,138             | C879597US                 | United States | 02/27/1998  | 07/18/2000 | MULTI-CHIP PACKAGING USING BUMP TECHNOLOGY                                                                                                                                     |
| 6,043,120             | C915697US CIP             | United States | 03/03/1998  | 03/28/2000 | ELIMINATION OF OXYNITRIDE (ONO) ETCH RESIDUE AND POLYSILICON STRINGERS THROUGH ISOLATION OF FLOATING GATES ON ADJACENT BITLINES BY POLYSILICON OXIDATION                       |
| 5,990,515             | C917697US                 | United States | 03/30/1998  | 11/23/1999 | A TRENCHED GATE NON-VOLATILE SEMICONDUCTOR DEVICE AND METHOD WITH CORNER DOPING AND SIDEWALL DOPING                                                                            |
| 6,118,147             | C918697US                 | United States | 07/07/1998  | 09/12/2000 | DOUBLE DENSITY NON-VOLATILE MEMORY CELLS                                                                                                                                       |
| 6,232,632             | C918697US CON             | United States | 11/09/1999  | 05/15/2001 | DOUBLE DENSITY NON-VOLATILE MEMORY CELLS                                                                                                                                       |
| 6,030,868             | C921697US CIP             | United States | 03/03/1998  | 02/29/2000 | ELIMINATION OF OXYNITRIDE (ONO) ETCH RESIDUE AND POLYSILICON STRINGERS THROUGH ISOLATION OF FLOATING GATES ON ADJACENT BITLINES BY POLYSILICON OXIDATION                       |
| 09/468,510            | C921697US DIV             | United States | 12/15/1999  |            | ELIMINATION OF OXYNITRIDE (ONO) ETCH RESIDUE AND POLYSILICON STRINGERS THROUGH ISOLATION OF FLOATING GATES ON ADJACENT BITLINES BY POLYSILICON OXIDATION                       |
| 6,110,833             | C922697US CIP             | United States | 03/03/1998  | 08/29/2000 | ELIMINATION OF OXYNITRIDE (ONO) ETCH RESIDUE AND POLYSILICON STRINGERS THROUGH ISOLATION OF FLOATING GATES ON ADJACENT BITLINES BY POLYSILICON OXIDATION                       |
| 6,455,888             | C922697US DIV             | United States | 02/17/2000  | 09/24/2002 | MEMORY CELL STRUCTURE FOR ELIMINATION OF OXYNITRIDE (ONO) ETCH RESIDUE AND POLYSILICON STRINGERS                                                                               |
| 6,001,689             | D001US                    | United States | 01/16/1998  | 12/14/1999 | PROCESS FOR FABRICATING A FLASH MEMORY WITH DUAL FUNCTION CONTROL LINES                                                                                                        |
| 6,218,689             | D010106US                 | United States | 08/06/1999  | 04/17/2001 | METHOD FOR PROVIDING A DOPANT LEVEL FOR POLYSILICON FOR FLASH MEMORY DEVICES                                                                                                   |
| 6,506,683             | D0122US                   | United States | 10/06/1999  | 01/14/2003 | IN-SITU PROCESS FOR FABRICATING A SEMICONDUCTOR DEVICE WITH INTEGRAL REMOVAL OF ANTIREFLECTION AND ETCH STOP LAYERS                                                            |
| 5,978,267             | D016US                    | United States | 10/20/1998  | 11/02/1999 | BIT LINE BIASING METHOD TO ELIMINATE PROGRAM DISTURBANCE IN A NON-VOLATILE MEMORY DEVICE AND MEMORY DEVICE EMPLOYING THE SAME                                                  |
| 6,381,550             | D0178US                   | United States | 05/28/1999  | 04/30/2002 | METHOD OF UTILIZING FAST CHIP ERASE TO SCREEN ENDURANCE REJECTS                                                                                                                |
| 6,146,944             | D019US                    | United States | 03/16/1998  | 11/14/2000 | LARGE ANGLE IMPLANTATION TO PREVENT FIELD TURN-ON UNDER SELECT GATE TRANSISTOR FIELD OXIDE REGION FOR NON-VOLATILE MEMORY MEMORY DEVICES                                       |
| 6,100,593             | D021US                    | United States | 02/27/1998  | 08/08/2000 | MULTIPLE CHIP HYBRID PACKAGE USING BUMP TECHNOLOGY                                                                                                                             |
| 6,369,421             | D103US                    | United States | 06/29/1998  | 04/09/2002 | EEPROM HAVING STACKED DIELECTRIC TO INCREASE PROGRAMMING SPEED                                                                                                                 |
| 5,973,958             | D105US                    | United States | 06/23/1998  | 10/26/1999 | AN INTERLACED STORAGE AND SENSE TECHNIQUE FOR FLASH MULTI-LEVEL DEVICES                                                                                                        |
| 6,146,795             | D107US                    | United States | 09/02/1998  | 11/14/2000 | METHOD FOR MANUFACTURING MEMORY DEVICE                                                                                                                                         |
| 6,091,631             | D119US                    | United States | 07/01/1998  | 07/18/2000 | A PROGRAM/VERIFY TECHNIQUE FOR MULTI-LEVEL FLASH CELLS ENABLING DIFFERENT THRESHOLD LEVELS TO BE SIMULTANEOUSLY PROGRAMMED                                                     |
| 6,150,285             | D125US                    | United States | 06/17/1998  | 11/21/2000 | METHOD FOR ESTABLISHING INTER-LAYER DIELECTRIC FOR 0.25u AND SMALLER SEMICONDUCTOR CHIP TECHNOLOGY WHILE MINIMIZING HYDROGEN EMBRITTLEMENT AND SEMICONDUCTOR CHIP MADE THEREBY |
| 6,566,252             | D125US DIV                | United States | 10/11/2000  | 05/20/2003 | METHOD FOR SIMULTANEOUS DEPOSITION AND SPUTTERING TEOS AND DEVICE THEREBY FORMED                                                                                               |
| 5,995,417             | D138                      | United States | 10/05/1999  | 01/08/2003 | SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON-VOLATILE MEMORY ARRAY                                                                                                          |
| 6,275,894             | D139US                    | United States | 09/22/1999  |            | BANK SELECTOR CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                                                             |
| 6,633,949             | D139US DIV                | United States | 06/26/2001  | 10/14/2003 | BANK SELECTOR CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                                                             |
| 6,470,414             | D139US DIV2               | United States | 06/26/2001  | 10/22/2002 | BANK SELECTOR CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                                                             |
| 6,100,754             | D140US                    | United States | 08/03/1998  | 08/08/2000 | VT REFERENCE VOLTAGE FOR EXTREMELY LOW POWER-SUPPLY                                                                                                                            |
| 5,995,415             | D168US                    | United States | 09/23/1998  | 11/30/1999 | SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                                                                  |
| 6,033,955             | D169US                    | United States | 09/23/1998  | 03/07/2000 | METHOD OF MAKING FLEXIBLY PARTITIONED METAL LINE SEGMENTS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                         |
| 6,005,803             | D170US                    | United States | 09/23/1998  | 12/21/1999 | MEMORY ADDRESS DECODING CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                                                   |
| 6,438,726             | D225US                    | United States | 05/18/1999  | 08/20/2002 | METHOD OF DUAL USE OF NON-VOLATILE MEMORY FOR ERROR CORRECTION                                                                                                                 |
| 6,584,594             | D243                      | United States | 05/18/1999  | 06/24/2003 | DATA PRE-READING AND ERROR CORRECTION CIRCUIT FOR A MEMORY DEVICE                                                                                                              |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                           |
|-----------------------|---------------------------|---------------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------|
| 5,930,172             | D244US                    | United States | 06/23/1998  | 07/27/1999 | A PAGE BUFFER FOR A MULTI-LEVEL FLASH MEMORY WITH A LIMITED NUMBER OF LATCHES PER MEMORY CELL                                   |
| 6,204,516             | D268US                    | United States | 09/30/1998  | 03/20/2001 | METHOD AND APPARATUS FOR DETERMINING THE ROBUSTNESS OF MEMORY CELLS TO ALPHA-PARTICLE/COSMIC RAY INDUCED SOFT ERRORS            |
| 6,348,356             | D268US DIV                | United States | 09/19/2000  | 02/19/2002 | METHOD AND APPARATUS FOR DETERMINING THE ROBUSTNESS OF MEMORY CELLS TO ALPHA-PARTICLE/COSMIC RAY INDUCED SOFT ERRORS            |
| 6,143,608             | D355US                    | United States | 03/31/1999  | 11/07/2000 | BARRIER LAYER DECREASES NITROGEN CONTAMINATION OF PERIPHERAL GATE REGIONS DURING TUNNEL OXIDE NITRIDATION                       |
| 09/561,665            | D561                      | United States | 05/02/2000  |            | SION ARC FOR IMPROVED CRITICAL DIMENSION CONTROL ON OXIDE FILMS                                                                 |
| 6,475,868             | D613US                    | United States | 08/17/2000  | 11/05/2002 | OXYGEN IMPLANTATION FOR REDUCTION OF JUNCTION CAPACITANCE IN MOS TRANSISTORS                                                    |
| 6,506,640             | D617US                    | United States | 09/22/2000  | 01/14/2003 | MULTIPLE CHANNEL IMPLANTATION TO FORM RETROGRADE CHANNEL PROFILE AND TO ENGINEER THRESHOLD VOLTAGE AND SUBSURFACE PUNCH-THROUGH |
| 6,713,842             | D653US                    | United States | 08/17/2000  | 03/30/2004 | MASK FOR AND METHOD OF FORMING A CHARACTER ON A SUBSTRATE                                                                       |
| 6,246,118             | D725US                    | United States | 02/18/1999  | 06/12/2001 | LOW DIELECTRIC SEMICONDUCTOR DEVICE WITH RIGID, CONDUCTIVELY LINED INTERCONNECTION SYSTEM                                       |
| 6,667,552             | D726US                    | United States | 02/18/1999  | 12/23/2003 | LOW DIELECTRIC METAL SILICIDE LINED INTERCONNECTION SYSTEM                                                                      |
| 6,074,917             | D800US                    | United States | 11/11/1998  | 06/13/2000 | LPCVD OXIDE AND RTA FOR TOP OXIDE OF ONO FILM TO IMPROVE RELIABILITY FOR FLASH MEMORY DEVICES                                   |
| 6,238,975             | D802US                    | United States | 11/25/1998  | 05/29/2001 | METHOD FOR IMPROVING ELECTROSTATIC DISCHARGE (ESD) ROBUSTNESS                                                                   |
| 6,218,245             | D803US                    | United States | 11/24/1998  | 04/17/2001 | METHOD FOR FABRICATING A HIGH-DENSITY AND HIGH-RELIABILITY EEPROM DEVICE                                                        |
| 6,579,781             | D827                      | United States | 07/19/2000  | 06/17/2003 | ELIMINATION OF N+ CONTACT IMPLANT FROM FLASH TECHNOLOGIES BY REPLACEMENT WITH STANDARD DOUBLE-DIFFUSED AND N+ IMPLANTS          |
| 6,277,690             | D828US                    | United States | 11/02/2000  | 08/21/2001 | ELIMINATION OF N+ IMPLANT FROM FLASH TECHNOLOGY BY REPLACEMENT WITH STANDARD MEDIUM-DOPED-DRAIN (MDD) IMPLANT                   |
| 6,440,789             | D829US                    | United States | 11/01/2000  | 08/27/2002 | PHOTORESIST SPACER PROCESS SIMPLIFICATION TO ELIMINATE STANDARD POLYSILICON OR OXIDE SPACER PROCESS FOR FLASH MEMORY CIRCUITS   |
| 6,188,609             | D832US                    | United States | 05/06/1999  | 02/13/2001 | RAMPED OR STEPPED GATE CHANNEL ERASE FOR FLASH MEMORY APPLICATION                                                               |
| 6,141,255             | D833US                    | United States | 09/02/1999  | 10/31/2000 | 1 TRANSISTOR FOR EEPROM APPLICATION                                                                                             |
| 6,240,016             | D834US                    | United States | 01/31/2000  | 05/29/2001 | METHOD TO REDUCE READ GATE DISTURB FOR FLASH EEPROM APPLICATION                                                                 |
| 6,255,165             | D837US                    | United States | 10/18/1999  | 07/03/2001 | NITRIDE PLUG TO REDUCE GATE EDGE LIFTING                                                                                        |
| 6,329,273             | D838US                    | United States | 10/29/1999  | 12/11/2001 | SOLID-SOURCE DOPING FOR SOURCE/DRAIN TO ELIMINATE IMPLANT DAMAGE                                                                |
| 6,294,430             | D840US                    | United States | 01/31/2000  | 09/25/2001 | NITRIDIZATION OF THE PRE-DDI SCREEN OXIDE                                                                                       |
| 6,207,978             | D841US                    | United States | 03/01/2000  | 03/27/2001 | FLASH MEMORY CELLS HAVING A MODULATION DOPED METEROJUNCTION STRUCTURE                                                           |
| 6,285,588             | D842US                    | United States | 01/31/2000  | 09/04/2001 | ERASE SCHEME TO TIGHTEN THE THRESHOLD VOLTAGE DISTRIBUTION OF EEPROM FLASH MEMORY CELLS                                         |
| 6,172,909             | D844US                    | United States | 08/09/1999  | 01/09/2001 | RAMPED GATE TECHNIQUE FOR SOFT PROGRAMMING TO TIGHTEN THE VI DISTRIBUTION                                                       |
| 6,233,175             | D845US                    | United States | 10/21/2000  | 05/05/2001 | SELF-LIMITING MULTI-LEVEL PROGRAMMING STATES                                                                                    |
| 6,452,840             | D846US                    | United States | 10/21/2000  | 09/17/2002 | FEEDBACK METHOD TO OPTIMIZE ELECTRIC FIELD DURING CHANNEL ERASE OF FLASH MEMORY DEVICES                                         |
| 6,147,907             | D847US                    | United States | 10/29/1999  | 11/14/2000 | BIASING SCHEME TO REDUCE STRESS ON NON-SELECTED CELLS DURING READ                                                               |
| 6,049,479             | D848US                    | United States | 09/23/1999  | 04/11/2000 | OPERATIONAL APPROACH FOR THE SUPPRESSION OF BI-DIRECTIONAL TUNNEL OXIDE OF A FLASH CELL                                         |
| 6,198,664             | D849US                    | United States | 01/31/2000  | 03/06/2001 | APDE SCHEME FOR FLASH MEMORY APPLICATION                                                                                        |
| 6,137,727             | D851US                    | United States | 01/24/2000  | 10/24/2000 | REDUCTION OF OXIDE STRESS THROUGH THE USE OF FORWARD BIASED BODY VOLTAGE                                                        |
| 6,178,117             | D852US                    | United States | 01/24/2000  | 01/23/2001 | BACKGROUND CORRECTION FOR CHARGE GAIN AND LOSS                                                                                  |
| 6,160,740             | D853US                    | United States | 01/24/2000  | 12/12/2000 | METHOD TO PROVIDE A REDUCED CONSTANT E-FIELD DURING ERASE OF EEPROMS FOR RELIABILITY IMPROVEMENT                                |
| 09/522,209            | D854                      | United States | 03/09/2000  |            | POLYSILICON SOURCE CONNECTION FOR FLASH NOR ARRAYS                                                                              |
| 60/163,760            | D855                      | United States | 11/05/1999  |            | DEPOSITED SCREEN OXIDE FOR REDUCING GATE EDGE LIFTING                                                                           |
| 6,518,072             | D855US                    | United States | 01/03/2000  | 02/11/2003 | DEPOSITED SCREEN OXIDE FOR REDUCING GATE EDGE LIFTING                                                                           |
| 60/163,761            | D856                      | United States | 11/05/1999  |            | USE OF ETCH TO BLUNT GATE CORNERS                                                                                               |
| 6,238,978             | D856US                    | United States | 01/03/2000  | 05/29/2001 | USE OF ETCH TO BLUNT GATE CORNERS                                                                                               |
| 6,576,949             | D861                      | United States | 08/30/1999  | 06/10/2003 | INTEGRATED CIRCUIT HAVING OPTIMIZED GATE COUPLING CAPACITANCE                                                                   |
| 6,232,635             | D862US                    | United States | 04/06/2000  | 05/15/2001 | NEW METHOD TO FABRICATE A HIGH COUPLING FLASH CELL WITH LESS SILICIDE SEAM PROBLEM                                              |
| 6,530,997             | D867US                    | United States | 04/06/2000  | 03/11/2003 | USE OF GASEOUS SILICON HYDRIDES AS A REDUCING AGENT TO REMOVE RE-SUPUTTERED SILICON OXIDE                                       |
| 6,682,978             | D877US                    | United States | 02/15/2000  | 01/27/2004 | INTEGRATED CIRCUIT HAVING INCREASED GATE COUPLING CAPACITANCE                                                                   |
| 6,323,516             | D878US                    | United States | 09/03/1999  | 11/27/2001 | A FLASH MEMORY DEVICE AND FABRICATION METHOD HAVING A HIGH COUPLING RATIO                                                       |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                    |
|-----------------------|--------------------------|---------------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------|
| 6,346,466             | D880US                   | United States | 03/30/2000  | 02/12/2002 | PLANARIZATION OF A POLYSILICON LAYER SURFACE BY CHEMICAL MECHANICAL POLISH TO IMPROVE LITHOGRAPHY AND SILICIDE FORMATION |
| 6,548,336             | D880US DIV               | United States | 02/08/2002  | 04/15/2003 | PLANARIZATION OF A POLYSILICON LAYER SURFACE BY CHEMICAL MECHANICAL POLISH TO IMPROVE LITHOGRAPHY AND SILICIDE FORMATION |
| 6,410,443             | D883US                   | United States | 02/22/2000  | 06/25/2002 | METHOD FOR REMOVING SEMICONDUCTOR ARC USING ARC CMP BUFFING                                                              |
| 6,551,923             | D884                     | United States | 11/01/1999  | 04/22/2003 | DUAL WIDTH CONTACT FOR CHARGE GAIN REDUCTION                                                                             |
| 7,141,482             | D885US                   | United States | 11/02/2004  | 11/28/2006 | METHOD OF MAKING A MEMORY CELL                                                                                           |
| 6,486,506             | D887US                   | United States | 03/23/2000  | 11/26/2002 | FLASH MEMORY WITH LESS SUSCEPTIBILITY TO CHARGE GAIN AND CHARGE LOSS                                                     |
| 09/422,282            | D891US                   | United States | 10/21/1999  |            | A METHOD FOR ACHIEVING A HIGH-COUPPLING RATIO IN FLASH MEMORY DEVICES                                                    |
| 60/151,453            | D891US PROV              | United States | 08/30/1999  |            | A METHOD FOR ACHIEVING A HIGH-COUPPLING RATIO IN FLASH MEMORY DEVICES                                                    |
| 6,635,943             | D892US                   | United States | 03/22/2000  | 10/21/2003 | METHOD AND SYSTEM FOR REDUCING CHARGE GAIN AND CHARGE LOSS IN INTERLAYER DIELECTRIC FORMATION                            |
| 6,197,635             | D893US                   | United States | 10/13/1999  | 03/06/2001 | METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITH REDUCED MASKING AND WITHOUT ARC LOSS IN PERIPHERAL CIRCUITRY REGION  |
| 6,235,587             | D894US                   | United States | 10/13/1999  | 05/22/2001 | METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITH REDUCED ARC LOSS IN PERIPHERAL CIRCUITRY REGION                      |
| 6,200,857             | D895US                   | United States | 10/13/1999  | 03/13/2001 | METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITHOUT REDUCED ARC LOSS IN PERIPHERAL CIRCUITRY REGION                   |
| 60/224,658            | D897                     | United States | 08/11/2000  |            | PROCESS FOR TREATING ONO DIELECTRIC FILM OF A FLOATING GATE MEMORY CELL                                                  |
| 6,709,927             | D897US                   | United States | 08/10/2001  | 03/23/2004 | PROCESS FOR TREATING ONO DIELECTRIC FILM OF A FLOATING GATE MEMORY CELL                                                  |
| 09/927,988            | D898                     | United States | 08/10/2001  |            | PROCESS FOR TREATING ONO DIELECTRIC FILM OF A FLOATING GATE TYPE MEMORY CELL                                             |
| 60/224,814            | D898                     | United States | 08/11/2000  |            | PROCESS FOR TREATING ONO DIELECTRIC FILM OF A FLOATING GATE TYPE MEMORY CELL                                             |
| 6,304,487             | D898US                   | United States | 02/28/2000  | 10/16/2001 | REGISTER DRIVEN MEANS TO CONTROL PROGRAMMING VOLTAGES                                                                    |
| 09/433,591            | D900                     | United States | 11/02/1999  |            | METHOD AND SYSTEM FOR REDUCING ARC LAYER REMOVAL DURING REMOVAL OF PHOTORESIST                                           |
| 7,015,134             | D900US DIV               | United States | 02/19/2002  | 03/21/2006 | METHOD FOR REDUCING ANTI-REFLECTIVE COATING LAYER REMOVAL DURING REMOVAL OF PHOTORESIST                                  |
| 6,369,416             | D902US                   | United States | 09/23/1999  | 04/09/2002 | SEMICONDUCTOR DEVICE WITH CONTACTS HAVING A SLOPED PROFILE                                                               |
| 6,342,415             | D903US                   | United States | 09/23/1999  | 01/29/2002 | METHOD AND SYSTEM FOR PROVIDING REDUCED-SIZED CONTACTS IN A SEMICONDUCTOR DEVICE                                         |
| 6,235,584             | D908US                   | United States | 10/05/1999  | 05/22/2001 | METHOD AND SYSTEM FOR REDUCING SHORT CHANNEL EFFECTS IN A MEMORY DEVICE                                                  |
| 09/410,962            | D914US                   | United States | 10/05/1999  |            | METHOD AND SYSTEM FOR REDUCING SHORT CHANNEL EFFECTS IN A MEMORY DEVICE BY REDUCTION OF DRAIN THERMAL CYCLING            |
| 60/254,048            | D915                     | United States | 12/06/2000  |            | NOVEL NITRIDING PRETREATMENT OF FLASH ONO NITRIDE FOR OXIDE DEPOSITION                                                   |
| 6,620,705             | D915US                   | United States | 12/05/2001  | 09/16/2003 | NITRIDING PRETREATMENT OF FLASH ONO NITRIDE FOR OXIDE DEPOSITION                                                         |
| 6,858,496             | D916US                   | United States | 12/05/2001  | 02/22/2005 | NOVEL OXIDIZING PRETREATMENT OF FLASH ONO NITRIDE FOR OXIDE DEPOSITION                                                   |
| 6,268,624             | D917                     | United States | 07/31/1999  | 07/31/2001 | METHOD FOR INHIBITING TUNNEL OXIDE GROWTH AT THE EDGES OF A FLOATING GATE DURING SEMICONDUCTOR DEVICE PROCESSING         |
| 6,337,246             | D917US DIV               | United States | 04/02/2001  | 01/08/2002 | METHOD FOR INHIBITING TUNNEL OXIDE GROWTH AT THE EDGES OF A FLOATING GATE DURING SEMICONDUCTOR DEVICE PROCESSING         |
| 6,512,264             | D925US                   | United States | 06/14/2000  | 01/28/2003 | FLASH MEMORY HAVING PRE-INTERPOLY DIELECTRIC TREATMENT LAYER AND METHOD OF FORMING                                       |
| 6,716,702             | D925US DIV               | United States | 11/08/2002  | 04/06/2004 | METHOD OF FORMING FLASH MEMORY HAVING PRE-INTERPOLY DIELECTRIC TREATMENT LAYER                                           |
| 6,306,777             | D928                     | United States | 06/15/2000  | 10/23/2001 | FLASH MEMORY HAVING A TREATMENT LAYER DISPOSED BETWEEN AN INTERPOLY DIELECTRIC STRUCTURE AND METHOD OF FORMING           |
| 6,798,002             | D931US                   | United States | 06/30/2000  | 09/28/2004 | DUAL-PURPOSE ANTI-REFLECTIVE COATING AND SPACER FOR FLASH MEMORY AND OTHER DUAL GATE TECHNOLOGIES AND METHOD FOR FORMING |
| 6,867,097             | D932US                   | United States | 10/28/1999  | 03/15/2005 | POLISHED FLASH PROCESS WITH METAL GATES AND IMPROVED PLANARITY                                                           |
| 09/632,376            | D932US DIV               | United States | 08/03/2000  |            | POLISHED FLASH PROCESS WITH METAL GATES AND IMPROVED PLANARITY                                                           |
| 6,808,996             | D940US                   | United States | 08/18/1999  | 10/26/2004 | METHOD FOR PROTECTING GATE EDGES FROM CHARGE GAIN/LOSS IN SEMICONDUCTOR DEVICE                                           |
| 6,248,627             | D941US                   | United States | 08/18/1999  | 06/19/2001 | METHOD FOR PROTECTING GATE EDGES FROM CHARGE GAIN/LOSS IN SEMICONDUCTOR DEVICE                                           |
| 6,455,373             | D941US DIV               | United States | 04/12/2001  | 09/24/2002 | SEMICONDUCTOR DEVICE HAVING GATE EDGES PROTECTED FROM CHARGE GAIN/LOSS                                                   |
| 09/484,858            | D946                     | United States | 01/18/2000  |            | NOVEL CAPPING LAYER                                                                                                      |
| 6,448,608             | D946US CON               | United States | 08/04/2000  | 09/10/2002 | CAPPING LAYER                                                                                                            |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                 |
|-----------------------|--------------------------|---------------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6,548,334             | D946US DIV               | United States | 06/24/2002  | 04/15/2003 | CAPPING LAYER                                                                                                                                         |
| 6,465,835             | D949US                   | United States | 01/18/2000  | 10/15/2002 | CHARGE GAIN/CHARGE LOSS JUNCTION LEAKAGE PREVENTION FOR FLASH TECHNOLOGY BY USING ISOLATION/CAPPING LAYER BETWEEN LIGHTLY DOPED DRAIN AND GATE        |
| 6,589,841             | D949US DIV               | United States | 06/25/2002  | 07/08/2003 | CHARGE GAIN/CHARGE LOSS JUNCTION LEAKAGE PREVENTION FOR FLASH TECHNOLOGY BY USING DOUBLE ISOLATION/CAPPING LAYER BETWEEN LIGHTLY DOPED DRAIN AND GATE |
| 7,964,905             | D955US                   | United States | 06/06/2000  | 06/21/2011 | ANTI-REFLECTIVE INTERPOLY DIELECTRIC                                                                                                                  |
| 6,787,840             | D956US                   | United States | 01/27/2000  | 09/07/2004 | NITRIDATED TUNNEL OXIDE BARRIERS FOR FLASH MEMORY TECHNOLOGY CIRCUITRY                                                                                |
| 6,509,604             | D958US                   | United States | 01/26/2000  | 01/21/2003 | NITRADATION BARRIERS FOR NITRIDATED TUNNEL OXIDE FOR CIRCUITRY FOR FLASH TECHNOLOGY AND FOR LOCOS/STI ISOLATION                                       |
| 6,605,511             | D958US DIV               | United States | 11/15/2002  | 08/12/2003 | METHOD OF FORMING NITRIDATED TUNNEL OXIDE BARRIERS FOR FLASH MEMORY TECHNOLOGY CIRCUITRY AND STI AND LOCOS ISOLATION                                  |
| 6,294,460             | D962US                   | United States | 05/31/2000  | 09/25/2001 | SEMICONDUCTOR MANUFACTURING METHOD USING A HIGH EXTINCTION COEFFICIENT DIELECTRIC PHOTOMASK                                                           |
| 6,380,067             | D963US                   | United States | 05/31/2000  | 04/30/2002 | METHOD FOR CREATING PARTIALLY UV TRANSPARENT ANTI-REFLECTIVE COATING FOR SEMICONDUCTORS                                                               |
| 6,359,307             | D968US                   | United States | 01/29/2000  | 03/19/2002 | METHOD FOR FORMING SELF-ALIGNED CONTACTS AND INTERCONNECTION LINES USING DUAL DAMASCENE TECHNIQUES                                                    |
| 6,348,379             | D969US                   | United States | 02/11/2000  | 02/19/2002 | METHOD FOR FORMING SELF-ALIGNED CONTACTS USING CONSUMABLE SPACERS                                                                                     |
| 6,509,229             | D969US CON               | United States | 05/07/2001  | 01/21/2003 | METHOD FOR FORMING SELF-ALIGNED CONTACTS USING CONSUMABLE SPACERS                                                                                     |
| 6,348,406             | D970US                   | United States | 05/31/2000  | 02/19/2002 | METHOD FOR USING A LOW DIELECTRIC CONSTANT LAYER AS A SEMICONDUCTOR ANTI-REFLECTIVE COATING                                                           |
| 6,376,389             | D971US                   | United States | 05/31/2000  | 04/23/2002 | METHOD FOR ELIMINATING ANTI-REFLECTIVE COATING IN SEMICONDUCTORS                                                                                      |
| 60/239,467            | D973                     | United States | 10/10/2000  |            | METHOD FOR FORMING SELF-ALIGNED CONTACTS AND LOCAL INTERCONNECTS FOR SALICIDED GATES USING A SECONDARY SPACER                                         |
| 6,306,713             | D973US                   | United States | 03/05/2001  | 10/23/2001 | METHOD FOR FORMING SELF-ALIGNED CONTACTS AND LOCAL INTERCONNECTS FOR SALICIDED GATES USING A SECONDARY SPACER                                         |
| 6,482,699             | D974US                   | United States | 10/10/2000  | 11/19/2002 | METHOD FOR FORMING SELF-ALIGNED CONTACTS AND LOCAL INTERCONNECTS USING DECOUPLED LOCAL INTERCONNECT PROCESS                                           |
| 6,271,087             | D976US                   | United States | 10/10/2000  | 08/07/2001 | METHOD FOR FORMING SELF-ALIGNED CONTACTS AND LOCAL INTERCONNECTS USING SELF-ALIGNED LOCAL INTERCONNECTS                                               |
| 6,420,752             | D977US                   | United States | 02/11/2000  | 07/16/2002 | SEMICONDUCTOR DEVICE WITH SELF-ALIGNED CONTACTS USING A LINER OXIDE LAYER                                                                             |
| 6,475,847             | D977US DIV               | United States | 03/27/2002  | 11/05/2002 | METHOD FOR FORMING A SEMICONDUCTOR DEVICE WITH SELF-ALIGNED CONTACTS USING A LINER OXIDE LAYER                                                        |
| 6,136,649             | D980US                   | United States | 10/12/1999  | 10/24/2000 | METHOD FOR REMOVING ANTI-REFLECTIVE COATING LAYER USING PLASMA ETCH PROCESS AFTER CONTACT CMP                                                         |
| 6,291,296             | D981US                   | United States | 10/12/1999  | 09/18/2001 | METHOD FOR REMOVING ANTI-REFLECTIVE COATING LAYER USING PLASMA ETCH PROCESS BEFORE CONTACT CMP                                                        |
| 6,327,183             | D983US                   | United States | 01/10/2000  | 12/04/2001 | NONLINEAR STEPPED PROGRAMMING VOLTAGE                                                                                                                 |
| 6,141,244             | D984US                   | United States | 09/02/1999  | 10/31/2000 | MULTI LEVEL SENSING OF NAND MEMORY CELLS BY EXTERNAL BIAS CURRENT                                                                                     |
| 6,246,610             | D985US                   | United States | 02/22/2000  | 06/12/2001 | SYMMETRICAL PROGRAM/ERASE SCHEME TO IMPROVE ERASE TIME DEGRADATION IN NAND DEVICES                                                                    |
| 6,246,611             | D987US                   | United States | 02/28/2000  | 06/12/2001 | A SYSTEM FOR ERASING A MEMORY CELL                                                                                                                    |
| 6,545,912             | D988US                   | United States | 11/30/2000  | 04/08/2003 | ERASE VERIFY MODE TO EVALUATE NEGATIVE V <sub>ts</sub>                                                                                                |
| 6,181,605             | D990                     | United States | 10/06/1999  | 01/30/2001 | GLOBAL ERASE/PROGRAM VERIFICATION APPARATUS AND METHOD                                                                                                |
| 6,351,017             | D992US                   | United States | 03/22/2000  | 02/26/2002 | HIGH VOLTAGE TRANSISTOR WITH MODIFIED FIELD IMPLANT MASK                                                                                              |
| 6,514,830             | D992US DIV               | United States | 01/11/2002  | 02/04/2003 | METHOD OF MANUFACTURING HIGH VOLTAGE TRANSISTOR WITH MODIFIED FIELD IMPLANT MASK                                                                      |
| 6,166,951             | D993US                   | United States | 08/06/1999  | 12/26/2000 | MULTI STATE SENSING OF NAND MEMORY CELLS BY APPLYING REVERSE-BIAS VOLTAGE                                                                             |
| 6,504,757             | D994                     | United States | 08/03/2001  | 01/07/2003 | DOUBLE BOOSTING SCHEME FOR NAND TO IMPROVE PROGRAM INHIBIT CHARACTERISTICS                                                                            |
| 6,188,606             | D995US                   | United States | 08/06/1999  | 02/13/2001 | MULTI-STATE SENSING OF NAND MEMORY CELLS BY VARYING SOURCE BIAS                                                                                       |
| 6,185,130             | D996US                   | United States | 10/18/1999  | 02/06/2001 | PROGRAMMABLE CURRENT SOURCE                                                                                                                           |
| 60/254,067            | D997                     | United States | 12/06/2000  |            | USING PROGRAMMABLE/ERASABLE CAMS TO ADJUST CURRENT REFERENCE USED IN NAND SENSING                                                                     |
| 6,525,966             | D997US                   | United States | 12/05/2001  | 02/25/2003 | METHOD AND APPARATUS ADJUSTING ON-CHIP CURRENT REFERENCE FOR EEPROM SENSING                                                                           |
| 6,812,521             | D998US                   | United States | 01/27/2000  | 11/02/2004 | METHOD AND APPARATUS FOR IMPROVED PERFORMANCE OF FLASH MEMORY CELL DEVICES                                                                            |
| 6,177,316             | D999US                   | United States | 10/07/1999  | 01/23/2001 | POST BARRIER METAL CONTACT IMPLANTATION TO MINIMIZE OUT DIFFUSION FOR NAND DEVICE                                                                     |
| 6,529,410             | DA01000US                | United States | 09/20/2000  | 03/04/2003 | NEW NAND ARRAY STRUCTURE USING SUBSTRATE HOT ELECTRON INJECTION SCHEME FOR PROGRAMMING                                                                |
| 6,933,554             | DA01001US                | United States | 07/11/2001  | 08/23/2005 | RECESSED TUNNEL OXIDE PROFILE FOR IMPROVED RELIABILITY IN NAND DEVICES                                                                                |
| 6,269,025             | DA01002                  | United States | 02/09/2000  | 07/31/2001 | MEMORY SYSTEM HAVING A PROGRAM AND ERASE VOLTAGE MODIFIER                                                                                             |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                            |
|-----------------------|--------------------------|---------------|-------------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6,153,470             | DA01004US                | United States | 08/12/1999  | 11/28/2000 | FLOATING GATE ENGINEERING TO IMPROVE TUNNEL OXIDE RELIABILITY FOR FLASH DEVICES                                                                                  |
| 6,580,639             | DA01007                  | United States | 08/10/1999  | 06/17/2003 | METHOD OF REDUCING PROGRAM DISTURBS IN NAND TYPE FLASH MEMORY DEVICES                                                                                            |
| 6,295,228             | DA01009                  | United States | 02/28/2000  | 09/25/2001 | A SYSTEM FOR PROGRAMMING MEMORY CELLS                                                                                                                            |
| 6,365,945             | DA01011US                | United States | 05/02/2000  | 04/02/2002 | SUBMICRON SEMICONDUCTOR DEVICE HAVING A SELF-ALIGNED CHANNEL STOP REGION AND A METHOD FOR FABRICATING THE SEMICONDUCTOR DEVICE USING A TRIM AND ETCH             |
| 6,727,195             | DA01012US                | United States | 02/06/2001  | 04/27/2004 | METHOD AND SYSTEM FOR DECREASING THE SPACES BETWEEN WORDLINES                                                                                                    |
| 6,445,051             | DA01018US                | United States | 05/02/2000  | 09/03/2002 | METHOD AND SYSTEM FOR PROVIDING CONTACTS WITH GREATER TOLERANCE FOR MISALIGNMENT IN A FLASH MEMORY                                                               |
| 6,448,594             | DA01019US                | United States | 03/30/2000  | 09/10/2002 | METHOD AND SYSTEM FOR PROCESSING A SEMICONDUCTOR DEVICE                                                                                                          |
| 6,306,706             | DA01021US                | United States | 03/30/2000  | 10/23/2001 | METHOD AND SYSTEM FOR FABRICATING A FLASH MEMORY ARRAY                                                                                                           |
| 09/368,323            | DA01022                  | United States | 08/03/1999  |            | METHOD AND SYSTEM FOR ETCHING TUNNEL OXIDE TO REDUCE UNDERCUTTING DURING MEMORY ARRAY FABRICATION                                                                |
| 6,472,327             | DA01022US DIV            | United States | 08/08/2001  | 10/29/2002 | METHOD AND SYSTEM FOR ETCHING TUNNEL OXIDE TO REDUCE UNDERCUTTING DURING MEMORY ARRAY FABRICATION                                                                |
| 09/376,396            | DA01023                  | United States | 08/18/1999  |            | METHOD FOR CONTACT SIZE CONTROL FOR NAND TECHNOLOGY                                                                                                              |
| 09/775,723            | DA01023US DIV            | United States | 02/01/2001  |            | METHOD FOR CONTACT SIZE CONTROL FOR NAND TECHNOLOGY                                                                                                              |
| 6,300,658             | DA01024US                | United States | 08/03/1999  | 10/09/2001 | METHOD FOR REDUCED GATE ASPECT RATIO TO IMPROVE GAP-FILL AFTER SPACER ETCH                                                                                       |
| 6,376,309             | DA01024US DIV            | United States | 03/16/2001  | 04/23/2002 | METHOD FOR REDUCED GATE ASPECT RATIO TO IMPROVE GAP-FILL AFTER SPACER ETCH                                                                                       |
| 6,610,580             | DA01025US                | United States | 05/02/2000  | 08/26/2003 | FLASH MEMORY ARRAY AND A METHOD AND SYSTEM OF FABRICATION THEREOF                                                                                                |
| 8,183,619             | DA01028US                | United States | 03/30/2000  | 05/22/2012 | METHOD AND SYSTEM FOR PROVIDING CONTACT TO A FIRST POLYSILICON LAYER IN A FLASH MEMORY DEVICE                                                                    |
| 8,507,969             | DA01028US CON            | United States | 05/07/2012  | 08/13/2013 | METHOD AND SYSTEM FOR PROVIDING CONTACT TO A FIRST POLYSILICON LAYER IN A FLASH MEMORY DEVICE                                                                    |
| 8,329,530             | DA01028US CON2           | United States | 08/03/2012  | 12/11/2012 | METHOD AND SYSTEM FOR PROVIDING CONTACT TO A FIRST POLYSILICON LAYER IN A FLASH MEMORY DEVICE                                                                    |
| 6,323,047             | DA01029US                | United States | 08/03/1999  | 11/27/2001 | METHOD FOR MONITORING SECOND GATE OVER-ETCH IN A SEMICONDUCTOR DEVICE                                                                                            |
| 6,410,949             | DA01029US DIV            | United States | 01/31/2001  | 06/25/2002 | METHOD FOR MONITORING SECOND GATE OVER-ETCH IN A SEMICONDUCTOR DEVICE                                                                                            |
| 6,448,593             | DA01031                  | United States | 01/26/2000  | 09/10/2002 | TYPE-1 POLYSILICON ELECTROSTATIC DISCHARGE TRANSISTORS                                                                                                           |
| 09/495,425            | DA01032                  | United States | 01/31/2000  |            | FLASH MEMORY HAVING IMPROVED CORE FIELD ISOLATION IN SELECT GATE REGIONS                                                                                         |
| 60/172,355            | DA01032PROV              | United States | 12/16/1999  |            | FLASH MEMORY HAVING IMPROVED CORE FIELD ISOLATION IN SELECT GATE REGIONS                                                                                         |
| 6,815,292             | DA01032US DIV            | United States | 09/27/2002  | 11/09/2004 | FLASH MEMORY HAVING IMPROVED CORE FIELD ISOLATION IN SELECTIVE GATE REGIONS                                                                                      |
| 6,448,609             | DA01033US                | United States | 10/28/1999  | 09/10/2002 | METHOD AND SYSTEM FOR PROVIDING A POLYSILICON STRINGER MONITOR                                                                                                   |
| 6,602,776             | DA01033US DIV            | United States | 05/23/2002  | 08/05/2003 | METHOD AND SYSTEM FOR PROVIDING A POLYSILICON STRINGER MONITOR                                                                                                   |
| 6,638,358             | DA01035US                | United States | 01/13/2000  | 10/28/2003 | METHOD AND SYSTEM FOR PROCESSING A SEMICONDUCTOR DEVICE                                                                                                          |
| 6,240,017             | DA01055US                | United States | 07/14/1999  | 05/29/2001 | REDUCTION OF VOLTAGE STRESS ACROSS A GATE OXIDE AND ACROSS A JUNCTION WITHIN A HIGH VOLTAGE TRANSISTOR FOR AN ERASABLE MEMORY DEVICE                             |
| 6,275,424             | DA01055US DIV            | United States | 01/31/2001  | 08/14/2001 | REDUCTION OF VOLTAGE STRESS ACROSS A GATE OXIDE AND ACROSS A JUNCTION WITHIN A HIGH VOLTAGE TRANSISTOR FOR AN ERASABLE MEMORY DEVICE                             |
| 6,380,029             | DA01068US                | United States | 12/04/1998  | 04/30/2002 | METHOD OF FORMING ONO STACKED FILMS AND DCS TUNGSTEN SILICIDE GATE TO IMPROVE POLYCIDAL GATE PERFORMANCE FOR FLASH MEMORY DEVICES                                |
| 6,355,522             | DA01068US CIP            | United States | 03/05/1999  | 03/12/2002 | EFFECT OF DOPED AMORPHOUS SI THICKNESS ON BETTER POLY 1 CONTACT RESISTANCE PERFORMANCE FOR NAND TYPE FLASH MEMORY DEVICES                                        |
| 6,162,684             | DA01069US                | United States | 03/11/1999  | 12/19/2000 | AMONIA ANNEALED AND WET OXIDIZED LPCVD OXIDE TO REPLACE ONO FILM FOR HIGH INTEGRATED FLASH MEMORY DEVICES                                                        |
| 6,184,084             | DA01070US                | United States | 03/05/1999  | 02/06/2001 | METHOD TO ELIMINATE SILICIDE CRACKING FOR NAND TYPE FLASH MEMORY DEVICES BY IMPLANTING A POLISH RATE IMPROVER INTO THE SECOND POLYSILICON LAYER AND POLISHING IT |
| 6,309,927             | DA01096US                | United States | 03/05/1999  | 10/30/2001 | METHOD OF FORMING HIGH K TANTALUM PENTOXIDE TA2O5 INSTEAD OF ONO STACKED FILMS TO INCREASE COUPLING RATIO AND IMPROVE RELIABILITY FOR FLASH MEMORY DEVICES       |
| 6,338,001             | E0014US                  | United States | 02/22/1999  | 01/08/2002 | IN-LINE YIELD PREDICTION USING ADC DETERMINED KILL RATIOS, DIE HEALTH STATISTICS AND DIE STACKING                                                                |
| 6,515,344             | E0082US                  | United States | 10/30/2000  | 02/04/2003 | THIN OXIDE ANTI-FUSE                                                                                                                                             |
| 6,381,179             | E0187US                  | United States | 09/07/2000  | 04/30/2002 | USING NEGATIVE GATE ERASE TO INCREASE THE CYCLING ENDURANCE OF A NON-VOLATILE MEMORY CELL WITH AN OXIDE-NITRIDE-OXIDE (ONO) STRUCTURE                            |
| 6,501,681             | E0188US                  | United States | 10/04/2000  | 12/31/2002 | USING A LOW DRAIN BIAS DURING ERASE VERIFY TO ENSURE COMPLETE REMOVAL OF RESIDUAL CHARGE IN THE NITRIDE IN SONOS NON-VOLATILE MEMORIES                           |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                               |
|-----------------------|--------------------------|---------------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------|
| 60/217,137            | E0189                    | United States | 07/10/2000  |            | USING HOT CARRIER INJECTION TO CONTROL OVER-PROGRAMMING IN A NON-VOLATILE MEMORY CELL HAVING AN OXIDE-NITRIDE-OXIDE (ONO) STRUCTURE |
| 6,519,182             | E0189US                  | United States | 07/10/2001  | 02/11/2003 | USING HOT CARRIER INJECTION TO CONTROL OVER-PROGRAMMING IN A NON-VOLATILE MEMORY CELL HAVING AN OXIDE-NITRIDE-OXIDE (ONO) STRUCTURE |
| 6,418,054             | E0190US                  | United States | 08/31/1999  | 07/09/2002 | EMBEDDED METHODOLOGY TO PROGRAM/ERASE REFERENCE CELLS USED IN SENSING FLASH CELLS                                                   |
| 6,288,951             | E0192US                  | United States | 09/29/2000  | 09/11/2001 | METHOD AND APPARATUS FOR CONTINUOUSLY REGULATING A CHARGE PUMP OUTPUT VOLTAGE USING A CAPACITOR DIVIDER                             |
| 6,411,069             | E0193US                  | United States | 08/31/1999  | 06/25/2002 | CONTINUOUS CAPACITOR DIVIDER SAMPLED REGULATION SCHEME                                                                              |
| 6,204,159             | E0197US                  | United States | 07/09/1999  | 03/20/2001 | NEW METHOD OF FORMING SELECT GATE TO IMPROVE RELIABILITY AND PERFORMANCE FOR NAND-TYPE FLASH MEMORY DEVICES                         |
| 6,287,917             | E0198US                  | United States | 09/08/1999  | 09/11/2001 | PROCESS FOR FABRICATING AN MNOS FLASH MEMORY DEVICE                                                                                 |
| 6,178,129             | E0208US                  | United States | 10/19/1999  | 01/23/2001 | SEPARATE OUTPUT POWER SUPPLY TO REDUCE OUTPUT NOISE FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE                                |
| 6,201,747             | E0233US                  | United States | 09/30/1999  | 03/13/2001 | METHOD AND APPARATUS FOR MEASURING SUBTHRESHOLD CURRENT IN A MEMORY ARRAY                                                           |
| 6,259,645             | E0234US                  | United States | 04/26/2000  | 07/10/2001 | MATCHING LOADING BETWEEN REFERENCE AND CELL WITH REDUCED TRANSISTOR COUNT IN A DUAL-BANK FLASH MEMORY                               |
| 6,243,291             | E0241US                  | United States | 02/15/2000  | 06/05/2001 | TWO-STAGE PIPELINE SENSING FOR PAGE MODE FLASH MEMORY                                                                               |
| 6,542,435             | E0242                    | United States | 03/21/2000  | 04/01/2003 | METHOD AND APPARATUS FOR EQUALIZATION OF ADDRESS TRANSITION DETECTION PULSE WIDTH                                                   |
| 6,160,750             | E0243US                  | United States | 02/04/2000  | 12/12/2000 | NOISE REDUCTION DURING SIMULTANEOUS OPERATION FOR FLASH MEMORY DEVICE                                                               |
| 6,118,702             | E0244US                  | United States | 10/19/1999  | 09/12/2000 | SOURCE BIAS COMPENSATION FOR PAGE MODE READ OPERATION IN A FLASH MEMORY DEVICE                                                      |
| 6,147,906             | E0248US                  | United States | 10/14/1999  | 11/14/2000 | METHOD AND SYSTEM FOR SAVING OVERHEAD PROGRAM TIME IN A MEMORY DEVICE                                                               |
| 6,212,098             | E0249US                  | United States | 06/22/2000  | 04/03/2001 | VOLTAGE PROTECTION OF WRITE PROTECT CAMS                                                                                            |
| 6,285,594             | E0250US                  | United States | 03/13/2000  | 09/04/2001 | WORDLINE VOLTAGE PROTECTION                                                                                                         |
| 6,088,287             | E0251US                  | United States | 08/23/1999  | 07/11/2000 | FLASH MEMORY ARCHITECTURE EMPLOYING THREE LAYER METAL INTERCONNECT                                                                  |
| 6,269,026             | E0255US                  | United States | 04/12/2000  | 07/31/2001 | CHARGE SHARING TO HELP BOOST THE WORDLINES DURING APDE VERIFY                                                                       |
| 6,359,824             | E0256US                  | United States | 06/09/2000  | 03/19/2002 | ACTIVATION OF WORDLINE DECODERS TO TRANSFER A HIGH VOLTAGE SUPPLY                                                                   |
| 6,144,606             | E0258US                  | United States | 10/14/1999  | 11/07/2000 | METHOD AND SYSTEM FOR BI-DIRECTIONAL VOLTAGE REGULATION DETECTION                                                                   |
| 60/185,149            | E0259                    | United States | 02/25/2000  |            | THREE METAL PROCESS FOR OPTIMIZING LAYOUT DENSITY                                                                                   |
| 6,459,625             | E0259US                  | United States | 01/23/2001  | 10/01/2002 | THREE METAL PROCESS FOR OPTIMIZING LAYOUT DENSITY                                                                                   |
| 6,118,694             | E0261US                  | United States | 10/14/1999  | 09/12/2000 | DISTRIBUTING CFI DEVICES IN EXISTING DECODERS                                                                                       |
| 6,430,087             | E0264US                  | United States | 04/12/2000  | 08/06/2002 | TRIMMING METHOD AND SYSTEM FOR WORDLINE BOOSTER TO MINIMIZE PROCESS VARIATION OF BOOSTED WORDLINE VOLTAGE                           |
| 60/184,978            | E0267                    | United States | 02/25/2000  |            | SERIAL SEQUENCING OF AUTOMATIC PROGRAM DISTURB ERASE VERIFY DURING A FAST ERASE MODE                                                |
| 6,370,065             | E0267US                  | United States | 09/22/2000  | 04/09/2002 | SERIAL SEQUENCING OF AUTOMATIC PROGRAM DISTURB ERASE VERIFY DURING A FAST ERASE MODE                                                |
| 6,175,523             | E0269                    | United States | 10/25/1999  | 01/16/2001 | PRECHARGING MECHANISM AND METHOD FOR NAND-BASED FLASH MEMORY DEVICES                                                                |
| 6,240,020             | E0270                    | United States | 10/25/1999  | 05/29/2001 | A METHOD OF BITLINE SHIELDING IN CONJUNCTION WITH A PRECHARGING SCHEME FOR NAND-BASED FLASH MEMORY DEVICES                          |
| 6,732,308             | E0275US                  | United States | 09/19/2000  | 05/04/2004 | INTEGRATION OF EMBEDDED AND TEST MODE TIMER                                                                                         |
| 6,222,768             | E0283US                  | United States | 04/26/2000  | 04/24/2001 | AUTO-ADJUSTING WINDOW PLACEMENT SCHEME FOR AN NROM VIRTUAL GROUND ARRAY                                                             |
| 6,472,898             | E0284US                  | United States | 11/22/2000  | 10/29/2002 | METHOD AND SYSTEM FOR TESTING A SEMICONDUCTOR MEMORY DEVICE                                                                         |
| 6,269,023             | E0288US                  | United States | 10/23/2000  | 07/31/2001 | METHOD OF PROGRAMMING A NON-VOLATILE MEMORY CELL USING A CURRENT LIMITER                                                            |
| 6,272,043             | E0289US                  | United States | 06/23/2000  | 08/07/2001 | APPARATUS AND METHOD OF DIRECT CURRENT SENSING FROM SOURCE SIDE IN A VIRTUAL GROUND ARRAY                                           |
| 6,215,702             | E0295US                  | United States | 02/26/2000  | 04/10/2001 | METHOD OF MAINTAINING CONSTANT ERASING SPEED FOR NON-VOLATILE MEMORY CELLS                                                          |
| 6,331,952             | E0296US                  | United States | 10/26/2000  | 12/18/2001 | POSITIVE GATE ERASURE FOR NON-VOLATILE MEMORY CELLS                                                                                 |
| 6,490,205             | E0297US                  | United States | 10/26/2000  | 12/03/2002 | METHOD OF ERASING A NON-VOLATILE MEMORY CELL USING A SUBSTRATE BIAS                                                                 |
| 6,266,281             | E0298US                  | United States | 02/16/2000  | 07/24/2001 | METHOD OF ERASING NON-VOLATILE MEMORY CELLS                                                                                         |
| 6,331,953             | E0300US                  | United States | 10/26/2000  | 12/18/2001 | INTELLIGENT RAMPED GATE AND RAMPED DRAIN ERASURE FOR NON-VOLATILE MEMORY CELLS                                                      |
| 6,243,300             | E0301US                  | United States | 02/16/2000  | 06/05/2001 | SUBSTRATE HOLE INJECTION FOR NEUTRALIZING SPILLOVER CHARGE GENERATED DURING PROGRAMING OF A NON-VOLATILE MEMORY CELL                |
| 6,275,414             | E0302US CON              | United States | 11/22/2000  | 08/14/2001 | UNIFORM BITLINE STRAPPING OF NON-VOLATILE MEMORY CELL                                                                               |
| 6,538,270             | E0303US                  | United States | 11/22/2000  | 03/25/2003 | STAGGERED BITLINE STRAPPING OF A NON-VOLATILE MEMORY CELL                                                                           |
| 6,593,606             | E0304US                  | United States | 11/22/2000  | 07/15/2003 | STAGGERED BITLINE STRAPPING OF A NON-VOLATILE MEMORY CELL                                                                           |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                               |
|-----------------------|--------------------------|---------------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 60/213,394            | E0305                    | United States | 06/23/2000  |            | METHOD OF PROGRAMMING A NON-VOLATILE MEMORY CELL USING A SUBSTRATE BIAS                                                                                             |
| 6,456,536             | E0305US                  | United States | 06/19/2001  | 09/24/2002 | METHOD OF PROGRAMMING A NON-VOLATILE MEMORY CELL USING A SUBSTRATE BIAS                                                                                             |
| 09/697,791            | E0309                    | United States | 10/26/2000  |            | NON-VOLATILE MEMORY CELL WITH A NITRIDATED OXIDE LAYER                                                                                                              |
| 6,750,157             | E0309US CIP              | United States | 07/19/2002  | 06/15/2004 | NON-VOLATILE MEMORY CELL WITH A NITRIDATED OXIDE LAYER                                                                                                              |
| 6,417,081             | E0311US                  | United States | 11/22/2000  | 07/09/2002 | PROCESS FOR REDUCTION OF CAPACITANCE OF A BITLINE FOR A NON-VOLATILE MEMORY CELL                                                                                    |
| 60/227,836            | E0312                    | United States | 08/25/2000  |            | METHOD OF PROGRAMMING A NON-VOLATILE MEMORY CELL USING A VERTICAL ELECTRIC FIELD                                                                                    |
| 6,487,121             | E0312US                  | United States | 07/05/2001  | 11/26/2002 | METHOD OF PROGRAMMING A NON-VOLATILE MEMORY CELL USING A VERTICAL ELECTRIC FIELD                                                                                    |
| 60/213,397            | E0313                    | United States | 06/23/2000  |            | METHOD OF DRAIN AVALANCHE PROGRAMMING OF A NON-VOLATILE MEMORY CELL                                                                                                 |
| 6,456,531             | E0313US                  | United States | 06/19/2001  | 09/24/2002 | METHOD OF DRAIN AVALANCHE PROGRAMMING OF A NON-VOLATILE MEMORY CELL                                                                                                 |
| 6,618,290             | E0319US                  | United States | 06/13/2001  | 09/09/2003 | METHOD OF PROGRAMMING A NON-VOLATILE MEMORY CELL USING A BAKING PROCESS                                                                                             |
| 60/227,883            | E0321                    | United States | 08/25/2000  |            | METHOD OF PROGRAMMING A NON-VOLATILE MEMORY CELL USING A DRAIN BIAS                                                                                                 |
| 6,459,618             | E0321US                  | United States | 06/13/2001  | 10/01/2002 | METHOD OF PROGRAMMING A NON-VOLATILE MEMORY CELL USING A DRAIN BIAS                                                                                                 |
| 6,349,062             | E0322US                  | United States | 10/11/2000  | 02/19/2002 | SELECTIVE ERASURE OF A NON-VOLATILE MEMORY CELL OF A FLASH MEMORY DEVICE                                                                                            |
| 6,366,501             | E0324US                  | United States | 10/11/2000  | 04/02/2002 | SELECTIVE ERASURE OF A NON-VOLATILE MEMORY CELL OF A FLASH MEMORY DEVICE                                                                                            |
| 6,399,446             | E0325US                  | United States | 10/29/1999  | 06/04/2002 | PROCESS FOR FABRICATING HIGH DENSITY MEMORY CELLS USING A METALLIC HARD MASK                                                                                        |
| 6,486,029             | E0328US                  | United States | 07/28/2000  | 11/26/2002 | INTEGRATION OF AN ION IMPLANT HARD MASK STRUCTURE INTO A PROCESS FOR FABRICATING HIGH DENSITY MEMORY CELLS                                                          |
| 6,376,341             | E0329US                  | United States | 07/28/2000  | 04/23/2002 | OPTIMIZATION OF THERMAL CYCLE FOR FORMATION OF POCKET IMPLANTS                                                                                                      |
| 6,326,268             | E0330US                  | United States | 10/25/1999  | 12/04/2001 | METHOD OF FABRICATING A MONOS FLASH CELL USING SHALLOW TRENCH ISOLATION                                                                                             |
| 6,207,502             | E0331US                  | United States | 10/25/1999  | 03/27/2001 | METHOD OF USING SOURCE/DRAIN NITRIDE FOR PERIPHERY FIELD OXIDE AND BIT-LINE OXIDE                                                                                   |
| 6,406,960             | E0334US                  | United States | 10/25/1999  | 06/18/2002 | PROCESS FOR FABRICATING AN ONO STRUCTURE HAVING A SILICON-RICH SILICON NITRIDE LAYER                                                                                |
| 6,458,677             | E0337US                  | United States | 10/25/1999  | 10/01/2002 | PROCESS FOR FABRICATING AN ONO STRUCTURE                                                                                                                            |
| 6,410,388             | E0338US                  | United States | 07/20/2000  | 06/25/2002 | PROCESS FOR OPTIMIZING POCKET IMPLANT PROFILE BY RTA IMPLANT ANNEALING FOR A NON-VOLATILE SEMICONDUCTOR DEVICE                                                      |
| 6,537,881             | E0339US                  | United States | 10/16/2000  | 03/25/2003 | PROCESS FOR FABRICATING A NON-VOLATILE MEMORY DEVICE                                                                                                                |
| 6,319,775             | E0340US                  | United States | 10/25/1999  | 11/20/2001 | NITRIDATION PROCESS FOR FABRICATING AN ONO FLOATING GATE ELECTRODE IN A TWO-BIT EEPROM DEVICE                                                                       |
| 6,436,766             | E0342US                  | United States | 10/29/1999  | 08/20/2002 | PROCESS FOR FABRICATING HIGH DENSITY MEMORY CELLS USING A POLYCYLICON HARD MASK                                                                                     |
| 6,458,656             | E0347US                  | United States | 07/28/2000  | 10/01/2002 | PROCESS FOR CREATING A FLASH MEMORY CELL USING A PHOTORESIST FLOW OPERATION                                                                                         |
| 6,362,052             | E0349US                  | United States | 07/28/2000  | 03/26/2002 | USE OF AN ETCH TO REDUCE THICKNESS AND ROUND THE EDGES OF A RESIST MASK DURING THE CREATION OF A MEMORY CELL                                                        |
| 6,168,993             | E0350US                  | United States | 01/19/2000  | 01/02/2001 | PROCESS FOR FABRICATING A SEMICONDUCTOR DEVICE HAVING A GRADED JUNCTION                                                                                             |
| 6,376,308             | E0351US                  | United States | 01/19/2000  | 04/23/2002 | PROCESS FOR FABRICATING AN EEPROM DEVICE HAVING A POCKET SUBSTRATE REGION                                                                                           |
| 6,391,730             | E0353US                  | United States | 09/25/2000  | 05/21/2002 | PROCESS FOR FABRICATING SHALLOW POCKET REGIONS IN A NON-VOLATILE SEMICONDUCTOR DEVICE                                                                               |
| 6,475,915             | E0354                    | United States | 10/19/1999  | 11/05/2002 | ONO ETCH USING Cl <sub>2</sub> /He CHEMISTRY                                                                                                                        |
| 6,562,683             | E0355                    | United States | 08/31/2000  | 05/13/2003 | BIT-LINE OXIDATION BY REMOVING ONO OXIDE PRIOR TO BIT-LINE IMPLANT                                                                                                  |
| 6,297,143             | E0360US                  | United States | 10/25/1999  | 10/02/2001 | PROCESS FOR FORMING A BIT-LINE IN A MONOS DEVICE                                                                                                                    |
| 60/234,523            | E0363                    | United States | 09/21/2000  |            | HIGHLY CONDUCTIVE SEMICONDUCTOR STRUCTURES, METHOD OF FORMING SAME VIA DAMASCENE, AND ELECTRICAL DEVICES INCORPORATING HIGHLY CONDUCTIVE SEMICONDUCTOR STRUCTURES   |
| 6,627,526             | E0363US                  | United States | 03/13/2001  | 09/30/2003 | METHOD FOR FABRICATING A CONDUCTIVE STRUCTURE FOR A SEMICONDUCTOR DEVICE                                                                                            |
| 60/234,522            | E0365                    | United States | 09/21/2000  |            | HIGHLY CONDUCTIVE SEMICONDUCTOR STRUCTURES, METHOD OF FORMING SAME VIA PLASMA ETCH, AND ELECTRICAL DEVICES INCORPORATING HIGHLY CONDUCTIVE SEMICONDUCTOR STRUCTURES |
| 7,217,652             | E0365US                  | United States | 03/13/2001  | 05/15/2007 | METHOD OF FORMING HIGHLY CONDUCTIVE SEMICONDUCTOR STRUCTURES VIA PLASMA ETCH                                                                                        |
| 7,012,008             | E0370US                  | United States | 12/01/2000  | 03/14/2006 | A DUAL SPACER PROCESS NON-VOLATILE MEMORY DEVICES                                                                                                                   |
| 6,573,151             | E0374                    | United States | 06/19/2001  | 06/03/2003 | METHOD OF FORMING ZERO MARKS                                                                                                                                        |
| 60/227,121            | E0374                    | United States | 08/22/2000  |            | METHOD OF FORMING ZERO MARKS                                                                                                                                        |
| 6,242,306             | E0376US                  | United States | 07/28/2000  | 06/05/2001 | DUAL BIT ISOLATION SCHEME FOR FLASH MEMORY DEVICES HAVING POLYSILICON FLOATING GATES                                                                                |
| 6,680,507             | E0376US DIV              | United States | 04/11/2001  | 01/20/2004 | DUAL BIT ISOLATION SCHEME FOR FLASH MEMORY DEVICES HAVING POLYSILICON FLOATING GATES                                                                                |
| 6,261,904             | E0377US                  | United States | 06/19/2000  | 07/17/2001 | DUAL BIT ISOLATION SCHEME FOR FLASH DEVICES                                                                                                                         |
| 6,355,514             | E0378US                  | United States | 06/19/2000  | 03/12/2002 | DUAL BIT ISOLATION SCHEME FOR FLASH DEVICES                                                                                                                         |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                     |
|-----------------------|---------------------------|---------------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 6,530,068             | E0407US                   | United States | 08/03/1999  | 03/04/2003 | DEVICE MODELING AND CHARACTERIZATION STRUCTURE WITH MULTIPLEXED PADS                                                                      |
| 6,242,790             | E0421US                   | United States | 08/30/1999  | 06/05/2001 | USING POLYSILICON FUSE FOR IC PROGRAMMING                                                                                                 |
| 6,329,687             | E0431US                   | United States | 01/27/2000  | 12/11/2001 | TWO-BIT FLASH CELL WITH TWO FLOATING GATE REGIONS                                                                                         |
| 6,438,031             | E0432US                   | United States | 10/26/2000  | 08/20/2002 | METHOD OF PROGRAMMING A NON-VOLATILE MEMORY CELL USING A SUBSTRATE BIAS                                                                   |
| 6,452,441             | E0451US                   | United States | 10/01/1999  | 09/17/2002 | LOW THRESHOLD VOLTAGE DEVICE WITH CHARGE PUMP FOR REDUCING STANDBY CURRENT IN AN INTEGRATED CIRCUIT HAVING REDUCED SUPPLY VOLTAGE         |
| 6,284,602             | E0456US                   | United States | 09/20/1999  | 09/04/2001 | PROCESS TO REDUCE POST CYCLING PROGRAM VT DISPERSION FOR NAND FLASH MEMORY DEVICES                                                        |
| 6,380,033             | E0457US                   | United States | 09/20/1999  | 04/30/2002 | PROCESS TO IMPROVE READ DISTURB FOR NAND FLASH MEMORY DEVICES                                                                             |
| 60/208,449            | E0462                     | United States | 05/31/2000  |            | DUAL PORTED CAMS FOR SIMULTANEOUS OPERATION FLASH MEMORY                                                                                  |
| 6,396,749             | E0462US                   | United States | 04/10/2001  | 05/28/2002 | DUAL-PORTED CAMS FOR SIMULTANEOUS OPERATION FLASH MEMORY                                                                                  |
| 6,377,488             | E0463US                   | United States | 08/24/2000  | 04/23/2002 | FAST ERASE MEMORY DEVICE AND METHOD FOR REDUCING ERASE TIME IN A MEMORY DEVICE                                                            |
| 6,567,289             | E0466                     | United States | 08/23/2000  | 05/20/2003 | PHYSICAL MEMORY LAYOUT WITH VARIOUS SIZED MEMORY SECTORS                                                                                  |
| 6,292,425             | E0470US                   | United States | 10/25/2000  | 09/18/2001 | POWER SAVING ON THE FLY DURING READING OF DATA FROM A MEMORY DEVICE                                                                       |
| 6,654,848             | E0471US                   | United States | 09/15/2000  | 11/25/2003 | SIMULTANEOUS EXECUTION OF COMMAND MODES IN A FLASH MEMORY DEVICE                                                                          |
| 6,957,297             | E0471US CON               | United States | 06/23/2003  | 10/18/2005 | SIMULTANEOUS EXECUTION OF COMMAND MODES IN A FLASH MEMORY DEVICE                                                                          |
| 6,285,583             | E0472US                   | United States | 02/17/2000  | 09/04/2001 | HIGH SPEED SENSING TO DETECT WRITE PROTECT STATE IN A FLASH MEMORY DEVICE                                                                 |
| 6,215,705             | E0476US                   | United States | 02/10/2000  | 04/10/2001 | SIMULTANEOUS PROGRAM, PROGRAM VERIFY SCHEME                                                                                               |
| 6,236,603             | E0477US                   | United States | 01/21/2000  | 05/22/2001 | HIGH SPEED CHARGING OF CORE CELL DRAIN LINES IN A MEMORY DEVICE                                                                           |
| 6,424,569             | E0480                     | United States | 02/25/2000  | 07/23/2002 | USER SELECTABLE CELL PROGRAMMING                                                                                                          |
| 6,219,276             | E0481                     | United States | 02/25/2000  | 04/17/2001 | MULTI-LEVEL CELL PROGRAMMING                                                                                                              |
| 6,205,055             | E0482US                   | United States | 02/25/2000  | 03/20/2001 | DYNAMIC MEMORY CELL PROGRAMMING VOLTAGE                                                                                                   |
| 6,728,913             | E0483                     | United States | 02/25/2000  | 04/27/2004 | DATA RECYCLING IN MEMORY                                                                                                                  |
| 6,297,988             | E0484US                   | United States | 02/25/2000  | 10/02/2001 | MODE INDICATOR FOR MULTI-LEVEL MEMORY                                                                                                     |
| 6,535,419             | E0484US CON               | United States | 07/13/2001  | 03/18/2003 | MIXED MODE MULTI-LEVEL INDICATOR                                                                                                          |
| 6,707,713             | E0485                     | United States | 02/21/2001  | 10/11/2004 | INTERLACED MULTI-LEVEL MEMORY                                                                                                             |
| 6,180,454             | E0497US                   | United States | 10/29/1999  | 01/30/2001 | METHOD FOR FORMING FLASH MEMORY DEVICES                                                                                                   |
| 6,376,877             | E0498US                   | United States | 02/24/2000  | 04/23/2002 | DOUBLE SELF-ALIGNING SHALLOW TRENCH ISOLATION SEMICONDUCTOR AND MANUFACTURING METHOD THEREFOR                                             |
| 6,225,849             | E0504US                   | United States | 02/25/2000  | 05/01/2001 | HIGH SPEED, HIGH PRECISION, POWER SUPPLY AND PROCESS INDEPENDENT BOOST LEVEL CLAMPING TECHNIQUE                                           |
| 6,495,853             | E0540US                   | United States | 08/10/2000  | 12/17/2002 | SELF-ALIGNED GATE SEMICONDUCTOR                                                                                                           |
| 6,448,606             | E0559US                   | United States | 02/24/2000  | 09/10/2002 | SEMICONDUCTOR WITH INCREASED GATE COUPLING COEFFICIENT                                                                                    |
| 10/142,212            | E0559US DIV               | United States | 05/08/2002  |            | SEMICONDUCTOR WITH INCREASED GATE COUPLING COEFFICIENT AND MANUFACTURING METHOD THEREOF                                                   |
| 6,622,201             | E0584US                   | United States | 03/14/2000  | 09/16/2003 | CHAINED ARRAY OF SEQUENTIAL ACCESS MEMORIES ENABLING CONTINUOUS READ                                                                      |
| 6,449,190             | E0971US                   | United States | 01/17/2001  | 09/10/2002 | ADAPTIVE REFERENCE CELLS FOR A MEMORY DEVICE                                                                                              |
| 6,622,274             | E0975US                   | United States | 09/05/2000  | 09/16/2003 | METHOD OF MICRO-ARCHITECTURAL IMPLEMENTATION ON BIST FRONTED STATE MACHINE UTILIZING 'DEATH LOGIC' STATE TRANSITION FOR AREA MINIMIZATION |
| 6,587,982             | E0976US                   | United States | 09/05/2000  | 07/01/2003 | METHOD OF MICRO-ARCHITECTURAL IMPLEMENTATION OF INTERFACE BETWEEN BIST STATE MACHINE AND TESTER INTERFACE TO ENABLE BIST CYCLING          |
| 6,969,654             | E1017US                   | United States | 11/28/2000  | 11/29/2005 | FLASH NVROM DEVICES WITH UV CHARGE IMMUNITY                                                                                               |
| 6,838,869             | E1019US                   | United States | 04/02/2001  | 01/04/2005 | CLOCKED BASED METHOD AND DEVICES FOR MEASURING VOLTAGE-VARIABLE CAPACITANCES AND OTHER ON-CHIP PARAMETERS                                 |
| 6,343,033             | E1021US                   | United States | 02/25/2000  | 01/29/2002 | VARIABLE PULSE WIDTH MEMORY PROGRAMMING                                                                                                   |
| 6,205,074             | E1030US                   | United States | 07/06/2000  | 03/20/2001 | TEMPERATURE COMPENSATED BIAS GENERATOR                                                                                                    |
| 6,815,286             | ESC001US CIP              | United States | 09/11/2002  | 11/09/2004 | MEMORY DEVICE                                                                                                                             |
| 6,806,526             | ESC002US CIP              | United States | 11/27/2002  | 10/19/2004 | MEMORY DEVICE                                                                                                                             |
| 6,838,720             | ESC003US CIP              | United States | 04/15/2003  | 01/04/2005 | MEMORY DEVICE WITH ACTIVE AND PASSIVE LAYERS                                                                                              |
| 6,858,481             | ESC004US CIP              | United States | 04/15/2003  | 02/22/2005 | MEMORY DEVICE WITH ACTIVE AND PASSIVE LAYERS                                                                                              |
| 6,864,522             | ESC005US CIP              | United States | 04/15/2003  | 03/08/2005 | MEMORY DEVICE                                                                                                                             |
| 6,768,157             | ESC006US CIP              | United States | 04/15/2003  | 07/27/2004 | MEMORY DEVICE                                                                                                                             |
| 6,560,729             | F0004                     | United States | 07/03/2000  | 05/06/2003 | AUTOMATED DETERMINATION AND DISPLAY OF THE PHYSICAL LOCATION OF A FAILED CELL IN AN ARRAY OF MEMORY CELLS                                 |
| 6,436,778             | F0005US                   | United States | 06/12/2001  | 08/20/2002 | RE-OXIDATION APPROACH TO IMPROVE PERIPHERAL GATE OXIDE INTEGRITY IN A TUNNEL NITRIDE OXIDATION PROCESS                                    |
| 09/618,323            | F0007                     | United States | 07/18/2000  |            | AMORPHOUS SILICON DEPOSITION AND OXIDATION FOR INCREASING ONO BARRIER HEIGHT IN FLASH MEMORY DEVICES                                      |
| 6,284,600             | F0009US                   | United States | 07/03/2000  | 09/04/2001 | SPECIES IMPLANTATION FOR MINIMIZING INTERFACE DEFECT DENSITY IN FLASH MEMORY DEVICES                                                      |
| 6,399,984             | F0009US DIV               | United States | 06/15/2001  | 06/04/2002 | SPECIES IMPLANTATION FOR MINIMIZING INTERFACE DEFECT DENSITY IN FLASH MEMORY DEVICES                                                      |
| 6,403,420             | F0014US                   | United States | 07/28/2000  | 06/11/2002 | NITROGEN IMPLANT AFTER BIT-LINE FORMATION FOR ONO FLASH MEMORY DEVICES                                                                    |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                                |
|-----------------------|---------------------------|---------------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6,252,803             | F0055US                   | United States | 10/23/2000  | 06/26/2001 | AUTOMATIC PROGRAM DISTURB WITH INTELLIGENT SOFT<br>PROGRAMMING FOR FLASH CELLS                                                                                                       |
| 6,407,960             | F0070US                   | United States | 09/01/2000  | 06/18/2002 | ARRANGEMENT FOR PROGRAMMING SELECTED DEVICE REGISTERS<br>DURING INITIALIZATION FROM AN EXTERNAL MEMORY                                                                               |
| 6,363,014             | F0073US                   | United States | 10/23/2000  | 03/26/2002 | LOW COLUMN LEAKAGE NOR FLASH ARRAY- SINGLE CELL<br>IMPLEMENTATION                                                                                                                    |
| 6,449,188             | F0145US                   | United States | 06/19/2001  | 09/10/2002 | LOW COLUMN LEAKAGE NOR FLASH ARRAY-DOUBLE CELL<br>IMPLEMENTATION                                                                                                                     |
| 6,331,951             | F0257US                   | United States | 11/21/2000  | 12/18/2001 | METHOD AND SYSTEM FOR EMBEDDED CHIP ERASE VERIFICATION                                                                                                                               |
| 6,529,412             | F0258US                   | United States | 01/16/2002  | 03/04/2003 | SOURCE SIDE SENSING SCHEME FOR VIRTUAL GROUND READ OF<br>FLASH EPROM ARRAY WITH ADJACENT BIT PRECHARGE                                                                               |
| 6,424,570             | F0259US                   | United States | 06/26/2001  | 07/23/2002 | MODULATED CHARGE PUMP WHICH USES AN ANALOG TO DIGITAL<br>CONVERTER TO COMPENSATE FOR SUPPLY VOLTAGE VARIATIONS                                                                       |
| 6,515,902             | F0260US                   | United States | 06/04/2001  | 02/04/2003 | METHOD AND APPARATUS FOR BOOSTING BITLINES FOR LOW VCC<br>READ                                                                                                                       |
| 6,532,175             | F0262US                   | United States | 01/16/2002  | 03/11/2003 | METHOD AND APPARATUS FOR SOFT PROGRAM VERIFICATION IN A<br>MEMORY DEVICE                                                                                                             |
| 6,515,903             | F0263US                   | United States | 01/16/2002  | 02/04/2003 | NEGATIVE PUMP REGULATOR USING MOS CAPACITOR                                                                                                                                          |
| 6,459,628             | F0264US                   | United States | 04/02/2001  | 10/01/2002 | SYSTEM AND METHOD TO FACILITATE STABILIZATION OF REFERENCE<br>VOLTAGE SIGNALS IN MEMORY DEVICES                                                                                      |
| 6,549,477             | F0264US DIV               | United States | 08/19/2002  | 04/15/2003 | SYSTEM AND METHOD TO FACILITATE STABILIZATION OF REFERENCE<br>VOLTAGE SIGNALS IN MEMORY DEVICES                                                                                      |
| 7,057,949             | F0265US                   | United States | 01/16/2002  | 06/06/2006 | METHOD AND APPARATUS FOR PRE-CHARGING NEGATIVE PUMP<br>MOS REGULATION CAPACITORS                                                                                                     |
| 6,512,701             | F0266US                   | United States | 06/21/2001  | 01/28/2003 | ERASE METHOD FOR DUAL BIT VIRTUAL GROUND FLASH                                                                                                                                       |
| 60/265,426            | F0267                     | United States | 01/31/2001  |            | DATA RETENTION CHARACTERISTICS AS A RESULT OF HIGH<br>TEMPERATURE BAKE                                                                                                               |
| 6,344,994             | F0267US                   | United States | 02/28/2001  | 02/05/2002 | DATA RETENTION CHARACTERISTICS AS A RESULT OF HIGH<br>TEMPERATURE BAKE                                                                                                               |
| 60/265,277            | F0268                     | United States | 01/31/2001  |            | SINGLE BIT ARRAY EDGES                                                                                                                                                               |
| 6,493,261             | F0268US                   | United States | 02/28/2001  | 12/10/2002 | SINGLE BIT ARRAY EDGES                                                                                                                                                               |
| 6,442,074             | F0269US                   | United States | 02/28/2001  | 08/27/2002 | TAILORED ERASE METHOD USING HIGHER PROGRAM VT AND HIGHER<br>NEGATIVE GATE ERASE                                                                                                      |
| 6,567,303             | F0272                     | United States | 01/16/2002  | 05/20/2003 | CHARGE INJECTION                                                                                                                                                                     |
| 6,307,784             | F0273US                   | United States | 02/28/2001  | 10/23/2001 | NEGATIVE GATE ERASE                                                                                                                                                                  |
| 6,456,533             | F0274US                   | United States | 02/28/2001  | 09/24/2002 | HIGHER PROGRAM VT AND FASTER PROGRAMMING RATES BASED<br>ON IMPROVED ERASE METHODS                                                                                                    |
| 6,590,811             | F0274US DIV               | United States | 06/17/2002  | 07/08/2003 | HIGHER PROGRAM VT AND FASTER PROGRAMMING RATES BASED<br>ON IMPROVED ERASE METHODS                                                                                                    |
| 6,900,085             | F0279US                   | United States | 06/26/2001  | 05/31/2005 | ESD IMPLANT FOLLOWING SPACER DEPOSITION                                                                                                                                              |
| 6,465,303             | F0280US                   | United States | 06/20/2001  | 10/15/2002 | METHOD OF MANUFACTURING SPACER ETCH MASK FOR SILICON-<br>OXIDE-NITRIDE-OXIDE-SILICON (SONOS) TYPE NONVOLATILE<br>MEMORY                                                              |
| 6,630,384             | F0282US                   | United States | 10/05/2001  | 10/07/2003 | METHOD OF FABRICATING DOUBLE DENSED CORE GATES IN SONOS<br>FLASH MEMORY                                                                                                              |
| 6,566,194             | F0283                     | United States | 10/01/2001  | 05/20/2003 | SALICIDED GATE FOR VIRTUAL GROUND ARRAYS                                                                                                                                             |
| 6,645,801             | F0284US                   | United States | 10/01/2001  | 11/11/2003 | SALICIDED GATE FOR VIRTUAL GROUND ARRAYS                                                                                                                                             |
| 6,596,591             | F0285US                   | United States | 12/18/2000  | 07/22/2003 | METHODS TO FORM REDUCED DIMENSION BIT-LINE ISOLATION IN<br>THE MANUFACTURE OF NON-VOLATILE MEMORY DEVICES                                                                            |
| 6,770,938             | F0466US                   | United States | 01/16/2002  | 08/03/2004 | IMPROVED DIODE FABRICATION FOR ESD/EOS PROTECTION                                                                                                                                    |
| 6,524,914             | F0499US                   | United States | 10/30/2000  | 02/25/2003 | SOURCE SIDE BORON IMPLANTING AND DIFFUSING DEVICE<br>ARCHITECTURE FOR DEEP SUBSTANCE 0.18UM FLASH MEMORY                                                                             |
| 6,589,804             | F0636US                   | United States | 07/12/2001  | 07/08/2003 | OXIDE/NITRIDE OR OXIDE/NITRIDE/OXIDE THICKNESS MEASUREMENT<br>USING SCATTEROMETRY                                                                                                    |
| 6,500,768             | F0750US                   | United States | 10/30/2000  | 12/31/2002 | METHOD FOR SELECTIVE REMOVAL OF ONO LAYER                                                                                                                                            |
| 6,356,482             | F0752US                   | United States | 09/07/2000  | 03/12/2002 | USING NEGATIVE GATE ERASE VOLTAGE TO SIMULTANEOUSLY<br>ERASE TWO BITS FROM A NON-VOLATILE MEMORY CELL WITH AN<br>OXIDE-NITRIDE-OXIDE (ONO) STRUCTURE                                 |
| 6,549,466             | F0753                     | United States | 09/07/2000  | 04/15/2003 | USING A NEGATIVE GATE ERASE VOLTAGE APPLIED IN STEPS OF<br>DECREASING AMOUNTS TO REDUCE ERASE TIME FOR A NON-<br>VOLATILE MEMORY CELL WITH AN OXIDE-NITRIDE-OXIDE (ONO)<br>STRUCTURE |
| 6,693,009             | F0756US                   | United States | 11/15/2000  | 02/17/2004 | FLASH MEMORY CELL WITH MINIMIZED FLOATING GATE TO<br>DRAIN/SOURCE OVERLAP FOR MINIMIZING CHARGE LEAKAGE                                                                              |
| 6,489,253             | F0899                     | United States | 02/16/2001  | 12/03/2002 | METHOD OF FORMING A VOID-FREE INTERLAYER DIELECTRIC (ILD0)<br>FOR 0.18-UM FLASH MEMORY TECHNOLOGY AND SEMICONDUCTOR<br>DEVICE THEREBY FORMED                                         |
| 6,627,973             | F0899US DIV               | United States | 09/13/2002  | 09/30/2003 | VOID-FREE INTERLAYER DIELECTRIC (ILD0) FOR 0.18-MICRON FLASH<br>MEMORY SEMICONDUCTOR DEVICE                                                                                          |
| 6,306,707             | F0902US                   | United States | 11/20/2000  | 10/23/2001 | DOUBLE LAYER HARD MASK TO IMPROVE OXIDE QUALITY FOR NON-<br>VOLATILE FLASH MEMORY PRODUCTS                                                                                           |
| 6,400,624             | F0911US                   | United States | 02/26/2001  | 06/04/2002 | CONFIGURE REGISTERS AND LOADS TO TAILOR A MULTI-LEVEL CELL<br>FLASH DESIGN                                                                                                           |
| 6,424,566             | F0912US                   | United States | 02/08/2001  | 07/23/2002 | PROGRAM RECONNAISSANCE TO ELIMINATE VARIATIONS IN VT<br>DISTRIBUTIONS OF MULTI-LEVEL CELL FLASH MEMORY DESIGNS                                                                       |
| 6,684,353             | F0913US                   | United States | 12/07/2000  | 01/27/2004 | RELIABILITY MONITOR FOR MEMORY ARRAY                                                                                                                                                 |
| 6,785,856             | F0915US                   | United States | 12/07/2000  | 08/31/2004 | INTERNAL SELF-TEST CIRCUIT FOR A MEMORY ARRAY                                                                                                                                        |
| 6,452,869             | F0916                     | United States | 02/26/2001  | 09/17/2002 | ADDRESS BROADCASTING TO A PAGED DEVICE TO ELIMINATE<br>ACCESS LATENCY PENALTY                                                                                                        |
| 6,466,483             | F0917US                   | United States | 02/08/2001  | 10/15/2002 | PIGGYBACK PROGRAMMING USING TIMING CONTROL FOR MULTI-<br>LEVEL CELL FLASH MEMORY DEVICE                                                                                              |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                              |
|-----------------------|---------------------------|---------------|-------------|------------|------------------------------------------------------------------------------------------------------------------------------------|
| 6,418,053             | F0918US                   | United States | 02/08/2001  | 07/09/2002 | PIGGYBACK PROGRAMMING USING GRADUATED STEPS FOR MULTI-LEVEL CELL FLASH MEMORY DESIGNS                                              |
| 7,872,916             | F0919TW                   | United States | 12/09/2008  | 01/18/2011 | DETERMINISTIC-PROGRAMMING METHODOLOGY FOR FLASH MEMORY DEVICES                                                                     |
| 6,614,683             | F0920US                   | United States | 02/26/2001  | 09/02/2003 | ASCENDING STAIRCASE READ TECHNIQUE FOR A MULTILEVEL CELL NAND FLASH MEMORY DEVICE                                                  |
| 6,307,783             | F0921                     | United States | 02/26/2001  | 10/23/2001 | DESCENDING STAIRCASE READ TECHNIQUE FOR A MULTILEVEL CELL NAND FLASH MEMORY DEVICE                                                 |
| 6,671,207             | F0922US                   | United States | 02/08/2001  | 12/30/2003 | PIGGYBACK PROGRAMMING WITH STAIRCASE VERIFY FOR MULTI-LEVEL CELL MEMORY DESIGNS                                                    |
| 6,552,929             | F0923                     | United States | 02/08/2001  | 04/22/2003 | PIGGYBACK PROGRAMMING USING AN EXTENDED FIRST PULSE FOR MULTI-LEVEL CELL FLASH MEMORY DESIGNS                                      |
| 6,496,410             | F0924US                   | United States | 02/08/2001  | 12/17/2002 | CONCURRENT PROGRAM RECONNAISSANCE WITH PIGGYBACK PULSES FOR MULTI-LEVEL CELL FLASH MEMORY DESIGNS                                  |
| 6,538,923             | F0925US                   | United States | 02/26/2001  | 03/25/2003 | STAIRCASE PROGRAM VERIFY FOR MULTILEVEL CELL FLASH MEMORY DESIGNS                                                                  |
| 6,653,189             | F0932US                   | United States | 10/30/2000  | 11/25/2003 | SOURCE SIDE BORON IMPLANT AND DRAIN SIDE MDD IMPLANT FOR DEEP SUB 0.18 MICRON FLASH MEMORY                                         |
| 7,002,381             | F0958US                   | United States | 12/11/2001  | 02/21/2006 | SWITCHED-CAPACITOR CONTROLLER TO CONTROL THE RISE TIMES OF ON-CHIP GENERATED HIGH VOLTAGES                                         |
| 6,966,016             | F1024US                   | United States | 04/16/2001  | 11/15/2005 | SYSTEM AND METHOD FOR ERASE TEST OF INTEGRATED CIRCUIT DEVICE HAVING NON-HOMOGENEOUSLY SIZED SECTORS                               |
| 6,534,363             | F1053US                   | United States | 03/12/2001  | 03/18/2003 | HIGH VOLTAGE OXIDATION METHOD FOR HIGHLY RELIABLE FLASH MEMORY DEVICES                                                             |
| 6,514,822             | F1054US                   | United States | 04/27/2001  | 02/04/2003 | METHOD AND SYSTEM FOR REDUCING THINNING OF FIELD ISOLATION STRUCTURES IN A FLASH MEMORY DEVICE                                     |
| 6,438,037             | F1067US                   | United States | 05/09/2001  | 08/20/2002 | THRESHOLD VOLTAGE COMPACTING FOR NON-VOLATILE SEMICONDUCTOR MEMORY DESIGNS                                                         |
| 6,376,312             | F1097US                   | United States | 03/26/2001  | 04/23/2002 | FORMATION OF NON-VOLATILE MEMORY DEVICE COMPRISED OF AN ARRAY OF VERTICAL FIELD EFFECT TRANSISTOR STRUCTURES                       |
| 60/273,615            | F1101                     | United States | 03/05/2001  |            | PASSWORD DYNAMIC PROTECTION OF FLASH MEMORY DATA                                                                                   |
| 6,731,536             | F1101US                   | United States | 03/05/2002  | 05/04/2004 | PASSWORD AND DYNAMIC PROTECTION OF FLASH MEMORY DATA                                                                               |
| 7,453,116             | F1104US DIV               | United States | 03/07/2006  | 11/18/2008 | SEMICONDUCTOR MEMORY DEVICE AND METHOD OF FABRICATING THE SAME                                                                     |
| 6,873,022             | F1114US                   | United States | 09/19/2003  | 03/29/2005 | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME                                                                         |
| 7,202,540             | F1123US                   | United States | 02/28/2005  | 04/10/2007 | SEMICONDUCTOR MEMORY DEVICE                                                                                                        |
| 7,759,745             | F1123US CON               | United States | 01/23/2007  | 07/20/2010 | SEMICONDUCTOR MEMORY DEVICE                                                                                                        |
| 7,482,226             | F1123US DIV               | United States | 01/23/2007  | 01/27/2009 | SEMICONDUCTOR MEMORY DEVICE                                                                                                        |
| 8,542,051             | FMA13-                    | United States | 08/25/2011  | 09/24/2013 | LEVEL SHIFT CIRCUIT AND SEMICONDUCTOR DEVICE                                                                                       |
| 5,594,382             | FMA13-0001JP              | United States | 03/20/1995  | 01/14/1997 | CONSTANT VOLTAGE CIRCUIT                                                                                                           |
| 5,530,818             | FMA13-0002JP              | United States | 07/08/1993  | 06/25/1996 | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE FOR OPTIONALLY SELECTING THE CORRESPONDENCE BETWEEN A CHIP-SELECT SIGNAL AND ADDRESS SPACE |
| 5,406,232             | FMA13-0003JP              | United States | 07/28/1993  | 04/11/1995 | SEMICONDUCTOR CAPACITOR ELEMENT AND A CIRCUIT EMPLOYING THE SAME                                                                   |
| 5,650,741             | FMA13-0005JP              | United States | 03/27/1996  | 07/22/1997 | POWER LINE CONNECTION CIRCUIT AND POWER LINE SWITCH IC FOR THE SAME                                                                |
| 5,606,282             | FMA13-0008JP              | United States | 04/12/1996  | 02/25/1997 | TRANSIMPEDANCE AMPLIFIER                                                                                                           |
| 5,488,327             | FMA13-0009JP              | United States | 12/28/1994  | 01/30/1996 | SUPPLY VOLTAGE GENERATOR                                                                                                           |
| 5,617,310             | FMA13-0011KR              | United States | 03/16/1995  | 04/01/1997 | MULTIPLE OPERATION MODE MICROCONTROLLER                                                                                            |
| 5,671,186             | FMA13-0014KR              | United States | 06/01/1995  | 09/23/1997 | SEMICONDUCTOR MEMORY DEVICE HAVING BIT LINE PRECHARGER                                                                             |
| 5,528,171             | FMA13-0015KR              | United States | 09/19/1994  | 06/18/1996 | ECL-TO-CMOS SIGNAL LEVEL CONVERTER                                                                                                 |
| 5,905,361             | FMA13-0017TW              | United States | 08/31/1995  | 05/18/1999 | CHARGING-AND-DISCHARGING DEVICE, CONSTANT-VOLTAGE AND CONSTANT-CURRENT CONTROL CIRCUIT, AND ELECTRONIC DEVICE                      |
| 8,832,460             | FMA13-00191US             | United States | 10/16/2009  | 09/09/2014 | INTER-BUS COMMUNICATION INTERFACE DEVICE AND DATA SECURITY DEVICE                                                                  |
| 5,822,762             | FMA13-0022TW              | United States | 09/26/1995  | 10/13/1998 | INFORMATION PROCESSING DEVICE WITH DECISION CIRCUITS AND PARTITIONED ADDRESS AREAS                                                 |
| 5,739,667             | FMA13-0024KR              | United States | 12/26/1995  | 04/14/1998 | CONTROL SYSTEM FOR CHARGING BATTERIES AND ELECTRONIC APPARATUS USING SAME                                                          |
| 6,535,960             | FMA13-0024US              | United States | 05/08/1998  | 03/18/2003 | PARTITIONED CACHE MEMORY WITH SWITCHABLE ACCESS PATHS                                                                              |
| 7,586,371             | FMA13-00303US             | United States | 10/30/2006  | 09/08/2009 | REGULATOR CIRCUIT                                                                                                                  |
| 8,456,235             | FMA13-00303US DIV         | United States | 08/04/2009  | 06/04/2013 | REGULATOR CIRCUIT                                                                                                                  |
| 7,873,875             | FMA13-00304US             | United States | 07/26/2007  | 01/18/2011 | DEBUGGING SYSTEM, DEBUGGING CIRCUIT AND INFORMATION PROCESSING APPARATUS                                                           |
| 11/360,603            | FMA13-00305US             | United States | 02/24/2006  |            | IMAGE PROCESSOR AND IMAGE PROCESSING METHOD                                                                                        |
| 8,630,511             | FMA13-00305US CIP         | United States | 09/14/2006  | 01/14/2014 | IMAGE PROCESSING APPARATUS AND METHOD FOR IMAGE RESIZING MATCHING DATA SUPPLY SPEED                                                |
| 7,791,306             | FMA13-00306US             | United States | 08/28/2007  | 09/07/2010 | APPARATUS, METHOD, AND SYSTEM FOR CONTROLLING STEPPING MOTOR                                                                       |
| 8,311,054             | FMA13-00307US             | United States | 09/29/2006  | 11/13/2012 | TRANSMITTING/RECEIVING SYSTEM, NODE AND COMMUNICATION METHOD                                                                       |
| 8,078,887             | FMA13-00308US             | United States | 03/06/2008  | 12/13/2011 | POWER SUPPLY VOLTAGE REGULATOR CIRCUIT AND MICROCOMPUTER                                                                           |
| 7,847,607             | FMA13-00309US             | United States | 11/26/2007  | 12/07/2010 | PLL CIRCUIT                                                                                                                        |
| 8,032,794             | FMA13-00310US             | United States | 07/26/2007  | 10/04/2011 | ERROR PROCESSING METHOD AND INFORMATION PROCESSING APPARATUS                                                                       |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                                              |
|-----------------------|---------------------------|---------------|-------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8,527,254             | FMA13-00311US             | United States | 02/01/2008  | 09/03/2013 | SIMULATOR ENGINE DEVELOPMENT SYSTEM AND SIMULATOR<br>ENGINE DEVELOPMENT METHOD                                                                                                                     |
| 7,683,598             | FMA13-00312US             | United States | 10/25/2007  | 03/23/2010 | POWER SUPPLY CIRCUIT, POWER SUPPLY CONTROL CIRCUIT, AND<br>POWER SUPPLY CONTROL METHOD                                                                                                             |
| 7,876,076             | FMA13-00313US             | United States | 04/23/2007  | 01/25/2011 | CIRCUIT FOR PREVENTING THROUGH CURRENT IN DC-DC<br>CONVERTER                                                                                                                                       |
| 7,656,143             | FMA13-00314US             | United States | 07/13/2007  | 02/02/2010 | DC-DC CONVERTER                                                                                                                                                                                    |
| 7,948,219             | FMA13-00315US             | United States | 09/25/2007  | 05/24/2011 | CONTROL CIRCUIT OF SYNCHRONOUS RECTIFICATION TYPE POWER<br>SUPPLY UNIT, SYNCHRONOUS RECTIFICATION TYPE POWER SUPPLY<br>UNIT AND CONTROL METHOD THEREOF                                             |
| 8,725,485             | FMA13-00316US             | United States | 02/26/2008  | 05/13/2014 | SIMULATION METHOD AND SIMULATION APPARATUS                                                                                                                                                         |
| 7,777,474             | FMA13-00317US             | United States | 04/26/2007  | 08/17/2010 | DC-DC CONVERTER WITH OSCILLATOR AND MONITORING FUNCTION                                                                                                                                            |
| 8,079,014             | FMA13-00318US             | United States | 07/09/2007  | 12/13/2011 | SOFTWARE DEVELOPMENT APPARATUS AND METHOD                                                                                                                                                          |
| 7,944,190             | FMA13-00319US             | United States | 08/15/2007  | 05/17/2011 | CONTROL CIRCUIT OF POWER SUPPLY UNIT WHICH CONTROLS<br>OUTPUT POWER OF EXTERNAL POWER SUPPLY BASED UPON<br>CURRENT FROM THE EXTERNAL POWER SUPPLY, POWER SUPPLY<br>UNIT AND CONTROL METHOD THEREOF |
| 7,957,165             | FMA13-00320US             | United States | 02/15/2008  | 06/07/2011 | DC-DC CONVERTER WITH A PLURALITY OF SOFT-START CONTROL<br>CIRCUITS                                                                                                                                 |
| 7,952,234             | FMA13-00321US             | United States | 02/07/2008  | 05/31/2011 | POWER SUPPLY CIRCUIT, POWER SUPPLY CONTROL CIRCUIT AND<br>POWER SUPPLY CONTROL METHOD                                                                                                              |
| 8,406,364             | FMA13-00322US             | United States | 02/20/2008  | 03/26/2013 | FRACTIONAL FREQUENCY DIVIDER PLL DEVICE AND CONTROL<br>METHOD THEREOF                                                                                                                              |
| 7,696,738             | FMA13-00323US             | United States | 09/14/2007  | 04/13/2010 | METHOD AND CIRCUIT FOR CONTROLLING DC-DC CONVERTER                                                                                                                                                 |
| 8,117,524             | FMA13-00324US             | United States | 03/13/2008  | 02/14/2012 | DATA RECOVERY CIRCUIT                                                                                                                                                                              |
| 8,423,834             | FMA13-00325US             | United States | 02/25/2008  | 04/16/2013 | COMPUTER SYSTEM AND MEMORY SYSTEM                                                                                                                                                                  |
| 7,821,236             | FMA13-00327US             | United States | 11/09/2007  | 10/26/2010 | CONTROL CIRCUIT FOR DETECTING A REVERSE CURRENT IN A DC-<br>DC CONVERTER                                                                                                                           |
| 7,843,179             | FMA13-00328US             | United States | 11/09/2007  | 11/30/2010 | CONTROL CIRCUIT FOR SYNCHRONOUS RECTIFIER-TYPE DC-DC<br>CONVERTER, SYNCHRONOUS RECTIFIER-TYPE DC-DC CONVERTER<br>AND CONTROL METHOD THEREOF                                                        |
| 7,733,074             | FMA13-00329US             | United States | 11/08/2007  | 06/08/2010 | CONTROL CIRCUIT OF CURRENT MODE DC-DC CONVERTER AND<br>CONTROL METHOD OF CURRENT MODE DC-DC CONVERTER                                                                                              |
| 7,649,391             | FMA13-00330US             | United States | 03/14/2008  | 01/19/2010 | CLOCK SIGNAL TRANSMISSION CIRCUIT                                                                                                                                                                  |
| 8,760,133             | FMA13-00331PCT            | United States | 10/21/2008  | 06/24/2014 | LINEAR DROP-OUT REGULATOR CIRCUIT (as amended)                                                                                                                                                     |
| 7,532,071             | FMA13-00333US             | United States | 11/15/2007  | 05/12/2009 | OPERATIONAL AMPLIFIER CIRCUIT                                                                                                                                                                      |
| 8,605,756             | FMA13-00334JP             | United States | 04/28/2010  | 12/10/2013 | SIGNAL PROCESSOR AND COMMUNICATION DEVICE                                                                                                                                                          |
| 8,278,983             | FMA13-00334US<br>CON      | United States | 11/01/2010  | 10/02/2012 | PLL CIRCUIT                                                                                                                                                                                        |
| 8,638,140             | FMA13-00334US DIV         | United States | 07/26/2012  | 01/28/2014 | PLL CIRCUIT                                                                                                                                                                                        |
| 8,067,964             | FMA13-00335US             | United States | 03/14/2007  | 11/29/2011 | OUTPUT CIRCUIT                                                                                                                                                                                     |
| 7,801,178             | FMA13-00337US             | United States | 03/12/2008  | 09/21/2010 | IEEE 1394 TRANSMITTER, IEEE 1394 RECEIVER AND AUDIO DATA<br>CONTENT TRANSMISSION METHOD                                                                                                            |
| 8,248,046             | FMA13-00338US             | United States | 03/17/2008  | 08/21/2012 | DC-DC CONVERTER FOR PULSE FREQUENCY MODULATION CONTROL<br>AND POWER SUPPLY SYSTEM                                                                                                                  |
| 8,933,682             | FMA13-00339JP             | United States | 08/10/2010  | 01/13/2015 | BAND GAP REFERENCE CIRCUIT                                                                                                                                                                         |
| 7,714,557             | FMA13-00340US             | United States | 03/27/2008  | 05/11/2010 | DC-DC CONVERTER, POWER SUPPLY SYSTEM, AND POWER SUPPLY<br>METHOD                                                                                                                                   |
| 8,072,199             | FMA13-00341US             | United States | 03/25/2008  | 12/06/2011 | CONTROL CIRCUIT FOR STEP-DOWN DC-DC CONVERTER, STEP-<br>DOWN DC-DC CONVERTER AND CONTROL METHOD THEREOF                                                                                            |
| 8,516,441             | FMA13-00342US             | United States | 03/08/2007  | 08/20/2013 | SOFTWARE OPTIMIZATION DEVICE AND SOFTWARE OPTIMIZATION<br>METHOD                                                                                                                                   |
| 8,745,446             | FMA13-00343PCT            | United States | 03/23/2010  | 06/03/2014 | INTEGRATED CIRCUIT, DEBUGGING CIRCUIT, AND DEBUGGING<br>COMMAND CONTROL METHOD                                                                                                                     |
| 8,972,795             | FMA13-00343US             | United States | 11/27/2013  | 03/03/2015 | PROCESSOR SYSTEM OPTIMIZATION (as amended)                                                                                                                                                         |
| 7,045,990             | FMA13-00344TW             | United States | 09/22/2003  | 05/16/2006 | PORTABLE DEVICE HAVING A CHARGING CIRCUIT AND<br>SEMICONDUCTOR DEVICE FOR USE IN THE CHARGING CIRCUIT OF<br>THE SAME                                                                               |
| 12/625,041            | FMA13-00346JP             | United States | 11/24/2009  |            | INTERFACE APPARATUS AND RESYNCHRONIZATION METHOD                                                                                                                                                   |
| 7,982,431             | FMA13-00347US             | United States | 02/14/2008  | 07/19/2011 | DETECTION CIRCUIT                                                                                                                                                                                  |
| 8,618,781             | FMA13-00348JP<br>DIV2     | United States | 10/23/2009  | 12/31/2013 | OUTPUT VOLTAGE CONTROLLER, ELECTRONIC DEVICE, AND OUTPUT<br>VOLTAGE CONTROL METHOD                                                                                                                 |
| 7,894,221             | FMA13-00350US             | United States | 01/28/2008  | 02/22/2011 | DETECTION CIRCUIT                                                                                                                                                                                  |
| 8,139,895             | FMA13-00351US             | United States | 03/18/2008  | 03/20/2012 | IMAGE RECOGNITION DEVICE AND IMAGE ROTATING METHOD                                                                                                                                                 |
| 8,659,346             | FMA13-00352PCT            | United States | 07/13/2010  | 02/25/2014 | BODY-BIAS VOLTAGE CONTROLLER AND METHOD OF CONTROLLING<br>BODY-BIAS VOLTAGE                                                                                                                        |
| 8,575,898             | FMA13-00353PCT            | United States | 02/01/2010  | 11/05/2013 | CHARGING CIRCUIT, CHARGING APPARATUS, ELECTRONIC<br>EQUIPMENT AND CHARGING METHOD                                                                                                                  |
| 14/085,013            | FMA13-00353US             | United States | 11/20/2013  |            | SIGNAL PROCESSOR AND COMMUNICATION DEVICE                                                                                                                                                          |
| 8,593,126             | FMA13-00356JP             | United States | 05/15/2012  | 11/26/2013 | POWER SUPPLY DEVICE, CONTROL CIRCUIT, ELECTRONIC DEVICE<br>AND CONTROL METHOD FOR POWER SUPPLY                                                                                                     |
| 8,385,128             | FMA13-00357CN DIV         | United States | 02/03/2011  | 02/26/2013 | SEMICONDUCTOR MEMORY                                                                                                                                                                               |
| 12/791,280            | FMA13-00357TW             | United States | 06/01/2010  |            | MULTIPLEXING AUXILIARY PROCESSING ELEMENT AND<br>SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                                                  |
| 8,234,613             | FMA13-00358US             | United States | 07/02/2009  | 07/31/2012 | PROGRAM, DESIGN APPARATUS, AND DESIGN METHOD FOR<br>DYNAMIC RECONFIGURABLE CIRCUIT                                                                                                                 |
| 7,990,207             | FMA13-00359US             | United States | 05/06/2008  | 08/02/2011 | CONSTANT VOLTAGE CIRCUIT, CONSTANT VOLTAGE SUPPLY SYSTEM<br>AND CONSTANT VOLTAGE SUPPLY METHOD                                                                                                     |
| 7,956,586             | FMA13-00360JP DIV         | United States | 06/15/2007  | 06/07/2011 | STEP-UP/STEP-DOWN TYPE DC-DC CONVERTER, AND CONTROL<br>CIRCUIT AND CONTROL METHOD OF THE SAME                                                                                                      |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                               |
|-----------------------|--------------------------|---------------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7,805,650             | FMA13-00361US            | United States | 09/11/2008  | 09/28/2010 | SEMICONDUCTOR INTEGRATED CIRCUIT AND DEBUG MODE DETERMINATION METHOD                                                                                                                |
| 8,352,533             | FMA13-00364US            | United States | 12/11/2008  | 01/08/2013 | SEMICONDUCTOR INTEGRATED CIRCUIT IN A CARRY COMPUTATION NETWORK HAVING A LOGIC BLOCKS WHICH ARE DYNAMICALLY RECONFIGURABLE                                                          |
| 8,422,404             | FMA13-00365US            | United States | 03/27/2009  | 04/16/2013 | METHOD AND DEVICE FOR TRANSMITTING PACKETS                                                                                                                                          |
| 8,237,417             | FMA13-00366US            | United States | 11/19/2008  | 08/07/2012 | DC-DC CONVERTER, DC-DC CONVERTER CONTROL METHOD, AND ELECTRONIC DEVICE                                                                                                              |
| 8,621,643             | FMA13-00368JP            | United States | 12/11/2011  | 12/31/2013 | SEMICONDUCTOR DEVICE                                                                                                                                                                |
| 14/149,628            | FMA13-00369JP DIV        | United States | 01/07/2014  |            | MULTI-LAYER INTER-GATE DIELECTRIC STRUCTURE                                                                                                                                         |
| 8,504,862             | FMA13-00369US            | United States | 07/31/2008  | 08/06/2013 | DEVICE AND METHOD FOR PREVENTING LOST SYNCHRONIZATION                                                                                                                               |
| 8,775,853             | FMA13-00369US CIP        | United States | 04/16/2013  | 07/08/2014 | DEVICE AND METHOD FOR PREVENTING LOST SYNCHRONIZATION                                                                                                                               |
| 8,850,257             | FMA13-00369US CON        | United States | 06/26/2013  | 09/30/2014 | DEVICE AND METHOD FOR PREVENTING LOST SYNCHRONIZATION                                                                                                                               |
| 6,118,316             | FMA13-0036JP             | United States | 11/15/1996  | 09/12/2000 | SEMICONDUCTOR INTEGRATED CIRCUIT INCLUDING PLURALITY OF PHASE-LOCKED LOOPS                                                                                                          |
| 8,283,934             | FMA13-00370US            | United States | 03/10/2009  | 10/09/2012 | CAPACITANCE SENSOR FOR DETECTING A CHARGE VOLTAGE OF A MULTI-CAPACITOR CIRCUIT                                                                                                      |
| 8,299,765             | FMA13-00371US            | United States | 02/12/2009  | 10/30/2012 | POWER SUPPLY CONTROL DEVICE AND POWER SUPPLY CONTROL METHOD                                                                                                                         |
| 8,107,487             | FMA13-00372US            | United States | 05/01/2009  | 01/31/2012 | PACKET COMMUNICATION DEVICE FOR COMMUNICATING PACKET TO BE TRANSFERRED THROUGH PACKET COMMUNICATION WHICH IS TIME-MANAGED IN CONSTANT CYCLE AND PACKET COMMUNICATION METHOD THEREOF |
| 8,824,469             | FMA13-00372US DIV        | United States | 12/07/2011  | 09/02/2014 | PACKET COMMUNICATION DEVICE FOR COMMUNICATING PACKET TO BE TRANSFERRED THROUGH PACKET COMMUNICATION WHICH IS TIME-MANAGED IN CONSTANT CYCLE AND PACKET COMMUNICATION METHOD THEREOF |
| 8,233,257             | FMA13-00373US            | United States | 02/12/2009  | 07/31/2012 | POWER SUPPLY CIRCUIT, OVERCURRENT PROTECTION CIRCUIT FOR THE SAME, AND ELECTRONIC DEVICE                                                                                            |
| 7,990,134             | FMA13-00374US            | United States | 03/06/2009  | 08/02/2011 | CORRECTING CIRCUIT, CORRECTING METHOD, AND SENSOR APPARATUS                                                                                                                         |
| 12/428,212            | FMA13-00375US            | United States | 04/22/2009  |            | LINE PLOTTING METHOD                                                                                                                                                                |
| 7,403,582             | FMA13-00379JP DIV2       | United States | 07/27/2004  | 07/22/2008 | SERIAL COMMUNICATION DEVICE                                                                                                                                                         |
| 6,765,420             | FMA13-00380TW            | United States | 12/24/2002  | 07/20/2004 | PULSE WIDTH DETECTION CIRCUIT FILTERING THE INPUT SIGNAL AND GENERATING A BINARY SIGNAL                                                                                             |
| 7,012,454             | FMA13-00381TW            | United States | 03/10/2004  | 03/14/2006 | CLOCK SHIFT CIRCUIT FOR GRADUAL FREQUENCY CHANGE                                                                                                                                    |
| 7,336,124             | FMA13-00381US            | United States | 06/08/2006  | 02/26/2008 | OPERATIONAL AMPLIFIER, LINE DRIVER, AND LIQUID CRYSTAL DISPLAY DEVICE                                                                                                               |
| 7,880,537             | FMA13-00381US DIV        | United States | 12/19/2007  | 02/01/2011 | OPERATIONAL AMPLIFIER, LINE DRIVER, AND LIQUID CRYSTAL DISPLAY DEVICE                                                                                                               |
| 6,516,378             | FMA13-00382TW            | United States | 10/26/1999  | 02/04/2003 | MICROPROCESSOR FOR CONTROLLING BUSES                                                                                                                                                |
| 5,990,742             | FMA13-00383US            | United States | 05/13/1998  | 11/23/1999 | DIFFERENTIAL AMPLIFIER CIRCUIT                                                                                                                                                      |
| 8,595,562             | FMA13-00389JP            | United States | 01/26/2011  | 11/26/2013 | SEMICONDUCTOR INTEGRATED CIRCUIT, OPERATING METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT, AND DEBUG SYSTEM                                                                            |
| 14/137,203            | FMA13-00389US            | United States | 12/20/2013  |            | DC-DC CONVERTER WITH ADAPTIVE PHASE COMPENSATION CONTROLLER                                                                                                                         |
| 5,883,527             | FMA13-0038KR             | United States | 01/28/1997  | 03/16/1999 | TRI-STATE OUTPUT CIRCUIT FOR SEMICONDUCTOR DEVICE                                                                                                                                   |
| 8,063,667             | FMA13-00392US            | United States | 06/12/2009  | 11/22/2011 | PEAK HOLD CIRCUIT                                                                                                                                                                   |
| 8,285,902             | FMA13-00394US            | United States | 12/10/2009  | 10/09/2012 | DATA TRANSFER APPARATUS AND DATA TRANSFER METHOD                                                                                                                                    |
| 8,190,928             | FMA13-00397US            | United States | 02/25/2009  | 05/29/2012 | POWER-ON DETECTION CIRCUIT AND MICROCONTROLLER                                                                                                                                      |
| 8,248,043             | FMA13-00398US            | United States | 11/12/2009  | 08/21/2012 | CONTROL CIRCUIT FOR DC-DC CONVERTER, CONTROL METHOD FOR DC-DC CONVERTER, AND ELECTRONIC DEVICE                                                                                      |
| 8,680,832             | FMA13-00402US            | United States | 11/27/2012  | 03/25/2014 | CONTROL CIRCUIT OF STEP-DOWN DC-DC CONVERTER, CONTROL CIRCUIT OF STEP-UP DC-DC CONVERTER AND STEP-UP/STEP-DOWN DC-DC CONVERTER                                                      |
| 14/220,628            | FMA13-00402US DIV        | United States | 03/20/2014  |            | CONTROL CIRCUIT OF STEP-DOWN DC-DC CONVERTER, CONTROL CIRCUIT OF STEP-UP DC-DC CONVERTER AND STEP-UP/STEP-DOWN DC-DC CONVERTER                                                      |
| 8,578,216             | FMA13-00403JP            | United States | 03/11/2010  | 11/05/2013 | EXECUTION HISTORY TRACING METHOD                                                                                                                                                    |
| 8,291,360             | FMA13-00405US            | United States | 07/15/2009  | 10/16/2012 | DATA CONVERSION APPARATUS, METHOD, AND COMPUTER-READABLE RECORDING MEDIUM STORING PROGRAM FOR GENERATING CIRCUIT CONFIGURATION INFORMATION FROM CIRCUIT DESCRIPTION                 |
| 7,889,568             | FMA13-00406US            | United States | 07/14/2009  | 02/15/2011 | MEMORY, MEMORY OPERATING METHOD, AND MEMORY SYSTEM                                                                                                                                  |
| 8,522,081             | FMA13-00408US            | United States | 11/13/2008  | 08/27/2013 | MICROCOMPUTER OUTPUTTING FAILURE DETECTION RESULT                                                                                                                                   |
| 8,462,167             | FMA13-00409US            | United States | 10/29/2009  | 06/11/2013 | MEMORY ACCESS CONTROL CIRCUIT AND IMAGE PROCESSING SYSTEM                                                                                                                           |
| 5,850,137             | FMA13-0040JP DIV         | United States | 12/02/1996  | 12/15/1998 | CHARGING APPARATUS AND CURRENT/VOLTAGE DETECTOR FOR USE THEREIN                                                                                                                     |
| 7,965,476             | FMA13-00411US            | United States | 12/11/2009  | 06/21/2011 | CURRENT PRODUCING CIRCUIT, CURRENT PRODUCING METHOD, AND ELECTRONIC DEVICE                                                                                                          |
| 7,952,509             | FMA13-00414US            | United States | 11/17/2009  | 05/31/2011 | SUCCESSIVE APPROXIMATION A/D CONVERTER                                                                                                                                              |
| 12/354,413            | FMA13-00416US            | United States | 01/15/2009  |            | POWER SUPPLY APPARATUS AND POWER SUPPLY METHOD                                                                                                                                      |
| 8,324,873             | FMA13-00416US CIP        | United States | 12/13/2009  | 12/04/2012 | POWER SUPPLY APPARATUS AND POWER SUPPLY METHOD                                                                                                                                      |
| 13/746,477            | FMA13-00417US            | United States | 01/22/2013  |            | ANALOG CIRCUIT CELL ARRAY HAVING A PLURALITY OF TRANSISTORS EACH INCLUDING TWO CONNECTED GATE ELECTRODES AND TWO CONNECTED SOURCE REGIONS (as amended)                              |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                   |
|-----------------------|--------------------------|---------------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7,948,304             | FMA13-00419US            | United States | 11/16/2009  | 05/24/2011 | CONSTANT-VOLTAGE GENERATING CIRCUIT AND REGULATOR CIRCUIT                                                                                                               |
| 5,793,257             | FMA13-0041JP             | United States | 01/06/1997  | 08/11/1998 | OSCILLATOR HAVING SWITCHING CAPACITORS AND PHASE-LOCKED LOOP EMPLOYING SAME                                                                                             |
| 8,593,447             | FMA13-00420JP            | United States | 06/04/2010  | 11/26/2013 | VOLTAGE ADJUSTMENT CIRCUIT AND DISPLAY DEVICE DRIVING CIRCUIT                                                                                                           |
| 14/068,652            | FMA13-00420US            | United States | 10/31/2013  |            | EXECUTION HISTORY TRACING METHOD                                                                                                                                        |
| 14/218,169            | FMA13-00421US            | United States | 03/18/2014  |            | DEBUG CONTROL CIRCUIT                                                                                                                                                   |
| 8,570,021             | FMA13-00422JP            | United States | 06/14/2010  | 10/29/2013 | DC/DC CONVERTER AND DC/DC CONVERTER CONTROL METHOD                                                                                                                      |
| 12/795,462            | FMA13-00423JP            | United States | 06/07/2010  |            | COMPUTER SYSTEM INCLUDING RECONFIGURABLE ARITHMETIC DEVICE WITH NETWORK OF PROCESSOR ELEMENTS (as amended)                                                              |
| 8,107,299             | FMA13-00424US            | United States | 11/17/2009  | 01/31/2012 | SEMICONDUCTOR MEMORY AND METHOD AND SYSTEM FOR ACTUATING SEMICONDUCTOR MEMORY                                                                                           |
| 13/022,992            | FMA13-00425JP            | United States | 02/08/2011  |            | RECEIVING APPARATUS AND METHOD FOR SETTING GAIN                                                                                                                         |
| 7,961,055             | FMA13-00426US            | United States | 11/12/2009  | 06/14/2011 | PLL CIRCUIT AND OSCILLATOR DEVICE                                                                                                                                       |
| 5,818,303             | FMA13-0042TW             | United States | 07/24/1997  | 10/06/1998 | FRACTIONAL N-FREQUENCY SYNTHESIZER AND SPURIOUS SIGNAL CANCEL CIRCUIT                                                                                                   |
| 8,718,571             | FMA13-00433JP            | United States | 06/04/2010  | 05/06/2014 | OUTPUT CIRCUIT OF HIGH-FREQUENCY TRANSMITTER                                                                                                                            |
| 14/089,048            | FMA13-00433US            | United States | 11/25/2013  |            | VOLTAGE ADJUSTMENT CIRCUIT AND DISPLAY DEVICE DRIVING CIRCUIT                                                                                                           |
| 8,587,265             | FMA13-00434JP            | United States | 03/04/2010  | 11/19/2013 | CONTROL CIRCUIT FOR DC-DC CONVERTER, DC-DC CONVERTER, AND METHOD FOR CONTROLLING DC-DC CONVERTER                                                                        |
| 7,625,118             | FMA13-00435JP            | United States | 09/25/2007  | 12/01/2009 | CIRCUIT FOR CORRECTING SENSOR TEMPERATURE CHARACTERISTICS                                                                                                               |
| 8,572,592             | FMA13-00436JP            | United States | 02/09/2006  | 10/29/2013 | EXTENDED LANGUAGE SPECIFICATION ASSIGNING METHOD, PROGRAM DEVELOPING METHOD AND COMPUTER-READABLE STORAGE MEDIUM                                                        |
| 8,035,367             | FMA13-00439US            | United States | 03/27/2009  | 10/11/2011 | ELECTRONIC DEVICE, DETECTION CIRCUIT AND VOLTAGE CONTROL METHOD                                                                                                         |
| 5,870,000             | FMA13-0043TW             | United States | 02/24/1997  | 02/09/1999 | OSCILLATION CIRCUIT AND PLL CIRCUIT USING SAME                                                                                                                          |
| 12/606,870            | FMA13-00440JP            | United States | 10/27/2009  |            | COMMUNICATION APPARATUS, DATA COMMUNICATION METHOD, AND NETWORK SYSTEM                                                                                                  |
| 8,841,874             | FMA13-00442JP            | United States | 07/22/2011  | 09/23/2014 | METHOD OF DETECTING AN OPERATING CONDITION OF AN ELECTRIC STEPPER MOTOR                                                                                                 |
| 7,098,147             | FMA13-00444JP            | United States | 08/20/2003  | 08/29/2006 | SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE                                                                                           |
| 8,314,599             | FMA13-00445US            | United States | 06/05/2009  | 11/20/2012 | DC/DC CONVERTER CONTROL CIRCUIT AND DC/DC CONVERTER CONTROL METHOD                                                                                                      |
| 8,922,181             | FMA13-00446JP            | United States | 06/21/2010  | 12/30/2014 | POWER CONTROL CIRCUIT PERFORMING SOFT START OPERATION, POWER SUPPLY DEVICE, AND ELECTRONIC DEVICE                                                                       |
| 6,366,767             | FMA13-00448JP DIV        | United States | 05/11/1999  | 04/02/2002 | LOCAL OSCILLATION CIRCUIT AND A RECEIVING CIRCUIT INCLUDING THE LOCAL OSCILLATION CIRCUIT                                                                               |
| 6,922,794             | FMA13-00449TW            | United States | 09/24/2001  | 07/26/2005 | MICROCOMPUTER WITH DEBUG SUPPORTING FUNCTION                                                                                                                            |
| 6,163,170             | FMA13-0044JP             | United States | 05/16/1997  | 12/19/2000 | LEVEL CONVERTER AND SEMICONDUCTOR DEVICE                                                                                                                                |
| 7,253,691             | FMA13-00450TW            | United States | 08/28/2003  | 08/07/2007 | PLL CLOCK GENERATOR CIRCUIT AND CLOCK GENERATION METHOD                                                                                                                 |
| 11/198,225            | FMA13-00450US            | United States | 08/08/2005  |            | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, AND ADJUSTMENT METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                                                               |
| 7,459,960             | FMA13-00450US DIV        | United States | 06/01/2006  | 12/02/2008 | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, AND ADJUSTMENT METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                                                               |
| 12/723,320            | FMA13-00452JP            | United States | 03/12/2010  |            | RECONFIGURABLE CIRCUIT WITH SUSPENSION CONTROL CIRCUIT                                                                                                                  |
| 8,149,026             | FMA13-00455US            | United States | 06/29/2010  | 04/03/2012 | DRIVER CIRCUIT AND ADJUSTMENT METHOD THEREOF                                                                                                                            |
| 7,936,156             | FMA13-00457JP            | United States | 06/10/2008  | 05/03/2011 | DC-DC CONVERTER AND CONTROL METHOD THEREOF                                                                                                                              |
| 7,916,503             | FMA13-00458JP            | United States | 03/26/2008  | 03/29/2011 | DC-DC CONVERTER, POWER SUPPLY VOLTAGE SUPPLYING METHOD, AND POWER SUPPLY VOLTAGE SUPPLYING SYSTEM                                                                       |
| 8,319,482             | FMA13-00459US            | United States | 03/02/2010  | 11/27/2012 | POWER SUPPLY AND POWER CONTROL DEVICE                                                                                                                                   |
| 6,462,609             | FMA13-00460JP            | United States | 03/26/2001  | 10/08/2002 | TRIMMING CIRCUIT OF SEMICONDUCTOR APPARATUS                                                                                                                             |
| 8,345,503             | FMA13-00461JP            | United States | 09/28/2010  | 01/01/2013 | BOOSTER CIRCUIT AND SEMICONDUCTOR MEMORY                                                                                                                                |
| 8,436,687             | FMA13-00463US            | United States | 12/21/2010  | 05/07/2013 | OSCILLATING APPARATUS                                                                                                                                                   |
| 13/028,840            | FMA13-00464JP            | United States | 02/16/2011  |            | SEMICONDUCTOR CIRCUIT AND DESIGNING APPARATUS                                                                                                                           |
| 8,335,110             | FMA13-00466US            | United States | 08/04/2010  | 12/18/2012 | SEMICONDUCTOR MEMORY, SYSTEM, AND METHOD OF CONTROLLING SEMICONDUCTOR MEMORY                                                                                            |
| 12/844,928            | FMA13-00470US            | United States | 07/28/2010  |            | DC-DC CONVERTER, CONTROL CIRCUIT, AND POWER SUPPLY CONTROL METHOD                                                                                                       |
| 8,344,711             | FMA13-00471JP DIV        | United States | 04/19/2010  | 01/01/2013 | POWER SUPPLY DEVICE, CONTROL CIRCUIT AND METHOD FOR CONTROLLING POWER SUPPLY DEVICE                                                                                     |
| 14/107,729            | FMA13-00471US            | United States | 12/16/2013  |            | OUTPUT VOLTAGE CONTROLLER, ELECTRONIC DEVICE, AND OUTPUT VOLTAGE CONTROL METHOD                                                                                         |
| 8,699,549             | FMA13-00472PCT           | United States | 12/02/2011  | 04/15/2014 | COMMUNICATION DEVICE, COMMUNICATION SYSTEM, AND COMMUNICATION METHOD                                                                                                    |
| 8,368,577             | FMA13-00474US            | United States | 02/28/2011  | 02/05/2013 | A/D CONVERTER                                                                                                                                                           |
| 12/617,608            | FMA13-00475JP DIV        | United States | 11/12/2009  |            | AN ANALOG CIRCUIT CELL ARRAY INCLUDING PLURALITY OF TWO CHANNEL MOSFETS HAVING TWO GATE ELECTRODES CONNECTED TOGETHER AND TWO SOURCE REGIONS CONNECTED TOGETHER FOR USE |
| 8,514,632             | FMA13-00476US            | United States | 02/07/2011  | 08/20/2013 | SEMICONDUCTOR MEMORY INCLUDING PROGRAM CIRCUIT OF NONVOLATILE MEMORY CELLS AND SYSTEM                                                                                   |
| 8,742,730             | FMA13-00477JP            | United States | 02/18/2010  | 06/03/2014 | CHARGING CIRCUIT                                                                                                                                                        |
| 7,554,784             | FMA13-00478JP DIV        | United States | 06/09/2006  | 06/30/2009 | SURGE DETECTION CIRCUIT                                                                                                                                                 |
| 8,928,177             | FMA13-00479US            | United States | 02/25/2011  | 01/06/2015 | CONTROL CIRCUIT AND ELECTRONIC DEVICE                                                                                                                                   |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                      |
|-----------------------|---------------------------|---------------|-------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12/973,730            | FMA13-00480JP             | United States | 12/20/2010  |            | RECONFIGURABLE CIRCUIT HAVING ROWS OF A MATRIX OF REGISTERS CONNECTED TO CORRESPONDING PORTS AND A SEMICONDUCTOR INTEGRATED CIRCUIT (as amended)                           |
| 7,663,345             | FMA13-00481JP             | United States | 08/30/2006  | 02/16/2010 | CIRCUIT AND METHOD FOR CONTROLLING DC-DC CONVERTER                                                                                                                         |
| 8,612,805             | FMA13-00482JP             | United States | 03/20/2007  | 12/17/2013 | PROCESSOR SYSTEM OPTIMIZATION SUPPORTING APPARATUS AND SUPPORTING METHOD                                                                                                   |
| 8,988,052             | FMA13-00483JP             | United States | 04/15/2011  | 03/24/2015 | CONTROL CIRCUIT FOR POWER SUPPLY INCLUDING A DETECTION CIRCUIT AND A REGULATION CIRCUIT FOR REGULATING SWITCHING TIMING (as amended)                                       |
| 8,618,783             | FMA13-00484JP             | United States | 11/12/2009  | 12/31/2013 | DC-DC CONVERTER WITH ADAPTIVE PHASE COMPENSATION CONTROLLER                                                                                                                |
| 7,663,356             | FMA13-00486JP             | United States | 06/07/2006  | 02/16/2010 | CURRENT-CONTROLLED DC-DC CONVERTER CONTROL CIRCUIT, CURRENT-CONTROLLED DC-DC CONVERTER, AND METHOD FOR CONTROLLING CURRENT-CONTROLLED DC-DC CONVERTER                      |
| 6,114,890             | FMA13-0048KR              | United States | 11/10/1997  | 09/05/2000 | SKEW-REDUCTION CIRCUIT                                                                                                                                                     |
| 13/073,691            | FMA13-00490US             | United States | 03/28/2011  |            | RECONFIGURABLE CIRCUIT WITH DATA LATENCY MANAGEMENT (as amended)                                                                                                           |
| 8,635,397             | FMA13-00493JP             | United States | 03/23/2011  | 01/21/2014 | DATA WRITING METHOD AND SYSTEM                                                                                                                                             |
| 8,410,767             | FMA13-00494JP             | United States | 06/01/2009  | 04/02/2013 | CONTROL CIRCUIT OF DC-DC CONVERTER APPLYING OFFSET TO COIL CURRENT, DC-DC CONVERTER APPLYING OFFSET TO COIL CURRENT AND CONTROL METHOD OF DC-DC CONVERTER                  |
| 14/080,844            | FMA13-00494US             | United States | 11/15/2013  |            | SEMICONDUCTOR INTEGRATED CIRCUIT, OPERATING METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT, AND DEBUG SYSTEM                                                                   |
| 7,071,675             | FMA13-00497JP DIV1        | United States | 03/05/2004  | 07/04/2006 | BAND DISTRIBUTION INSPECTING DEVICE AND BAND DISTRIBUTION INSPECTING METHOD                                                                                                |
| 7,793,085             | FMA13-00498JP DIV         | United States | 12/30/2004  | 09/07/2010 | MEMORY CONTROL CIRCUIT AND MICROPROCESSORY SYSTEM FOR PRE-FETCHING INSTRUCTIONS                                                                                            |
| 7,250,773             | FMA13-00498US             | United States | 09/14/2006  | 07/31/2007 | CIRCUIT FOR DETECTING DIFFERENCE IN CAPACITANCE                                                                                                                            |
| 7,372,740             | FMA13-00499JP DIV         | United States | 05/11/2005  | 05/13/2008 | SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                |
| 8,878,504             | FMA13-00501JP             | United States | 07/20/2011  | 11/04/2014 | SWITCHING REGULATOR                                                                                                                                                        |
| 8,493,050             | FMA13-00502JP             | United States | 11/26/2010  | 07/23/2013 | CONTROL CIRCUIT FOR SWITCHING POWER SUPPLY UNIT, ELECTRONIC DEVICE AND METHOD FOR CONTROLLING SWITCHING POWER SUPPLY UNIT                                                  |
| 14/149,484            | FMA13-00502US             | United States | 01/07/2014  |            | DATA WRITING METHOD AND SYSTEM                                                                                                                                             |
| 8,638,082             | FMA13-00503JP DIV2        | United States | 01/18/2011  | 01/28/2014 | CONTROL CIRCUIT FOR STEP-DOWN AND BOOST TYPE SWITCHING SUPPLY CIRCUIT AND METHOD FOR SWITCHING SUPPLY CIRCUIT                                                              |
| 13/749,246            | FMA13-00503US             | United States | 03/14/2011  | 12/17/2014 | SEMICONDUCTOR MEMORY READ AND WRITE ACCESS                                                                                                                                 |
| 8,718,038             | FMA13-00505JP             | United States | 08/26/2011  | 05/06/2014 | NODE SYSTEM AND SUPERVISORY NODE                                                                                                                                           |
| 8,611,160             | FMA13-00508JP             | United States | 06/10/2011  | 12/17/2013 | NONVOLATILE SEMICONDUCTOR STORAGE DEVICE AND DATA WRITE METHOD FOR THE SAME                                                                                                |
| 8,897,289             | FMA13-00508US             | United States | 03/20/2014  | 11/25/2014 | NODE SYSTEM AND SUPERVISORY NODE                                                                                                                                           |
| 6,897,635             | FMA13-00511JP             | United States | 04/14/2003  | 05/24/2005 | METHOD FOR PREDICTING REMAINING CHARGE OF PORTABLE ELECTRONICS BATTERY                                                                                                     |
| 8,922,289             | FMA13-00511US             | United States | 07/09/2013  | 12/30/2014 | OSCILLATION CIRCUIT                                                                                                                                                        |
| 8,339,206             | FMA13-00512US             | United States | 12/02/2011  | 12/25/2012 | PLL                                                                                                                                                                        |
| 5,304,954             | FMA13-00513JP             | United States | 07/12/1993  | 04/19/1994 | PLL SYNTHESIZER HAVING FREQUENCY DIVIDERS WITH RESET CONTROL                                                                                                               |
| 8,957,648             | FMA13-00514US             | United States | 05/27/2011  | 02/17/2015 | OUTPUT SWITCHING CIRCUIT                                                                                                                                                   |
| 14/598,647            | FMA13-00514US CON         | United States | 01/16/2015  |            | OUTPUT SWITCHING CIRCUIT                                                                                                                                                   |
| 8,605,733             | FMA13-00515JP             | United States | 12/22/2010  | 12/10/2013 | METHOD OF DATA TRANSMISSION, DATA TRANSMITTING APPARATUS, AND NETWORK SYSTEM                                                                                               |
| 8,698,473             | FMA13-00516JP             | United States | 06/30/2011  | 04/15/2014 | SWITCHING REGULATOR                                                                                                                                                        |
| 8,786,358             | FMA13-00517JP             | United States | 02/28/2011  | 07/22/2014 | REFERENCE VOLTAGE CIRCUIT AND SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                                             |
| 8,830,097             | FMA13-00518JP             | United States | 07/25/2012  | 09/09/2014 | A/D CONVERTER                                                                                                                                                              |
| 5,917,366             | FMA13-0051KR              | United States | 07/24/1997  | 06/29/1999 | VOLTAGE BOOSTER CIRCUIT AND A VOLTAGE DROP CIRCUIT WITH CHANGEABLE OPERATING LEVELS                                                                                        |
| 10/790,176            | FMA13-00520JP             | United States | 03/02/2004  |            | INTER-BUS COMMUNICATION INTERFACE DEVICE AND DATA SECURITY DEVICE                                                                                                          |
| 8,508,146             | FMA13-00521US             | United States | 11/28/2011  | 08/13/2013 | ELECTRONIC DEVICE, CONTROL CIRCUIT, AND METHOD FOR CONTROLLING LIGHT EMITTING ELEMENT                                                                                      |
| 8,819,401             | FMA13-00522US             | United States | 08/19/2011  | 08/26/2014 | SEMICONDUCTOR DEVICE AND RESET CONTROL METHOD IN SEMICONDUCTOR DEVICE                                                                                                      |
| 12/569,193            | FMA13-00523JP             | United States | 09/29/2009  |            | DISPLAY CONTROL DEVICE TO DISPLAY IMAGE DATA                                                                                                                               |
| 8,513,938             | FMA13-00524US             | United States | 12/11/2011  | 08/20/2013 | REFERENCE VOLTAGE CIRCUIT AND SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                                             |
| 8,674,632             | FMA13-00525US             | United States | 02/13/2012  | 03/18/2014 | MOTOR CONTROL DEVICE, CONTROL PROGRAM THEREFOR, AND METHOD FOR THE CONTROL                                                                                                 |
| 8,823,344             | FMA13-00526US             | United States | 12/16/2011  | 09/02/2014 | CONTROL CIRCUIT, ELECTRONIC DEVICE, AND METHOD FOR CONTROLLING POWER SUPPLY                                                                                                |
| 8,914,554             | FMA13-00528JP             | United States | 10/24/2011  | 12/16/2014 | COMMUNICATION NETWORK DEVICE THAT COMPARES FIRST AND SECOND IDENTIFICATION NUMBER OF PACKET TO DETERMINE IF THEY ARE IN CONFORMANCE OR NON-CONFORMANCE WITH SELF-ID PACKET |
| 14/069,979            | FMA13-00528US             | United States | 11/01/2013  |            | POWER SUPPLY DEVICE, CONTROL CIRCUIT, ELECTRONIC DEVICE AND CONTROL METHOD FOR POWER SUPPLY                                                                                |
| 8,436,598             | FMA13-00529JP             | United States | 09/28/2009  | 05/07/2013 | OUTPUT-VOLTAGE CONTROL DEVICE, OUTPUT-VOLTAGE CONTROL METHOD, AND ELECTRONIC APPARATUS                                                                                     |
| 8,379,464             | FMA13-00531JP             | United States | 02/10/2011  | 02/19/2013 | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                                                                                                                                    |
| 13/589,354            | FMA13-00532US             | United States | 08/20/2012  |            | CLOCK DATA RECOVERY CIRCUIT AND CLOCK DATA RECOVERY METHOD                                                                                                                 |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                         |
|-----------------------|--------------------------|---------------|-------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| 7,705,483             | FMA13-00533TW            | United States | 09/25/2006  | 04/27/2010 | DC-DC CONVERTER CONTROL CIRCUIT, DC-DC CONVERTER, POWER SUPPLY UNIT, AND DC-DC CONVERTER CONTROL METHOD                                       |
| 6,346,795             | FMA13-00535JP            | United States | 01/26/2001  | 02/12/2002 | DISCHARGE CONTROL CIRCUIT OF BATTERIES                                                                                                        |
| 6,480,069             | FMA13-00536TW            | United States | 03/02/2001  | 11/12/2002 | ACTIVE LOAD CIRCUIT, AND OPERATIONAL AMPLIFIER AND COMPARATOR HAVING THE SAME                                                                 |
| 6,864,869             | FMA13-00537JP            | United States | 12/11/2000  | 03/08/2005 | DATA DRIVER AND DISPLAY UTILIZING THE SAME                                                                                                    |
| 6,690,236             | FMA13-00537US            | United States | 09/10/2002  | 02/10/2004 | GAIN VARIABLE AMPLIFIER                                                                                                                       |
| 6,864,729             | FMA13-00538JP            | United States | 03/01/2002  | 03/08/2005 | MODE SWITCHING METHOD FOR PLL CIRCUIT AND MODE CONTROL CIRCUIT FOR PLL CIRCUIT                                                                |
| 6,731,099             | FMA13-00539TW            | United States | 02/27/2002  | 05/04/2004 | DC-DC CONVERTER WITH CONTROL CIRCUIT CAPABLE OF GENERATING STEP-UP AND STEP-DOWN SIGNALS                                                      |
| 6,795,516             | FMA13-00540JP            | United States | 03/10/2000  | 09/21/2004 | RESET CIRCUIT AND PLL FREQUENCY SYNTHESIZER                                                                                                   |
| 6,611,132             | FMA13-00541TW            | United States | 03/05/2002  | 08/26/2003 | DC-DC CONVERTER, POWER SUPPLY CIRCUIT, METHOD FOR CONTROLLING DC-DC CONVERTER, AND METHOD FOR CONTROLLING POWER SUPPLY CIRCUIT                |
| 7,342,454             | FMA13-00542KR            | United States | 04/11/2006  | 03/11/2008 | ANALOG MULTISTAGE AMPLIFICATION CIRCUIT IN THE FIELD OF SENSOR                                                                                |
| 6,847,346             | FMA13-00543US            | United States | 10/24/2002  | 01/25/2005 | SEMICONDUCTOR DEVICE EQUIPPED WITH TRANSFER CIRCUIT FOR CASCADE CONNECTION                                                                    |
| 7,019,501             | FMA13-00544US            | United States | 03/23/2004  | 03/28/2006 | DC/DC CONVERTER                                                                                                                               |
| 6,944,794             | FMA13-00545JP            | United States | 01/29/2002  | 09/13/2005 | MICROCONTROLLER WITH DEBUG SUPPORT UNIT                                                                                                       |
| 6,885,221             | FMA13-00545US            | United States | 07/23/2004  | 04/26/2005 | SIGNAL DETECTION APPARATUS, SIGNAL DETECTION METHOD, SIGNAL TRANSMISSION SYSTEM, AND COMPUTER READABLE PROGRAM TO EXECUTE SIGNAL TRANSMISSION |
| 6,975,148             | FMA13-00547TW            | United States | 12/23/2003  | 12/13/2005 | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT, JITTER GENERATION CIRCUIT AND SEMICONDUCTOR DEVICE                                                  |
| 7,092,226             | FMA13-00548TW            | United States | 03/11/2005  | 08/15/2006 | CONSTANT-VOLTAGE POWER SUPPLY CIRCUIT                                                                                                         |
| 7,671,872             | FMA13-00549TW            | United States | 04/11/2006  | 03/02/2010 | METHOD AND APPARATUS FOR DETERMINING CHROMINANCE SPACE                                                                                        |
| 7,310,026             | FMA13-00550US            | United States | 11/14/2005  | 12/18/2007 | SEMICONDUCTOR INTEGRATED CIRCUIT WITH FUNCTION TO DETECT STATE OF STABLE OSCILLATION                                                          |
| 7,180,512             | FMA13-00551TW            | United States | 01/03/2003  | 02/20/2007 | INTEGRATED CIRCUIT FREE FROM ACCUMULATION OF DUTY RATIO ERRORS                                                                                |
| 7,295,039             | FMA13-00552JP            | United States | 03/04/2005  | 11/13/2007 | BUFFER CIRCUIT                                                                                                                                |
| 7,199,745             | FMA13-00553JP            | United States | 11/15/2005  | 04/03/2007 | SUCCESSIVE APPROXIMATION A/D CONVERTER PROVIDED WITH A SAMPLE-HOLD AMPLIFIER                                                                  |
| 7,336,107             | FMA13-00554TW            | United States | 04/06/2006  | 02/26/2008 | COMPARATOR CIRCUIT AND CONTROL METHOD THEREOF                                                                                                 |
| 7,525,364             | FMA13-00555JP            | United States | 07/27/2006  | 04/28/2009 | DELAY CONTROL CIRCUIT                                                                                                                         |
| 7,719,136             | FMA13-00556TW            | United States | 06/05/2006  | 05/18/2010 | POWER SOURCE CONTROL CIRCUIT, POWER SUPPLY DEVICE, AND CONTROL METHOD FOR THE SAME                                                            |
| 7,586,788             | FMA13-00557JP            | United States | 12/01/2006  | 09/08/2009 | NONVOLATILE SEMICONDUCTOR MEMORY HAVING VOLTAGE ADJUSTING CIRCUIT                                                                             |
| 7,557,587             | FMA13-00557US            | United States | 03/21/2007  | 07/07/2009 | CONTROL APPARATUS, SEMICONDUCTOR INTEGRATED CIRCUIT APPARATUS, AND SOURCE VOLTAGE SUPPLY CONTROL SYSTEM                                       |
| 7,301,413             | FMA13-00558JP            | United States | 09/14/2004  | 11/27/2007 | VOLTAGE CONTROLLED OSCILLATOR AND PLL CIRCUIT                                                                                                 |
| 7,161,337             | FMA13-00559JP            | United States | 06/06/2005  | 01/09/2007 | MULTIPHASE DC-DC CONVERTER                                                                                                                    |
| 7,642,945             | FMA13-00560US            | United States | 02/22/2008  | 01/05/2010 | AD CONVERTER CIRCUIT AND MICROCONTROLLER                                                                                                      |
| 7,679,343             | FMA13-00561TW            | United States | 09/13/2007  | 03/16/2010 | POWER SUPPLY SYSTEM AND METHOD FOR CONTROLLING OUTPUT VOLTAGE                                                                                 |
| 11/511,318            | FMA13-00562TW            | United States | 08/29/2006  |            | TEMPERATURE CHARACTERISTIC CORRECTION METHOD AND SENSOR AMPLIFICATION CIRCUIT                                                                 |
| 7,675,267             | FMA13-00563US            | United States | 09/27/2006  | 03/09/2010 | CONTROL CIRCUIT OF POWER SUPPLY AND CONTROL METHOD OF THE POWER SUPPLY                                                                        |
| 8,508,307             | FMA13-00565TW            | United States | 06/10/2011  | 08/13/2013 | OSCILLATION CIRCUIT                                                                                                                           |
| 8,099,540             | FMA13-00566TW            | United States | 10/11/2006  | 01/17/2012 | RECONFIGURABLE CIRCUIT                                                                                                                        |
| 7,733,995             | FMA13-00568JP            | United States | 12/19/2005  | 06/08/2010 | NOISE FILTER AND FILTERING METHOD                                                                                                             |
| 7,512,873             | FMA13-00569TW            | United States | 07/28/2006  | 03/31/2009 | PARALLEL PROCESSING APPARATUS DYNAMICALLY SWITCHING OVER CIRCUIT CONFIGURATION                                                                |
| 7,545,054             | FMA13-00570JP            | United States | 06/06/2006  | 06/09/2009 | DC LINEAR REGULATOR SINGLE CONTROLLER WITH PLURAL LOADS                                                                                       |
| 7,861,235             | FMA13-00571US            | United States | 07/09/2007  | 12/28/2010 | PROGRAM CONTROL DEVICE AND PROGRAM CONTROL METHOD                                                                                             |
| 7,904,674             | FMA13-00572US            | United States | 11/14/2007  | 03/08/2011 | METHOD FOR CONTROLLING SEMICONDUCTOR MEMORY DEVICE                                                                                            |
| 7,960,946             | FMA13-00573US            | United States | 02/15/2008  | 06/14/2011 | POWER SUPPLY CIRCUIT, POWER SUPPLY CONTROL CIRCUIT, AND POWER SUPPLY CONTROL METHOD                                                           |
| 13/942,018            | FMA13-00574US            | United States | 07/15/2013  |            | ADJUSTING APPARATUS AND ADJUSTMENT METHOD                                                                                                     |
| 6,757,349             | FMA13-0058JP             | United States | 06/29/1998  | 06/29/2004 | PLL FREQUENCY SYNTHESIZER WITH LOCK DETECTION CIRCUIT                                                                                         |
| 5,914,903             | FMA13-0063KR             | United States | 01/30/1998  | 06/22/1999 | SEMICONDUCTOR MEMORY DEVICE                                                                                                                   |
| 6,031,425             | FMA13-0064JP             | United States | 01/27/1998  | 02/29/2000 | LOW POWER PRESCALER FOR A PLL CIRCUIT                                                                                                         |
| 6,321,280             | FMA13-0065KR             | United States | 02/01/1999  | 11/20/2001 | SYSTEM LSI HAVING COMMUNICATION FUNCTION                                                                                                      |
| 6,060,914             | FMA13-0066JP             | United States | 08/10/1998  | 05/09/2000 | SEMICONDUCTOR DEVICE INCLUDING A BOOST CIRCUIT                                                                                                |
| 6,895,496             | FMA13-0067KR             | United States | 03/12/1999  | 05/17/2005 | MICROCONTROLLER HAVING PREFETCH FUNCTION                                                                                                      |
| 6,075,477             | FMA13-0069KR             | United States | 07/27/1998  | 06/13/2000 | VOLTAGE SELECTOR FOR A D/A CONVERTER                                                                                                          |
| 6,147,923             | FMA13-0070TW             | United States | 06/30/1999  | 11/14/2000 | VOLTAGE BOOSTING CIRCUIT                                                                                                                      |
| 6,249,169             | FMA13-0071JP             | United States | 12/29/1998  | 06/19/2001 | TRANSISTOR OUTPUT CIRCUIT                                                                                                                     |
| 5,999,448             | FMA13-0072KR             | United States | 12/30/1998  | 12/07/1999 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND METHOD OF REPRODUCING DATA OF NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                             |
| 6,286,070             | FMA13-0073KR             | United States | 02/25/1999  | 09/04/2001 | SHARED MEMORY ACCESS DEVICE AND METHOD                                                                                                        |
| 6,484,270             | FMA13-0074JP             | United States | 05/04/1999  | 11/19/2002 | ELECTRIC DEVICE WITH FLASH MEMORY BUILT-IN                                                                                                    |
| 6,608,612             | FMA13-0075KR             | United States | 11/17/1999  | 08/19/2003 | SELECTOR AND MULTILAYER INTERCONNECTION WITH REDUCED OCCUPIED AREA ON SUBSTRATE                                                               |
| 6,218,810             | FMA13-0076JP             | United States | 03/01/2000  | 04/17/2001 | OUTPUT CIRCUIT AND BATTERY PACK                                                                                                               |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                          |
|-----------------------|---------------------------|---------------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6,476,954             | FMA13-0077JP              | United States | 03/19/1999  | 11/05/2002 | OPTICAL COMMUNICATION DEVICE AND RECEIVING CIRCUIT THEREOF                                                                                                                     |
| 5,963,474             | FMA13-0078KR              | United States | 09/25/1998  | 10/05/1999 | SECONDARY STORAGE DEVICE USING NONVOLATILE SEMICONDUCTOR MEMORY                                                                                                                |
| 6,353,864             | FMA13-0078US              | United States | 08/14/2001  | 03/05/2002 | SYSTEM LSI HAVING COMMUNICATION FUNCTION                                                                                                                                       |
| 5,982,661             | FMA13-0079JP              | United States | 02/10/1999  | 11/09/1999 | MEMORY DEVICE                                                                                                                                                                  |
| 6,304,241             | FMA13-0080US              | United States | 06/03/1998  | 10/16/2001 | DRIVER FOR A LIQUID-CRYSTAL DISPLAY PANEL                                                                                                                                      |
| 6,181,610             | FMA13-0082US              | United States | 12/22/1999  | 01/30/2001 | SEMICONDUCTOR DEVICE HAVING CURRENT AUXILIARY CIRCUIT FOR OUTPUT CIRCUIT                                                                                                       |
| 6,545,919             | FMA13-0083JP              | United States | 12/03/1999  | 04/08/2003 | SEMICONDUCTOR MEMORY AND OUTPUT SIGNAL CONTROL METHOD AND CIRCUIT IN SEMICONDUCTOR MEMORY                                                                                      |
| 6,598,176             | FMA13-0087TW              | United States | 12/27/1999  | 07/22/2003 | APPARATUS FOR ESTIMATING MICROCONTROLLER AND METHOD THEREOF                                                                                                                    |
| 6,778,448             | FMA13-0087US              | United States | 02/10/2003  | 08/17/2004 | SEMICONDUCTOR MEMORY AND OUTPUT SIGNAL CONTROL METHOD AND CIRCUIT IN SEMICONDUCTOR MEMORY                                                                                      |
| 6,456,170             | FMA13-0088JP              | United States | 03/30/2000  | 09/24/2002 | COMPARATOR AND VOLTAGE CONTROLLED OSCILLATOR CIRCUIT                                                                                                                           |
| 7,317,690             | FMA13-0089KR DIV          | United States | 03/10/2000  | 01/08/2008 | METHOD OF CONSTRUCTING NETWORK TOPOLOGY AND INTERFACE CIRCUIT                                                                                                                  |
| 6,674,277             | FMA13-0091TW              | United States | 08/18/2000  | 01/06/2004 | FREQUENCY MEASUREMENT CIRCUIT                                                                                                                                                  |
| 6,864,873             | FMA13-0092JP              | United States | 12/11/2000  | 03/08/2005 | SEMICONDUCTOR INTEGRATED CIRCUIT FOR DRIVING LIQUID CRYSTAL PANEL                                                                                                              |
| 6,466,065             | FMA13-0093PCT             | United States | 09/22/2000  | 10/15/2002 | PRESALER AND PLL CIRCUIT                                                                                                                                                       |
| 6,917,191             | FMA13-0093US              | United States | 11/05/2003  | 07/12/2005 | FREQUENCY MEASUREMENT CIRCUIT                                                                                                                                                  |
| 6,333,675             | FMA13-0094JP DIV          | United States | 04/06/2000  | 12/25/2001 | VARIABLE GAIN AMPLIFIER WITH GAIN CONTROL VOLTAGE BRANCH CIRCUIT                                                                                                               |
| 7,103,132             | FMA13-0095TW              | United States | 03/20/2000  | 09/05/2006 | PHASE COMPARATOR AND METHOD OF CONTROLLING POWER SAVING OPERATION OF THE SAME, AND SEMICONDUCTOR INTEGRATED CIRCUIT                                                            |
| 6,747,624             | FMA13-0097JP              | United States | 02/09/2000  | 06/08/2004 | DRIVING CIRCUIT FOR SUPPLYING TONE VOLTAGES TO LIQUID CRYSTAL DISPLAY PANEL                                                                                                    |
| 6,194,871             | FMA13-0098JP DIV          | United States | 04/24/2000  | 02/27/2001 | CHARGE AND DISCHARGE CONTROL CIRCUIT AND APPARATUS FOR SECONDARY BATTERY                                                                                                       |
| 6,320,359             | FMA13-0099JP              | United States | 09/28/2000  | 11/20/2001 | DC-DC CONVERTER AND CONTROLLER FOR DETECTING A MALFUNCTION THEREIN                                                                                                             |
| 6,515,525             | FMA13-0100TW              | United States | 03/16/2001  | 02/04/2003 | FRACTIONAL-N-PLL FREQUENCY SYNTHESIZER AND PHASE ERROR CANCELING METHOD THEREFOR                                                                                               |
| 6,337,563             | FMA13-0101JP              | United States | 01/26/2001  | 01/08/2002 | DC-DC CONVERTER AND SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE FOR DC-DC CONVERTER                                                                                                |
| 5,565,797             | FMA13-0102KR DIV3         | United States | 08/07/1995  | 10/15/1996 | CLOCK SIGNAL GENERATING DEVICE                                                                                                                                                 |
| 5,801,514             | FMA13-0102US DIV          | United States | 04/09/1997  | 09/15/1998 | CHARGING-AND-DISCHARGING CONTROL DEVICE, A BATTERY PACK, AND AN ELECTRONIC APPARATUS WITH IMPROVED CHARGE AND DISCHARGE CONTROL                                                |
| 5,808,444             | FMA13-0102US DIV          | United States | 12/12/1997  | 12/28/1999 | CHARGING-AND-DISCHARGING DEVICE, BATTERY PACK AND ELECTRONIC APPARATUS INCLUDING THEM                                                                                          |
| 6,008,629             | FMA13-0102US DIV          | United States | 01/17/1997  | 09/01/1998 | CHARGING-AND-DISCHARGING DEVICE FOR AN ELECTRONIC APPARATUS, AND AN ELECTRONIC APPARATUS INCLUDING THE SAME, UTILIZING A CHARGING DEVICE PROVIDING A CONSTANT CHARGING CURRENT |
| 6,529,083             | FMA13-0103JP              | United States | 03/30/2000  | 03/04/2003 | CLOCK CONTROL CIRCUIT                                                                                                                                                          |
| 6,518,845             | FMA13-0104KR              | United States | 03/16/2001  | 02/11/2003 | PLL FREQUENCY SYNTHESIZER CIRCUIT                                                                                                                                              |
| 6,597,162             | FMA13-0105TW              | United States | 01/11/2001  | 07/22/2003 | PLL SEMICONDUCTOR DEVICE WITH TESTABILITY, AND METHOD AND APPARATUS FOR TESTING SAME                                                                                           |
| 7,460,097             | FMA13-0105US              | United States | 09/01/2004  | 12/02/2008 | SEMICONDUCTOR INTEGRATED CIRCUIT FOR DRIVING LIQUID CRYSTAL PANEL                                                                                                              |
| 6,373,225             | FMA13-0106JP              | United States | 03/23/2001  | 04/16/2002 | CHARGE CIRCUIT THAT PERFORMS CHARGE CONTROL BY COMPARING A PLURALITY OF BATTERY VOLTAGES                                                                                       |
| 6,826,192             | FMA13-0108TW              | United States | 01/19/2001  | 11/30/2004 | INTERFACE APPARATUS                                                                                                                                                            |
| 6,876,185             | FMA13-0108US              | United States | 06/03/2003  | 04/05/2005 | PLL SEMICONDUCTOR DEVICE WITH TESTABILITY, AND METHOD AND APPARATUS FOR TESTING SAME                                                                                           |
| 6,647,475             | FMA13-0109JP              | United States | 02/26/2001  | 11/11/2003 | PROCESSOR CAPABLE OF ENABLING/DISABLING MEMORY ACCESS                                                                                                                          |
| 6,456,141             | FMA13-0110TW              | United States | 08/07/2001  | 09/24/2002 | CURRENT PULSE RECEIVING CIRCUIT                                                                                                                                                |
| 7,424,383             | FMA13-0111TW              | United States | 02/08/2001  | 09/09/2008 | ABNORMALITY DETECTION DEVICE FOR DETECTING AN ABNORMALITY IN A COMMUNICATION BUS                                                                                               |
| 6,784,866             | FMA13-0112JP              | United States | 04/02/2001  | 08/31/2004 | DOT-INVERSION DATA DRIVER FOR LIQUID CRYSTAL DISPLAY DEVICE                                                                                                                    |
| 6,452,449             | FMA13-0114JP              | United States | 09/18/2000  | 04/08/2011 | GAIN VARIABLE AMPLIFIER                                                                                                                                                        |
| 6,538,834             | FMA13-0114US              | United States | 07/03/2002  | 03/25/2003 | SERVO CONTROLLER AND SERVO CONTROL METHOD                                                                                                                                      |
| 6,462,686             | FMA13-0115JP              | United States | 02/14/2001  | 10/08/2002 | SERVO CONTROLLER AND SERVO CONTROL METHOD                                                                                                                                      |
| 6,775,741             | FMA13-0116JP              | United States | 01/25/2001  | 08/10/2004 | CACHE SYSTEM WITH LIMITED NUMBER OF TAG MEMORY ACCESSES                                                                                                                        |
| 6,552,958             | FMA13-0118JP              | United States | 02/04/2002  | 04/22/2003 | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                                                                                                                                        |
| 7,152,177             | FMA13-0119JP              | United States | 08/28/2001  | 12/19/2006 | MICROCOMPUTER AND COMPUTER SYSTEM                                                                                                                                              |
| 6,714,063             | FMA13-0119US              | United States | 08/08/2002  | 03/30/2004 | CURRENT PULSE RECEIVING CIRCUIT                                                                                                                                                |
| 6,891,408             | FMA13-0119US DIV          | United States | 01/30/2001  | 07/17/2009 | CURRENT PULSE RECEIVING CIRCUIT                                                                                                                                                |
| 6,674,657             | FMA13-0120JP              | United States | 01/10/2002  | 01/06/2004 | OVERVOLTAGE-PROTECTIVE DEVICE FOR POWER SYSTEM, AC/DC CONVERTER AND DC/DC CONVERTER CONSTITUTING THE POWER SYSTEM                                                              |
| 6,788,113             | FMA13-0121JP              | United States | 10/11/2001  | 09/07/2004 | DIFFERENTIAL SIGNAL OUTPUT APPARATUS, SEMICONDUCTOR INTEGRATED CIRCUIT APPARATUS HAVING THE DIFFERENTIAL SIGNAL OUTPUT APPARATUS, AND DIFFERENTIAL SIGNAL TRANSMISSION SYSTEM  |

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| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                   |
|-----------------------|--------------------------|---------------|-------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 6,781,412             | FMA13-0122TW             | United States | 02/13/2002  | 08/24/2004 | LOGIC CIRCUIT FOR FAST CARRY/BORROW                                                                                                     |
| 6,586,990             | FMA13-0123JP             | United States | 03/22/2002  | 07/01/2003 | OPERATIONAL AMPLIFIER HAVING OFFSET CANCEL FUNCTION                                                                                     |
| 6,653,871             | FMA13-0124JP             | United States | 02/13/2002  | 11/25/2003 | METHOD OF AND CIRCUIT FOR CONTROLLING A CLOCK                                                                                           |
| 6,510,090             | FMA13-0125JP             | United States | 03/25/2002  | 01/21/2003 | SEMICONDUCTOR MEMORY DEVICE                                                                                                             |
| 6,828,764             | FMA13-0127JP             | United States | 03/21/2002  | 12/07/2004 | REGULATOR CIRCUIT AND CONTROL METHOD THEREOF                                                                                            |
| 6,903,609             | FMA13-0129TW             | United States | 03/29/2002  | 06/07/2005 | OPERATIONAL AMPLIFIER                                                                                                                   |
| 7,342,436             | FMA13-0130JP             | United States | 12/12/2002  | 03/11/2008 | BIPOLAR SUPPLY VOLTAGE GENERATOR AND SEMICONDUCTOR<br>DEVICE FOR SAME                                                                   |
| 7,342,946             | FMA13-0131JP             | United States | 02/11/2002  | 03/11/2008 | DEVICE FOR PROCESSING DATA SIGNALS, METHOD THEREOF, AND<br>DEVICE FOR MULTIPLEXING DATA SIGNALS                                         |
| 7,113,041             | FMA13-0131US             | United States | 04/19/2005  | 09/26/2006 | OPERATIONAL AMPLIFIER                                                                                                                   |
| 7,136,956             | FMA13-0132JP             | United States | 03/06/2002  | 11/14/2006 | SEMICONDUCTOR DEVICE                                                                                                                    |
| 6,882,133             | FMA13-0133TW             | United States | 04/30/2002  | 04/19/2005 | DC/DC CONVERTER CONTROL CIRCUITS AND DC/DC CONVERTER<br>SYSTEMS WITH POWER SAVING MODE IN ACCORDANCE WITH AN<br>EXTERNAL CONTROL SIGNAL |
| 6,690,225             | FMA13-0135JP             | United States | 01/23/2003  | 02/10/2004 | DC OFFSET CANCEL CIRCUIT                                                                                                                |
| 6,867,623             | FMA13-0136TW             | United States | 10/24/2002  | 03/15/2005 | RECEIVING CIRCUIT                                                                                                                       |
| 6,696,821             | FMA13-0137JP             | United States | 01/16/2003  | 02/24/2004 | DC-DC CONVERTER, DUTY-RATIO SETTING CIRCUIT AND ELECTRIC<br>APPLIANCE USING THEM                                                        |
| 7,028,237             | FMA13-0139JP             | United States | 03/12/2003  | 04/11/2006 | INTERNAL BUS TESTING DEVICE AND METHOD                                                                                                  |
| 7,434,079             | FMA13-0139US             | United States | 12/13/2005  | 10/07/2008 | MICROCOMPUTER, METHOD OF CONTROLLING CACHE MEMORY, AND<br>METHOD OF CONTROLLING CLOCK                                                   |
| 7,064,743             | FMA13-0140JP             | United States | 01/29/2003  | 06/20/2006 | FINGER MOVEMENT DETECTION METHOD AND APPARATUS                                                                                          |
| 6,870,778             | FMA13-0141JP             | United States | 02/27/2003  | 03/22/2005 | SEMICONDUCTOR DEVICE INCLUDING A VOLTAGE MONITORING<br>CIRCUIT                                                                          |
| 6,946,905             | FMA13-0142JP             | United States | 11/22/2002  | 09/20/2005 | OFFSET CANCEL CIRCUIT OF VOLTAGE FOLLOWER EQUIPPED WITH<br>OPERATIONAL AMPLIFIER                                                        |
| 7,580,020             | FMA13-0142US             | United States | 07/17/2006  | 08/25/2009 | SEMICONDUCTOR DEVICE AND LIQUID CRYSTAL PANEL DRIVER<br>DEVICE                                                                          |
| 7,098,878             | FMA13-0143JP             | United States | 07/26/2002  | 08/29/2006 | SEMICONDUCTOR DEVICE AND LIQUID CRYSTAL PANEL DRIVER<br>DEVICE                                                                          |
| 6,768,682             | FMA13-0146JP             | United States | 09/30/2002  | 07/27/2004 | NONVOLATILE SEMICONDUCTOR MEMORY AND METHOD FOR<br>CONTROLLING PROGRAMMING VOLTAGE OF NONVOLATILE<br>SEMICONDUCTOR MEMORY               |
| 7,358,946             | FMA13-0146US             | United States | 07/15/2005  | 04/15/2008 | OFFSET CANCEL CIRCUIT OF VOLTAGE FOLLOWER EQUIPPED WITH<br>OPERATIONAL AMPLIFIER                                                        |
| 6,968,172             | FMA13-0147TW             | United States | 01/23/2003  | 11/22/2005 | DC OFFSET CANCEL CIRCUIT                                                                                                                |
| 6,788,152             | FMA13-0148JP             | United States | 04/18/2003  | 09/07/2004 | AMPLIFICATION CIRCUIT AND OPTICAL COMMUNICATION APPARATUS<br>PROVIDED WITH THE AMPLIFICATION CIRCUIT                                    |
| 6,727,771             | FMA13-0149TW             | United States | 10/09/2001  | 04/27/2004 | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE WITH VARIABLE<br>GAIN AMPLIFIER                                                                 |
| 10/850,395            | FMA13-0149US DIV         | United States | 05/21/2004  |            | DC COMPONENT CANCELLATION CIRCUIT                                                                                                       |
| 6,975,540             | FMA13-0150JP             | United States | 07/08/2003  | 12/13/2005 | SEMICONDUCTOR MEMORY DEVICE FOR DIFFERENTIAL DATA<br>AMPLIFICATION AND METHOD THEREFOR                                                  |
| 7,007,134             | FMA13-0151TW             | United States | 01/31/2003  | 02/28/2006 | MICROCOMPUTER, METHOD OF CONTROLLING CACHE MEMORY, AND<br>METHOD OF CONTROLLING CLOCK                                                   |
| 6,806,782             | FMA13-0153JP             | United States | 04/21/2003  | 10/19/2004 | FREQUENCY SYNTHESIZER CIRCUIT                                                                                                           |
| 6,917,541             | FMA13-0155JP             | United States | 02/01/2002  | 07/12/2005 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                 |
| RE43911               | FMA13-0156JP DIV8        | United States | 03/07/2003  | 01/08/2013 | CONTROL SYSTEM FOR CHARGING BATTERIES AND ELECTRONIC<br>APPARATUS USING SAME                                                            |
| RE42,114              | FMA13-0156US RE1         | United States | 04/12/2000  | 02/08/2011 | CONTROL SYSTEM FOR CHARGING BATTERIES AND ELECTRONIC<br>APPARATUS USING SAME                                                            |
| 5,617,347             | FMA13-0156US RE12        | United States | 03/17/1995  | 04/01/1997 | CACHE MEMORY SYSTEM AND METHOD THEREOF FOR STORING A<br>STAGED MEMORY ITEM AND A CACHE TAG WITHIN A SINGLE CACHE<br>ARRAY STRUCTURE     |
| 8,049,539             | FMA13-0158JP             | United States | 03/31/2003  | 11/01/2011 | CIRCUIT WITH VARIATION CORRECTION FUNCTION                                                                                              |
| 6,741,105             | FMA13-0161JP             | United States | 04/18/2003  | 05/25/2004 | DIFFERENTIAL CIRCUIT AND PEAK HOLD CIRCUIT INCLUDING<br>DIFFERENTIAL CIRCUIT                                                            |
| 6,879,521             | FMA13-0162JP             | United States | 02/21/2003  | 04/12/2005 | THRESHOLD VOLTAGE ADJUSTMENT METHOD OF NON-VOLATILE<br>SEMICONDUCTOR MEMORY DEVICE AND NON-VOLATILE<br>SEMICONDUCTOR MEMORY DEVICE      |
| 7,176,663             | FMA13-0163JP             | United States | 07/23/2003  | 02/13/2007 | CONTROL CIRCUIT FOR DC/DC CONVERTER                                                                                                     |
| 6,853,257             | FMA13-0164TW             | United States | 05/22/2003  | 02/08/2005 | PLL CIRCUIT INCLUDING A VOLTAGE CONTROLLED OSCILLATOR AND<br>A METHOD FOR CONTROLLING A VOLTAGE CONTROLLED<br>OSCILLATOR                |
| 6,842,063             | FMA13-0165JP             | United States | 07/24/2003  | 01/11/2005 | ANALOG SWITCH CIRCUIT                                                                                                                   |
| 6,990,642             | FMA13-0167JP             | United States | 08/06/2003  | 01/24/2006 | DESIGN METHOD FOR INTEGRATED CIRCUIT HAVING SCAN FUNCTION                                                                               |
| 6,940,338             | FMA13-0168JP             | United States | 11/12/2003  | 09/06/2005 | SEMICONDUCTOR INTEGRATED CIRCUIT                                                                                                        |
| 7,215,312             | FMA13-0169KR             | United States | 04/30/2003  | 05/08/2007 | SEMICONDUCTOR DEVICE, DISPLAY DEVICE, AND SIGNAL<br>TRANSMISSION SYSTEM                                                                 |
| 6,862,217             | FMA13-0170JP             | United States | 09/22/2003  | 03/01/2005 | CONTROL METHOD OF NON-VOLATILE SEMICONDUCTOR MEMORY<br>CELL AND NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE                                |
| 6,943,616             | FMA13-0171TW             | United States | 08/27/2003  | 09/13/2005 | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, AND ADJUSTMENT<br>METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                            |
| 7,122,995             | FMA13-0172US             | United States | 05/04/2005  | 10/17/2006 | MULTI-PHASE DC-DC CONVERTER AND CONTROL CIRCUIT FOR MULTI-<br>PHASE DC-DC CONVERTER                                                     |
| 7,174,435             | FMA13-0177TW             | United States | 11/19/2003  | 02/06/2007 | MEMORY CONTROL CIRCUIT, MEMORY DEVICE, AND<br>MICROCOMPUTER                                                                             |
| 7,095,260             | FMA13-0177US             | United States | 09/02/2005  | 08/22/2006 | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT, JITTER<br>GENERATION CIRCUIT AND SEMICONDUCTOR DEVICE                                         |
| 11/476,125            | FMA13-0177US DIV         | United States | 06/28/2006  |            | JITTER GENERATION CIRCUIT AND SEMICONDUCTOR DEVICE                                                                                      |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                                                                                                                                                                     |
|-----------------------|--------------------------|---------------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7,006,936             | FMA13-0178TW             | United States | 04/10/2003  | 02/28/2006 | PULSE WIDTH MEASURING DEVICE WITH AUTOMATIC RANGE<br>SETTING FUNCTION                                                                                                                                                                                                                                                     |
| 7,042,299             | FMA13-0185PCT            | United States | 04/15/2003  | 05/09/2006 | CRYSTAL OSCILLATION CIRCUIT                                                                                                                                                                                                                                                                                               |
| 7,622,760             | FMA13-0186JP             | United States | 03/03/2003  | 11/24/2009 | MOS TYPE VARIABLE CAPACITANCE DEVICE                                                                                                                                                                                                                                                                                      |
| 7,500,021             | FMA13-0190PCT            | United States | 05/21/2004  | 03/03/2009 | OPERATION MODE CONTROL CIRCUIT, MICROCOMPUTER INCLUDING<br>THE SAME, AND CONTROL SYSTEM USING THE MICROCOMPUTER                                                                                                                                                                                                           |
| 11/501,870            | FMA13-0191JP-1           | United States | 08/10/2006  |            | METHOD AND APPARATUS FOR SUPPORTING SOFTWARE TUNING<br>FOR MULTI-CORE PROCESSOR, AND COMPUTER PRODUCT                                                                                                                                                                                                                     |
| 14/297,200            | FMA13-0191US DIV         | United States | 06/05/2014  |            | INTER-BUS COMMUNICATION INTERFACE DEVICE                                                                                                                                                                                                                                                                                  |
| 7,034,514             | FMA13-0193JP             | United States | 03/25/2004  | 04/25/2006 | SEMICONDUCTOR INTEGRATED CIRCUIT USING BAND-GAP<br>REFERENCE CIRCUIT                                                                                                                                                                                                                                                      |
| 7,081,792             | FMA13-0194JP             | United States | 03/29/2004  | 07/25/2006 | OPERATIONAL AMPLIFIER, LINE DRIVER, AND LIQUID CRYSTAL<br>DISPLAY DEVICE                                                                                                                                                                                                                                                  |
| 7,454,650             | FMA13-0195JP             | United States | 03/02/2004  | 11/18/2008 | MICROCONTROLLER HAVING A SYSTEM RESOURCE PRESCALER<br>THEREON                                                                                                                                                                                                                                                             |
| 7,084,658             | FMA13-0196JP             | United States | 06/17/2004  | 08/01/2006 | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                                                                                                                                                                                                                                                                                   |
| 7,279,990             | FMA13-0197US             | United States | 11/28/2003  | 10/09/2007 | SIGMA-DELTA MODULATOR FOR PLL CIRCUITS                                                                                                                                                                                                                                                                                    |
| 7,068,116             | FMA13-0200KR             | United States | 06/29/2004  | 06/27/2006 | OSCILLATION CIRCUIT AND SEMICONDUCTOR DEVICE FREE FROM<br>THE INFLUENCE OF SOURCE VOLTAGE, TEMPERATURE AND<br>FLUCTUATIONS IN THE INVERTER THRESHOLD VOLTAGE                                                                                                                                                              |
| 7,518,390             | FMA13-0200US             | United States | 06/05/2006  | 04/14/2009 | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE WITH A TEST<br>CIRCUIT THAT MEASURES A PERIOD TO SELECT A TEST MODE                                                                                                                                                                                                               |
| 7,098,709             | FMA13-0201JP             | United States | 06/15/2004  | 08/29/2006 | SPREAD-SPECTRUM CLOCK GENERATOR                                                                                                                                                                                                                                                                                           |
| 7,613,956             | FMA13-0202JP             | United States | 01/18/2005  | 11/03/2009 | MICROCOMPUTER CAPABLE OF MONITORING INTERNAL MEMORY                                                                                                                                                                                                                                                                       |
| 7,119,550             | FMA13-0203JP DIV         | United States | 09/16/2004  | 10/10/2006 | CAPACITANCE DIFFERENCE DETECTING CIRCUIT AND MEMS SENSOR                                                                                                                                                                                                                                                                  |
| 7,414,453             | FMA13-0203US             | United States | 01/08/2007  | 08/19/2008 | LEVEL CONVERSION CIRCUIT                                                                                                                                                                                                                                                                                                  |
| 7,310,507             | FMA13-0204JP             | United States | 01/28/2005  | 12/18/2007 | FILTER CIRCUIT PERMITTING ADJUSTMENT OF CUTOFF FREQUENCY                                                                                                                                                                                                                                                                  |
| 7,262,587             | FMA13-0205JP             | United States | 11/05/2004  | 08/28/2007 | CIRCUIT AND METHOD FOR CONTROLLING DC-DC CONVERTER                                                                                                                                                                                                                                                                        |
| 7,176,740             | FMA13-0206JP             | United States | 09/24/2004  | 02/13/2007 | LEVEL CONVERSION CIRCUIT                                                                                                                                                                                                                                                                                                  |
| 7,908,453             | FMA13-0207JP             | United States | 06/28/2005  | 03/15/2011 | SEMICONDUCTOR DEVICE HAVING A DYNAMICALLY<br>RECONFIGURABLE CIRCUIT CONFIGURATION                                                                                                                                                                                                                                         |
| 7,075,159             | FMA13-0208JP             | United States | 08/05/2004  | 07/11/2006 | HORIZONTAL MOS TRANSISTOR                                                                                                                                                                                                                                                                                                 |
| 7,012,411             | FMA13-0209JP             | United States | 03/29/2004  | 03/14/2006 | SWITCHING REGULATOR CONTROL CIRCUIT, SWITCHING<br>REGULATOR AND SWITCHING REGULATOR CONTROL METHOD                                                                                                                                                                                                                        |
| 8,230,133             | FMA13-0210TW             | United States | 01/18/2005  | 07/24/2012 | MICROCOMPUTER WITH INTERNAL DMA                                                                                                                                                                                                                                                                                           |
| 7,720,138             | FMA13-0211TW             | United States | 05/18/2005  | 05/18/2010 | COMMUNICATION SYSTEM                                                                                                                                                                                                                                                                                                      |
| 7,245,178             | FMA13-0212JP             | United States | 11/17/2006  | 07/17/2007 | ANALOG FILTER CIRCUIT AND ADJUSTMENT METHOD THEREOF                                                                                                                                                                                                                                                                       |
| 7,250,745             | FMA13-0216JP             | United States | 10/27/2004  | 07/31/2007 | CONTROL CIRCUIT OF DC-DC CONVERTER AND ITS CONTROL<br>METHOD                                                                                                                                                                                                                                                              |
| 7,091,518             | FMA13-0217PCT            | United States | 01/27/2005  | 08/15/2006 | SEMICONDUCTOR DEVICE                                                                                                                                                                                                                                                                                                      |
| 7,405,627             | FMA13-0218JP             | United States | 09/08/2004  | 07/29/2008 | PLL FREQUENCY SYNTHESIZER                                                                                                                                                                                                                                                                                                 |
| 7,405,602             | FMA13-0219JP             | United States | 02/24/2005  | 07/29/2008 | RESET CONTROL CIRCUIT AND RESET CONTROL METHOD                                                                                                                                                                                                                                                                            |
| 7,596,025             | FMA13-0219US             | United States | 04/30/2007  | 09/29/2009 | SEMICONDUCTOR MEMORY DEVICE AND METHOD OF CONTROLLING<br>SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                                                                                                      |
| 7,898,860             | FMA13-0219US CON         | United States | 08/18/2009  | 03/01/2011 | SEMICONDUCTOR MEMORY DEVICE AND METHOD OF CONTROLLING<br>SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                                                                                                      |
| 7,196,379             | FMA13-0221JP             | United States | 10/18/2004  | 03/27/2007 | MOS CAPACITOR DEVICE                                                                                                                                                                                                                                                                                                      |
| 7,149,830             | FMA13-0222JP             | United States | 09/23/2004  | 12/12/2006 | SEMICONDUCTOR DEVICE AND MICROCONTROLLER                                                                                                                                                                                                                                                                                  |
| 7,224,606             | FMA13-0224TW             | United States | 03/01/2005  | 05/29/2007 | SEMICONDUCTOR MEMORY DEVICE AND METHOD OF CONTROLLING<br>SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                                                                                                      |
| 7,119,555             | FMA13-0225JP             | United States | 11/05/2004  | 10/10/2006 | CIRCUIT FOR DETECTING DIFFERENCE IN CAPACITANCE                                                                                                                                                                                                                                                                           |
| 7,701,178             | FMA13-0226TW             | United States | 10/01/2004  | 04/20/2010 | CHARGE CONTROL THAT KEEPS CONSTANT INPUT VOLTAGE<br>SUPPLIED TO BATTERY PACK                                                                                                                                                                                                                                              |
| 7,580,963             | FMA13-0227JP             | United States | 01/14/2005  | 08/25/2009 | SEMICONDUCTOR DEVICE HAVING AN ARITHMETIC UNIT OF A<br>RECONFIGURABLE CIRCUIT CONFIGURATION IN ACCORDANCE WITH<br>STORED CONFIGURATION DATA AND A MEMORY STORING FIXED<br>VALUE DATA TO BE SUPPLIED TO THE ARITHMETIC UNIT, REQUIRING<br>NO DATA AREA FOR STORING FIXED VALUE DATA TO BE SET IN A<br>CONFIGURATION MEMORY |
| 7,135,895             | FMA13-0228KR             | United States | 10/29/2004  | 11/14/2006 | SEMICONDUCTOR DEVICE HAVING OUTPUT CIRCUIT ADAPTIVELY<br>SUPPRESSING SSO NOISE                                                                                                                                                                                                                                            |
| 11/092,770            | FMA13-0231US             | United States | 03/30/2005  |            | SEMICONDUCTOR DEVICE, PRINTED-CIRCUIT BOARD AND<br>ELECTRONICS DEVICE                                                                                                                                                                                                                                                     |
| 7,352,163             | FMA13-0232TW             | United States | 05/19/2005  | 04/01/2008 | EARLY EFFECT CANCELLING CIRCUIT, DIFFERENTIAL AMPLIFIER,<br>LINEAR REGULATOR, AND EARLY EFFECT CANCELING METHOD                                                                                                                                                                                                           |
| 7,224,152             | FMA13-0233TW             | United States | 05/04/2005  | 05/29/2007 | DC-DC CONVERTER AND CONTROL CIRCUIT FOR DC-DC CONVERTER                                                                                                                                                                                                                                                                   |
| 7,471,099             | FMA13-0234JP             | United States | 03/22/2005  | 12/30/2008 | SEMICONDUCTOR DEVICE WITH MECHANISM FOR LEAK DEFECT<br>DETECTION                                                                                                                                                                                                                                                          |
| 8,717,833             | FMA13-0234US             | United States | 04/23/2008  | 05/06/2014 | SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                                                                                                                                                               |
| 14/251,448            | FMA13-0234US DIV         | United States | 04/11/2014  |            | SEMICONDUCTOR MEMORY DEVICE                                                                                                                                                                                                                                                                                               |
| 7,373,531             | FMA13-0236KR             | United States | 05/05/2005  | 05/13/2008 | SIGNAL DETECTION METHOD, FREQUENCY DETECTION METHOD,<br>POWER CONSUMPTION CONTROL METHOD, SIGNAL DETECTING<br>DEVICE, FREQUENCY DETECTING DEVICE, POWER CONSUMPTION<br>CONTROL DEVICE AND ELECTRONIC APPARATUS                                                                                                            |
| 7,624,205             | FMA13-0237TW             | United States | 06/07/2005  | 11/24/2009 | MICROCONTROLLER                                                                                                                                                                                                                                                                                                           |
| 8,503,501             | FMA13-0238US             | United States | 05/18/2005  | 08/06/2013 | SPREAD SPECTRUM CLOCK GENERATION CIRCUIT AND A METHOD<br>OF CONTROLLING THEREOF                                                                                                                                                                                                                                           |
| 7,301,412             | FMA13-0239JP             | United States | 09/01/2005  | 11/27/2007 | VARIABLE CAPACITY CIRCUIT AND CONTROL METHOD OF VARIABLE<br>CAPACITY CIRCUIT                                                                                                                                                                                                                                              |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                         |
|-----------------------|---------------------------|---------------|-------------|------------|---------------------------------------------------------------------------------------------------------------|
| 7,482,882             | FMA13-0240TW              | United States | 06/03/2005  | 01/27/2009 | VOLTAGE CONTROL OSCILLATION CIRCUIT AND ADJUSTING METHOD FOR THE SAME                                         |
| 7,253,679             | FMA13-0241TW              | United States | 09/14/2005  | 08/07/2007 | OPERATIONAL AMPLIFIER AND METHOD FOR CANCELING OFFSET VOLTAGE OF OPERATIONAL AMPLIFIER                        |
| 7,388,438             | FMA13-0242JP              | United States | 01/26/2005  | 06/17/2008 | ?? MODULATOR FOR PLL CIRCUIT                                                                                  |
| 8,024,495             | FMA13-0243KR              | United States | 06/30/2005  | 09/20/2011 | COMMUNICATION DATA CONTROLLER                                                                                 |
| 7,518,437             | FMA13-0245JP              | United States | 12/08/2005  | 04/14/2009 | CONSTANT CURRENT CIRCUIT AND CONSTANT CURRENT GENERATING METHOD                                               |
| 7,345,536             | FMA13-0246TW              | United States | 07/15/2005  | 03/18/2008 | AMPLIFIER CIRCUIT AND CONTROL METHOD THEREOF                                                                  |
| 7,215,165             | FMA13-0247JP              | United States | 11/07/2005  | 05/08/2007 | CLOCK GENERATING CIRCUIT AND CLOCK GENERATING METHOD                                                          |
| 7,372,760             | FMA13-0248JP              | United States | 08/22/2005  | 05/13/2008 | SEMICONDUCTOR DEVICE AND ENTRY INTO TEST MODE WITHOUT USE OF UNNECESSARY TERMINAL                             |
| 7,978,750             | FMA13-0249JP              | United States | 06/29/2005  | 07/12/2011 | MICROCONTROLLER                                                                                               |
| 7,355,481             | FMA13-0250JP              | United States | 08/11/2005  | 04/08/2008 | AMPLIFICATION CIRCUIT AND CONTROL METHOD OF AMPLIFICATION CIRCUIT                                             |
| RE41915               | FMA13-0254US              | United States | 05/27/2004  | 11/09/2010 | CHARGE/DISCHARGE CONTROL CIRCUIT AND SECONDARY BATTERY                                                        |
| 7,876,077             | FMA13-0255TW              | United States | 07/21/2005  | 01/25/2011 | CONTROL CIRCUIT AND CONTROL METHOD OF CURRENT MODE CONTROL TYPE DC-DC CONVERTER                               |
| 7,368,983             | FMA13-0255US              | United States | 07/24/2007  | 05/06/2008 | OPERATIONAL AMPLIFIER AND METHOD FOR CANCELING OFFSET VOLTAGE OF OPERATIONAL AMPLIFIER                        |
| 7,423,415             | FMA13-0256TW              | United States | 02/10/2006  | 09/09/2008 | DC-DC CONVERTER AND ITS CONTROL METHOD, AND SWITCHING REGULATOR AND ITS CONTROL METHOD                        |
| 7,266,015             | FMA13-0257TW              | United States | 12/20/2005  | 09/04/2007 | REDUNDANCY SUBSTITUTION METHOD, SEMICONDUCTOR MEMORY DEVICE AND INFORMATION PROCESSING APPARATUS              |
| 7,236,047             | FMA13-0260TW              | United States | 10/28/2005  | 06/26/2007 | BAND GAP CIRCUIT                                                                                              |
| 7,233,273             | FMA13-0261JP              | United States | 03/01/2006  | 06/19/2007 | ANALOG-TO-DIGITAL CONVERTER                                                                                   |
| 7,199,653             | FMA13-0262JP              | United States | 01/20/2006  | 04/03/2007 | SEMICONDUCTOR DEVICE WITH OPERATION MODE SET BY EXTERNAL RESISTOR                                             |
| 11/340,871            | FMA13-0263US              | United States | 01/27/2006  |            | RECONFIGURABLE INTEGRATED CIRCUIT DEVICE                                                                      |
| 7,734,896             | FMA13-0264JP              | United States | 03/28/2006  | 06/08/2010 | ENHANCED PROCESSOR ELEMENT STRUCTURE IN A RECONFIGURABLE INTEGRATED CIRCUIT DEVICE                            |
| 7,489,175             | FMA13-0266TW              | United States | 03/29/2006  | 02/10/2009 | CLOCK SUPPLY CIRCUIT AND METHOD                                                                               |
| 7,279,870             | FMA13-0267JP              | United States | 01/31/2006  | 10/09/2007 | DC-DC CONVERTER AND METHOD OF CONTROLLING DC-DC CONVERTER                                                     |
| 8,868,822             | FMA13-0268JP              | United States | 03/03/2011  | 10/21/2014 | DATA-PROCESSING METHOD, PROGRAM, AND SYSTEM                                                                   |
| 7,782,144             | FMA13-0269KR              | United States | 12/28/2005  | 08/24/2010 | ACTIVE FILTER IN PLL CIRCUIT                                                                                  |
| 7,515,159             | FMA13-0269TW              | United States | 02/03/2006  | 04/07/2009 | RECONFIGURABLE ADDRESS GENERATION CIRCUIT FOR IMAGE PROCESSING, AND RECONFIGURABLE LSI COMPRISING THE SAME    |
| 7,609,039             | FMA13-0272JP              | United States | 03/09/2006  | 10/27/2009 | CONTROLLER AND CONTROL METHOD FOR DC-DC CONVERTER                                                             |
| 7,227,784             | FMA13-0273TW              | United States | 02/22/2006  | 06/05/2007 | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE PERFORMING ERASE OPERATION THAT CREATES NARROW THRESHOLD DISTRIBUTION |
| 11/370,888            | FMA13-0274JP DIV          | United States | 03/09/2006  |            | CONTROL APPARATUS AND SEMICONDUCTOR INTEGRATED CIRCUIT APPARATUS                                              |
| 7,193,401             | FMA13-0275JP              | United States | 03/14/2006  | 03/20/2007 | CONTROL CIRCUIT AND CONTROL METHOD FOR DC-DC CONVERTER                                                        |
| 7,276,944             | FMA13-0276TW              | United States | 12/21/2005  | 10/02/2007 | CLOCK GENERATION CIRCUIT AND CLOCK GENERATION METHOD                                                          |
| 7,420,404             | FMA13-0277JP              | United States | 06/07/2006  | 09/02/2008 | PHASE ADJUSTER CIRCUIT AND PHASE ADJUSTING METHOD                                                             |
| 7,268,448             | FMA13-0278TW              | United States | 03/07/2006  | 09/11/2007 | PLURAL OUTPUT SWITCHING REGULATOR WITH PHASE COMPARISON AND DELAY MEANS                                       |
| 7,595,621             | FMA13-0279TW              | United States | 03/28/2006  | 09/29/2009 | DC-DC CONVERTER CONTROL CIRCUIT AND DC-DC CONVERTER CONTROL METHOD                                            |
| 7,298,117             | FMA13-0280TW              | United States | 02/27/2006  | 11/20/2007 | STEP-UP (BOOST) DC REGULATOR WITH TWO-LEVEL BACK-BIAS SWITCH GATE VOLTAGE                                     |
| 7,449,926             | FMA13-0281TW              | United States | 05/31/2006  | 11/11/2008 | CIRCUIT FOR ASYNCHRONOUSLY RESETTING SYNCHRONOUS CIRCUIT                                                      |
| 7,359,251             | FMA13-0282US              | United States | 09/11/2006  | 04/15/2008 | NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE, ERASE METHOD FOR SAME, AND TEST METHOD FOR SAME                     |
| 7,729,896             | FMA13-0283JP              | United States | 05/24/2006  | 06/01/2010 | CYCLE SIMULATION METHOD, CYCLE SIMULATOR, AND COMPUTER PRODUCT                                                |
| 7,679,411             | FMA13-0283US              | United States | 10/17/2008  | 03/16/2010 | RESET SIGNAL GENERATION CIRCUIT                                                                               |
| 7,781,909             | FMA13-0284JP              | United States | 09/07/2006  | 08/24/2010 | CONTROL CIRCUIT OF POWER SUPPLY, POWER SUPPLY AND CONTROL METHOD THEREOF                                      |
| 7,911,003             | FMA13-0285US              | United States | 08/30/2006  | 03/22/2011 | SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE                                                                       |
| 7,857,505             | FMA13-0287JP              | United States | 11/14/2006  | 12/28/2010 | METHOD AND CIRCUIT FOR CORRECTING SENSOR TEMPERATURE DEPENDENCY CHARACTERISTIC                                |
| 7,315,158             | FMA13-0288US              | United States | 07/28/2006  | 01/01/2008 | PULSE WIDTH MODULATION CIRCUIT                                                                                |
| 7,573,970             | FMA13-0289US              | United States | 08/28/2006  | 08/11/2009 | PRESALER AND BUFFER                                                                                           |
| 7,750,741             | FMA13-0290JP              | United States | 08/17/2006  | 07/06/2010 | PLL CIRCUIT AND SEMICONDUCTOR DEVICE                                                                          |
| 7,783,693             | FMA13-0293JP              | United States | 05/31/2006  | 08/24/2010 | RECONFIGURABLE CIRCUIT                                                                                        |
| 7,342,443             | FMA13-0294JP              | United States | 06/12/2006  | 03/11/2008 | OPERATIONAL AMPLIFIER                                                                                         |
| 7,456,623             | FMA13-0295JP              | United States | 05/19/2006  | 11/25/2008 | DC-DC CONVERTER AND CONTROL CIRCUIT FOR DC-DC CONVERTER                                                       |
| 7,663,923             | FMA13-0296TW              | United States | 05/23/2006  | 02/16/2010 | SEMICONDUCTOR MEMORY DEVICE AND CONTROL METHOD THEREOF                                                        |
| 7,679,214             | FMA13-0299KR              | United States | 08/30/2006  | 03/16/2010 | ELECTRONIC DEVICE INCORPORATING SYSTEM POWER SUPPLY UNIT AND METHOD FOR SUPPLYING POWER SUPPLY VOLTAGE        |
| 7,456,657             | FMA13-0300US              | United States | 07/21/2006  | 11/25/2008 | COMMON INPUT/OUTPUT TERMINAL CONTROL CIRCUIT                                                                  |
| 8,582,681             | FMA13-0301JP              | United States | 03/24/2009  | 11/12/2013 | SIGNAL RECEIVER APPARATUS AND WAVEFORM SHAPING METHOD                                                         |
| 7,242,170             | FMA13-0302TW              | United States | 04/06/2006  | 07/10/2007 | CONTROL CIRCUIT HAVING ERROR AMPLIFIER FOR DC-DC CONVERTER AND CONTROL METHOD THEREFOR                        |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                                 |
|-----------------------|---------------------------|---------------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7,777,473             | FMA13-0302US              | United States | 10/23/2008  | 08/17/2010 | DC-DC CONVERTER AND CONTROL CIRCUIT FOR DC-DC CONVERTER                                                                                                                               |
| 6,617,179             | G0025US                   | United States | 06/05/2001  | 09/09/2003 | METHOD AND SYSTEM FOR QUALIFYING AN ONO LAYER IN A SEMICONDUCTOR DEVICE                                                                                                               |
| 6,400,608             | G0063US                   | United States | 04/25/2001  | 06/04/2002 | ACCURATE VERIFY APPARATUS AND METHOD FOR NOR FLASH MEMORY CELLS IN THE PRESENCE OF HIGH COLUMN LEAKAGE                                                                                |
| 6,440,797             | G0067US                   | United States | 09/28/2001  | 08/27/2002 | NITRIDE BARRIER LAYER FOR PROTECTION OF ONO STRUCTURE FROM TOP OXIDE LOSS IN FABRICATION OF SONOS FLASH MEMORY                                                                        |
| 6,680,509             | G0067US DIV               | United States | 05/30/2002  | 01/20/2004 | NITRIDE BARRIER LAYER FOR PROTECTION OF ONO STRUCTURE FROM TOP OXIDE LOSS IN FABRICATION OF SONOS FLASH MEMORY                                                                        |
| 6,436,768             | G0074US                   | United States | 06/27/2001  | 08/20/2002 | SOURCE DRAIN IMPLANT DURING ONO FORMATION FOR IMPROVED ISOLATION OF SONOS DEVICES                                                                                                     |
| 6,897,533             | G01251US                  | United States | 09/18/2002  | 05/24/2005 | METHOD FOR FORMING MULTI-BIT SILICON NITRIDE TRAPPING NON-VOLATILE MEMORY CELL                                                                                                        |
| 6,475,863             | G0164US                   | United States | 05/17/2002  | 11/05/2002 | METHOD FOR FABRICATING SELF-ALIGNED GATE OF FLASH MEMORY CELL                                                                                                                         |
| 6,525,959             | G0185US                   | United States | 07/30/2001  | 02/25/2003 | NOR ARRAY WITH BURIED TRENCH SOURCE LINE                                                                                                                                              |
| 6,852,594             | G0186US                   | United States | 01/18/2002  | 02/08/2005 | TWO-STEP SOURCE SIDE IMPLANT FOR IMPROVING SOURCE RESISTANCE AND SHORT CHANNEL EFFECT IN DEEP SUB-0.18um FLASH MEMORY TECHNOLOGY                                                      |
| 6,664,191             | G0187US                   | United States | 10/09/2001  | 12/16/2003 | NON SELF-ALIGNED SHALLOW TRENCH ISOLATION PROCESS WITH DISPOSABLE SPACE TO DEFINE SUB-LITHOGRAPHIC POLY SPACE                                                                         |
| 6,888,157             | G0188US                   | United States | 07/27/2001  | 05/03/2005 | N-GATE/N-SUBSTRATE OR P-GATE/P-SUBSTRATE CAPACITOR TO CHARACTERIZE POLYSILICON GATE DEPLETION EVALUATION                                                                              |
| 6,541,338             | G0189US                   | United States | 07/30/2001  | 04/01/2003 | LOW DEFECT DENSITY PROCESS FOR DEEP SUB-0.18UM FLASH MEMORY TECHNOLOGIES                                                                                                              |
| 6,510,085             | G0190US                   | United States | 05/18/2001  | 01/21/2003 | METHOD OF CHANNEL HOT ELECTRON PROGRAMMING FOR SHORT CHANNEL NOR FLASH ARRAYS                                                                                                         |
| 6,525,368             | G0194US                   | United States | 06/27/2001  | 02/25/2003 | HIGH DENSITY FLASH EEPROM ARRAY WITH SOURCE SIDE INJECTION                                                                                                                            |
| 6,996,004             | G0206US                   | United States | 11/04/2003  | 02/07/2006 | MINIMIZATION OF FG-FG COUPLING IN FLASH MEMORY                                                                                                                                        |
| 6,469,939             | G0259US                   | United States | 10/01/2001  | 10/22/2002 | FLASH MEMORY DEVICE WITH INCREASE OF EFFICIENCY DURING AN APDE (AUTOMATIC PROGRAM DISTURB AFTER ERASE) PROCESS                                                                        |
| 60/291,861            | G0259US PROV              | United States | 05/18/2001  |            | FLASH MEMORY DEVICE WITH INCREASE EFFICIENCY DURING AN APDE (AUTOMATIC PROGRAM DISTURB AFTER ERASE) PROCESS                                                                           |
| 6,486,682             | G0260US                   | United States | 07/13/2001  | 11/26/2002 | DETERMINATION OF DIELECTRIC CONSTANTS OF THIN DIELECTRIC MATERIALS IN A MOS (METAL OXIDE SEMICONDUCTOR) STACK                                                                         |
| 6,500,713             | G0283US                   | United States | 12/20/2001  | 12/31/2002 | METHOD FOR REPAIRING DAMAGE TO CHARGE TRAPPING DIELECTRIC LAYER FROM BIT LINE IMPLANTATION                                                                                            |
| 6,706,576             | G0286US                   | United States | 03/14/2002  | 03/16/2004 | LASER THERMAL ANNEALING OF SILICON NITRIDE FOR INCREASED DENSITY AND ETCH SELECTIVITY                                                                                                 |
| 7,670,936             | G0293US                   | United States | 10/18/2002  | 03/02/2010 | NITRIDATION OF GATE OXIDE BY LASER PROCESSING                                                                                                                                         |
| 6,872,643             | G0295US                   | United States | 03/05/2003  | 03/29/2005 | IMPLANT DAMAGE REMOVAL BY LASER THERMAL ANNEALING                                                                                                                                     |
| 7,001,814             | G0313US                   | United States | 05/16/2003  | 02/21/2006 | LASER THERMAL ANNEALING METHODS FOR FLASH MEMORY DEVICES                                                                                                                              |
| 10/200,540            | G0391                     | United States | 07/07/2003  |            | BUILT-IN-SELF-TEST (BIST) OF FLASH MEMORY CELLS AND IMPLEMENTATION OF BIST INTERFACE                                                                                                  |
| 10/200,543            | G0393                     | United States | 07/22/2002  |            | PATTERN GENERATOR IN BIST (Built-In-Self-Test) SYSTEM FOR TESTING FLASH MEMORY CELLS                                                                                                  |
| 6,665,214             | G0394US                   | United States | 07/22/2002  | 12/16/2003 | ON-CHIP ERASE PULSE COUNTER FOR EFFICIENT ERASE VERIFY BIST (BUILT-IN-SELF-TEST) MODE                                                                                                 |
| 6,631,086             | G0395US                   | United States | 07/22/2002  | 10/07/2003 | ON-CHIP REPAIR OF DEFECTIVE ADDRESS OF CORE FLASH MEMORY CELLS                                                                                                                        |
| 10/200,538            | G0396                     | United States | 07/22/2002  |            | BACK-END BIST (BUILT-IN-SELF-TEST) STATE MACHINE FOR TESTING FLASH MEMORY CELLS                                                                                                       |
| 7,028,240             | G0399US                   | United States | 07/22/2002  | 04/11/2006 | DIAGNOSTIC MODE FOR TESTING FUNCTIONALITY OF BIST (BUILT-IN-SELF-TEST) BACK-END STATE MACHINE                                                                                         |
| 7,010,736             | G0401US                   | United States | 07/22/2002  | 03/07/2006 | ADDRESS SEQUENCER WITHIN BIST (BUILT-IN-SELF-TEST) SYSTEM                                                                                                                             |
| 6,707,718             | G0405US                   | United States | 07/22/2002  | 03/16/2004 | GENERATION OF MARGINING VOLTAGE ON-CHIP DURING TESTING CAM PORTION OF FLASH MEMORY DEVICE                                                                                             |
| 6,894,925             | G0432US                   | United States | 01/14/2003  | 05/17/2005 | FLASH MEMORY CELL PROGRAMMING METHOD AND SYSTEM                                                                                                                                       |
| 6,590,260             | G0436US                   | United States | 03/20/2002  | 07/08/2003 | MEMORY DEVICE HAVING IMPROVED PROGRAMMABILITY                                                                                                                                         |
| 6,777,957             | G0438US                   | United States | 06/18/2002  | 08/17/2004 | A TEST STRUCTURE TO MEASURE INTERLAYER DIELECTRIC EFFECTS AND BREAKDOWN AND DETECT METAL DEFECTS IN FLASH MEMORIES                                                                    |
| 6,731,130             | G0439US                   | United States | 12/12/2001  | 05/04/2004 | METHOD OF DETERMINING GATE OXIDE THICKNESS OF AN OPERATIONAL MOSFET                                                                                                                   |
| 6,764,920             | G0440US                   | United States | 04/19/2002  | 07/20/2004 | METHOD FOR REDUCING SHALLOW TRENCH ISOLATION EDGE THINNING TUNNEL OXIDES USING PARTIAL NITRIDE STRIP AND SMALL BIRD'S BEAK FORMATION FOR HIGH PERFORMANCE FLASH MEMORY DEVICES        |
| 6,825,083             | G0443US                   | United States | 04/19/2002  | 11/30/2004 | METHOD FOR REDUCING SHALLOW TRENCH ISOLATION EDGE THINNING ON THIN GATE OXIDES TO IMPROVE PERIPHERAL TRANSISTOR RELIABILITY AND PERFORMANCE FOR HIGH PERFORMANCE FLASH MEMORY DEVICES |
| 6,734,080             | G0444US                   | United States | 05/31/2002  | 05/11/2004 | A SEMICONDUCTOR ISOLATION MATERIAL DEPOSITION SYSTEM AND METHOD                                                                                                                       |
| 6,756,806             | G0445US                   | United States | 03/28/2002  | 06/29/2004 | METHOD OF DETERMINING LOCATION OF GATE OXIDE BREAKDOWN OF MOSFET                                                                                                                      |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                                                                         |
|-----------------------|---------------------------|---------------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 6,759,295             | G0456US                   | United States | 08/20/2002  | 07/06/2004 | METHOD OF DETERMINING THE ACTIVE REGION WIDTH BETWEEN SHALLOW TRENCH ISOLATION STRUCTURES USING A GATE CURRENT MEASUREMENT TECHNIQUE FOR FABRICATING A FLASH MEMORY SEMICONDUCTOR DEVICE AND DEVICE THEREBY FORMED            |
| 6,818,462             | G0457                     | United States | 08/19/2002  | 11/16/2004 | METHOD OF DETERMINING THE ACTIVE REGION WIDTH BETWEEN SHALLOW TRENCH ISOLATION STRUCTURES USING A C-V MEASUREMENT TECHNIQUE FOR FABRICATING A FLASH MEMORY SEMICONDUCTOR DEVICE AND A DEVICE THEREBY FORMED                   |
| 6,884,638             | G0458US                   | United States | 08/20/2002  | 04/26/2005 | METHOD OF FABRICATING A FLASH MEMORY SEMICONDUCTOR DEVICE BY DETERMINING THE ACTIVE REGION WIDTH BETWEEN SHALLOW TRENCH ISOLATION STRUCTURES USING AN OVERDRIVE CURRENT MEASUREMENT TECHNIQUE AND A DEVICE THEREBY FABRICATED |
| 6,674,138             | G0463US                   | United States | 12/31/2001  | 01/06/2004 | USE OF HIGH-K DIELECTRIC MATERIALS IN MODIFIED ONO STRUCTURE FOR SEMICONDUCTOR DEVICES                                                                                                                                        |
| 6,803,272             | G0463US DIV               | United States | 08/22/2003  | 10/12/2004 | USE OF HIGH-K DIELECTRIC MATERIALS IN MODIFIED ONO STRUCTURE FOR SEMICONDUCTOR DEVICES                                                                                                                                        |
| 6,693,321             | G0464US                   | United States | 05/15/2002  | 02/17/2004 | REPLACING LAYERS OF AN INTERGATE DIELECTRIC LAYER WITH HIGH-K MATERIAL FOR IMPROVED SCALABILITY                                                                                                                               |
| 10/189,643            | G0468US                   | United States | 07/03/2002  |            | METHOD OF INTERPOLY HIGH-K DIELECTRIC INTEGRATION TO MINIMIZE LEAKAGE AND FLOATING GATE CONTAMINATION                                                                                                                         |
| 60/412,739            | G0472                     | United States | 09/23/2002  |            | Bilayer Floating Gate For Improved Work Function Between Floating Gate And A High-K Dielectric Layer                                                                                                                          |
| 6,630,383             | G0472US                   | United States | 10/17/2002  | 10/07/2003 | BILAYER FLOATING GATE FOR IMPROVED WORK FUNCTION BETWEEN FLOATING GATE AND A HIGH-K DIELECTRIC LAYER                                                                                                                          |
| 6,750,066             | G0475US                   | United States | 04/08/2002  | 06/15/2004 | PRECISION HIGH-K INTERGATE DIELECTRIC LAYER                                                                                                                                                                                   |
| 6,753,570             | G0476US                   | United States | 08/20/2002  | 06/22/2004 | MEMORY DEVICE AND METHOD OF MAKING                                                                                                                                                                                            |
| 6,548,855             | G0478                     | United States | 05/16/2002  | 04/15/2003 | NON-VOLATILE MEMORY DIELECTRIC AS CHARGE PUMP DIELECTRIC                                                                                                                                                                      |
| 6,642,573             | G0481US                   | United States | 03/13/2002  | 11/04/2003 | USE OF HIGH-K DIELECTRIC MATERIAL IN MODIFIED ONO STRUCTURE FOR SEMICONDUCTOR DEVICES                                                                                                                                         |
| 10/265,955            | G0487US                   | United States | 10/07/2002  |            | MEMORY DEVICES CONTAINING A HIGH-K DIELECTRIC LAYER                                                                                                                                                                           |
| 8,691,647             | G0487US DIV               | United States | 08/27/2004  | 04/08/2014 | MEMORY DEVICES CONTAINING A HIGH-K DIELECTRIC LAYER                                                                                                                                                                           |
| 6,639,271             | G0495US                   | United States | 12/20/2001  | 10/28/2003 | FULLY ISOLATED DIELECTRIC MEMORY CELL STRUCTURE FOR A DUAL BIT NITRIDE STORAGE DEVICE AND PROCESS FOR MAKING SAME                                                                                                             |
| 6,861,307             | G0495US DIV1              | United States | 07/31/2003  | 03/01/2005 | FULLY ISOLATED DIELECTRIC MEMORY CELL STRUCTURE FOR A DUAL BIT NITRIDE STORAGE DEVICE AND PROCESS FOR MAKING SAME                                                                                                             |
| 7,001,807             | G0495US DIV2              | United States | 11/24/2004  | 02/21/2006 | FULLY ISOLATED DIELECTRIC MEMORY CELL STRUCTURE FOR A DUAL BIT NITRIDE STORAGE DEVICE AND PROCESS FOR MAKING SAME                                                                                                             |
| 6,627,945             | G0502US                   | United States | 07/03/2002  | 09/30/2003 | MEMORY DEVICE AND METHOD OF MAKING                                                                                                                                                                                            |
| 6,735,123             | G0503US                   | United States | 06/07/2002  | 05/11/2004 | HIGH DENSITY DUAL BIT FLASH MEMORY CELL WITH NON PLANAR STRUCTURE                                                                                                                                                             |
| 6,593,590             | G0514US                   | United States | 03/28/2002  | 07/15/2003 | A TEST STRUCTURE APPARATUS FOR MEASURING STANDBY CURRENT IN FLASH MEMORY DEVICES                                                                                                                                              |
| 6,596,586             | G0515US                   | United States | 05/21/2002  | 07/22/2003 | METHOD OF FORMING LOW RESISTANCE COMMON SOURCE LINE FOR FLASH MEMORY DEVICES                                                                                                                                                  |
| 60/344,191            | G0573                     | United States | 12/28/2001  |            | TREATMENT OF DIELECTRIC MATERIAL TO ENHANCE ETCH RATE                                                                                                                                                                         |
| 6,905,971             | G0573US                   | United States | 12/30/2002  | 06/14/2005 | TREATMENT OF DIELECTRIC MATERIAL TO ENHANCE ETCH RATE                                                                                                                                                                         |
| 6,762,454             | G0576US                   | United States | 04/08/2002  | 07/13/2004 | STACKED POLYSILICON LAYER FOR BORON PENETRATION INHIBITION                                                                                                                                                                    |
| 10/215,071            | G0683                     | United States | 08/07/2002  |            | METHOD FOR FORMING TRENCHES FOR USE AS SHALLOW TRENCH ISOLATION (STI) REGIONS WITH A TAPERED PROFILE                                                                                                                          |
| 10/032,631            | G0689                     | United States | 12/27/2001  |            | SHALLOW TRENCH ISOLATION APPROACH FOR IMPROVED STI CORNER ROUNDING                                                                                                                                                            |
| 6,885,250             | G0689US                   | United States | 05/12/2004  | 04/26/2005 | CASCADE AMPLIFIER CIRCUIT FOR PRODUCING A FAST, STABLE AND ACCURATE BITLINE VOLTAGE                                                                                                                                           |
| 7,439,141             | G0689US CIP               | United States | 10/22/2002  | 10/21/2008 | SHALLOW TRENCH ISOLATION APPROACH FOR IMPROVED STI CORNER ROUNDING                                                                                                                                                            |
| 6,670,691             | G0692US                   | United States | 06/18/2002  | 12/30/2003 | SHALLOW TRENCH ISOLATION FILL PROCESS                                                                                                                                                                                         |
| 6,610,577             | G0693US                   | United States | 05/15/2002  | 08/26/2003 | SELF-ALIGNED POLYSILICON POLISH                                                                                                                                                                                               |
| 6,607,925             | G0695US                   | United States | 06/06/2002  | 08/19/2003 | HARD MASK REMOVAL PROCESS INCLUDING ISOLATION DIELECTRIC REFILL                                                                                                                                                               |
| 6,806,165             | G0713US                   | United States | 04/09/2002  | 10/19/2004 | ISOLATION TRENCH FILL PROCESS                                                                                                                                                                                                 |
| 6,566,230             | G0719                     | United States | 12/27/2001  | 05/20/2003 | SHALLOW TRENCH ISOLATION SPACER FOR WEEF IMPROVEMENT                                                                                                                                                                          |
| 6,605,517             | G0724US                   | United States | 05/15/2002  | 08/12/2003 | METHOD FOR MINIMIZING NITRIDE RESIDUE ON A SILICON WAFER                                                                                                                                                                      |
| 6,740,926             | G0727US                   | United States | 12/27/2001  | 05/25/2004 | PLANAR TRANSISTOR STRUCTURE USING ISOLATION IMPLANTS FOR IMPROVED V <sub>SS</sub> RESISTANCE AND FOR PROCESS SIMPLIFICATION                                                                                                   |
| 6,811,932             | G0729                     | United States | 06/06/2002  | 11/02/2004 | METHOD AND SYSTEM FOR DETERMINING FLOW RATES FOR CONTACT FORMATION                                                                                                                                                            |
| 7,015,135             | G0730US                   | United States | 12/10/2002  | 03/21/2006 | METHOD AND SYSTEM FOR REDUCING CONTACT DEFECTS USING NON CONVENTIONAL CONTACT FORMATION METHOD FOR SEMICONDUCTOR CELLS                                                                                                        |
| 6,806,155             | G0750US                   | United States | 05/15/2002  | 10/19/2004 | METHOD AND SYSTEM FOR SCALING A NONVOLATILE MEMORY CELLS                                                                                                                                                                      |
| 6,723,638             | G0752US                   | United States | 02/05/2003  | 04/20/2004 | IMPROVED PERFORMANCE IN FLASH MEMORY DEVICES                                                                                                                                                                                  |
| 6,700,201             | G0761US                   | United States | 12/11/2001  | 03/02/2004 | REDUCTION OF SECTOR CONNECTING LINE CAPACITANCE USING STAGGERED METAL LINES                                                                                                                                                   |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                              |
|-----------------------|---------------------------|---------------|-------------|------------|------------------------------------------------------------------------------------------------------------------------------------|
| 6,953,752             | G0764US                   | United States | 02/05/2003  | 10/11/2005 | REDUCED SILICON GOUGING AND COMMON SOURCE LINE RESISTANCE IN SEMICONDUCTOR DEVICES                                                 |
| 6,754,109             | G0766US                   | United States | 10/29/2002  | 06/22/2004 | METHOD OF PROGRAMMING IN-SERIES MEMORY CELLS                                                                                       |
| 10/303,365            | G0770US                   | United States | 11/25/2002  |            | PROVISION OF LOW COMMON SOURCE RESISTANCE IN FLASH MEMORY CELL ARCHITECTURE                                                        |
| 6,617,639             | G0772US                   | United States | 06/21/2002  | 09/09/2003 | USE OF HIGH-K DIELECTRIC MATERIAL FOR ONO AND TUNNEL OXIDE TO IMPROVE FLOATING GATE FLASH MEMORY COUPLING                          |
| 6,654,285             | G0786US                   | United States | 02/27/2002  | 11/25/2003 | METHOD OF MATCHING CORE CELL AND REFERENCE CELL SOURCE RESISTANCES                                                                 |
| 6,781,885             | G0793US                   | United States | 03/05/2003  | 08/24/2004 | METHOD OF PROGRAMMING A MEMORY CELL                                                                                                |
| 6,737,703             | G0798US                   | United States | 03/12/2002  | 05/18/2004 | MEMORY ARRAY WITH BURIED BIT LINES                                                                                                 |
| 6,653,190             | G0802US                   | United States | 12/15/2001  | 11/25/2003 | FLASH MEMORY WITH CONTROLLED WORDLINE WIDTH                                                                                        |
| 7,755,938             | G0807US                   | United States | 04/19/2004  | 07/13/2010 | METHOD FOR READING A MEMORY ARRAY WITH NEIGHBOR EFFECT CANCELLATION                                                                |
| 7,208,382             | G0808US                   | United States | 05/16/2002  | 04/24/2007 | SEMICONDUCTOR DEVICE WITH HIGH CONDUCTIVITY REGION USING SHALLOW TRENCH                                                            |
| 11/685,711            | G0808US DIV               | United States | 03/13/2007  |            | SEMICONDUCTOR DEVICE WITH HIGH CONDUCTIVITY REGION USING SHALLOW TRENCH                                                            |
| 6,770,523             | G0809US                   | United States | 07/02/2002  | 08/03/2004 | METHOD FOR SEMICONDUCTOR WAFER PLANARIZATION BY CMP STOP LAYER FORMATION                                                           |
| 7,052,969             | G0810US                   | United States | 07/03/2002  | 05/30/2006 | METHOD FOR SEMICONDUCTOR WAFER PLANARIZATION BY ISOLATION MATERIAL GROWTH                                                          |
| 6,620,717             | G0811US                   | United States | 03/14/2002  | 09/16/2003 | MEMORY WITH DISPOSABLE ARC FOR WORDLINE FORMATION                                                                                  |
| 6,773,988             | G0812US                   | United States | 09/13/2002  | 08/10/2004 | MEMORY WORDLINE SPACER                                                                                                             |
| 7,053,446             | G0812US DIV               | United States | 06/08/2004  | 05/30/2006 | MEMORY WORDLINE SPACER                                                                                                             |
| 6,994,939             | G0814US                   | United States | 10/29/2002  | 02/07/2006 | SEMICONDUCTOR MANUFACTURING RESOLUTION ENHANCEMENT SYSTEM AND METHOD FOR SIMULTANEOUSLY PATTERNING DIFFERENT FEATURE TYPES         |
| 6,901,010             | G0861US                   | United States | 04/08/2002  | 05/31/2005 | IMPROVED ERASE METHOD FOR SINGLE SIDED MIRROR OPERATION                                                                            |
| 6,700,815             | G0862US                   | United States | 04/08/2002  | 03/02/2004 | REFRESH SCHEME FOR DYNAMIC PAGE PROGRAMMING                                                                                        |
| 6,639,844             | G0863US                   | United States | 03/12/2003  |            | OVERERASE CORRECTION METHOD                                                                                                        |
| 6,690,602             | G0864US                   | United States | 04/08/2002  | 02/10/2004 | ALGORITHM DYNAMIC REFERENCE PROGRAMMING                                                                                            |
| 7,076,703             | G0865US                   | United States | 11/26/2002  | 07/11/2006 | METHOD AND SYSTEM FOR DEFINING A REDUNDANCY WINDOW AROUND A PARTICULAR COLUMN IN A MEMORY ARRAY                                    |
| 10/155,767            | G0866US                   | United States | 05/24/2002  |            | STEPPED PRE-ERASE VOLTAGE FOR MIRRORBIT ERASE                                                                                      |
| 6,813,752             | G0867                     | United States | 11/26/2002  | 11/02/2004 | METHOD OF DETERMINING CHARGE LOSS ACTIVATION ENERGY OF A MEMORY ARRAY                                                              |
| 7,023,740             | G0870US                   | United States | 01/12/2004  | 04/04/2006 | SUBSTRATE BIAS FOR PROGRAMMING NON-VOLATILE MEMORY                                                                                 |
| 7,049,188             | G0871US                   | United States | 11/26/2002  | 05/23/2006 | LATERAL DOPED CHANNEL                                                                                                              |
| 6,743,677             | G0872US                   | United States | 11/27/2002  | 06/01/2004 | METHOD FOR FABRICATING NITRIDE MEMORY CELLS USING A FLOATING GATE FABRICATION PROCESS                                              |
| 10/722,207            | G0873US                   | United States | 11/24/2003  |            | A STRUCTURE AND METHOD TO FORM A BURIED POLY BITLINE                                                                               |
| 7,232,729             | G0874US                   | United States | 05/06/2003  | 06/19/2007 | METHOD FOR MANUFACTURING A DOUBLE BITLINE IMPLANT                                                                                  |
| 6,643,177             | G0875US                   | United States | 01/21/2003  | 11/04/2003 | METHOD FOR IMPROVING READ MARGIN IN A FLASH MEMORY DEVICE                                                                          |
| 6,897,110             | G0877US                   | United States | 11/26/2002  | 05/24/2005 | METHOD OF PROTECTING A MEMORY ARRAY FROM CHARGE DAMAGE DURING FABRICATION                                                          |
| 6,906,959             | G0878US                   | United States | 11/27/2002  | 06/14/2005 | A METHOD AND SYSTEM FOR ERASING A NITRIDE MEMORY DEVICE                                                                            |
| 6,654,283             | G0929US                   | United States | 12/11/2001  | 11/25/2003 | FLASH MEMORY ARRAY ARCHITECTURE AND METHOD FOR PROGRAMMING, ERASING AND READING THEREOF                                            |
| 6,646,914             | G0930US                   | United States | 03/12/2002  | 11/11/2003 | FLASH MEMORY ARRAY ARCHITECTURE HAVING STAGGERED METAL LINES                                                                       |
| 6,768,683             | G0931US                   | United States | 03/12/2002  | 07/27/2004 | LOW COLUMN LEAKAGE FLASH MEMORY ARRAY                                                                                              |
| 10/159,324            | G1125                     | United States | 05/31/2002  |            | HIGH DENSITY PLASMA FORMED OXIDE DEVICE ISOLATION                                                                                  |
| 6,859,748             | G1126US                   | United States | 07/03/2002  | 02/22/2005 | TEST STRUCTURE FOR MEASURING EFFECT OF TRENCH ISOLATION ON OXIDE IN A MEMORY DEVICE                                                |
| 6,643,185             | G1127US                   | United States | 08/07/2002  | 11/04/2003 | METHOD FOR REPAIRING OVER-ERASURE OF FAST BITS IN FLOATING GATE MEMORY DEVICES                                                     |
| 6,861,696             | G1135US                   | United States | 05/03/2003  | 03/01/2005 | STRUCTURE AND METHOD FOR A TWO-BIT MEMORY CELL                                                                                     |
| 6,716,710             | G1142US                   | United States | 04/19/2002  | 04/06/2004 | USING A FIRST LINER LAYER AS A SPACER IN A SEMICONDUCTOR DEVICE                                                                    |
| 6,689,666             | G1144US                   | United States | 04/19/2002  | 02/10/2004 | REPLACING A FIRST LINER LAYER WITH A THICKER OXIDE LAYER WHEN FORMING A SEMICONDUCTOR DEVICE                                       |
| 6,642,106             | G1145US                   | United States | 05/31/2002  | 11/04/2003 | METHOD FOR INCREASING CORE GAIN IN FLASH MEMORY DEVICE USING STRAINED SILICON                                                      |
| 6,784,682             | G1148US                   | United States | 03/28/2002  | 08/31/2004 | METHOD OF DETECTING SHALLOW TRENCH ISOLATION CORNER THINNING BY ELECTRICAL TRAPPING                                                |
| 6,734,028             | G1150US                   | United States | 03/28/2002  | 05/11/2004 | METHOD OF DETECTING SHALLOW TRENCH ISOLATION CORNER THINNING BY ELECTRICAL STRESS                                                  |
| 6,576,487             | G1244US                   | United States | 04/19/2002  | 06/10/2003 | METHOD TO DISTINGUISH AN STI OUTER EDGE CURRENT COMPONENT WITH AN STI NORMAL CURRENT COMPONENT                                     |
| 6,461,905             | G1247US                   | United States | 02/22/2002  | 10/08/2002 | DUMMY GATE PROCESS TO REDUCE THE VSS RESISTANCE OF FLASH PRODUCTS                                                                  |
| 6,836,432             | G1255US                   | United States | 02/11/2002  | 12/28/2004 | PARTIAL PAGE PROGRAMMING OF MULTI LEVEL FLASH                                                                                      |
| 6,606,273             | H0053US                   | United States | 04/11/2002  | 08/12/2003 | METHODS AND SYSTEMS FOR FLASH MEMORY TUNNEL OXIDE RELIABILITY TESTING                                                              |
| 6,570,787             | H0054US                   | United States | 04/19/2002  | 05/27/2003 | PROGRAMMING WITH FLOATING SOURCE FOR LOW POWER, LOW LEAKAGE AND HIGH DENSITY FLASH MEMORY DEVICES                                  |
| 6,646,462             | H0055US                   | United States | 06/24/2002  | 11/11/2003 | EXTRACTION OF DRAIN JUNCTION OVERLAP WITH THE GATE AND THE CHANNEL LENGTH FOR ULTRA-SMALL CMOS DEVICES WITH ULTRA-THIN GATE OXIDES |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                            |
|-----------------------|---------------------------|---------------|-------------|------------|----------------------------------------------------------------------------------------------------------------------------------|
| 6,754,106             | H0062US                   | United States | 09/16/2002  | 06/22/2004 | REFERENCE CELL WITH VARIOUS LOAD CIRCUITS COMPENSATING FOR SOURCE SIDE LOADING EFFECTS IN A NON-VOLATILE MEMORY                  |
| 6,828,623             | H0068US                   | United States | 08/30/2002  | 12/07/2004 | FLOATING GATE MEMORY DEVICE WITH HOMOGENEOUS OXINITRIDE TUNNELING DIELECTRIC                                                     |
| 6,991,987             | H0069US                   | United States | 11/27/2002  | 01/31/2006 | A METHOD FOR PRODUCING A LOW DEFECT HOMOGENEOUS OXINITRIDE                                                                       |
| 6,822,259             | H0070US                   | United States | 04/19/2002  | 11/23/2004 | METHOD OF DETECTING AND DISTINGUISHING STACK GATE EDGE DEFECTS AT THE SOURCE OR DRAIN JUNCTION                                   |
| 6,864,106             | H0071US                   | United States | 08/12/2002  | 03/08/2005 | METHOD AND SYSTEM FOR DETECTING TUNNEL OXIDE ENCROACHMENT ON A MEMORY DEVICE                                                     |
| 6,696,331             | H0176US                   | United States | 08/12/2002  | 02/24/2004 | METHOD OF PROTECTING A STACKED GATE STRUCTURE DURING FABRICATION                                                                 |
| 6,583,009             | H0184US                   | United States | 06/24/2002  | 06/24/2003 | INNOVATIVE NARROW GATE FORMATION FOR FLOATING GATE FLASH TECHNOLOGY                                                              |
| 6,797,565             | H0185US                   | United States | 09/16/2002  | 09/28/2004 | METHODS FOR FABRICATING AND PLANARIZATION DUAL POLY SCALABLE SONOS FLASH MEMORY                                                  |
| 6,570,211             | H0187US                   | United States | 06/26/2002  | 05/27/2003 | 2BIT/CELL ARCHITECTURE FOR FLOATING GATE FLASH MEMORY PRODUCT AND ASSOCIATED METHOD                                              |
| 6,716,698             | H0188US                   | United States | 09/10/2002  | 04/06/2004 | VIRTUAL GROUND SILICIDE BIT-LINE PROCESS FOR FLOATING GATE FLASH MEMORY                                                          |
| 6,809,402             | H0191US                   | United States | 08/14/2002  | 10/26/2004 | REFLOWABLE-DOPED HDP FILM                                                                                                        |
| 6,771,543             | H0198US                   | United States | 08/22/2002  | 08/03/2004 | A PRECHARGING SCHEME FOR READING A MEMORY CELL                                                                                   |
| 6,819,612             | H0201US                   | United States | 03/13/2003  | 11/16/2004 | APPARATUS AND METHOD FOR A SENSE AMPLIFIER CIRCUIT THAT SAMPLES AND HOLDS A REFERENCE VOLTAGE                                    |
| 6,784,061             | H0211US                   | United States | 06/25/2002  | 08/31/2004 | A PROCESS TO IMPROVE THE V <sub>SS</sub> LINE FORMATION FOR HIGH DENSITY FLASH MEMORY AND RELATED STRUCTURE ASSOCIATED THEREWITH |
| 6,808,945             | H0224US                   | United States | 01/08/2003  | 10/26/2004 | METHOD AND SYSTEM FOR TESTING TUNNEL OXIDE ON A MEMORY-RELATED STRUCTURE                                                         |
| 11/000,685            | H0290                     | United States | 12/01/2004  |            | POLYMER-BASED TRANSISTOR DEVICES, METHODS, AND SYSTEMS                                                                           |
| 6,847,047             | H0297US                   | United States | 11/04/2002  | 01/25/2005 | CONTROL OF MEMORY ARRAYS UTILIZING ZENER DIODE-LIKE DEVICES                                                                      |
| 11/194,207            | H0297US CIP               | United States | 08/01/2005  |            | THIN FILM DIODE CHARACTERISTICS FOR SELECTING NANOSCALE RESISTIVE MEMORY CELL IN MEMORY ARRAY                                    |
| 6,943,370             | H0297US CON               | United States | 06/30/2004  | 09/13/2005 | CONTROL OF MEMORY ARRAYS UTILIZING ZENER DIODE-LIKE DEVICES                                                                      |
| 7,499,309             | H0301US                   | United States | 04/02/2004  | 03/03/2009 | USING ORGANIC SEMICONDUCTOR MEMORY IN CONJUNCTION WITH A MEMS ACTUATOR                                                           |
| 7,273,766             | H0322US                   | United States | 01/12/2005  | 09/25/2007 | VARIABLE DENSITY AND VARIABLE PERSISTENT ORGANIC MEMORY DEVICES, METHODS, AND FABRICATION                                        |
| 10/951,375            | H0325US                   | United States | 09/28/2004  |            | CONTROL OF MEMORY DEVICES POSSESSING VARIABLE RESISTANCE CHARACTERISTICS                                                         |
| 7,443,710             | H0325US CON               | United States | 11/08/2004  | 10/28/2008 | CONTROL OF MEMORY DEVICES POSSESSING VARIABLE RESISTANCE CHARACTERISTICS                                                         |
| 6,803,267             | H0338US                   | United States | 07/07/2003  | 10/12/2004 | SILICON CONTAINING MATERIAL FOR PATTERNING POLYMERIC MEMORY ELEMENT                                                              |
| 6,798,068             | H0343US                   | United States | 11/26/2002  | 09/28/2004 | MOCVD FORMATION OF Cu <sub>2</sub> S                                                                                             |
| 6,746,971             | H0344US                   | United States | 12/05/2002  | 06/08/2004 | METHOD OF FORMING COPPER SULFIDE FOR MEMORY CELL                                                                                 |
| 10/817,131            | H0346US                   | United States | 04/02/2004  |            | IN-SITU SURFACE TREATMENT FOR MEMORY CELL FORMATION                                                                              |
| 6,982,188             | H0350US                   | United States | 12/03/2003  | 01/03/2006 | PATTERN RECOGNITION AND METROLOGY STRUCTURE FOR AN X-INITIATIVE LAYOUT DESIGN                                                    |
| 6,656,763             | H0354US                   | United States | 03/10/2003  | 12/02/2003 | SPIN ON POLYMERS FOR ORGANIC MEMORY DEVICES                                                                                      |
| 6,686,263             | H0362US                   | United States | 12/09/2002  | 02/03/2004 | SELECTIVE FORMATION OF TOP MEMORY ELECTRODE BY ELECTROLESS FORMATION OF CONDUCTIVE MATERIALS                                     |
| 7,608,855             | H0368US                   | United States | 04/02/2004  | 10/27/2009 | POLYMER DIELECTRICS FOR ME ARRAY INTERN CONNECT                                                                                  |
| 6,836,398             | H0374US                   | United States | 10/31/2002  | 12/28/2004 | SYSTEM AND METHOD OF FORMING A PASSIVE LAYER BY A CMP PROCESS                                                                    |
| 6,773,954             | H0376US                   | United States | 12/05/2002  | 08/10/2004 | METHODS OF FORMING PASSIVE LAYERS IN ORGANIC MEMORY CELLS                                                                        |
| 7,323,418             | H0383US                   | United States | 04/08/2005  | 01/29/2008 | ETCH-BACK PROCESS FOR CAPPING A POLYMER MEMORY DEVICE                                                                            |
| 7,220,985             | H0385US                   | United States | 12/09/2002  | 05/22/2007 | SELF ALIGNED MEMORY ELEMENT AND WORDLINE                                                                                         |
| 7,645,632             | H0385US DIV               | United States | 05/18/2007  | 01/12/2010 | SELF ALIGNED MEMORY ELEMENT AND WORDLINE                                                                                         |
| 6,825,060             | H0389US                   | United States | 04/02/2003  | 11/30/2004 | PHOTOSENSITIVE POLYMERIC MEMORY ELEMENTS                                                                                         |
| 6,878,961             | H0389US DIV               | United States | 09/28/2004  | 04/12/2005 | PHOTOSENSITIVE POLYMERIC MEMORY ELEMENTS                                                                                         |
| 6,900,488             | H0390US                   | United States | 10/31/2002  | 05/31/2005 | MULTI-CELL ORGANIC MEMORY ELEMENT AND METHODS OF OPERATING AND FABRICATING                                                       |
| 6,955,939             | H0398US                   | United States | 11/03/2003  | 10/18/2005 | MEMORY ELEMENT FORMATION WITH PHOTSENSITIVE POLYMER DIELECTRIC                                                                   |
| 7,374,654             | H0400US                   | United States | 11/01/2004  | 05/20/2008 | METHOD OF MAKING AN ORGANIC MEMORY CELL                                                                                          |
| 7,115,440             | H0406US                   | United States | 10/01/2004  | 10/03/2006 | SO <sub>2</sub> TREATMENT OF OXIDIZED CuO FOR COPPER SULFIDE FORMATION OF MEMORY ELEMENT GROWTH                                  |
| 7,015,504             | H0416US                   | United States | 11/03/2003  | 03/21/2006 | SIDEWELL FORMATION FOR HIGH DENSITY POLYMER MEMORY ELEMENT ARRAY                                                                 |
| 6,936,545             | H0421US                   | United States | 10/01/2003  | 08/30/2005 | ORGANIC MEMORY CELL FORMATION ON Ag SUBSTRATE                                                                                    |
| 6,787,458             | H0422US                   | United States | 07/07/2003  | 09/07/2004 | POLYMER MEMORY DEVICE FORMED IN VIA OPENING                                                                                      |
| 6,852,586             | H0423US                   | United States | 10/01/2003  | 02/08/2005 | SELF ASSEMBLY OF CONDUCTING POLYMER FOR FORMATION OF POLYMER MEMORY CELL                                                         |
| 6,893,895             | H0424US                   | United States | 07/07/2004  | 05/17/2005 | CUS FORMATION BY ANODIC SULFIDE PASSIVATION OF CU SURFACE                                                                        |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                 |
|-----------------------|---------------------------|---------------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------------------|
| 7,012,013             | H0430US                   | United States | 12/03/2003  | 03/14/2006 | DIELECTRIC PATTERN FORMATION FOR ORGANIC ELECTRONIC DEVICES                                                                           |
| 6,753,247             | H0432US                   | United States | 10/31/2002  | 06/22/2004 | MEMORY CELL FORMATION WITH PROCESS FOR PATTERNING CONDUCTING POLYMER FILMS                                                            |
| 6,770,905             | H0433US                   | United States | 12/05/2002  | 08/03/2004 | IMPLANTATION FOR THE FORMATION OF CUX LAYER IN AN ORGANIC MEMORY DEVICE                                                               |
| 6,870,183             | H0434US                   | United States | 11/04/2002  | 03/22/2005 | STACKED ORGANIC MEMORY DEVICES AND METHODS OF OPERATING AND FABRICATING                                                               |
| 6,979,837             | H0434US CON               | United States | 05/19/2004  | 12/27/2005 | STACKED ORGANIC MEMORY DEVICES AND METHODS OF OPERATING AND FABRICATING                                                               |
| 7,465,956             | H0434US CON               | United States | 10/17/2005  | 12/16/2008 | STACKED ORGANIC MEMORY DEVICES AND METHODS OF OPERATING AND FABRICATING                                                               |
| 8,003,436             | H0434US DIV               | United States | 12/03/2008  | 08/23/2011 | STACKED ORGANIC MEMORY DEVICES AND METHODS OF OPERATING AND FABRICATING                                                               |
| 8,044,387             | H0435US                   | United States | 07/07/2004  | 10/25/2011 | SEMICONDUCTOR DEVICE BUILT ON PLASTIC SUBSTRATE                                                                                       |
| 6,977,389             | H0437US                   | United States | 06/02/2003  | 12/20/2005 | PLANAR POLYMER MEMORY DEVICE                                                                                                          |
| 8,012,673             | H0438US                   | United States | 03/01/2005  | 09/06/2011 | PROCESSING A COPOLYMER TO FORM A POLYMER MEMORY CELL                                                                                  |
| 7,632,706             | H0439US                   | United States | 10/21/2005  | 12/15/2009 | SYSTEM AND METHOD FOR PROCESSING AN ORGANIC MEMORY CELL                                                                               |
| 7,259,039             | H0442US                   | United States | 04/02/2004  | 08/21/2007 | MEMORY DEVICE AND METHODS OF USING AND MAKING THE DEVICE                                                                              |
| 60/485,699            | H0442US PROV              | United States | 07/09/2003  |            | ORGANIC MEMORY DEVICE AND METHODS OF USING AND MAKING THE DEVICE                                                                      |
| 6,960,783             | H0443US                   | United States | 05/13/2003  | 11/01/2005 | ERASING AND PROGRAMMING AN ORGANIC MEMORY DEVICE AND METHODS OF OPERATING AND FABRICATING                                             |
| 7,012,298             | H0444US                   | United States | 08/05/2002  | 03/14/2006 | NON-VOLATILE MEMORY DEVICE                                                                                                            |
| 60/390,116            | H0444US PROV              | United States | 06/21/2002  |            | NON-VOLATILE MEMORY DEVICE                                                                                                            |
| 6,917,068             | H0445US CIP               | United States | 06/05/2003  | 07/12/2005 | SEMICONDUCTOR DEVICE HAVING CONDUCTIVE STRUCTURES FORMED NEAR A GATE ELECTRODE                                                        |
| 6,660,588             | H0462US                   | United States | 09/16/2002  | 12/09/2003 | HIGH DENSITY FLOATING GATE FLASH MEMORY AND FABRICATION PROCESSES THEREFOR                                                            |
| 6,812,514             | H0462US DIV               | United States | 09/10/2003  | 11/02/2004 | HIGH DENSITY FLOATING GATE FLASH MEMORY AND FABRICATION PROCESSES THEREFOR                                                            |
| 6,894,473             | H0474US                   | United States | 03/05/2003  | 05/17/2005 | FAST BANDGAP REFERENCE CIRCUIT FOR USE IN A LOW POWER SUPPLY A/D BOOSTER                                                              |
| 6,885,590             | H0496US                   | United States | 01/14/2003  | 04/26/2005 | MEMORY DEVICE HAVING A P+ GATE AND THIN BOTTOM OXIDE AND METHOD OF ERASING SAME                                                       |
| 6,778,437             | H0502US                   | United States | 08/07/2003  | 08/17/2004 | MEMORY CIRCUIT FOR PROVIDING WORD LINE REDUNDANCY IN A MEMORY SECTOR                                                                  |
| 10/387,827            | H0506                     | United States | 03/12/2003  |            | A METHOD FOR REDUCING SERIES RESISTANCE IN A FLASH MEMORY ARRAY                                                                       |
| 6,751,146             | H0511US                   | United States | 01/07/2003  | 06/15/2004 | SYSTEM AND METHOD FOR CHARGE RESTORATION IN A NON-VOLATILE MEMORY DEVICE                                                              |
| 7,020,022             | H0513US                   | United States | 07/09/2004  | 03/28/2006 | METHOD OF REFERENCE CELL DESIGN FOR OPTIMIZED MEMORY CIRCUIT YIELD                                                                    |
| 6,867,119             | H0514US                   | United States | 10/30/2002  | 03/15/2005 | NITROGEN OXIDATION TO REDUCE ENCROACHMENT                                                                                             |
| 6,878,589             | H0515US                   | United States | 05/06/2003  | 04/12/2005 | METHOD AND SYSTEM FOR IMPROVING SHORT CHANNEL EFFECT ON A FLOATING GATE DEVICE                                                        |
| 6,939,766             | H0517US                   | United States | 07/09/2003  | 09/06/2005 | A METHOD FOR FABRICATING A FLASH MEMORY DEVICE                                                                                        |
| 10/408,000            | H0519                     | United States | 04/03/2003  |            | METHOD FOR FORMING SOURCE AND DRAIN REGIONS TO REDUCE SHORT-CHANNEL EFFECTS IN NON-VOLATILE MEMORY DEVICE FABRICATION                 |
| 6,833,297             | H0520US                   | United States | 10/04/2002  | 12/21/2004 | METHOD FOR REDUCING DRAIN INDUCED BARRIER LOWERING IN A MEMORY DEVICE                                                                 |
| 6,937,518             | H0523US                   | United States | 07/10/2003  | 08/30/2005 | PROGRAMMING OF A FLASH MEMORY CELL                                                                                                    |
| 6,897,518             | H0534US                   | United States | 07/10/2003  | 05/24/2005 | FLASH MEMORY CELL HAVING REDUCED LEAKAGE CURRENT                                                                                      |
| 6,888,763             | H0539US                   | United States | 02/04/2003  | 05/03/2005 | COMPENSATED OSCILLATOR CIRCUIT FOR CHARGE PUMPS                                                                                       |
| 10/636,846            | H0540US                   | United States | 08/06/2003  |            | APPARATUS AND METHOD FOR BOOSTING A PASS GATE PUMP FOR A FLASH MEMORY                                                                 |
| 7,116,154             | H0541US                   | United States | 08/06/2003  | 10/03/2006 | LOW POWER CHARGE PUMP                                                                                                                 |
| 7,067,381             | H0542US                   | United States | 08/06/2003  | 06/27/2006 | STRUCTURE AND METHOD TO REDUCE DRAIN INDUCED BARRIER LOWERING                                                                         |
| 7,109,555             | H0544US                   | United States | 04/28/2004  | 09/19/2006 | METHOD FOR PROVIDING SHORT CHANNEL EFFECT CONTROL USING A SILICIDE VSS LINE                                                           |
| 6,908,816             | H0545US                   | United States | 10/28/2003  | 06/21/2005 | METHOD FOR FORMING A DIELECTRIC SPACER IN A NON-VOLATILE MEMORY DEVICE                                                                |
| 7,009,271             | H0546US                   | United States | 04/13/2004  | 03/07/2006 | A MEMORY DEVICE WITH AN ALTERNATING V <sub>ss</sub> INTERCONNECTION                                                                   |
| 8,530,977             | H0548US                   | United States | 06/27/2003  | 09/10/2013 | AN APPARATUS AND METHOD FOR A METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR WITH SOURCE SIDE PUNCH-THROUGH PROTECTION IMPLANT     |
| 8,633,083             | H0548US DIV               | United States | 08/12/2013  | 01/21/2014 | APPARATUS AND METHOD FOR A METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR WITH SOURCE SIDE PUNCH-THROUGH PROTECTION IMPLANT        |
| 6,939,770             | H0552US                   | United States | 07/11/2003  | 09/06/2005 | METHOD OF FABRICATING SEMICONDUCTOR DEVICE HAVING TRIPLE LDD STRUCTURE AND LOWER GATE RESISTANCE FORMED WITH A SINGLE IMPLANT PROCESS |
| 7,084,458             | H0552US DIV               | United States | 05/02/2005  | 08/01/2006 | SEMICONDUCTOR DEVICE HAVING TRIPLE LDD STRUCTURE AND LOWER GATE RESISTANCE FORMED WITH A SINGLE IMPLANT PROCESS                       |
| 7,011,998             | H0554US                   | United States | 01/12/2004  | 03/14/2006 | A HIGH VOLTAGE TRANSISTOR SCALING TILT ION IMPLANT SYSTEM AND METHOD                                                                  |

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| PATENT OR APPL<br>NO. | SPANION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                     |
|-----------------------|--------------------------|---------------|-------------|------------|---------------------------------------------------------------------------------------------------------------------------|
| 7,026,230             | H0558US                  | United States | 09/11/2003  | 04/11/2006 | A METHOD FOR FABRICATING A MEMORY DEVICE                                                                                  |
| 7,414,281             | H0561US                  | United States | 09/09/2003  | 08/19/2008 | FLASH MEMORY WITH HIGH-K DIELECTRIC BETWEEN SUBSTRATE AND GATE                                                            |
| 6,961,267             | H0562US                  | United States | 12/16/2003  | 11/01/2005 | METHOD AND DEVICE FOR PROGRAMMING CELLS IN A MEMORY ARRAY IN A NARROW DISTRIBUTION                                        |
| 7,288,809             | H0563US                  | United States | 12/16/2003  | 10/30/2007 | FLASH MEMORY WITH BURIED BIT LINES                                                                                        |
| 6,950,344             | H0564US                  | United States | 11/24/2003  | 09/27/2005 | READING FLASH MEMORY                                                                                                      |
| 6,819,615             | H0565US                  | United States | 10/31/2002  | 11/16/2004 | MEMORY DEVICE HAVING RESISTIVE ELEMENT COUPLED TO REFERENCE CELL FOR IMPROVED RELIABILITY                                 |
| 10/358,496            | H0567                    | United States | 02/04/2003  |            | TRANSISTOR FABRICATION METHOD WITH LDD IMPLANT AFTER SPACER FORMATION                                                     |
| 6,795,342             | H0570                    | United States | 07/24/2003  | 12/05/2007 | SYSTEM FOR PROGRAMMING A NON-VOLATILE MEMORY CELL                                                                         |
| 6,795,357             | H0570US                  | United States | 10/30/2002  | 09/21/2004 | IMPROVED METHOD FOR READING A NON-VOLATILE MEMORY CELL                                                                    |
| 6,788,583             | H0575US                  | United States | 12/02/2002  | 09/07/2004 | PRE-CHARGE METHOD FOR READING A NON-VOLATILE MEMORY CELL                                                                  |
| 6,911,704             | H0576US                  | United States | 10/14/2003  | 06/28/2005 | MEMORY CELL ARRAY WITH STAGGERED LOCAL INTERCONNECT STRUCTURE                                                             |
| 6,965,143             | H0577US                  | United States | 10/10/2003  | 11/15/2005 | RECESS CHANNEL FLASH ARCHITECTURE FOR REDUCED SHORT CHANNEL EFFECT                                                        |
| 6,744,675             | H0585US                  | United States | 11/26/2002  | 06/01/2004 | PROGRAM ALGORITHM INCLUDING SOFT ERASE FOR SONOS MEMORY DEVICE                                                            |
| 6,956,768             | H0587US                  | United States | 04/15/2003  | 10/18/2005 | METHOD OF PROGRAMMIN DUAL CELL MEMORY DEVICE TO STORE MULTIPLE DATA STATES PER CELL                                       |
| 6,778,442             | H0588US                  | United States | 04/24/2003  | 08/17/2004 | METHOD OF DUAL CELL MEMORY DEVICE OPERATION FOR IMPROVED END-OF-LIFE READ MARGIN                                          |
| 6,775,187             | H0589US                  | United States | 04/24/2003  | 08/10/2004 | METHOD OF PROGRAMMING A DUAL CELL MEMORY DEVICE                                                                           |
| 6,735,114             | H0591US                  | United States | 02/04/2003  | 05/11/2004 | METHOD OF IMPROVING DYNAMIC REFERENCE TRACKING FOR FLASH MEMORY UNIT                                                      |
| 6,868,014             | H0599US                  | United States | 05/06/2003  | 03/15/2005 | MEMORY DEVICE WITH REDUCED OPERATING VOLTAGE HAVING DIELECTRIC STACK                                                      |
| 6,894,932             | H0600US                  | United States | 11/18/2003  | 05/17/2005 | DUAL CELL MEMORY DEVICE HAVING A TOP DIELECTRIC STACK                                                                     |
| 7,151,292             | H0609US                  | United States | 01/15/2003  | 12/19/2006 | DIELECTRIC MEMORY CELL STRUCTURE WITH COUNTER DOPED CHANNEL REGION                                                        |
| 6,768,673             | H0620US                  | United States | 04/24/2003  | 07/27/2004 | METHOD OF PROGRAMMING AND READING A DUAL CELL MEMORY DEVICE                                                               |
| 6,822,909             | H0622US                  | United States | 04/24/2003  | 11/23/2004 | METHOD OF CONTROLLING PROGRAM THERESHOLD VOLTAGE DISTRIBUTION OF A DUAL CELL MEMORY DEVICE                                |
| 6,771,545             | H0625US                  | United States | 01/29/2003  | 08/03/2004 | IMPROVED METHOD FOR READING A NON-VOLATILE MEMORY CELL ADJACENT TO AN INACTIVE REGION OF A NON-VOLATILE MEMORY CELL ARRAY |
| 6,967,873             | H0626US                  | United States | 10/02/2003  | 11/22/2005 | MEMORY DEVICE AND METHOD USING POSITIVE GATE STRESS TO RECOVER OVERERASED CELL                                            |
| 6,862,221             | H0628US                  | United States | 06/11/2003  | 03/01/2005 | MEMORY DEVICE HAVING A THIN TOP DIELECTRIC AND METHOD OF ERASING SAME                                                     |
| 6,735,124             | H0629US                  | United States | 12/10/2002  | 05/11/2004 | FLASH MEMORY DEVICE HAVING FOUR-BIT CELL                                                                                  |
| 6,927,129             | H0630US                  | United States | 04/08/2004  | 08/09/2005 | NARROW WIDE SPACER                                                                                                        |
| 7,070,911             | H0631US                  | United States | 01/23/2003  | 07/04/2006 | A STRUCTURE AND METHOD FOR REDUCING STANDING WAVES IN A PHOTORESIST                                                       |
| 7,078,314             | H0632US                  | United States | 04/03/2003  | 07/18/2006 | MEMORY DEVICE HAVING IMPROVED PERIPHERY AND CORE ISOLATION                                                                |
| 6,943,401             | H0634US                  | United States | 09/11/2003  | 09/13/2005 | A FLASH MEMORY CELL DRAIN AND SOURCE FABRICATION SYSTEM AND METHOD                                                        |
| 6,919,247             | H0635US                  | United States | 09/04/2003  | 07/19/2005 | METHOD OF FABRICATING A FLOATING GATE                                                                                     |
| 7,217,964             | H0636US                  | United States | 09/09/2003  | 05/15/2007 | METHOD AND APPARATUS FOR COUPLING TO A SOURCE LINE IN A MEMORY DEVICE                                                     |
| 7,361,587             | H0637US                  | United States | 09/02/2004  | 04/22/2008 | SEMICONDUCTOR CONTACT AND NITRIDE SPACER FORMATION SYSTEM AND METHOD                                                      |
| 7,572,727             | H0638US                  | United States | 09/02/2004  | 08/11/2009 | A SEMICONDUCTOR CONTACT FORMATION SYSTEM AND METHOD                                                                       |
| 7,977,797             | H0638US DIV              | United States | 08/11/2009  | 07/12/2011 | INTEGRATED CIRCUIT WITH CONTACT REGION AND MULTIPLE ETCH STOP INSULATION LAYER                                            |
| 6,867,063             | H0639US                  | United States | 09/30/2002  | 03/15/2005 | ORGANIC SPIN-ON ANTI-REFLECTIVE COATING OVER INORGANIC ANTI-REFLECTIVE COATING                                            |
| 10/721,433            | H0641US                  | United States | 11/24/2003  |            | DUAL POLYSILICON STRUCTURE WITH NARROW SPACING                                                                            |
| 7,323,726             | H0642US                  | United States | 09/09/2003  | 01/29/2008 | METHOD AND APPARATUS FOR COUPLING TO A COMMON LINE IN AN ARRAY                                                            |
| 6,774,432             | H0671US                  | United States | 02/05/2003  | 08/10/2004 | UV BLOCKING LAYER FOR REDUCING UV-INDUCED CHARGING OF SONOS DUAL-BIT FLASH MEMORY DEVICES IN BEOL PROCESSING              |
| 7,018,896             | H0671US DIV1             | United States | 04/05/2004  | 03/28/2006 | UV BLOCKING LAYER FOR REDUCING UV-INDUCED CHARGING OF SONOS DUAL-BIT FLASH MEMORY DEVICES IN BEOL PROCESSING              |
| 6,989,563             | H0672US                  | United States | 02/02/2004  | 01/24/2006 | IMPROVED CONTACT INTEGRATION AND ENHANCED INTERLEVEL DIELECTRIC CHEMICAL MECHANICAL POLISHING PROCESS                     |
| 7,091,088             | H0675US                  | United States | 06/03/2004  | 08/15/2006 | UV-BLOCKING ETCH STOP LAYER FOR REDUCING UV-INDUCED CHARGING OF CHARGE STORAGE LAYER IN MEMORY DEVICES IN BEOL PROCESSING |
| 7,118,967             | H0677US                  | United States | 02/19/2003  | 10/10/2006 | PROTECTION OF CHARGE TAPPING DIELECTRIC FLASH MEMORY DEVICES FROM UV-INDUCED CHARGING IN BEOL PROCESSING                  |
| 6,933,219             | H0680US                  | United States | 11/18/2003  | 08/23/2005 | TIGHTLY SPACED GATE FORMATION THROUGH DAMASCENE PROCESS                                                                   |
| 7,881,142             | H0685US                  | United States | 09/30/2005  | 02/01/2011 | STORAGE DEVICE AND CONTROL METHOD THEREOF                                                                                 |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                            |
|-----------------------|--------------------------|---------------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 13/313,699            | H0685US DIV              | United States | 12/07/2011  |            | HIGH SPEED SERIAL PERIPHERAL INTERFACE MEMORY SUBSYSTEM                                                                                          |
| 10/619,804            | H0686                    | United States | 07/14/2003  |            | PROCESS FOR CORE AND PERIPHERY MASKING WITH TRANSISTOR SPACER AND SMALL CORE SPACE FORMATION                                                     |
| 6,835,662             | H0688US                  | United States | 07/14/2003  | 12/28/2004 | PARTIALLY DE-COUPLED CORE AND PERIPHERY GATE MODULE PROCESS                                                                                      |
| 6,855,608             | H0696US                  | United States | 06/17/2003  | 02/15/2005 | METHOD OF FABRICATING A PLANAR STRUCTURE TRAPPING MEMORY CELL ARRAY WITH RECTANGULAR GATES AND REDUCED BIT LINE RESISTANCE                       |
| 6,927,145             | H0697US                  | United States | 02/02/2004  | 08/09/2005 | BITLINE HARD MASK SPACER FLOW FOR MEMORY CELL SCALING                                                                                            |
| 7,018,868             | H0698US                  | United States | 02/02/2004  | 03/28/2006 | DISPOSABLE HARD MASK FOR MEMORY BITLINE SCALING                                                                                                  |
| 10/790,369            | H0700                    | United States | 03/01/2004  |            | METHOD OF FORMING SMALL PITCH STRING CONTACTS WITH DIPLE ILLUMINATION                                                                            |
| 7,060,564             | H0709US                  | United States | 08/06/2003  | 06/13/2006 | MEMORY DEVICE AND METHOD OF SIMULTANEOUS FABRICATION OF CORE AND PERIPHERY OF SAME                                                               |
| 6,963,108             | H0712US                  | United States | 10/10/2003  | 11/08/2005 | RECESSED CHANNEL                                                                                                                                 |
| 6,744,105             | H0715US                  | United States | 03/05/2003  | 06/01/2004 | MEMORY ARRAY HAVING SHALLOW BIT LINE WITH SILICIDE CONTACT PORTION AND METHOD OF FORMATION                                                       |
| 6,987,048             | H0718US                  | United States | 08/06/2003  | 01/17/2006 | MEMORY DEVICE HAVING SILICIDE BITLINE AND METHOD OF FORMING THE SAME                                                                             |
| 6,768,160             | H0726US                  | United States | 01/28/2003  | 07/27/2004 | NON-VOLATILE MEMORY CELL AND METHOD OF PROGRAMMING FOR IMPROVED DATA RETENTION                                                                   |
| 6,903,407             | H0742US                  | United States | 10/14/2003  | 06/07/2005 | TRAPPING DIELECTRIC MEMORY CELL STRUCTURE WITH GATE HOLE INJECTION ERASE                                                                         |
| 6,858,450             | H0750US                  | United States | 11/05/2002  | 02/22/2005 | METHOD OF ALTERNATING GROUNDED/FLOATING POLY LINES TO MONITOR SHORTS                                                                             |
| 6,828,607             | H0753US                  | United States | 12/09/2002  | 12/07/2004 | DISCONTINUOUS NITRIDE STRUCTURE FOR NON-VOLATILE TRANSISTORS                                                                                     |
| 10/460,810            | H0789                    | United States | 06/11/2003  |            | A MULTIPLE VT BITMAP TECHNIQUE FOR MEMORY TECHNOLOGIES                                                                                           |
| 10/460,029            | H0795                    | United States | 06/11/2003  |            | FLASH THRESHOLD VOLTAGE DISTRIBUTION CHARACTERIZATION FOR APPLICATION OF ERASE ALGORITHM GENERATION IN INTEGRATED CIRCUIT TECHNOLOGY DEVELOPMENT |
| 6,709,924             | H1087US                  | United States | 11/12/2002  | 03/23/2004 | FABRICATION OF SHALLOW TRENCH ISOLATION STRUCTURES WITH ROUNDED CORNER AND SELF-ALIGNED GATE                                                     |
| 6,767,791             | H1090US                  | United States | 02/10/2003  | 07/27/2004 | STRUCTURE AND METHOD FOR SUPPRESSING OXIDE ENCROACHMENT IN A FLOATING GATE MEMORY CELL                                                           |
| 6,737,701             | H1098US                  | United States | 12/05/2002  | 05/18/2004 | STRUCTURE AND METHOD FOR REDUCING CHARGE LOSS IN A MEMORY CELL                                                                                   |
| 7,196,372             | H1130US                  | United States | 07/08/2003  | 03/27/2007 | FLASH MEMORY DEVICE                                                                                                                              |
| 10/632,971            | H1156US                  | United States | 08/04/2003  |            | FINFET FLASH MEMORY                                                                                                                              |
| 6,747,900             | H1202US                  | United States | 01/21/2003  | 06/08/2004 | MEMORY CIRCUIT ARRANGEMENT FOR PROGRAMMING A MEMORY CELL                                                                                         |
| 6,768,677             | H1203US                  | United States | 11/22/2002  | 07/27/2004 | CASCADE AMPLIFIER CIRCUIT FOR PRODUCING A FAST, STABLE AND ACCURATE BITLINE VOLTAGE                                                              |
| 6,768,679             | H1204US                  | United States | 02/10/2003  | 07/27/2004 | SELECTION CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS                                                                                            |
| 6,731,542             | H1205US                  | United States | 12/05/2002  | 05/04/2004 | CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS                                                                                                      |
| 6,781,417             | H1206US                  | United States | 10/29/2002  | 08/24/2004 | BUFFER DRIVER CIRCUIT FOR PRODUCING A FAST, STABLE AND ACCURATE REFERENCE VOLTAGE                                                                |
| 6,628,545             | H1209US                  | United States | 11/26/2002  | 09/30/2003 | MEMORY CIRCUIT FOR SUPPRESSING BIT LINE CURRENT LEAKAGE                                                                                          |
| 6,670,227             | H1348US                  | United States | 02/10/2003  | 12/30/2003 | METHOD FOR FABRICATING DEVICES IN CORE AND PERIPHERY SEMICONDUCTOR REGIONS USING DUAL SPACERS                                                    |
| 7,023,046             | H1355US                  | United States | 07/11/2003  | 04/04/2006 | UNDOPED OXIDE LINER/BPSG FOR IMPROVED DATA RETENTION                                                                                             |
| 6,765,827             | H1356US                  | United States | 03/10/2003  | 07/20/2004 | METHOD AND SYSTEM FOR DETECTING DEFECTIVE MATERIAL SURROUNDING FLASH MEMORY CELLS                                                                |
| 7,073,104             | H1357US                  | United States | 03/10/2003  | 07/04/2006 | METHOD AND SYSTEM FOR APPLYING TESTING VOLTAGE SIGNAL                                                                                            |
| 7,060,554             | H1368US                  | United States | 07/11/2003  | 06/13/2006 | PECVD SILICON-RICH OXIDE LAYER FOR REDUCED UV CHARGING                                                                                           |
| 6,869,844             | H1369US                  | United States | 11/05/2003  | 03/22/2005 | METHOD AND STRUCTURE FOR PROTECTING NROM DEVICES FROM INDUCED CHARGE DAMAGE DURING DEVICE FABRICATION                                            |
| 6,717,850             | H1371US                  | United States | 12/05/2002  | 04/06/2004 | AN EFFICIENT METHOD TO DETECT PROCESS INDUCED DEFECTS IN THE GATE STACK OF FLASH MEMORY DEVICES                                                  |
| 6,797,650             | H1373US                  | United States | 01/14/2003  | 09/28/2004 | FLASH MEMORY DEVICES WITH OXYNITRIDE DIELECTRIC AS THE CHARGE STORAGE MEDIA                                                                      |
| 7,067,388             | H1375US                  | United States | 04/07/2004  | 06/27/2006 | A FLASH MEMORY DEVICE AND METHOD OF FORMING THE SAME WITH IMPROVED GATE BREAKDOWN AND ENDURANCE                                                  |
| 8,093,646             | H1375US DIV              | United States | 05/12/2006  | 01/10/2012 | A FLASH MEMORY DEVICE AND METHOD OF FORMING THE SAME WITH IMPROVED GATE BREAKDOWN AND ENDURANCE                                                  |
| 7,078,749             | H1409US                  | United States | 07/11/2003  | 07/18/2006 | MEMORY STRUCTURE HAVING TUNABLE INTERLAYER DIELECTRIC AND METHOD FOR FABRICATING SAME                                                            |
| 6,963,104             | H1414US                  | United States | 06/12/2003  | 11/08/2005 | NON-VOLATILE MEMORY DEVICE                                                                                                                       |
| 6,933,558             | H1415US                  | United States | 12/04/2003  | 08/23/2005 | FLASH MEMORY DEVICE                                                                                                                              |
| 6,958,512             | H1489US                  | United States | 02/03/2004  | 10/25/2005 | NON-VOLATILE MEMORY DEVICE                                                                                                                       |
| 7,279,735             | H1499US                  | United States | 05/05/2004  | 10/09/2007 | FLASH MEMORY DEVICE                                                                                                                              |
| 10/929,538            | H1500US                  | United States | 08/31/2004  |            | NON-VOLATILE MEMORY DEVICE                                                                                                                       |
| 6,744,674             | H1513US                  | United States | 03/13/2003  | 06/01/2004 | CIRCUIT FOR FAST AND ACCURATE MEMORY READ OPERATIONS                                                                                             |
| 10/733,435            | H1515                    | United States | 12/10/2003  |            | METHOD FOR INCREASING RELIABILITY OF A FLOATING GATE MEMORY DEVICE AND RELATED STRUCTURE                                                         |
| 6,897,476             | H1518US                  | United States | 08/07/2003  | 05/24/2005 | TEST STRUCTURE FOR DETERMINING ELECTROMIGRATION AND INTERLAYER DIELECTRIC FAILURE                                                                |
| 6,900,124             | H1631US                  | United States | 09/03/2003  | 05/31/2005 | PATTERNING FOR ELLIPTICAL V <sub>SS</sub> CONTACT ON FLASH MEMORY                                                                                |
| 7,018,922             | H1631US CON              | United States | 10/19/2004  | 03/28/2006 | PATTERNING FOR ELONGATED V <sub>SS</sub> CONTACT ON FLASH MEMORY                                                                                 |
| 6,998,677             | H1807US                  | United States | 03/08/2004  | 02/14/2006 | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE                                                                                                |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                        |
|-----------------------|---------------------------|---------------|-------------|------------|--------------------------------------------------------------------------------------------------------------|
| 7,026,843             | H1813US                   | United States | 01/16/2004  | 04/11/2006 | FLEXIBLE CASCODE AMPLIFIER CIRCUIT WITH HIGH GAIN FOR FLASH<br>MEMORY CELLS                                  |
| 10/705,346            | H1817                     | United States | 11/08/2003  |            | FLASH MEMORY DEVICE AND METHOD FOR SECURE ACCESS TO<br>PROTECTED DATA                                        |
| 7,211,473             | H1859US                   | United States | 01/12/2004  | 05/01/2007 | METHOD AND STRUCTURE FOR CONTROLLING FLOATING BODY<br>EFFECTS                                                |
| 10/789,520            | H1861                     | United States | 02/27/2004  |            | METHOD AND SYSTEM FOR INTEGRATED CIRCUIT PROGRESSIVE<br>RAMP FLASH ANNEAL                                    |
| 6,992,370             | H1862US                   | United States | 09/04/2003  | 01/31/2006 | MEMORY CELL STRUCTURE HAVING NITRIDE LAYER WITH REDUCED<br>CHARGE LOSS AND METHOD FOR FABRICATING SAME       |
| 6,825,526             | H1878US                   | United States | 01/16/2004  | 11/30/2004 | STRUCTURE FOR INCREASING DRIVE CURRENT IN A MEMORY ARRAY<br>AND RELATED METHOD                               |
| 6,963,506             | H1879US                   | United States | 10/03/2003  | 11/08/2005 | CIRCUIT AND TECHNIQUE FOR ACCURATELY SENSING LOW VOLTAGE<br>FLASH MEMORY DEVICES                             |
| 6,898,124             | H1880US                   | United States | 10/03/2003  | 05/24/2005 | EFFICIENT AND ACCURATE SENSING CIRCUIT AND TECHNIQUE FOR<br>LOW VOLTAGE FLASH MEMORY DEVICES                 |
| 6,798,275             | H1892US                   | United States | 04/03/2003  | 09/28/2004 | FAST, ACCURATE AND LOW POWER SUPPLY VOLTAGE BOOSTER<br>USING A/D CONVERTER                                   |
| 6,841,841             | H1928US                   | United States | 12/05/2003  | 01/11/2005 | NEUTRON DETECTING DEVICE                                                                                     |
| 6,958,271             | H1930US                   | United States | 08/04/2003  | 10/25/2005 | DUAL-LEVEL STACKED FLASH MEMORY CELL WITH A MOSFET<br>STORAGE TRANSISTOR                                     |
| 7,339,226             | H1930US DIV               | United States | 06/16/2005  | 03/04/2008 | DUAL-LEVEL STACKED FLASH MEMORY CELL WITH A MOSFET<br>STORAGE TRANSISTOR                                     |
| 7,199,416             | H1934US                   | United States | 11/10/2004  | 04/03/2007 | SYSTEMS AND METHOD FOR A MEMORY AND/OR SELECTION<br>ELEMENT FORMED WITHIN A RECESS IN A METAL LINE           |
| 6,723,605             | H1970US                   | United States | 12/15/2001  | 04/20/2004 | METHOD FOR MANUFACTURING MEMORY WITH HIGH CONDUCTIVITY<br>BITLINE AND SHALLOW TRENCH ISOLATION INTEGRATION   |
| 6,855,977             | H1971                     | United States | 05/07/2002  | 02/15/2005 | MEMORY DEVICE WITH A SELF-ASSEMBLED POLYMER FILM AND<br>METHOD OF MAKING THE SAME                            |
| 60/289,054            | H1971                     | United States | 05/07/2001  |            | SELF-ASSEMBLING MEMORY DEVICE                                                                                |
| 7,295,461             | H1971US CON               | United States | 10/04/2004  | 11/13/2007 | MEMORY DEVICE WITH A SELF-ASSEMBLED POLYMER FILM AND<br>METHOD OF MAKING THE SAME                            |
| 6,873,540             | H1972                     | United States | 05/07/2002  | 03/29/2005 | COMPOSITE MOLECULAR SWITCHING DEVICE                                                                         |
| 60/289,060            | H1972                     | United States | 05/07/2001  |            | COMPOSITE MOLECULAR SWITCHING DEVICE                                                                         |
| 7,113,420             | H1972US DIV               | United States | 01/12/2005  | 09/26/2006 | MOLECULAR MEMORY CELL                                                                                        |
| 6,627,944             | H1973                     | United States | 05/07/2002  | 09/30/2003 | FLOATING GATE MEMORY DEVICE USING COMPOSITE MOLECULAR<br>MATERIAL                                            |
| 60/289,091            | H1973                     | United States | 05/07/2001  |            | FLOATING GATE MEMORY DEVICE USING COMPOSITE MOLECULAR<br>MATERIAL                                            |
| 6,809,955             | H1975                     | United States | 05/07/2002  | 10/26/2004 | ADDRESSABLE AND ELECTRICALLY REVERSIBLE MEMORY SWITCH                                                        |
| 60/289,057            | H1975                     | United States | 05/07/2001  |            | ELECTRICALLY ADDRESSABLE MEMORY SWITCH                                                                       |
| 7,145,793             | H1975US CON               | United States | 06/21/2004  | 12/05/2006 | ELECTRICALLY ADDRESSABLE MEMORY SWITCH                                                                       |
| 6,781,868             | H1976                     | United States | 05/07/2002  | 08/24/2004 | MOLECULAR MEMORY DEVICE                                                                                      |
| 60/289,056            | H1976                     | United States | 05/07/2001  |            | ELECTRICALLY ADDRESSABLE MEMORY SWITCH WITH BUILT-IN<br>LEAKAGE CURRENT BARRIER                              |
| 7,157,750             | H1976US CON               | United States | 07/27/2004  | 01/02/2007 | MOLECULAR MEMORY DEVICE                                                                                      |
| 6,844,608             | H1977                     | United States | 05/07/2002  | 01/18/2005 | REVERSIBLE FIELD-PROGRAMMABLE ELECTRIC INTERCONNECTS                                                         |
| 60/289,061            | H1977                     | United States | 05/07/2001  |            | REVERSIBLY FIELD-PROGRAMMABLE ELECTRIC INTERCONNECTS                                                         |
| 7,183,141             | H1977US DIV               | United States | 12/30/2004  | 02/27/2007 | REVERSIBLE FIELD-PROGRAMMABLE ELECTRIC INTERCONNECTS                                                         |
| 7,012,276             | H1978                     | United States | 09/17/2002  | 03/14/2006 | ORGANIC THIN FILM ZENER DIODES                                                                               |
| 6,992,323             | H1979                     | United States | 08/13/2001  | 01/31/2006 | MEMORY CELL                                                                                                  |
| 6,962,849             | H1983US                   | United States | 12/05/2003  | 11/08/2005 | HARD MASK AND PACER FOR SUBLITHOGRAPHIC BITLINE                                                              |
| 7,160,773             | H1984US                   | United States | 05/05/2004  | 01/09/2007 | METHODS AND APPARATUS FOR WORDLINE PROTECTION IN FLASH<br>MEMORY DEVICES                                     |
| 6,958,272             | H1985US                   | United States | 01/12/2004  | 10/25/2005 | POCKET IMPLANT FOR COMPLEMENTARY BIT DISTURB<br>IMPROVEMENT AND CHARGING IMPROVEMENT OF SONOS MEMORY<br>CELL |
| 7,176,113             | H1986US                   | United States | 06/07/2004  | 02/13/2007 | LDC IMPLANT FOR MIRROR BIT TO IMPROVE VT ROLL OFF AND<br>FORMS SHARPER JUNCTION                              |
| 6,872,609             | H1987US                   | United States | 01/12/2004  | 03/29/2005 | NARROW BITLINE USING SAFIER FOR MIRROBIT                                                                     |
| 6,834,012             | H1988US                   | United States | 06/08/2004  | 12/21/2004 | MEMORY DEVICE AND METHODS OF USING NEGATIVE GATE STRESS<br>TO CORRECT OVER-ERASED MEMORY CELLS               |
| 6,934,190             | H1989US                   | United States | 06/09/2004  | 08/23/2005 | RAMP SOURCE HOT-HOLE PROGRAMMING FOR TRAP BASED<br>NONVOLATILE MEMORY DEVICES                                |
| 7,507,661             | H1990US                   | United States | 08/11/2004  | 03/24/2009 | METHOD OF FORMING NARROWLY SPACED FLASH MEMORY<br>CONTACT OPENINGS AND LITHOGRAPHY MASKS                     |
| 10/841,788            | H1991US                   | United States | 05/07/2004  |            | FLASH MEMORY CELL WITH THIN UPPER DIELECTRIC                                                                 |
| 7,120,063             | H1992US                   | United States | 05/07/2004  | 10/10/2006 | FLASH MEMORY CELL AND METHODS FOR PROGRAMMING AND<br>ERASING                                                 |
| 7,215,577             | H1992US DIV               | United States | 08/29/2006  | 05/08/2007 | FLASH MEMORY CELL AND METHODS FOR PROGRAMMING AND<br>ERASING                                                 |
| 6,989,320             | H1993US                   | United States | 05/11/2004  | 01/24/2006 | BITLINE IMPLANT UTILIZING DUAL POLY                                                                          |
| 7,020,021             | H1994US                   | United States | 11/04/2004  | 03/28/2006 | RAMPED SOFT PROGRAMMING FOR CONTROL OF ERASE VOLTAGE<br>DISTRIBUTIONS IN FLASH MEMORY DEVICES                |
| 7,142,455             | H1995US                   | United States | 05/04/2004  | 11/28/2006 | POSITIVE GATE STRESS DURING ERASE TO IMPROVE RETENTION IN<br>MULTY-LEVEL, NON-VOLATILE FLASH MEMORY          |
| 7,029,975             | H1996US                   | United States | 05/04/2004  | 04/18/2006 | METHOD AND APPARATUS FOR ELIMINATING WORD LINE BENDING BY<br>SOURCE SIDE IMPLANTATION                        |
| 7,272,060             | H1997US                   | United States | 12/01/2004  | 09/18/2007 | METHOD, SYSTEM, AND CIRCUIT FOR PERFORMING A MEMORY<br>RELATED OPERATION                                     |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                           |
|-----------------------|---------------------------|---------------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------|
| 7,307,002             | H1998US                   | United States | 04/04/2005  | 12/11/2007 | NON-CRITICAL COMPLEMENTARY MASKING METHOD FOR POLY-1<br>DEFINITION IN FLASH MEMORY DEVICE FABRICATION                                           |
| 10/789,533            | H1999                     | United States | 02/27/2004  |            | FABRICATING SEMICONDUCTORS USING THICK SOURCE DRAIN<br>NITRIDE TO ACHIEVE WIDE SILICON WIDTHS                                                   |
| 7,122,465             | H2003US                   | United States | 12/02/2004  | 10/17/2006 | METHOD FOR ACHIEVING INCREASED CONTROL OVER<br>INTERCONNECT LINE THICKNESS ACROSS A WAFER AND BETWEEN<br>WAFERS                                 |
| 7,026,702             | H2015US CIP               | United States | 02/11/2004  | 04/11/2006 | MEMORY DEVICE                                                                                                                                   |
| 7,254,053             | H2016US CIP               | United States | 02/11/2004  | 08/07/2007 | ACTIVE PROGRAMMING AND OPERATION OF A MEMORY DEVICE                                                                                             |
| 7,221,599             | H2018US                   | United States | 11/01/2004  | 05/22/2007 | POLYMER MEMORY CELL OPERATION                                                                                                                   |
| 10/921,587            | H2025                     | United States | 08/19/2004  |            | FLASH MEMORY CELL WITH EPITAXIAL BITLINES AND FABRICATION<br>METHOD THEREFOR                                                                    |
| 11/388,977            | H2075US                   | United States | 03/27/2006  |            | METHOD OF FORMING A CONTACT WITH DENSIFIED MOCVD TIN ON<br>CONTACT SIDEWALLS                                                                    |
| 7,262,422             | H2114US                   | United States | 07/01/2005  | 08/28/2007 | USE OF SUPERCRITICAL FLUID TO DRY WAFER AND CLEAN LENS IN<br>IMMERSION LITHOGRAPHY                                                              |
| 7,407,882             | H2135US                   | United States | 08/27/2004  | 08/05/2008 | SEMICONDUCTOR COMPONENT HAVING A CONTACT STRUCTURE<br>AND METHOD OF MANUFACTURE                                                                 |
| 7,344,912             | H2157US                   | United States | 03/01/2005  | 03/18/2008 | METHOD FOR PATTERNING ELECTRICALLY CONDUCTING<br>POLY(PHENYL ACETYLENE) AND POLY (DIPHENYL ACETYLENE)                                           |
| 11/109,965            | H2210US                   | United States | 04/19/2005  |            | SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE                                                                                               |
| 7,217,660             | H2211US                   | United States | 04/19/2005  | 05/15/2007 | METHOD FOR MANUFACTURING A SEMICONDUCTOR COMPONENT<br>THAT INHIBITS FORMATION OF WORMHOLES                                                      |
| 7,378,310             | H2215US                   | United States | 04/27/2005  | 05/27/2008 | METHOD FOR MANUFACTURING A MEMORY DEVICE HAVING A<br>NANOCRYSTAL CHARGE STORAGE REGION                                                          |
| 7,335,594             | H2216US                   | United States | 04/27/2005  | 02/26/2008 | METHOD FOR MANUFACTURING A MEMORY DEVICE HAVING A<br>NANOCRYSTAL CHARGE STORAGE REGION                                                          |
| 11/407,916            | H2242                     | United States | 04/21/2006  |            | METHOD OF REWORKING PHOTORESISTS                                                                                                                |
| 11/407,894            | H2243                     | United States | 04/21/2006  |            | METHOD TO CONTROL THE PRE METAL DIELECTRIC/SILICON<br>INTERFACE TO IMPROVE THE THRESHOLD VOLTAGE DISTRIBUTION<br>AFTER CYCLING                  |
| 11/407,935            | H2246US                   | United States | 04/21/2006  |            | PROTECTIVE UV BLOCKING LAYERS FOR PLASMA PROCESSING                                                                                             |
| 11/407,929            | H2247US                   | United States | 04/21/2006  |            | IMPROVING THE OPTICAL CHARACTERISTICS OF AMORPHOUS<br>CARBON                                                                                    |
| 8,415,256             | H2249CON                  | United States | 12/30/2010  | 04/09/2013 | GAP-FILLING WITH UNIFORM PROPERTIES                                                                                                             |
| 7,884,030             | H2249US                   | United States | 04/21/2006  | 02/08/2011 | GAP-FILLING WITH UNIFORM PROPERTIES                                                                                                             |
| 7,358,191             | H2256US                   | United States | 03/24/2006  | 04/15/2008 | METHOD FOR DECREASING SHEET RESISTIVITY VARIATIONS OF AN<br>INTERCONNECT METAL LAYER                                                            |
| 6,232,663             | JC137496US                | United States | 08/01/1997  | 05/15/2001 | SEMICONDUCTOR DEVICE HAVING INTERLAYER INSULATOR AND<br>METHOD FOR FABRICATING THEREOF                                                          |
| 6,187,640             | JC394297US                | United States | 11/17/1998  | 02/13/2001 | SEMICONDUCTOR DEVICE MANUFACTURING METHOD                                                                                                       |
| 6,579,769             | JC394297US DIV            | United States | 12/01/2000  | 06/17/2003 | SEMICONDUCTOR DEVICE MANUFACTURING METHOD INCLUDING<br>FORMING FOX WITH DUAL OXIDATION                                                          |
| 6,362,049             | JC684497US                | United States | 11/05/1999  | 03/26/2002 | HIGH YIELD PERFORMANCE SEMICONDUCTOR PROCESS FLOW FOR<br>NAND FLASH MEMORY PRODUCTS                                                             |
| 60/111,012            | JC684497US PROV           | United States | 12/04/1998  |            | HIGH YIELD, HIGH PERFORMANCE SEMICONDUCTOR PROCESS FLOW<br>FOR NAND FLASH MEMORY PRODUCTS                                                       |
| 09/163,155            | JC685497US CON            | United States | 10/02/2000  |            | HIGH TEMPERATURE DEPOSITION OF OXIDE LAYER THAT PROTECTS<br>AGAINST IMPLANTATION DAMAGE                                                         |
| 6,057,193             | JC688497US                | United States | 04/16/1998  | 05/02/2000 | ELIMINATION OF POLY-CAP FOR EASY POLY1 CONTACT FOR NAND<br>PRODUCT                                                                              |
| 6,312,991             | JC688497US CON1           | United States | 03/21/2000  | 11/06/2001 | ELIMINATION OF POLY-CAP FOR EASY POLY1 CONTACT FOR NAND<br>PRODUCT                                                                              |
| 6,177,312             | JC691497US                | United States | 03/26/1998  | 01/23/2001 | METHOD FOR REMOVING CONTAMINATE NITROGEN FROM THE<br>PERIPHERAL GATE REGION OF A NON-VOLATILE MEMORY DEVICE<br>DURING PRODUCTION OF SUCH DEVICE |
| 5,907,781             | JC818597US                | United States | 03/27/1998  | 05/25/1999 | PROCESS FOR FABRICATING AN INTEGRATED CIRCUIT WITH A SELF-<br>ALIGNED CONTACT                                                                   |
| 6,444,530             | JC818597US CON            | United States | 05/25/1999  | 09/03/2002 | PROCESS FOR FABRICATING AN INTEGRATED CIRCUIT WITH A SELF-<br>ALIGNED CONTACT                                                                   |
| 09/473,988            | JD811US                   | United States | 12/29/1999  |            | SEMICONDUCTOR DEVICE AND THE METHOD OF MANUFACTURING<br>THE SAME                                                                                |
| 6,285,599             | JD831US                   | United States | 05/02/2000  | 09/04/2001 | DECODED SOURCE LINES TO TIGHTEN ERASE VI DISTRIBUTION                                                                                           |
| 6,272,046             | JD850US                   | United States | 05/02/2000  | 08/07/2001 | INDIVIDUAL SOURCE LINE TO DECREASE COLUMN LEAKAGE                                                                                               |
| 6,727,143             | JD922US                   | United States | 03/22/2000  | 04/27/2004 | METHOD AND SYSTEM FOR REDUCING CHARGE GAIN AND CHARGE<br>LOSS WHEN USING AN ARC LAYER IN INTERLAYER DIELECTRIC<br>FORMATION                     |
| 6,492,229             | JDA01034                  | United States | 12/04/2000  | 12/10/2002 | SEMICONDUCTOR DEVICE HAVING REDUCED FIELD OXIDE RECESS<br>AND METHOD OF FABRICATION                                                             |
| 7,742,741             | JDE0584US                 | United States | 12/21/2005  | 06/22/2010 | PORTABLE WIRELESS DATA STORAGE DEVICE                                                                                                           |
| 10/939,729            | JH2118US                  | United States | 09/13/2004  |            | OPTICAL TECHNIQUE FOR MONITORING COPPER SULFIDE<br>FORMATION ON COPPER SURFACE                                                                  |
| 7,135,396             | JH2119US                  | United States | 09/13/2004  | 11/14/2006 | METHOD OF MAKING A SEMICONDUCTOR STRUCTURE                                                                                                      |
| 10/979,374            | JH2129                    | United States | 11/01/2004  |            | CONTROLLED ASH PROCESS ON HARDENED POLYMER FILM                                                                                                 |
| 7,294,573             | JH2153US                  | United States | 01/13/2005  | 11/13/2007 | METHOD FOR CONTROLLING POLY 1 THICKNESS AND UNIFORMITY IN<br>A MEMORY ARRAY FABRICATION PROCESS                                                 |
| 7,309,650             | JH2209US                  | United States | 02/24/2005  | 12/18/2007 | MEMORY DEVICE HAVING A NANOCRYSTAL CHARGE STORAGE<br>REGION AND METHOD"                                                                         |
| 7,994,047             | JH2223US                  | United States | 11/22/2005  | 08/09/2011 | INTEGRATED CIRCUIT CONTACT SYSTEM                                                                                                               |
| 11/201,885            | JH2225US                  | United States | 08/11/2005  |            | METHOD OF DEPOSITING GE USING PHYSICAL VAPOR DETECTION                                                                                          |
| 11/251,254            | JH2236                    | United States | 10/14/2005  |            | ALPHA PHASE TANTALUM DIFFUSION BARRIER FOR A TERMINAL<br>METAL LAYER AND METHOD FOR FABRICATING SAME                                            |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                          |
|-----------------------|---------------------------|---------------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------|
| 7,235,867             | JNY0040                   | United States | 11/01/2004  | 06/26/2007 | A SEMICONDUCTOR DEVICE WITH ELECTRICALLY BIASED DIE EDGE SEAL                                                                  |
| 10/940,369            | JTT5691US                 | United States | 09/14/2004  |            | METHOD AND SYSTEM FOR CALIBRATING INTEGRATED METROLOGY SYSTEMS AND STAND-ALONE METROLOGY SYSTEMS THAT ACQUIRE WAFER STATE DATA |
| 7,519,447             | JTT5695US                 | United States | 10/05/2004  | 04/14/2009 | METHOD AND APPARATUS FOR INTEGRATING MULTIPLE SAMPLE PLANS                                                                     |
| 7,277,824             | JTT5697US                 | United States | 07/13/2005  | 10/02/2007 | METHOD AND APPARATUS FOR CLASSIFYING FAULTS BASED ON WAFER STATE DATA AND SENSOR TOOL TRACE DATA                               |
| 7,282,374             | JTT5699US                 | United States | 11/03/2004  | 10/16/2007 | METHOD AND APPARATUS FOR COMPARING DEVICE AND NON-DEVICE STRUCTURES                                                            |
| 10/979,256            | JTT5710US                 | United States | 11/02/2004  |            | METHODS AND SYSTEMS FOR QUALIFYING PROCESSES AND TOOLS USING PROCESS THREADS THAT EXHIBIT DESIRED CHARACTERISTICS              |
| 7,315,765             | JTT5711US                 | United States | 07/29/2005  | 01/01/2008 | AUTOMATED CONTROL THREAD DETERMINATION BASED UPON POST-PROCESS CONSIDERATION                                                   |
| 7,337,032             | JTT5714US                 | United States | 10/04/2004  | 02/26/2008 | SCHEDULING AHEAD FOR VARIOUS PROCESSES                                                                                         |
| 11/360,043            | JTT5732US                 | United States | 02/23/2006  |            | METHOD AND APPARATUS FOR SCHEDULING AND DELIVERY OF SEND-AHEAD WAFERS                                                          |
| 7,299,106             | JTT5733US                 | United States | 04/19/2005  | 11/20/2007 | METHOD AND APPARATUS FOR SCHEDULING METROLOGY BASED ON A JEOPARDY COUNT                                                        |
| 11/243,931            | JTT5792US                 | United States | 10/05/2005  |            | METHOD AND APPARATUS FOR MODIFYING SAMPLING PLANS BASED ON WORK-IN-PROCESS LEVELS                                              |
| 7,460,920             | JTT5931US                 | United States | 02/22/2006  | 12/02/2008 | DETERMINING SCHEDULING PRIORITY USING FABRICATION SIMULATION                                                                   |
| 7,623,936             | JTT5932US                 | United States | 02/16/2006  | 11/24/2009 | DETERMINING SCHEDULING PRIORITY USING QUEUE TIME OPTIMIZATION                                                                  |
| 4,654,830             | M84-003                   | United States | 11/27/1984  | 03/31/1987 | METHOD AND STRUCTURE FOR DISABLING AND REPLACING DEFECTIVE MEMORY IN A PROM                                                    |
| 09/595,422            | P063US                    | United States | 06/15/2000  |            | FLASH MEMORY DEVICE AND A METHOD OF FABRICATION THEREOF                                                                        |
| 6,979,619             | P063US DIV                | United States | 08/28/2001  | 12/27/2005 | FLASH MEMORY DEVICE AND A METHOD OF FABRICATION THEREOF                                                                        |
| 10/119,571            | P065D1                    | United States | 04/09/2002  |            | METHOD AND SYSTEM FOR REDUCING SHORT CHANNEL EFFECTS IN A MEMORY DEVICE BY REDUCTION OF DRAIN THERMAL CYCLING                  |
| 10/689,298            | P065D1C1                  | United States | 10/20/2003  |            | METHOD AND SYSTEM FOR REDUCING SHORT CHANNEL EFFECTS IN A MEMORY DEVICE BY REDUCTION OF DRAIN THERMAL CYCLING                  |
| 6,509,202             | P100US                    | United States | 06/05/2001  | 01/21/2003 | METHOD AND SYSTEM FOR QUALIFYING AN ONO LAYER IN A SEMICONDUCTOR DEVICE                                                        |
| 7,864,606             | P-10174-US                | United States | 09/18/2008  | 01/04/2011 | METHOD, DEVICE AND SYSTEM FOR REGULATING ACCESS TO AN INTEGRATED CIRCUIT (IC) DEVICE                                           |
| 7,864,588             | P-10176-US                | United States | 09/17/2008  | 01/04/2011 | MINIMIZING READ DISTURB IN AN ARRAY FLASH CELL                                                                                 |
| 8,593,881             | P-10233-US                | United States | 11/22/2011  | 11/26/2013 | PRE-CHARGE SENSING SCHEME FOR NON-VOLATILE MEMORY (NVM)                                                                        |
| 8,120,960             | P-10233-US1D              | United States | 11/07/2008  | 02/21/2012 | METHOD AND APPARATUS FOR ACCESSING A NON-VOLATILE MEMORY ARRAY COMPRISING UNIDIRECTIONAL CURRENT FLOWING MULTIPLEXERS          |
| 7,924,628             | P-10234-US                | United States | 11/14/2008  | 04/12/2011 | OPERATION OF A NON-VOLATILE MEMORY (NVM)                                                                                       |
| 8,264,884             | P-10235-US                | United States | 02/23/2009  | 09/11/2012 | METHODS, CIRCUITS AND SYSTEMS FOR READING NON-VOLATILE MEMORY CELLS                                                            |
| 8,189,397             | P-10258-US                | United States | 01/08/2009  | 05/29/2012 | RETENTION IN NVM WITH TOP OR BOTTOM INJECTION                                                                                  |
| 6,768,165             | P-1025US                  | United States | 08/01/1997  | 07/27/2004 | TWO BIT NON-VOLATILE ELECTRICALLY ERASABLE AND PROGRAMMABLE SEMICONDUCTOR MEMORY CELL UTILIZING ASYMMETRICAL CHARGE TRAPPING   |
| 6,649,972             | P-1025US CON              | United States | 04/15/2002  | 11/18/2003 | TWO BIT NON-VOLATILE ELECTRICALLY ERASABLE AND PROGRAMMABLE SEMICONDUCTOR MEMORY CELL UTILIZING ASYMMETRICAL CHARGE TRAPPING   |
| 7,116,577             | P-1025US CON2             | United States | 06/09/2004  | 10/03/2006 | TWO BIT NON-VOLATILE ELECTRICALLY ERASABLE AND PROGRAMMABLE SEMICONDUCTOR MEMORY CELL UTILIZING ASYMMETRICAL CHARGE TRAPPING   |
| 7,400,529             | P-1025US CON3             | United States | 04/17/2007  | 07/15/2008 | A NON-VOLATILE MEMORY CELL AND NON-VOLATILE MEMORY DEVICE USING SAID CELLS                                                     |
| 7,405,969             | P-1025US CON4             | United States | 08/01/2006  | 07/29/2008 | NON-VOLATILE MEMORY CELL AND NON-VOLATILE MEMORY DEVICES                                                                       |
| 6,011,725             | P-1025US DIV              | United States | 02/04/1999  | 01/04/2000 | TWO BIT NON-VOLATILE ELECTRICALLY ERASABLE AND PROGRAMMABLE SEMICONDUCTOR MEMORY CELL UTILIZING ASYMMETRICAL CHARGE TRAPPING   |
| 7,945,825             | P-10285-US                | United States | 11/25/2008  | 05/17/2011 | RECOVERY WHILE PROGRAMMING NON-VOLATILE MEMORY (NVM)                                                                           |
| 8,253,452             | P-10294-US                | United States | 02/21/2006  | 08/28/2012 | CIRCUIT AND METHOD FOR POWERING UP AN INTEGRATED CIRCUIT AND AN INTEGRATED CIRCUIT UTILIZING SAME                              |
| 8,400,841             | P-10472-US                | United States | 06/15/2005  | 03/19/2013 | NOT FILED BY SKGF; AWAITING RECEIPT OF FILE/AUTHORIZATION TO PROCEED. PART OF TRANSFER-IN PORTFOLIO FOR SPANSION.              |
| 11/935,544            | P-10933-US                | United States | 11/06/2007  |            | PROCESS OF FORMING AN ELECTRONIC DEVICE INCLUDING DEPOSITING A CONDUCTIVE LAYER OVER A SEED LAYER                              |
| 5,966,603             | P-1164US                  | United States | 06/11/1997  | 10/12/1999 | NROM FABRICATION METHOD WITH A PERIPHERY PORTION                                                                               |
| 6,297,096             | P-1164US CON              | United States | 07/30/1999  | 10/02/2001 | AN NROM FABRICATION METHOD                                                                                                     |
| 6,803,279             | P-1164US CON2             | United States | 10/01/2001  | 10/12/2004 | NROM FABRICATION METHOD                                                                                                        |
| 7,943,979             | P-1164-US3                | United States | 10/12/2004  | 05/17/2011 | AN NROM FABRICATION METHOD                                                                                                     |
| 8,106,442             | P-1164-US4C               | United States | 10/31/2007  | 01/31/2012 | NROM FABRICATION METHOD                                                                                                        |
| 8,008,709             | P-1164-US5C               | United States | 12/27/2007  | 08/30/2011 | NROM fabrication method                                                                                                        |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                |
|-----------------------|---------------------------|---------------|-------------|------------|----------------------------------------------------------------------------------------------------------------------|
| 60/415,210            | P118PR                    | United States | 09/30/2002  |            | DIFFERENTIALLY MIS-ALIGNED CONTACTS IN FLASH ARRAYS TO CALIBRATE FAILURE MODES                                       |
| 7,032,193             | P118US                    | United States | 12/17/2002  | 04/18/2006 | DIFFERENTIALLY MIS-ALIGNED CONTACTS IN FLASH ARRAYS TO CALIBRATE FAILURE MODES                                       |
| 5,963,465             | P-1251US                  | United States | 12/12/1997  | 10/05/1999 | SYMMETRIC SEGMENTED MEMORY ARRAY ARCHITECTURE                                                                        |
| 6,633,496             | P-1251US CIP              | United States | 12/04/2000  | 10/14/2003 | Symmetric architecture for memory cells having widely spread metal bit lines                                         |
| 6,285,574             | P-1251US CIP1             | United States | 07/06/1999  | 09/04/2001 | SYMMETRIC SEGMENTED MEMORY ARRAY ARCHITECTURE                                                                        |
| 6,633,499             | P-1251US CIP2             | United States | 03/28/2000  | 10/14/2003 | A METHOD FOR REDUCING VOLTAGE DROPS IN SYMMETRIC ARRAY ARCHITECTURES                                                 |
| 6,430,077             | P-1251US CIP3             | United States | 03/28/2000  | 08/06/2002 | A METHOD FOR REGULATING READ VOLTAGE LEVEL AT THE DRAIN OF A CELL IN A SYMMETRIC ARRAY                               |
| 6,704,217             | P-1251US CON              | United States | 01/30/2002  | 03/09/2004 | SYMMETRIC SEGMENTED MEMORY ARRAY ARCHITECTURE                                                                        |
| 6,335,874             | P-1251US CON2             | United States | 09/11/2000  | 01/01/2002 | Symmetric segmented memory array architecture                                                                        |
| 6,030,871             | P-1273US                  | United States | 05/05/1998  | 02/29/2000 | PROCESS FOR PRODUCING TWO BIT ROM CELL UTILIZING ANGLED IMPLANT                                                      |
| 6,201,282             | P-1273US DIV              | United States | 12/23/1999  | 03/13/2001 | TWO BIT ROM CELL AND PROCESS FOR PRODUCING SAME                                                                      |
| 6,566,699             | P-1326US CON              | United States | 08/28/2001  | 05/20/2003 | NON-VOLATILE ELECTRICALLY ERASABLE AND PROGRAMMABLE SEMICONDUCTOR MEMORY CELL UTILIZING ASYMMETRICAL CHARGE TRAPPING |
| 6,803,299             | P-1326US CON2             | United States | 04/14/2003  | 10/12/2004 | NON-VOLATILE ELECTRICALLY ERASABLE AND PROGRAMMABLE SEMICONDUCTOR MEMORY CELL UTILIZING ASYMMETRICAL CHARGE TRAPPING |
| 6,552,387             | P-1326US DIV              | United States | 12/14/1998  | 04/22/2003 | NON-VOLATILE ELECTRICALLY ERASABLE AND PROGRAMMABLE SEMICONDUCTOR MEMORY CELL UTILIZING ASYMMETRICAL CHARGE TRAPPING |
| 6,215,148             | P-1452US                  | United States | 05/20/1998  | 04/10/2001 | NROM CELL WITH IMPROVED PROGRAMMING ERASING AND CYCLING                                                              |
| 6,348,711             | P-1452US CON              | United States | 10/06/1999  | 02/19/2002 | NROM CELL WITH SELF-ALIGNED PROGRAMMING AND ERASURE AREAS                                                            |
| 6,664,588             | P-1452US CON2             | United States | 06/14/2001  | 12/16/2003 | NROM CELL WITH SELF-ALIGNED PROGRAMMING AND ERASURE AREAS                                                            |
| 6,477,084             | P-1452US DIV              | United States | 02/07/2001  | 11/05/2002 | NROM CELL WITH IMPROVED PROGRAMMING ERASING AND CYCLING                                                              |
| 6,128,226             | P-1870US                  | United States | 02/04/1999  | 10/03/2000 | Method and apparatus for operating with a close to ground signal                                                     |
| 6,078,539             | P-1894US                  | United States | 02/04/1999  | 06/20/2000 | METHOD AND DEVICE FOR INITIATING A MEMORY ARRAY DURING POWER UP                                                      |
| 6,233,180             | P-1902US                  | United States | 02/04/1999  | 05/15/2001 | Device for determining the validity of word line conditions and for delaying data sensing operation                  |
| 6,134,156             | P-1907US                  | United States | 02/04/1999  | 10/17/2000 | METHOD FOR INITIATING A RETRIEVAL PROCEDURE IN VIRTUAL GROUND ARRAYS                                                 |
| 6,118,267             | P-1975US                  | United States | 02/04/1999  | 09/12/2000 | Apparatus for switching a reference voltage between high and low impedance states                                    |
| 6,133,095             | P-1978US                  | United States | 02/04/1999  | 10/17/2000 | Method for creating diffusion areas for sources and drains without an etch step                                      |
| 6,337,502             | P-2024US                  | United States | 06/18/1999  | 01/08/2002 | METHOD AND CIRCUIT FOR MINIMIZING THE CHARGING EFFECT DURING MANUFACTURE OF SEMICONDUCTOR DEVICES                    |
| 6,627,555             | P-2024US DIV              | United States | 02/05/2001  | 09/30/2003 | METHOD AND CIRCUIT FOR MINIMIZING THE CHARGING EFFECT DURING MANUFACTURE OF SEMICONDUCTOR DEVICES                    |
| 6,396,741             | P-2448US                  | United States | 05/04/2000  | 05/28/2002 | PROGRAMMING OF NONVOLATILE MEMORY CELLS                                                                              |
| 6,535,434             | P-2448US                  | United States | 04/05/2001  | 03/18/2003 | PROGRAMMING AND ERASING METHODS FOR A NON-VOLATILE MEMORY CELL                                                       |
| 6,584,017             | P-2448US CIP              | United States | 04/05/2001  | 06/24/2003 | PROGRAMMING AND ERASING METHODS FOR A NON-VOLATILE MEMORY CELL                                                       |
| 6,928,001             | P-2448US CIP              | United States | 12/07/2000  | 08/09/2005 | PROGRAMMING AND ERASING METHODS FOR A NON-VOLATILE MEMORY CELL                                                       |
| 7,064,983             | P-2448US CIP              | United States | 06/05/2003  | 06/20/2006 | PROGRAMMING AND ERASING METHODS FOR A NON-VOLATILE MEMORY CELL                                                       |
| 7,512,009             | P-2448US CIP              | United States | 04/27/2006  | 03/31/2009 | PROGRAMMING AND ERASING METHODS FOR A NON-VOLATILE MEMORY CELL                                                       |
| 7,701,779             | P-2448US CIP              | United States | 09/11/2006  | 04/20/2010 | PROGRAMMING AND ERASING METHODS FOR A NON-VOLATILE MEMORY CELL                                                       |
| 6,490,204             | P-2448US CON              | United States | 11/01/2001  |            | PROGRAMMING AND ERASING METHODS FOR A REFERENCE CELL OF AN NROM ARRAY                                                |
| 10/300,924            | P-2448US CON              | United States | 04/01/2002  |            | PROGRAMMING AND ERASING METHODS FOR A REFERENCE CELL OF AN NROM ARRAY                                                |
| 6,829,172             | P-2448US CON2             | United States | 05/28/2002  | 12/07/2004 | PROGRAMMING OF NONVOLATILE MEMORY CELLS                                                                              |
| 6,937,521             | P-2448US DIV              | United States | 05/28/2002  | 08/30/2005 | PROGRAMMING AND ERASING METHODS FOR A NON-VOLATILE MEMORY CELL                                                       |
| 6,292,394             | P-2505US                  | United States | 06/29/2000  | 09/18/2001 | METHOD FOR PROGRAMMING OF A SEMICONDUCTOR MEMORY CELL                                                                |
| 6,429,063             | P-2781US                  | United States | 03/06/2000  | 08/06/2002 | NROM CELL WITH GENERALLY DECOUPLED PRIMARY AND SECONDARY INJECTION                                                   |
| 6,614,692             | P-3364US                  | United States | 01/18/2001  | 09/02/2003 | AN EEPROM ARRAY AND METHOD FOR OPERATION THEREOF                                                                     |
| 7,518,908             | P-3364US CIP              | United States | 05/28/2002  | 04/14/2009 | AN EEPROM ARRAY AND METHOD FOR OPERATION THEREOF                                                                     |
| 6,885,585             | P-3454US                  | United States | 12/20/2001  | 04/26/2005 | AN NROM NOR ARRAY                                                                                                    |
| 6,636,440             | P-3688US                  | United States | 04/25/2001  | 10/21/2003 | METHOD FOR OPERATION OF AN EEPROM ARRAY INCLUDING REFRESH THEREOF                                                    |
| 6,677,805             | P-3819US                  | United States | 04/05/2001  | 01/13/2004 | CHARGE PUMP STAGE WITH BODY MINIMIZATION                                                                             |
| 6,864,739             | P-3819US CON              | United States | 12/22/2003  | 03/08/2005 | CHARGE PUMP STAGE WITH BODY EFFECT MINIMIZATION                                                                      |
| 6,643,181             | P-4006US                  | United States | 10/24/2001  | 11/04/2003 | METHOD FOR ERASING A MEMORY CELL                                                                                     |
| 6,888,757             | P-4006US CIP              | United States | 09/08/2003  | 05/03/2005 | METHOD FOR ERASING A MEMORY CELL                                                                                     |
| 7,098,107             | P-4007US                  | United States | 11/19/2001  | 08/29/2006 | PROTECTIVE LAYER IN MEMORY DEVICE AND METHOD THEREFOR                                                                |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSON<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                       |
|-----------------------|--------------------------|---------------|-------------|------------|-------------------------------------------------------------------------------------------------------------|
| 11/490,483            | P-4007US CON             | United States | 07/20/2006  |            | PROTECTIVE LAYER IN MEMORY DEVICE AN METHOD THEREFOR                                                        |
| 6,828,625             | P-4007US DIV             | United States | 07/08/2002  | 12/07/2004 | PROTECTIVE LAYER IN MEMORY DEVICE AN METHOD THEREFOR                                                        |
| 6,791,396             | P-4109US                 | United States | 10/24/2001  | 09/14/2004 | STACK ELEMENT CIRCUIT                                                                                       |
| 6,583,007             | P-4141US                 | United States | 12/20/2001  | 06/24/2003 | REDUCING SECONDARY INJECTION EFFECTS                                                                        |
| 6,917,544             | P-4629US                 | United States | 07/10/2002  | 07/12/2005 | A MULTIPLE USE MEMORY CHIP                                                                                  |
| 6,954,382             | P-4629US CON             | United States | 12/30/2004  | 10/11/2005 | A MULTIPLE USE MEMORY CHIP                                                                                  |
| 7,489,562             | P-4629US CON2            | United States | 10/31/2007  | 02/10/2009 | A MULTIPLE USE MEMORY CHIP                                                                                  |
| 7,573,745             | P-4629US CON3            | United States | 10/31/2007  | 08/11/2009 | A MULTIPLE USE MEMORY CHIP                                                                                  |
| 7,738,304             | P-4629US CON4            | United States | 10/11/2005  | 06/15/2010 | A MULTIPLE USE MEMORY CHIP                                                                                  |
| 6,975,536             | P-4675US                 | United States | 08/05/2002  | 12/13/2005 | Mass storage array and methods for operation thereof                                                        |
| 60/352,549            | P-4676IL                 | United States | 01/31/2002  |            | METHOD FOR OPERATING A MEMORY DEVICE                                                                        |
| 6,700,818             | P-4676US                 | United States | 08/05/2002  | 03/02/2004 | METHOD FOR OPERATING A MEMORY DEVICE                                                                        |
| 7,079,420             | P-4676US CIP             | United States | 12/30/2003  | 07/18/2006 | METHOD FOR OPERATING A MEMORY DEVICE                                                                        |
| 7,190,620             | P-4676US CIP2            | United States | 01/06/2005  | 03/13/2007 | METHOD FOR OPERATING A MEMORY DEVICE                                                                        |
| 7,420,848             | P-4676US CON             | United States | 01/09/2006  | 09/02/2008 | METHOD FOR OPERATING A MEMORY DEVICE                                                                        |
| 6,448,750             | P-4723US                 | United States | 04/05/2001  | 09/10/2002 | VOLTAGE REGULATOR FOR NON-VOLATILE MEMORY WITH LARGE POWER SUPPLY REJECTION RATIO AND MINIMAL CURRENT DRAIN |
| 6,665,769             | P-4724US                 | United States | 04/05/2001  | 12/16/2003 | METHOD AND APPARATUS FOR DYNAMICALLY MASKING AN N-BIT MEMORY ARRAY HAVING INDIVIDUALLY PROGRAMMABLE CELLS   |
| 6,577,514             | P-4726US                 | United States | 04/05/2001  | 06/10/2003 | CHARGE PUMP WITH CONSTANT BOOSTED OUTPUT VOLTAGE                                                            |
| 6,928,527             | P-4820US                 | United States | 08/05/2002  | 08/09/2005 | Look ahead methods and apparatus                                                                            |
| 7,062,619             | P-4875US                 | United States | 08/05/2002  | 06/13/2006 | Mass storage device architecture and operation                                                              |
| 6,781,897             | P-5083US                 | United States | 08/01/2002  | 08/24/2004 | Defects detection                                                                                           |
| 7,199,394             | P-5084US                 | United States | 08/17/2004  | 04/03/2007 | POLYMER MEMORY DEVICE WITH VARIABLE PERIOD OF RETENTION TIME                                                |
| 6,967,896             | P-5086US                 | United States | 01/30/2003  | 11/22/2005 | ADDRESS SCRAMBLE                                                                                            |
| 7,148,739             | P-5260US                 | United States | 12/19/2002  | 12/12/2006 | CHARGE PUMP ELEMENT WITH BODY EFFECT CANCELLATION FOR EARLY CHARGE PUMP STAGES                              |
| 6,906,966             | P-5262US                 | United States | 06/16/2003  | 06/14/2005 | FAST DISCHARGE FOR PROGRAM AND VERIFICATION                                                                 |
| 6,842,383             | P-5292US                 | United States | 01/30/2003  | 01/11/2005 | A METHOD AND CIRCUIT FOR OPERATING A MEMORY CELL USING A SINGLE CHARGE PUMP                                 |
| 6,885,244             | P-5414US                 | United States | 03/24/2003  | 04/26/2005 | OPERATIONAL AMPLIFIER WITH FAST RISE TIME                                                                   |
| 7,136,304             | P-5484US                 | United States | 10/27/2004  |            | METHOD SYSTEM AND CIRCUIT FOR PROGRAMMING A NON-VOLATILE MEMORY ARRAY                                       |
| 7,675,782             | P-5484US CON             | United States | 10/17/2006  | 03/09/2010 | METHOD SYSTEM AND CIRCUIT FOR PROGRAMMING A NON-VOLATILE MEMORY ARRAY                                       |
| 6,963,505             | P-5487US                 | United States | 10/29/2003  | 11/08/2005 | METHOD CIRCUIT AND SYSTEM FOR DETERMINING A REFERENCE VOLTAGE                                               |
| 6,992,932             | P-5487US CIP             | United States | 10/29/2003  | 01/31/2006 | A METHOD CIRCUIT AND SYSTEM FOR READ ERROR DETECTION IN A NON-VOLATILE MEMORY ARRAY                         |
| 7,352,627             | P-5589US                 | United States | 01/03/2006  | 04/01/2008 | METHOD SYSTEM AND CIRCUIT FOR OPERATING A NON-VOLATILE MEMORY ARRAY                                         |
| 7,715,237             | P-5589US CON             | United States | 02/26/2008  | 05/11/2010 | METHOD SYSTEM AND CIRCUIT FOR OPERATING A NON-VOLATILE MEMORY ARRAY                                         |
| 6,975,541             | P-5624US                 | United States | 03/24/2003  | 12/13/2005 | ALTERNATING APPLICATION OF PULSES ON TWO SIDES OF A CELL                                                    |
| 7,178,004             | P-5640US                 | United States | 09/03/2003  | 02/13/2007 | A MEMORY ARRAY PROGRAMMING CIRCUIT AND A METHOD FOR USING THE CIRCUIT                                       |
| 7,743,230             | P-5640US CON             | United States | 02/12/2007  | 06/22/2010 | A MEMORY ARRAY PROGRAMMING CIRCUIT AND A METHOD FOR USING THE CIRCUIT                                       |
| 7,142,464             | P-5675US                 | United States | 03/29/2004  | 11/28/2006 | APPARATUS AND METHODS FOR MULTI-LEVEL SENSING IN A MEMORY ARRAY                                             |
| 7,532,529             | P-5675US CON             | United States | 08/14/2006  | 05/12/2009 | APPARATUS AND METHODS FOR MULTI-LEVEL SENSING IN A MEMORY ARRAY                                             |
| 6,954,393             | P-6061US                 | United States | 09/16/2003  | 10/11/2005 | READING ARRAY CELL WITH MATCHED REFERENCE CELL                                                              |
| 7,123,532             | P-6061US CIP             | United States | 08/01/2005  | 10/17/2006 | OPERATING ARRAY CELLS WITH MATCHED REFERENCE CELLS                                                          |
| 7,457,183             | P-6061US CON             | United States | 10/16/2006  | 11/25/2008 | OPERATING ARRAY CELLS WITH MATCHED REFERENCE CELLS                                                          |
| 7,864,612             | P-6061-US3C              | United States | 11/24/2008  | 01/04/2011 | READING ARRAY CELL WITH MATCHEDREFERENCE CELL                                                               |
| 6,922,099             | P-6062US                 | United States | 10/21/2003  | 07/26/2005 | CLASS AB VOLTAGE REGULATOR                                                                                  |
| 8,339,865             | P-6273-US                | United States | 11/03/2008  | 12/25/2012 | NON BINARY FLASH ARRAY ARCHITECTURE AND METHOD OF OPERATION                                                 |
| 7,176,728             | P-6274US                 | United States | 02/10/2004  | 02/13/2007 | High voltage low power driver                                                                               |
| 7,256,438             | P-6414US                 | United States | 06/08/2004  | 08/14/2007 | MOS CAPACITOR WITH REDUCED PARASITIC CAPACITANCE                                                            |
| 7,095,655             | P-6415US                 | United States | 08/05/2005  |            | DYNAMIC MATCHING OF SIGNAL PATH AND REFERENCE PATH FOR SENSING                                              |
| 7,466,594             | P-6415US CON             | United States | 07/19/2006  | 12/16/2008 | DYNAMIC MATCHING OF SIGNAL PATH AND REFERENCE PATH FOR SENSING                                              |
| 7,187,595             | P-6416US                 | United States | 06/08/2004  | 03/06/2007 | REPLENISHMENT FOR INTERNAL VOLTAGE                                                                          |
| 7,190,212             | P-6417US                 | United States | 06/08/2004  | 03/13/2007 | POWER-UP AND BGREF CIRCUITRY                                                                                |
| 7,366,025             | P-6619US                 | United States | 06/10/2004  | 04/29/2008 | REDUCED POWER PROGRAMMING OF NON-VOLATILE CELLS                                                             |
| 7,599,227             | P-6619US CON             | United States | 04/14/2008  | 10/06/2009 | REDUCED POWER PROGRAMMING OF NON-VOLATILE CELLS                                                             |
| 7,257,025             | P-6628US                 | United States | 12/09/2005  |            | MEMORY FOR READING NON-VOLATILE MEMORY CELLS                                                                |
| 7,242,618             | P-6628US CIP             | United States | 08/15/2006  |            | METHOD FOR READING NON-VOLATILE MEMORY CELLS                                                                |
| 7,535,765             | P-6628US CIP2            | United States | 07/10/2007  | 05/19/2009 | NON-VOLATILE MEMORY DEVICE AND METHOD FOR READING CELLS                                                     |
| 7,652,930             | P-6715US                 | United States | 06/07/2005  | 01/26/2010 | METHOD CIRCUIT AND SYSTEM FOR ERASING ONE OR MORE NON-VOLATILE MEMORY CELLS                                 |
| 7,317,633             | P-7004US                 | United States | 07/05/2005  | 01/08/2008 | PROTECTION OF NROM DEVICES FROM CHARGE DAMAGE                                                               |
| 7,233,192             | P-7450US                 | United States | 04/06/2005  | 06/19/2007 | AN ON/OFF CHARGE PUMP                                                                                       |
| 8,098,525             | P-7465-US                | United States | 09/17/2008  | 01/17/2012 | PRE-CHARGE SENSING SCHEME FOR NON-VOLATILE MEMORY (NVM)                                                     |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                    |
|-----------------------|---------------------------|---------------|-------------|------------|------------------------------------------------------------------------------------------------------------------------------------------|
| 7,184,313             | P-7500US                  | United States | 06/17/2005  | 02/27/2007 | A METHOD CIRCUIT AND SYSTEM FOR COMPENSATING FOR TEMPERATURE INDUCED MARGIN LOSS IN NON-VOLATILE MEMORY CELLS                            |
| 7,339,826             | P-7632US                  | United States | 04/11/2005  | 03/04/2008 | THRESHOLD VOLTAGE SHIFT IN NROM CELLS                                                                                                    |
| 8,489,910             | P-7633US                  | United States | 06/17/2010  | 07/16/2013 | TIMING CONTROLLER, TIMING CONTROL METHOD, AND TIMING CONTROL SYSTEM                                                                      |
| 7,369,440             | P-7648US                  | United States | 01/19/2006  | 05/06/2008 | METHOD CIRCUIT AND SYSTEM FOR ERASING ONE OR MORE NON-VOLATILE MEMORY CELLS                                                              |
| 7,468,926             | P-7648US2                 | United States | 01/19/2006  | 12/23/2008 | PARTIAL ERASE VERIFY                                                                                                                     |
| 8,053,812             | P-7714-US                 | United States | 03/13/2006  | 11/08/2011 | Contact in planar NROM technology                                                                                                        |
| 5,768,192             | P-878US                   | United States | 07/23/1996  | 06/16/1998 | NON-VOLATILE SEMICONDUCTOR MEMORY CELL UTILIZING ASYMMETRICAL CHARGE TRAPPING                                                            |
| 7,668,017             | P-9014US                  | United States | 08/17/2005  | 02/23/2010 | A METHOD OF ERASING NON-VOLATILE MEMORY CELLS                                                                                            |
| 7,221,138             | P-9082US                  | United States | 09/27/2005  | 05/22/2007 | METHOD AND APPARATUS FOR MEASURING CHARGE PUMP OUTPUT CURRENT                                                                            |
| 7,202,654             | P-9083US                  | United States | 09/27/2005  | 04/10/2007 | DIODE STACK HIGH VOLTAGE REGULATOR                                                                                                       |
| 7,786,512             | P-9095US                  | United States | 07/18/2006  | 08/31/2010 | Dense non-volatile memory array and method of fabrication                                                                                |
| 8,339,102             | P-9126-US                 | United States | 11/15/2004  | 12/25/2012 | A SYSTEM AND METHOD FOR REGULATING LOADING ON AN INTEGRATED CIRCUIT POWER SUPPLY                                                         |
| 7,638,850             | P-9186US CIP              | United States | 05/24/2006  | 12/29/2009 | NON-VOLATILE MEMORY STRUCTURE AND METHOD OF FABRICATION                                                                                  |
| 7,964,459             | P-9186-US1D               | United States | 12/10/2009  | 06/21/2011 | NON-VOLATILE MEMORY STRUCTURE AND METHOD OF FABRICATION                                                                                  |
| 7,804,126             | P-9195US                  | United States | 07/18/2006  | 09/28/2010 | DENSE NON-VOLATILE MEMORY ARRAY AND METHOD OF FABRICATION                                                                                |
| 7,742,339             | P-9254US                  | United States | 07/10/2008  | 06/22/2010 | RD ALGORITHM IMPROVEMENT FOR NROM TECHNOLOGY                                                                                             |
| 7,808,818             | P-9258US                  | United States | 12/28/2006  | 10/05/2010 | SECONDARY INJECTION FOR NROM                                                                                                             |
| 7,760,554             | P-9300US                  | United States | 08/02/2006  | 07/20/2010 | NROM NON-VOLATILE MEMORY AND MODE OF OPERATION                                                                                           |
| 7,638,835             | P-9313US CIP              | United States | 12/28/2006  | 12/29/2009 | DOUBLE DENSITY NROM WITH NITRIDE (DNDS) STRIPS                                                                                           |
| 7,692,961             | P-9354US                  | United States | 08/02/2006  | 04/06/2010 | METHOD CIRCUIT AND DEVICE FOR DISTURB-CONTROL OF PROGRAMMING NON-VOLATILE MEMORY CELLS BY HOT-HOLE (HHI) INJECTION AND BY CHANNEL .....  |
| 7,590,001             | P-9373US                  | United States | 12/18/2007  | 09/15/2009 | FLASH MEMORY WITH OPTIMIZED WRITE SECTOR SPARES                                                                                          |
| 8,374,045             | P-9547-US                 | United States | 12/07/2010  | 02/12/2013 | METHODS CIRCUITS DEVICES AND SYSTEMS FOR OPERATING AN ARRAY OF NON-VOLATILE MEMORY CELLS                                                 |
| 7,605,579             | P-9557US                  | United States | 11/21/2006  | 10/20/2009 | MEASURING AND CONTROLLING CURRENT CONSUMPTION AND OUTPUT CURRENT OF CHARGE PUMPS                                                         |
| 7,811,887             | P-9603US                  | United States | 11/01/2007  | 10/12/2010 | FORMING SILICON TRENCH ISOLATION (STI) IN SEMICONDUCTOR DEVICES SELF-ALIGNED TO DIFFUSION                                                |
| 6,891,752             | SE0002                    | United States | 07/31/2002  | 05/10/2005 | SYSTEM AND METHOD OF ERASE VOLTAGE CONTROL DURING MULTIPLE SECTOR ERASE OF A FLASH MEMORY DEVICE                                         |
| 6,771,093             | SE0004US                  | United States | 09/25/2002  | 08/03/2004 | IMPLEMENTING REFERENCE CURRENT MEASUREMENT MODE WITHIN REFERENCE ARRAY PROGRAMMING MODE OR REFERENCE ARRAY ERASE MODE IN A SEMICONDUCTOR |
| 6,973,003             | SE0063US                  | United States | 10/01/2003  | 12/06/2005 | MEMORY DEVICE AND METHOD                                                                                                                 |
| 6,980,473             | SE0065US                  | United States | 10/01/2003  | 12/27/2005 | MEMORY DEVICE AND METHOD                                                                                                                 |
| 6,970,368             | SE0072US                  | United States | 08/26/2003  | 11/29/2005 | CAM (CONTENT ADDRESSABLE MEMORY) CELLS AS PART OF CORE ARRAY IN FLASH MEMORY DEVICE                                                      |
| 6,970,806             | SE0074US                  | United States | 11/07/2003  | 11/29/2005 | METHOD AND SYSTEM FOR TESTING ARTICLES OF MANUFACTURE                                                                                    |
| 7,254,692             | SE0099US                  | United States | 03/02/2004  | 08/07/2007 | TESTING FOR OPERATING LIFE OF A MEMORY DEVICE WITH ADDRESS CYCLING USING A GRAY CODE SEQUENCE                                            |
| 14/339,377            | SMA13-0003US              | United States | 07/23/2014  |            | DETECTING THE DRIFT OF THE DATA VALID WINDOW IN A TRANSACTION                                                                            |
| 14/315,713            | SMA13-0006US              | United States | 06/26/2014  |            | CONTROL CIRCUIT AND CONTROL METHOD FOR DIMMING A LIGHTING DEVICE                                                                         |
| 14/503,585            | SMA13-0007US              | United States | 10/01/2014  |            | ANALOG-DIGITAL CONVERSION SYSTEM AND METHOD FOR CONTROLLING THE SAME                                                                     |
| 14/464,783            | SMA14-0002US              | United States | 08/21/2014  |            | SWITCHING CIRCUIT                                                                                                                        |
| 14/446,678            | SMA14-0003US              | United States | 07/30/2014  |            | CRYSTAL OSCILLATION CIRCUIT                                                                                                              |
| 14/458,542            | SMA14-0004US              | United States | 08/13/2014  |            | INTEGRATION OF SEMICONDUCTOR MEMORY CELLS AND LOGIC CELLS                                                                                |
| 14/539,410            | SMA14-0006US              | United States | 11/12/2014  |            | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME                                                                               |
| 14/447,688            | SMA14-0007US              | United States | 07/31/2014  |            | CONTROL APPARATUS, BUCK-BOOST POWER SUPPLY AND CONTROL METHOD                                                                            |
| 14/448,442            | SMA14-0008US              | United States | 07/31/2014  |            | CONTROL APPARATUS, SWITCHING POWER SUPPLY AND CONTROL METHOD                                                                             |
| 14/472,043            | SMA14-0009US              | United States | 08/28/2014  |            | TEST CONTROL CIRCUIT, SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR TESTING THE SAME                                                        |
| 14/513,314            | SMA14-0010US              | United States | 10/14/2014  |            | CRYSTAL OSCILLATOR START-UP CIRCUIT                                                                                                      |
| 14/659,924            | SMA14-0013US              | United States | 03/17/2015  |            | DEVICE AND METHOD FOR RESISTING NON-INVASIVE ATTACKS                                                                                     |
| 14/517,201            | SMA14-0014US              | United States | 10/17/2014  |            | SIMULTANEOUS PROGRAMMING OF MANY BITS IN FLASH MEMORY                                                                                    |
| 14/536,015            | SMA14-0015US              | United States | 11/07/2014  |            | PROTECTING CIRCUIT AND INTEGRATED CIRCUIT                                                                                                |
| 14/619,592            | SMA14-0016US              | United States | 02/11/2015  |            | CONTROL CIRCUIT                                                                                                                          |
| 14/551,149            | SMA14-0018US              | United States | 11/24/2014  |            | TEMPERATURE DETECTION CIRCUIT AND TEMPERATURE MEASUREMENT CIRCUIT                                                                        |
| 14/635,459            | SMA14-0020US              | United States | 03/02/2015  |            | VOLTAGE DETECTOR AND METHOD FOR DETECTING VOLTAGE                                                                                        |
| 12/792,129            | SP09-0001US               | United States | 06/02/2010  |            | ELECTRONIC DEVICE HAVING A MOLDING COMPOUND INCLUDING A COMPOSITE MATERIAL                                                               |
| 61/221,485            | SP09-0001US PROV          | United States | 06/29/2009  |            | ELECTRONIC DEVICE HAVING A MOLDING COMPOUND INCLUDING ZINC                                                                               |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                                                             |
|-----------------------|---------------------------|---------------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8,208,296             | SP09-0003US               | United States | 02/16/2010  | 06/26/2012 | APPARATUS AND METHOD FOR EXTENDED NITRIDE LAYER IN A FLASH MEMORY                                                                                                                                                 |
| 8,877,641             | SP09-0004US               | United States | 12/28/2009  | 11/04/2014 | LINE EDGE ROUGHNESS IMPROVEMENT FOR SMALL PITCHES                                                                                                                                                                 |
| 14/517,470            | SP09-0004US DIV           | United States | 10/17/2014  |            | LINE EDGE ROUGHNESS IMPROVEMENT FOR SMALL PITCHES                                                                                                                                                                 |
| 12/960,411            | SP09-0007US               | United States | 12/03/2010  |            | METHOD AND APPARATUS FOR NAND MEMORY WITH RECESSED SOURCE/DRAIN REGION                                                                                                                                            |
| 8,836,012             | SP09-0008US               | United States | 10/04/2012  | 09/16/2014 | PROPOSED DUAL SPACER FORMATION                                                                                                                                                                                    |
| 8,114,756             | SP09-0012US               | United States | 08/04/2010  | 02/14/2012 | METHOD AND MANUFACTURE FOR HIGH VOLTAGE GATE OXIDE FORMATION AFTER SHALLOW TRENCH ISOLATION FORMATION                                                                                                             |
| 8,790,530             | SP09-0016US               | United States | 02/10/2010  | 07/29/2014 | PLANAR CELL ON CUT USING IN-SITU POLYMER DEPOSITION AND ETCH                                                                                                                                                      |
| 8,202,779             | SP09-0017US CIP           | United States | 09/27/2010  | 06/19/2012 | METHODS FOR FORMING A MEMORY CELL HAVING A TOP OXIDE SPACER                                                                                                                                                       |
| 7,943,980             | SP09-0017US DIV           | United States | 09/27/2010  | 05/17/2011 | METHODS FOR FORMING A MEMORY CELL HAVING A TOP OXIDE SPACER                                                                                                                                                       |
| 8,384,146             | SP09-0017US DIV2          | United States | 03/23/2012  | 02/26/2013 | METHODS FOR FORMING A MEMORY CELL HAVING A TOP OXIDE SPACER                                                                                                                                                       |
| 8,375,262             | SP09-0026US               | United States | 01/20/2010  | 02/12/2013 | FIELD PROGRAMMABLE REDUNDANT MEMORY FOR ELECTRONIC DEVICES                                                                                                                                                        |
| 8,825,920             | SP09-0027US               | United States | 01/20/2010  | 09/02/2014 | FIELD UPGRADABLE FIRMWARE FOR ELECTRONIC DEVICES                                                                                                                                                                  |
| 8,498,162             | SP09-0028US               | United States | 04/29/2011  | 07/30/2013 | FLASH MEMORY WRITE ALGORITHM WITH PULSE SKIPPING FOR FAST BITS                                                                                                                                                    |
| 8,842,477             | SP09-0030US               | United States | 06/01/2012  | 09/23/2014 | METHOD, APPARATUS, AND MANUFACTURE FOR FLASH MEMORY ADAPTIVE ALGORITHM                                                                                                                                            |
| 8,542,537             | SP09-0031US               | United States | 04/29/2011  | 09/24/2013 | METHOD AND APPARATUS FOR TEMPERATURE COMPENSATION FOR PROGRAMMING AND ERASE DISTRIBUTIONS IN A FLASH MEMORY                                                                                                       |
| 8,325,531             | SP09-0032US               | United States | 01/07/2010  | 12/04/2012 | MEMORY DEVICE                                                                                                                                                                                                     |
| 8,638,633             | SP09-0034US               | United States | 04/29/2011  | 01/28/2014 | APPARATUS AND METHOD FOR EXTERNAL CHARGE PUMP ON FLASH MEMORY MODULE                                                                                                                                              |
| 12/701,391            | SP09-0036US               | United States | 02/05/2010  |            | LAYOUT TO MASK METHODOLOGY FOR LAYERS REQUIRING DOUBLE PATTERNING                                                                                                                                                 |
| 8,244,964             | SP09-0037US               | United States | 12/23/2009  | 08/14/2012 | READ PREAMBLE FOR DATA CAPTURE OPTIMIZATION                                                                                                                                                                       |
| 8,551,858             | SP09-0039US CIP           | United States | 02/03/2010  | 10/08/2013 | SELF-ALIGNED SI RICH NITRIDE CHARGE TRAP LAYER ISOLATION FOR CHARGE TRAP FLASH MEMORY                                                                                                                             |
| 14/019,192            | SP09-0039US DIV           | United States | 09/05/2013  |            | SELF-ALIGNED SI RICH NITRIDE CHARGE TRAP LAYER ISOLATION FOR CHARGE TRAP FLASH MEMORY                                                                                                                             |
| 8,681,558             | SP09-0041US               | United States | 10/07/2009  | 03/25/2014 | PARALLEL BITLINE NONVOLATILE MEMORY EMPLOYING CHANNEL-BASED PROCESSING TECHNOLOGY                                                                                                                                 |
| 14/169,549            | SP09-0041US DIV           | United States | 01/31/2014  |            | PARALLEL BITLINE NONVOLATILE MEMORY EMPLOYING CHANNEL-BASED PROCESSING TECHNOLOGY                                                                                                                                 |
| 8,291,126             | SP09-0042US               | United States | 11/05/2012  | 05/13/2014 | VARIABLE READ LATENCY ON A SERIAL MEMORY BUS                                                                                                                                                                      |
| 8,725,920             | SP09-0042US               | United States | 03/23/2010  | 10/16/2012 | VARIABLE READ LATENCY ON A SERIAL MEMORY BUS                                                                                                                                                                      |
| 14/228,384            | SP09-0042US CON           | United States | 03/28/2014  |            | VARIABLE READ LATENCY ON A SERIAL MEMORY BUS                                                                                                                                                                      |
| 12/880,021            | SP09-0042US CON2          | United States | 09/10/2010  |            | APPARATUS, METHOD, AND MANUFACTURE FOR USING A READ PREAMBLE TO OPTIMIZE DATA CAPTURE                                                                                                                             |
| 8,349,685             | SP09-0044US               | United States | 12/03/2010  | 01/08/2013 | DUAL SPACER FORMATION IN FLASH MEMORY                                                                                                                                                                             |
| 12/722,014            | SP09-0046US               | United States | 03/11/2010  |            | NAND ARRAY SOURCE DRAIN DOPING SCHEME SELF-ALIGNED TO ARRAY MINI-SPACER                                                                                                                                           |
| 8,686,492             | SP09-0047US               | United States | 03/11/2010  | 04/01/2014 | NON-VOLATILE FINFET MEMORY DEVICE AND MANUFACTURING METHOD THEREOF                                                                                                                                                |
| 8,785,275             | SP09-0047US DIV           | United States | 02/03/2014  | 07/22/2014 | NON-VOLATILE FINFET MEMORY DEVICE AND MANUFACTURING METHOD THEREOF                                                                                                                                                |
| 8,598,646             | SP09-0048US               | United States | 01/13/2011  | 12/03/2013 | NON-VOLATILE FINFET MEMORY ARRAY AND MANUFACTURING METHOD THEREOF                                                                                                                                                 |
| 14/051,584            | SP09-0048US DIV           | United States | 10/11/2013  |            | NON-VOLATILE FINFET MEMORY ARRAY AND MANUFACTURING METHOD THEREOF                                                                                                                                                 |
| 8,134,853             | SP09-0049US               | United States | 12/18/2009  | 03/13/2012 | HIGH READ SPEED ELECTRONIC MEMORY WITH SERIAL ARRAY TRANSISTORS                                                                                                                                                   |
| 8,279,674             | SP09-0049US B             | United States | 06/28/2010  | 10/02/2012 | HIGH READ SPEED MEMORY WITH GATE ISOLATION                                                                                                                                                                        |
| 8,520,437             | SP09-0049US CON           | United States | 08/31/2012  | 08/27/2013 | HIGH READ SPEED MEMORY WITH GATE ISOLATION                                                                                                                                                                        |
| 8,291,165             | SP09-0050US               | United States | 03/12/2010  | 10/16/2012 | ELECTRONIC DEVICES USING REMOVABLE AND PROGRAMMABLE ACTIVE PROCESSING MODULES                                                                                                                                     |
| 12/723,590            | SP09-0051US               | United States | 03/12/2010  |            | HOME AND BUILDING AUTOMATION                                                                                                                                                                                      |
| 12/723,582            | SP09-0052US               | United States | 03/12/2010  |            | SYSTEM AND METHODS FOR CONTROLLING AN ELECTRONIC DEVICE                                                                                                                                                           |
| 6,995,437             | SP09-0053                 | United States | 06/16/2004  | 02/07/2006 | METHOD OF FORMING CORE AND PERIPHERY GATES INCLUDING TWO CRITICAL MASKING STEPS TO FORM A HARD MASK IN A CORE REGION THAT INCLUDES A CRITICAL DIMENSION LESS THAN ACHIEVABLE AT A RESOLUTION LIMIT OF LITHOGRAPHY |
| 8,417,874             | SP09-0053US               | United States | 01/21/2010  | 04/09/2013 | A PROGRAMMABLE READ PREAMBLE                                                                                                                                                                                      |
| 8,990,605             | SP09-0054US               | United States | 09/10/2010  | 03/24/2015 | APPARATUS AND METHOD FOR READ PREAMBLE DISABLE                                                                                                                                                                    |
| 8,140,778             | SP09-0055US               | United States | 09/10/2010  | 03/20/2012 | APPARATUS AND METHOD FOR DATA CAPTURE USING A READ PREAMBLE                                                                                                                                                       |
| 13/566,187            | SP09-0058US               | United States | 08/03/2012  |            | POWER SAVINGS APPARATUS AND METHOD FOR MEMORY DEVICE USING DELAY LOCKED LOOP                                                                                                                                      |
| 8,625,353             | SP09-0061US               | United States | 06/16/2011  | 01/07/2014 | METHOD, APPARATUS, AND MANUFACTURE FOR STAGGERED START FOR MEMORY MODULE                                                                                                                                          |
| 14/099,340            | SP09-0061US CON           | United States | 12/06/2013  |            | METHOD AND APPARATUS FOR STAGGERED START-UP OF A PREDEFINED, RANDOM, OR DYNAMIC NUMBER OF FLASH MEMORY DEVICES                                                                                                    |
| 12/964,523            | SP09-0072US               | United States | 12/09/2010  |            | HIGH PERFORMANCE LOW PROFILE QFN/LGA                                                                                                                                                                              |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                                                                             |
|-----------------------|---------------------------|---------------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13/046,433            | SP09-0073US               | United States | 03/11/2011  |            | MIXED WIRE BONDING PROFILE AND PAD-LAYOUT CONFIGURATIONS IN IC PACKAGING PROCESSES FOR HIGH-SPEED ELECTRONIC DEVICES                                                                                              |
| 8,276,104             | SP09-0075US               | United States | 12/09/2010  | 09/25/2012 | STRESS REDUCTION ON VIAS AND YIELD IMPROVEMENT IN LAYOUT DESIGN THROUGH AUTO GENERATION OF VIA FILL                                                                                                               |
| 14/135,863            | SP10-0003US               | United States | 12/20/2013  |            | CT-NOR DIFFERENTIAL BITLINE SENSING ARCHITECTURE                                                                                                                                                                  |
| 8,818,802             | SP10-0004US               | United States | 10/07/2009  | 08/26/2014 | REAL-TIME DATA PATTERN ANALYSIS SYSTEM AND METHOD OF OPERATION THEREOF                                                                                                                                            |
| 14/258,076            | SP10-0004US CON           | United States | 04/22/2014  |            | DATA PATTERN ANALYSIS (as amended)                                                                                                                                                                                |
| 12/979,654            | SP10-0005US               | United States | 12/28/2010  |            | SYSTEM, METHOD AND APPARATUS FOR REDUCING PLASMA NOISE ON POWER PATH OF ELECTRONSTATIC CHUCK                                                                                                                      |
| 13/669,633            | SP10-0006US               | United States | 11/06/2012  |            | WEAR LEVELING IN FLASH MEMORY DEVICES WITH TRIM COMMANDS                                                                                                                                                          |
| 8,461,053             | SP10-0007US               | United States | 12/17/2010  | 06/11/2013 | SELF-ALIGNED NAND FLASH SELECT-GATE WORDLINES FOR SPACER DOUBLE PATTERNING                                                                                                                                        |
| 8,874,253             | SP10-0007US DIV           | United States | 05/14/2013  | 10/28/2014 | SELF-ALIGNED NAND FLASH SELECT-GATE WORDLINES FOR SPACER DOUBLE PATTERNING                                                                                                                                        |
| 12/973,756            | SP10-0008US               | United States | 12/20/2010  |            | EDGE ROUNDED FIELD EFFECT TRANSISTORS AND METHODS OF MANUFACTURING                                                                                                                                                |
| 8,263,458             | SP10-0009US               | United States | 12/20/2010  | 09/11/2012 | PROCESS MARGIN ENGINEERING IN CHARGE TRAPPING FIELD EFFECT TRANSISTORS                                                                                                                                            |
| 8,652,907             | SP10-0010US               | United States | 03/24/2011  | 02/18/2014 | METHOD AND MANUFACTURE FOR HIGH VOLTAGE GATE OXIDE FORMATION AFTER SHALLOW TRENCH ISOLATION FORMATION                                                                                                             |
| 14/149,521            | SP10-0010US DIV           | United States | 01/07/2014  |            | INTEGRATING TRANSISTORS WITH DIFFERENT POLY-SILICON HEIGHTS ON THE SAME DIE                                                                                                                                       |
| 8,598,005             | SP10-0011US               | United States | 07/18/2011  | 12/03/2013 | METHOD AND MANUFACTURE FOR EMBEDDED FLASH TO ACHIEVE HIGH QUALITY SPACERS FOR CORE AND HIGH VOLTAGE DEVICES AND LOW TEMPERATURE SPACERS FOR HIGH PERFORMANCE LOGIC DEVICES                                        |
| 8,441,063             | SP10-0012US               | United States | 12/30/2010  | 05/14/2013 | MEMORY WITH EXTENDED CHARGE TRAPPING LAYER                                                                                                                                                                        |
| 8,809,206             | SP10-0013US               | United States | 02/07/2011  | 08/19/2014 | PATTERNED DUMMY WAFERS LOADING IN BATCH TYPE CVD                                                                                                                                                                  |
| 13/662,090            | SP10-0016US               | United States | 10/26/2012  |            | HRHP (HIGH-RELIABILITY HIGH-PERFORMANCE) NAND MEMORY CELL                                                                                                                                                         |
| 8,791,007             | SP11-0005US               | United States | 11/29/2011  | 07/29/2014 | DEVICE HAVING MULTIPLE WIRE BONDS FOR A BOND AREA AND METHODS THEREOF                                                                                                                                             |
| 8,536,908             | SP11-0012US               | United States | 09/29/2011  | 09/17/2013 | SMART VCC TRIP POINT MEASUREMENT                                                                                                                                                                                  |
| 8,981,823             | SP11-0012US DIV           | United States | 08/21/2013  | 03/17/2015 | APPARATUS AND METHOD FOR SMART VCC TRIP POINT DESIGN FOR TESTABILITY                                                                                                                                              |
| 6,780,708             | SP11-0015TW               | United States | 03/05/2003  | 08/24/2004 | METHOD OF FORMING CORE AND PERIPHERY GATES INCLUDING TWO CRITICAL MASKING STEPS TO FORM A HARD MASK IN A CORE REGION THAT INCLUDES A CRITICAL DIMENSION LESS THAN ACHIEVABLE AT A RESOLUTION LIMIT OF LITHOGRAPHY |
| 8,966,151             | SP11-0021US               | United States | 03/30/2012  | 02/24/2015 | A LOW PIN COUNT HIGH SPEED PERIPHERAL INTERFACE                                                                                                                                                                   |
| 13/269,423            | SP11-0025US               | United States | 10/07/2011  |            | CONTROL OF SEMICONDUCTOR MANUFACTURING PROCESSES                                                                                                                                                                  |
| 13/540,373            | SP11-0027PCT              | United States | 07/02/2012  |            | APPARATUS AND METHOD FOR ROUNDED ONO FORMATION IN A FLASH MEMORY DEVICE                                                                                                                                           |
| 8,799,598             | SP11-0027US               | United States | 02/17/2012  | 08/05/2014 | REDUNDANCY LOADING EFFICIENCY                                                                                                                                                                                     |
| 13/856,313            | SP11-0028PCT              | United States | 04/03/2013  |            | MODIFIED LOCAL SEGMENTED SELF-BOOSTING OF MEMORY CELL CHANNEL                                                                                                                                                     |
| 8,806,071             | SP11-0030PCT              | United States | 01/25/2012  | 08/12/2014 | CONTINUOUS READ BURST SUPPORT AT HIGH CLOCK RATES                                                                                                                                                                 |
| 13/678,255            | SP11-0034TW               | United States | 11/15/2012  |            | CONTROL OF SEMICONDUCTOR PROCESSING TOOLS USING A HIERARCHICAL ORGANIZATION OF DATA                                                                                                                               |
| 13/735,650            | SP11-0038US               | United States | 01/07/2013  |            | MULTI-CHIP PACKAGE ASSEMBLY WITH IMPROVED BOND WIRE SEPARATION                                                                                                                                                    |
| 5,630,099             | SP11-0039PCT              | United States | 12/10/1993  | 05/13/1997 | NON-VOLATILE MEMORY ARRAY CONTROLLER CAPABLE OF CONTROLLING MEMORY BANKS HAVING VARIABLE BIT WIDTHS                                                                                                               |
| 13/725,260            | SP11-0040US               | United States | 12/21/2012  |            | HIDDEN MARKOV MODEL ACCELERATOR FOR SPEECH RECOGNITION                                                                                                                                                            |
| 13/489,799            | SP11-0042US               | United States | 06/06/2012  |            | ACOUSTIC PROCESSING UNIT                                                                                                                                                                                          |
| 61/577,595            | SP11-0042US PROV          | United States | 12/19/2011  |            | ACOUSTIC PROCESSING UNIT                                                                                                                                                                                          |
| 13/856,614            | SP11-0043US               | United States | 04/04/2013  |            | ACOUSTIC PROCESSING UNIT WITH PARALLEL SPEAKER ADAPTATION                                                                                                                                                         |
| 13/524,584            | SP11-0044US               | United States | 06/15/2012  |            | POWER-EFFICIENT VOICE ACTIVATION                                                                                                                                                                                  |
| 61/589,113            | SP12-0003US PROV          | United States | 01/20/2012  |            | HW/SW ARCHITECTURE FOR SPEECH RECOGNITION                                                                                                                                                                         |
| 8,972,652             | SP12-0004US               | United States | 11/19/2012  | 03/03/2015 | LOW OVERHEAD FLASH BLOCK REFRESH                                                                                                                                                                                  |
| 8,901,756             | SP12-0012US               | United States | 12/21/2012  | 12/02/2014 | CHIP POSITIONING IN MULTI-CHIP PACKAGE                                                                                                                                                                            |
| 14/532,039            | SP12-0012US DIV           | United States | 11/04/2014  |            | CHIP POSITIONING IN MULTI-CHIP PACKAGE                                                                                                                                                                            |
| 8,724,388             | SP12-0013US               | United States | 04/02/2012  | 05/13/2014 | ADAPTIVELY PROGRAMMING OR ERASING FLASH MEMORY BLOCKS                                                                                                                                                             |
| 14/270,700            | SP12-0015US               | United States | 05/06/2014  |            | METHOD TO IMPROVE CHARGE TRAP FLASH MEMORY TOP OXIDE QUALITY                                                                                                                                                      |
| 8,835,277             | SP12-0016US               | United States | 11/19/2012  | 09/16/2014 | METHOD TO IMPROVE CHARGE TRAP FLASH MEMORY CORE CELL PERFORMANCE AND RELIABILITY                                                                                                                                  |
| 14/486,421            | SP12-0016US CON           | United States | 09/15/2014  |            | METHOD TO IMPROVE CHARGE TRAP FLASH MEMORY CORE CELL PERFORMANCE AND RELIABILITY                                                                                                                                  |
| 13/545,469            | SP12-0017US               | United States | 07/10/2012  |            | LEAKAGE REDUCING WRITELINE CHARGE PROTECTION CIRCUIT                                                                                                                                                              |
| 13/901,167            | SP12-0019US               | United States | 05/23/2013  |            | DIFFERENTIAL FILE SYSTEM FOR COMPUTER MEMORY                                                                                                                                                                      |
| 8,699,273             | SP12-0021US               | United States | 07/31/2012  | 04/15/2014 | BITLINE VOLTAGE REGULATION IN NON-VOLATILE MEMORY                                                                                                                                                                 |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                        |
|-----------------------|---------------------------|---------------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8,848,452             | SP12-0022US               | United States | 04/04/2013  | 09/30/2014 | ERASE VERIFICATION CIRCUITRY FOR SIMULTANEOUSLY AND CONSECUTIVELY VERIFYING A PLURALITY OF ODD AND EVEN-NUMBERED FLASH MEMORY TRANSISTORS AND METHOD THEREOF |
| 13/761,217            | SP12-0023US               | United States | 02/07/2013  |            | IMPROVED NON-VOLATILE MEMORY DEVICE                                                                                                                          |
| 14/095,150            | SP12-0025US               | United States | 12/03/2013  |            | REDUCTION OF CHARGING INDUCED DAMAGE IN PHOTOLITHOGRAPHY WET PROCESS                                                                                         |
| 8,866,213             | SP12-0026US               | United States | 01/30/2013  | 10/21/2014 | NON-VOLATILE MEMORY WITH SILICIDED BIT LINE CONTACTS                                                                                                         |
| 14/501,536            | SP12-0026US DIV           | United States | 09/30/2014  |            | NON-VOLATILE MEMORY WITH SILICIDED BIT LINE CONTACTS                                                                                                         |
| 13/737,321            | SP12-0027US               | United States | 01/09/2013  |            | PROGRAMMABLE AND FLEXIBLE REFERENCE CELL SELECTION METHOD FOR MEMORY DEVICES                                                                                 |
| 8,975,185             | SP12-0028US               | United States | 11/26/2012  | 03/10/2015 | METHOD FOR FORMING CHARGE TRAP SEPARATION IN A FLASH MEMORY SEMICONDUCTOR DEVICE                                                                             |
| 14/626,815            | SP12-0028US DIV           | United States | 02/19/2015  |            | FORMING CHARGE TRAP SEPARATION IN A FLASH MEMORY SEMICONDUCTOR DEVICE                                                                                        |
| 13/685,222            | SP12-0029US               | United States | 11/26/2012  |            | FORMING A SUBSTANTIALLY UNIFORM WING HEIGHT AMONG ELEMENTS IN A CHARGE TRAP SEMICONDUCTOR DEVICE                                                             |
| 13/725,415            | SP12-0030US               | United States | 12/21/2012  |            | MEMORY DEVICE INTERNAL DATA SEARCH                                                                                                                           |
| 8,996,374             | SP12-0031US               | United States | 11/06/2012  | 03/31/2015 | SENONE SCORING FOR MULTIPLE INPUT STREAMS                                                                                                                    |
| 8,760,930             | SP12-0032PCT              | United States | 02/18/2013  | 06/24/2014 | MEMORY DEVICE WITH SOURCE-SIDE SENSING                                                                                                                       |
| 13/725,173            | SP12-0033US               | United States | 12/21/2012  |            | HYBRID HASHING SCHEME FOR ACTIVE HMMS IN SPEECH RECOGNITION                                                                                                  |
| 13/644,895            | SP12-0034US               | United States | 10/04/2012  |            | SUPPLY POWER DEPENDENT CONTROLLABLE WRITE THROUGHPUT FOR MEMORY APPLICATIONS                                                                                 |
| 13/860,542            | SP12-0035US               | United States | 04/11/2013  |            | RESTORING ECC SYNDROME IN NON-VOLATILE MEMORY DEVICES                                                                                                        |
| 13/725,224            | SP12-0036US               | United States | 12/21/2012  |            | HISTOGRAM BASED PRE-PRUNING SCHEME FOR ACTIVE HMMS (as amended)                                                                                              |
| 8,964,484             | SP12-0037US               | United States | 12/28/2012  | 02/24/2015 | DESIGN FOR TEST (DFT) READ SPEED THROUGH TRANSITION DETECTOR IN BUILT-IN SELF-TEST (BIST) SORT                                                               |
| 13/735,156            | SP12-0041US               | United States | 01/07/2013  |            | BURIED HARD MASK FOR EMBEDDED SEMICONDUCTOR DEVICE PATTERNING                                                                                                |
| 9,009,049             | SP12-0042US               | United States | 11/06/2012  | 04/14/2015 | RECOGNITION OF SPEECH WITH DIFFERENT ACCENTS                                                                                                                 |
| 8,912,093             | SP12-0043US               | United States | 04/18/2013  | 12/16/2014 | DIE SEAL LAYOUT FOR VFTL DUAL DAMASCENE IN A SEMICONDUCTOR DEVICE                                                                                            |
| 14/566,462            | SP12-0043US DIV           | United States | 12/10/2014  |            | DIE SEAL LAYOUT FOR VFTL DUAL DAMASCENE IN A SEMICONDUCTOR DEVICE                                                                                            |
| 14/108,780            | SP12-0044US               | United States | 12/17/2013  |            | PROCESS FOR FORMING EDGE WORLDLINE IMPLANTS ADJACENT EDGE WORDLINES                                                                                          |
| 13/682,826            | SP12-0045US               | United States | 11/21/2012  |            | INTER-LAYER INSULATOR FOR ELECTRON DEVICES                                                                                                                   |
| 13/678,025            | SP12-0046US               | United States | 11/15/2012  |            | DISTRIBUTION OF GAS OVER A SEMICONDUCTOR WAFER IN BATCH PROCESSING (as amended)                                                                              |
| 13/790,979            | SP12-0051US               | United States | 03/08/2013  |            | PIPELINING IN A MEMORY                                                                                                                                       |
| 13/736,618            | SP12-0054US               | United States | 01/08/2013  |            | DISTRIBUTED SPEECH RECOGNITION SYSTEM                                                                                                                        |
| 62/044,609            | SP12-0055US PROV          | United States | 09/02/2014  |            | PULSE DRIVEN SYNCHRONIZER                                                                                                                                    |
| 13/917,141            | SP12-0060US               | United States | 06/13/2013  |            | SCREENING FOR REFERENCE CELLS IN A MEMORY                                                                                                                    |
| 13/867,618            | SP12-0064US               | United States | 04/22/2013  |            | CHARGE-TRAP NOR WITH SILICON-RICH NITRIDE AS A CHARGE TRAP LAYER                                                                                             |
| 8,836,006             | SP12-0067US               | United States | 12/14/2012  | 09/16/2014 | INTEGRATED CIRCUITS WITH NON-VOLATILE MEMORY AND METHODS FOR MANUFACTURE                                                                                     |
| 14/484,417            | SP12-0067US DIV           | United States | 09/12/2014  |            | INTEGRATED CIRCUITS WITH NON-VOLATILE MEMORY AND METHODS FOR MANUFACTURE                                                                                     |
| 8,822,289             | SP12-0068US               | United States | 12/14/2012  | 09/02/2014 | HIGH VOLTAGE GATE FORMATION                                                                                                                                  |
| 14/340,054            | SP12-0068US DIV           | United States | 07/24/2014  |            | HIGH VOLTAGE GATE FORMATION                                                                                                                                  |
| 13/715,577            | SP12-0069US               | United States | 12/14/2012  |            | MEMORY FIRST PROCESS FLOW AND DEVICE                                                                                                                         |
| 13/715,582            | SP12-0070US               | United States | 12/14/2012  |            | CHARGE TRAPPING SPLIT GATE EMBEDDED FLASH MEMORY AND ASSOCIATED METHODS                                                                                      |
| 13/715,181            | SP12-0072US               | United States | 12/14/2012  |            | THREE DIMENSIONAL CAPACITOR                                                                                                                                  |
| 13/715,673            | SP12-0073US               | United States | 12/14/2012  |            | USE DISPOSABLE GATE CAP TO FORM TRANSISTORS, AND SPLIT GATE CHARGE TRAPPING MEMORY CELLS                                                                     |
| 8,816,438             | SP12-0074US               | United States | 12/14/2012  | 08/26/2014 | PROCESS CHARGING PROTECTION FOR SPLIT GATE CHARGE TRAPPING FLASH                                                                                             |
| 13/715,185            | SP12-0075US               | United States | 12/14/2012  |            | CHARGE TRAPPING SPLIT GATE DEVICE AND METHOD OF FABRICATING SAME                                                                                             |
| 13/715,729            | SP12-0076US               | United States | 12/14/2012  |            | CHARGE TRAPPING DEVICE WITH IMPROVED SELECT GATE TO MEMORY GATE ISOLATION                                                                                    |
| 13/715,828            | SP12-0076US               | United States | 12/14/2012  |            | MEMORY GATE LANDING PAD MADE FROM DUMMY FEATURE                                                                                                              |
| 14/056,577            | SP12-0077US               | United States | 10/17/2013  |            | THREE-DIMENSIONAL CHARGE TRAPPING NAND CELL WITH DISCRETE CHARGE TRAPPING FILM                                                                               |
| 13/756,134            | SP12-0079US               | United States | 01/31/2013  |            | MANUFACTURING OF FET DEVICES HAVING LIGHTLY DOPED DRAIN AND SOURCE REGIONS                                                                                   |
| 13/856,671            | SP12-0081US               | United States | 04/04/2013  |            | AUTHENTICATION FOR RECOGNITION SYSTEMS                                                                                                                       |
| 14/073,031            | SP12-0084US               | United States | 11/06/2013  |            | METHODS, CIRCUITS, SYSTEMS AND COMPUTER EXECUTABLE INSTRUCTION SETS FOR PROVIDING ERROR CORRECTION OF STORED DATA AND DATA STORAGE DEVICES UTILIZING SAME    |
| 6,205,057             | SP12-0086US               | United States | 02/15/2000  | 03/20/2001 | SYSTEM AND METHOD FOR DETECTING FLASH MEMORY THRESHOLD VOLTAGES                                                                                              |
| 14/056,547            | SP13-0003US               | United States | 10/17/2013  |            | MULTIPLE PHASE-SHIFT PHOTOMASK AND SEMICONDUCTOR MANUFACTURING METHOD                                                                                        |
| 14/054,880            | SP13-0004US               | United States | 10/16/2013  |            | MEMORY PROGRAM UPON SYSTEM FAILURE                                                                                                                           |
| 14/051,828            | SP13-0006US               | United States | 10/11/2013  |            | SPACER FORMATION WITH STRAIGHT SIDEWALL                                                                                                                      |
| 14/143,317            | SP13-0007US               | United States | 12/30/2013  |            | FORMATION OF GATE SIDEWALL STRUCTURE                                                                                                                         |
| 14/136,358            | SP13-0008US               | United States | 12/20/2013  |            | GATE FORMATION MEMORY BY PLANARIZATION                                                                                                                       |

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| PATENT OR APPL NO. | SPANSION REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                    |
|--------------------|------------------------|---------------|-------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13/913,909         | SP13-0009US            | United States | 06/10/2013  |            | PROGRAMMABLE LATENCY COUNT TO ACHIEVE HIGHER MEMORY BANDWIDTH                                                                                            |
| 14/054,265         | SP13-0010US            | United States | 10/15/2013  |            | METHOD FOR PROVIDING READ DATA FLOW CONTROL OR ERROR REPORTING USING A READ DATA STROBE                                                                  |
| 14/051,859         | SP13-0012US            | United States | 10/11/2013  |            | ION IMPLANTATION-ASSISTED ETCH-BACK PROCESS FOR IMPROVING SPACER SHAPE AND SPACER WIDTH CONTROL                                                          |
| 14/054,884         | SP13-0013US            | United States | 10/16/2013  |            | HIDDEN MARKOV MODEL PROCESSING ENGINE                                                                                                                    |
| 8,995,198          | SP13-0014US            | United States | 10/10/2013  | 03/31/2015 | MULTI-PASS SOFT PROGRAMMING                                                                                                                              |
| 14/048,527         | SP13-0015US            | United States | 10/08/2013  |            | BURIED TRENCH ISOLATION IN INTEGRATED CIRCUITS                                                                                                           |
| 14/054,312         | SP13-0016US            | United States | 10/15/2013  |            | MANAGED-NAND WITH EMBEDDED RANDOM-ACCESS NON-VOLATILE MEMORY                                                                                             |
| 14/093,703         | SP13-0017US            | United States | 12/02/2013  |            | GENERATION OF WAKE-UP WORDS                                                                                                                              |
| 14/048,863         | SP13-0019US            | United States | 10/08/2013  |            | SELF-ALIGNED TRENCH ISOLATION IN INTEGRATED CIRCUITS                                                                                                     |
| 14/092,554         | SP13-0025US            | United States | 11/27/2013  |            | AUTO RESUME OF IRREGULAR ERASE STOPPAGE OF A MEMORY SECTOR                                                                                               |
| 14/207,303         | SP13-0029US            | United States | 03/12/2014  |            | BURIED TRENCH ISOLATION IN INTEGRATED CIRCUITS                                                                                                           |
| 14/284,727         | SP13-0030US            | United States | 05/22/2014  |            | OFFSET COMPENSATED HIGH SPEED LOW POWER SENSE AMPLIFIER                                                                                                  |
| 14/132,422         | SP13-0031US            | United States | 12/18/2013  |            | INCREASING LITHOGRAPHIC DEPTH-OF-FOCUS WINDOW USING WAFER TOPOGRAPHY                                                                                     |
| 14/100,673         | SP13-0032US            | United States | 12/09/2013  |            | SCATTERING BAR OPTIMIZATION APPARATUS AND METHOD                                                                                                         |
| 14/188,048         | SP13-0036US            | United States | 02/24/2014  |            | MEMORY SUBSYSTEM WITH WRAPPED-TO-CONTINUOUS READ                                                                                                         |
| 62/040,583         | SP13-0040US PROV       | United States | 08/22/2014  |            | PARTIAL-PARTIAL-HEIGHT GATE REPLACEMENT FOR SEMICONDUCTOR DEVICE FABRICATION                                                                             |
| 14/284,632         | SP13-0041US            | United States | 05/22/2014  |            | METHODS, CIRCUITS, DEVICES, AND SYSTEMS FOR SENSING AN NVN CELL                                                                                          |
| 14/284,812         | SP13-0042US            | United States | 05/22/2014  |            | HV STITCHING PROTECTED CURRENT CONTROLLED LEVEL SHIFTER                                                                                                  |
| 14/527,797         | SP13-0045US            | United States | 10/30/2014  |            | CHARGE-TRAPPING MEMORY DEVICE                                                                                                                            |
| 14/199,837         | SP13-0046US            | United States | 03/06/2014  |            | MEMORY ACCESS BASES ON ERASE CYCLE TIME                                                                                                                  |
| 14/278,114         | SP13-0048US            | United States | 05/15/2014  |            | TILTED IMPLANT FOR POLY RESISTORS                                                                                                                        |
| 14/319,079         | SP13-0049US            | United States | 06/30/2014  |            | BOOTING AN APPLICATION FROM MULTIPLE MEMORIES                                                                                                            |
| 14/518,560         | SP13-0050US            | United States | 10/20/2014  |            | OVERLAID ERASE BLOCK MAPPING                                                                                                                             |
| 14/450,727         | SP14-0001US            | United States | 08/04/2014  |            | SPLIT-GATE SEMICONDUCTOR DEVICE WITH L-SHAPED GATE                                                                                                       |
| 14/513,361         | SP14-0005US            | United States | 10/14/2014  |            | SYSTEM-ON-CHIP VERIFICATION                                                                                                                              |
| 14/562,789         | SP14-0006US            | United States | 12/08/2014  |            | METHODS, CIRCUITS, DEVICES, SYSTEMS AND MACHINE EXECUTABLE CODE FOR READING FROM A NON-VOLATILE MEMORY ARRAY                                             |
| 5,376,573          | TT0313JP               | United States | 12/10/1993  | 12/27/1994 | FLASH EPROM DEVICE UTILIZING A SINGLE MASKING STEP FOR ETCHING AND IMPLANTING SOURCE REGIONS WITHIN THE EPROM CORE AND REDUNDANCY AREAS                  |
| 5,801,076          | TT0347JP               | United States | 02/21/1995  | 09/01/1998 | METHOD OF MAKING NON-VOLATILE MEMORY DEVICE HAVING A FLOATING GATE WITH ENHANCED CHARGE RETENTION                                                        |
| 5,384,272          | TT0347US               | United States | 06/28/1994  | 01/24/1995 | METHOD FOR MANUFACTURING A NON-VOLATILE, VIRTUAL GROUND MEMORY ELEMENT                                                                                   |
| 5,581,502          | TT0497KR               | United States | 05/02/1995  | 12/03/1996 | METHOD FOR READING A NON-VOLATILE MEMORY ARRAY                                                                                                           |
| 5,805,013          | TT0497US               | United States | 03/12/1997  | 09/08/1998 | A NON-VOLATILE MEMORY DEVICES HAVING A FLOATING GATE WITH ENHANCED CHARGE RETENTION                                                                      |
| 5,546,340          | TT0607KR               | United States | 06/13/1995  | 08/13/1996 | NON-VOLATILE MEMORY ARRAY WITH OVER-ERASE CORRECTION                                                                                                     |
| 5,896,393          | TT0694US               | United States | 05/23/1996  | 04/20/1999 | SIMPLIFIED FILE MANAGEMENT SCHEME FOR FLASH MEMORY                                                                                                       |
| 5,811,334          | TT0866US               | United States | 12/29/1995  | 09/22/1998 | WAFER CLEANING PROCEDURE USEFUL IN MANUFACTURE OF A NON-VOLATILE MEMORY DEVICE                                                                           |
| 09/063,114         | TT0867US               | United States | 04/20/1998  |            | WAFER CLEANING PROCEDURE USEFUL IN MANUFACTURE OF A NON-VOLATILE MEMORY DEVICE                                                                           |
| 5,774,395          | TT0867US DIV           | United States | 11/27/1996  | 06/30/1998 | AN ELECTRICALLY ERASABLE REFERENCE CELL FOR ACCURATELY DETERMINING THRESHOLD VOLTAGE OF A NON-VOLATILE MEMORY AT A PLURALITY OF THRESHOLD VOLTAGE LEVELS |
| 6,823,435          | TT1328US               | United States | 11/20/1997  | 11/23/2004 | A NON-VOLATILE MEMORY SYSTEM HAVING A PROGRAMMABLY SELECTABLE BOOT CODE SECTION SIZE                                                                     |
| 7,206,914          | TT1393US               | United States | 10/19/2004  | 04/17/2007 | A NON-VOLATILE MEMORY SYSTEM HAVING A PROGRAMMABLY SELECTABLE BOOT CODE SECTION SIZE                                                                     |
| 5,999,476          | TT1393US CON           | United States | 11/21/1997  | 12/07/1999 | BIOS MEMORY AND MULTIMEDIA DATA STORAGE COMBINATION                                                                                                      |
| 5,717,632          | TT1396US               | United States | 11/27/1996  | 02/10/1998 | APPARATUS AND METHOD FOR MULTIPLE-LEVEL STORAGE IN NON-VOLATILE MEMORIES                                                                                 |
| 5,883,841          | TT1514US               | United States | 09/26/1997  | 03/16/1999 | SELECTIVE BIT LINE RECOVERY IN A MEMORY ARRAY                                                                                                            |
| 5,883,826          | TT1997US               | United States | 09/26/1997  | 03/16/1999 | MEMORY BLOCK SELECT USING MULTIPLE WORD LINES TO ADDRESS A SINGLE MEMORY CELL ROW                                                                        |
| 5,888,870          | TT2013US               | United States | 10/22/1997  | 03/30/1999 | MEMORY CELL FABRICATION EMPLOYING AN INTERPOLY GATE DIELECTRIC ARRANGED UPON A POLISHED FLOATING GATE                                                    |
| 6,048,766          | TT2035US               | United States | 10/14/1998  | 04/11/2000 | FLASH MEMORY DEVICE HAVING HIGH PERMITTIVITY STACKED DIELECTRIC AND FABRICATION THEREOF                                                                  |
| 6,417,539          | TT2307US               | United States | 08/04/1998  | 07/09/2002 | HIGH DENSITY MEMORY CELL ASSEMBLY AND METHODS                                                                                                            |
| 6,480,929          | TT2360US               | United States | 10/31/1998  | 11/12/2002 | PSEUDO- CONCURRENCY BETWEEN A VOLATILE MEMORY AND A NON-VOLITILE MEMORY ON A SAME DATA BUS                                                               |
| 6,225,646          | TT2492US               | United States | 01/14/2000  | 05/01/2001 | INTEGRATED CIRCUIT INCORPORATING A MEMORY CELL AND A TRANSISTOR ELEVATED ABOVE AN INSULATING BASE                                                        |
| 6,790,752          | TT3073US               | United States | 02/05/2003  | 09/14/2004 | METHODS OF CONTROLLING Vss IMPLANTS ON MEMORY DEVICES, AND SYSTEM FOR PERFORMING SAME                                                                    |
| 7,197,657          | TT5267US               | United States | 04/03/2003  | 03/27/2007 | BMC-HOSTED REAL-TIME CLOCK AND NON-VOLATILE RAM REPLACEMENT                                                                                              |
| 10/633,797         | TT5422US               | United States | 08/04/2003  |            | METHODS OF FORMING METAL SILICIDE REGIONS, AND SYSTEMS FOR PERFORMING SAME                                                                               |

# ASSIGNMENT SCHEDULE A

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY       | FILING DATE | ISSUE DATE | TITLE                                                                                                                                     |
|-----------------------|---------------------------|---------------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| 7,816,203             | TT5548US                  | United States | 03/16/2006  | 10/19/2010 | METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE                                                                                             |
| 6,670,616             | TT5847US                  | United States | 03/22/2002  | 12/30/2003 | ULTRAVIOLET-RAY IRRADIATION APPARATUS                                                                                                     |
| PCT/US2000/27903      | AF01002PCT                | WIPO          | 10/07/2000  |            | LOW VOLTAGE READ CASCODE FOR 2V/3V AND DIFFERENT BANK COMBINATIONS WITHOUT METAL OPTIONS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE |
| PCT/US2001/024109     | AF01073WO                 | WIPO          | 07/31/2001  |            | WORD LINE DECODING ARCHITECTURE IN A FLASH MEMORY                                                                                         |
| PCT/US01/24024        | AF01081US                 | WIPO          | 07/30/2001  |            | BURST READ WORDLINE BOOSTING                                                                                                              |
| PCT/US2001/018081     | AF01085WO                 | WIPO          | 06/04/2001  |            | METHOD TO REDUCE CAPACITIVE LOADING IN FLASH MEMORY X-DECODER FOR ACCURATE VOLTAGE CONTROL AT WORDLINES AND SELECT LINES                  |
| PCT/US2000/026814     | AF01086WO                 | WIPO          | 09/29/2000  |            | WORD LINE TRACKING IN WHOLE CHIP                                                                                                          |
| PCT/US2001/43543      | AF01090PC                 | WIPO          | 11/14/2001  |            | I/O PARTITIONING AND METHODOLOGY TO REDUCE BAND-TO-BAND TUNNELING CURRENT DURING ERASE                                                    |
| PCT/US2002/031331     | AF01091PCT                | WIPO          | 09/30/2002  |            | DRAIN SIDE SENSING SCHEME FOR VIRTUAL GROUND FLASH EPROM ARRAY WITH ADJACENT BIT CHARGE AND HOLD                                          |
| PCT/US2001/048734     | AF01096PCT                | WIPO          | 12/12/2001  |            | SOFT PROGRAM AND SOFT PROGRAM VERIFY OF THE CORE CELLS IN FLASH MEMORY ARRAY                                                              |
| PCT/US2003/006589     | AF01116WO                 | WIPO          | 03/03/2003  |            | METHOD FOR MULTI-BIT FLASH READS USING DUAL DYNAMIC REFERENCES                                                                            |
| PCT/US2002/39781      | AF01124WO                 | WIPO          | 12/11/2002  |            | MONOS DEVICE HAVING BURIED METAL SILICIDE BIT LINE                                                                                        |
| PCT/US2003/001855     | AF01132WO                 | WIPO          | 01/21/2003  |            | HARD MASK PROCESS FOR MEMORY DEVICE WITHOUT BITLINE SHORTS                                                                                |
| PCT/US2004/00502      | AF01186PCT                | WIPO          | 01/08/2004  |            | CHARGE-TRAPPING MEMORY ARRAYS RESISTANT TO DAMAGE FROM CONTACT HOLE FORMATION                                                             |
| PCT/US2004/011354     | AF01209PCT                | WIPO          | 04/13/2004  |            | METHOD FOR REDUCING SHORT CHANNEL EFFECTS IN MEMORY CELLS AND RELATED STRUCTURE                                                           |
| PCT/US2006/026045     | AF01293PCT                | WIPO          | 06/30/2006  |            | PREAMORPHIZATION TO MINIMIZE VOID FORMATION                                                                                               |
| PCT/JP2004/010493     | AF01349PCT                | WIPO          | 07/23/2004  |            | FILE MANAGEMENT FOR RECOVERING FROM SUDDEN POWER OFF                                                                                      |
| PCT/US2005/023632     | AF01361PCT                | WIPO          | 07/06/2004  |            | ERASE DISTRIBUTION IMPROVEMENT WITH ENHANCED DUMMY WORDLINES IN FLASH MEMORY                                                              |
| PCT/JP2004/008998     | AF01371WO                 | WIPO          | 06/25/2004  |            | SEMICONDUCTOR DEVICE AND SOURCE VOLTAGE CONTROL METHOD                                                                                    |
| PCT/JP2004/001938     | AF01372                   | WIPO          | 02/19/2004  |            | CURRENT-VOLTAGE CONVERTER CIRCUIT AND CONTROL METHOD THEREOF                                                                              |
| PCT/US2005/004539     | AF01386PCT                | WIPO          | 11/02/2005  |            | ERASE ALGORITHM FOR MULTI-LEVEL BIT FLASH MEMORY                                                                                          |
| PCT/JP2004/010914     | AF01403US                 | WIPO          | 07/30/2004  |            | SEMICONDUCTOR DEVICE AND WRITING METHOD                                                                                                   |
| PCT/JP2004/10844      | AF01412WO                 | WIPO          | 07/29/2004  |            | METHOD FOR SETTING INFORMATION IN NON-VOLATILE STORAGE DEVICE, NON-VOLATILE STORAGE DEVICE AND SYSTEM USING THE SAME                      |
| PCT/JP2004/017808     | AF01439WO                 | WIPO          | 11/30/2004  |            | NON-VOLATILE SELECT GATE IN NAND FLASH MEMORY                                                                                             |
| PCT/JP2004/010837     | AF01441CN                 | WIPO          | 07/29/2004  |            | METHODH FOR INITIALIZING NON-VOLATILE STORAGE DEVICE, AND NOT-VOLATILE STORAGE DEVICE                                                     |
| PCT/US2005/004552     | AF01453PCT                | WIPO          | 02/11/2005  |            | METHOD AND SYSTEMS FOR HIGH WRITE PERFORMANCE IN MULTI-BIT FLASH MEMORY DEVICES                                                           |
| PCT/JP2004/016118     | AF01472WO                 | WIPO          | 10/29/2004  |            | DRAIN VOLTAGE REGULATION                                                                                                                  |
| PCT/US2005/038379     | AF01578WO                 | WIPO          | 10/26/2005  |            | SYSTEM AND METHOD FOR PROTECTING SEMICONDUCTOR DEVICES                                                                                    |
| PCT/US2006/028506     | AF01602PCT                | WIPO          | 07/21/2006  |            | SYSTEM AND METHOD FOR IMPROVING MESA WIDTH IN A SEMICONDUCTOR DEVICE                                                                      |
| PCT/JP2004/015833     | AF01645WO                 | WIPO          | 10/26/2004  |            | NON-VOLATILE MEMORY DEVICE                                                                                                                |
| PCT/US2006/034990     | AF01673PCT                | WIPO          | 09/07/2006  |            | FLASH MEMORY PROGRAMMING USING AN INDICATION BIT TO INTERPRET STATE                                                                       |
| PCT/JP2005/002891     | AF01721                   | WIPO          | 02/23/2005  |            | SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREFOR                                                                                          |
| PCT/JP2005/001334     | AF01725WO                 | WIPO          | 01/31/2005  |            | REFERENCE CELL TRIMMING IN BIST                                                                                                           |
| PCT/JP2005/023011     | AF01770PCT                | WIPO          | 12/15/2005  |            | A NON VOLATILE MEMORY DEVICE AND ITS CONTROL METHOD                                                                                       |
| PCT/JP2005/015416     | AF01785                   | WIPO          | 08/25/2005  |            | MEMORY DEVICE AND CONTROL METHOD OF MEMORY DEVICE                                                                                         |
| PCT/JP2005/012033     | AF01789                   | WIPO          | 06/30/2005  |            | NON-VOLATILE MEMORY DEVICE AND CONTROL METHOD OF NON-VOLATILE MEMORY DEVICE                                                               |
| PCT/US2007/021857     | AF01836PCT                | WIPO          | 10/12/2007  |            | SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME                                                                                   |
| PCT/JP2005/018322     | AF01840PCT                | WIPO          | 10/04/2005  |            | SEMICONDUCTOR DEVICE AND METHOD FOR CONTROLLING SAME                                                                                      |
| PCT/US2007/026426     | AF01869PCT                | WIPO          | 12/27/2007  |            | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME                                                                                |
| PCT/JP2005/022572     | AF01870                   | WIPO          | 12/08/2005  |            | REAL-TIME EQUIPMENT CONTROL TO MAINTAIN YIELD                                                                                             |
| PCT/US2007/087831     | AF01889PCT                | WIPO          | 12/17/2007  |            | MEMORY AND DEVICE AND PASSWORD STORING METHOD THEREOF                                                                                     |
| PCT/US2007/026472     | AF01890PCT                | WIPO          | 12/28/2007  |            | SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME                                                                                 |
| PCT/US2007/026414     | AF01897PCT                | WIPO          | 12/28/2007  |            | SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME                                                                                   |
| PCT/US2007/026428     | AF01898PCT                | WIPO          | 12/27/2007  |            | SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME                                                                                |
| PCT/US2007/026473     | AF01906PCT                | WIPO          | 12/28/2007  |            | SEMICONDUCTOR DEVICE AND MWTHOD FOR MANUFACTURING THE SAME                                                                                |
| PCT/US2007/008533     | AF01907PCT                | WIPO          | 04/05/2007  |            | MULTI MEDIA CARD WITH HIGH STORAGE CAPACITY                                                                                               |
| PCT/JP2005/022646     | AF01908WO                 | WIPO          | 12/09/2005  |            | SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD                                                                                         |
| PCT/US2007/019710     | AF01938PCT                | WIPO          | 09/10/2007  |            | DAMASCENE METAL-INSULATOR-METAL (MIM) DEVICE WITH IMPROVED SCALEABILITY                                                                   |
| PCT/US2007/086398     | AF01944PCT                | WIPO          | 12/04/2007  |            | METHODS OF PROGARMING AND ERASING RESISTIVE MEMORY DEVICES                                                                                |
| PCT/US2007/008568     | AF01954PCT                | WIPO          | 04/05/2007  |            | MEMORY CELL ARRAY WITH LOW RESISTANCE COMMON SOURCE AND HIGH CURRENT DRIVABILITY                                                          |

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|-----------------------|---------------------------|---------|-------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------|
| PCT/US2007/086286     | AF01965PCT                | WIPO    | 12/03/2007  |            | BARRIER REGION FOR MEMORY DEVICES                                                                                                         |
| PCT/US2007/086329     | AF01989PCT                | WIPO    | 12/04/2007  |            | MEMORY DEVICE PROTECTION LAYER                                                                                                            |
| PCT/US2007/016620     | AF02037PCT                | WIPO    | 07/24/2007  |            | INTEGRATED CIRCUIT MEMORY SYSTEM EMPLOYING SILICON RICH LAYERS                                                                            |
| PCT/US2007/016250     | AF02041PCT                | WIPO    | 07/17/2007  |            | MEMORY CELL SYSTEM WITH CHARGE TRAP                                                                                                       |
| PCT/US2007/016251     | AF02044PCT                | WIPO    | 07/17/2007  |            | MEMORY CELL SYSTEM WITH MULTIPLE NITRIDE LAYERS                                                                                           |
| PCT/US2007/018761     | AF02067PCT                | WIPO    | 08/23/2007  |            | MEMORY ERASE MANAGEMENT SYSTEM                                                                                                            |
| PCT/US2007/012186     | AF02071PCT                | WIPO    | 05/21/2007  |            | MEMORY SYSTEM WITH SWITCH ELEMENT                                                                                                         |
| PCT/JP2006/314151     | AF02079PCT                | WIPO    | 11/28/2008  |            | A NONVOLATILE MEMORY DEVICE AND ITS ERASE CONTROL METHOD                                                                                  |
| PCT/JP2006/303702     | AF02083                   | WIPO    | 02/28/2006  |            | MIRROR BIT MEMORY DEVICE HAVING BOTH PSG SPACER AND SILICIDE LAYER ON THE BIT LINE                                                        |
| PCT/US2007/087769     | AF02117PCT                | WIPO    | 12/17/2007  |            | A SEMICONDUCTOR MEMORY COPMPRISING DUAL CHARGE STORAGE NODES AND METHODS FOR ITS FABRICATION                                              |
| PCT/US2007/088448     | AF02131PCT                | WIPO    | 12/20/2007  |            | FLASH MEMORY DEVICES AND METHODS FOR FABRICATING THE SAME                                                                                 |
| PCT/US2007/008576     | AF02136PCT                | WIPO    | 04/05/2007  |            | REDUCTION OF LEAKAGE CURRENT AND PROGRAM DISTURBS IN FLASH MEMORY DEVICES                                                                 |
| PCT/US2007/088206     | AF02139PCT                | WIPO    | 12/19/2007  |            | ERASING FLASH MEMORY USING ADAPTIVE DRAIN AND/OR GATE BIAS                                                                                |
| PCT/US2007/087782     | AF02141PCT                | WIPO    | 12/17/2007  |            | DUAL-BIT MEMORY DEVICE HAVING TRENCH ISOLATION MATERIAL DISPOSED NEAR BIT LINE CONTACT AREAS                                              |
| PCT/US2008/007557     | AF02150PCT                | WIPO    | 06/16/2008  |            | ERROR CORRECTION SCHEME FOR NON-VOLATILE MEMORY                                                                                           |
| PCT/JP2000/009609     | AF02188WO                 | WIPO    | 12/21/2000  |            | NONVOLATILE SEMICONDUCTOR MEMORY DEVICE                                                                                                   |
| PCT/JP2003/016156     | AF02230PCT                | WIPO    | 12/17/2003  |            | SEMICONDUCTOR DEVICE AND TEST METHOD                                                                                                      |
| PCT/JP2006/320696     | AF02243PCT                | WIPO    | 10/18/2006  |            | A VOLTAGE DETECTOR CIRCUIT                                                                                                                |
| PCT/US2008/063188     | AF02246PCT                | WIPO    | 05/09/2008  |            | COMPENSATION METHOD TO ARCHIEVE UNIFORM PROGRAMMING SPEED OF FLASH MEMORY DEVICES                                                         |
| PCT/US2008/004667     | AF02248PCT                | WIPO    | 05/10/2008  |            | FLASH MEMORY CELL WITH A FLAIR GATE                                                                                                       |
| PCT/US2007/085837     | AF02267PCT                | WIPO    | 11/29/2007  |            | MULTI-LEVEL OPERATION IN DUAL ELEMENT CELLS USING A SUPPLEMENTAL PROGRAMMING LEVEL                                                        |
| PCT/US2007/018730     | AF02272PCT                | WIPO    | 08/23/2007  |            | METHOD OF SELECTING OPERATING CHARACTERISTICS OF A RESISTIVE MEMORY DEVICE                                                                |
| PCT/US2007/018760     | AF02282PCT                | WIPO    | 09/01/2006  |            | MULTIPLE COMUNNICATION CHANNELS ON MMC OR SD CMD LINE                                                                                     |
| PCT/US2007/086647     | AF02286PCT                | WIPO    | 12/06/2007  |            | METHODS AND SYSTEMS FOR MEMORY DEVICES                                                                                                    |
| PCT/US2007/018771     | AF02301PCT                | WIPO    | 08/23/2007  |            | VIRTUAL MEMORY CARD CONTROLLER                                                                                                            |
| PCT/US2007/023300     | AF02315PCT                | WIPO    | 11/05/2007  |            | CONTROLLING A SEMICONDUCTOR DEVICE                                                                                                        |
| PCT/US2007/083826     | AF02329PCT                | WIPO    | 11/06/2007  |            | MULTIPLE STAKEHOLDER SECURE MEMORY PARTITIONING AND ACCESS CONTROL                                                                        |
| PCT/US2007/083830     | AF02335PCT                | WIPO    | 11/06/2007  |            | SECURE CO-PROCESSING MEMORY CONTROLLER INTEGRATED INTO AN EMBEDDED MEMORY SUBSYSTEM                                                       |
| PCT/US2007/083828     | AF02337PCT                | WIPO    | 11/06/2007  |            | USING SHARED MEMORY WITH AN EXECUTE-IN-PLACE PROCESSOR AND A CO-PROCESSOR                                                                 |
| PCT/US2007/086780     | AF02436PCT                | WIPO    | 12/07/2007  |            | RESISTANCE CHANGING MEMORY CELL ARCHITECTURE                                                                                              |
| PCT/US2008/063186     | AF02453PCT                | WIPO    | 05/09/2008  |            | SELF ALIGNED NARROW STORAGE ELEMENTS FOR ADVANCED MEMORY DEVICE                                                                           |
| PCT/US2008/008864     | AF02465PCT                | WIPO    | 07/21/2008  |            | TERMINATE CYCLE FOR BURST WRITE OPERATION                                                                                                 |
| PCT/US2008/057138     | AF02477PCT                | WIPO    | 03/14/2008  |            | DIVISION-BASED SENSING AND PARTITIONING OF ELECTRONIC MEMORY                                                                              |
| PCT/US2008/087829     | AF02503PCT                | WIPO    | 12/19/2008  |            | CONTROLLING AC DISTURBANCE WHILE PROGRAMMING                                                                                              |
| PCT/US2008/74291      | AF02517PCT                | WIPO    | 08/26/2008  |            | SACRIFICIAL NITRIDE AND GATE REPLACEMENT                                                                                                  |
| PCT/US2008/074292     | AF02518PCT                | WIPO    | 08/26/2008  |            | GATE REPLACEMENT WITH TOP OXIDE REGROWTH FOR THE TOP OXIDE IMPROVEMENT                                                                    |
| PCT/US2008/071544     | AF02527PCT                | WIPO    | 07/30/2008  |            | ORO AND ORPRO WITH BITLINE TRENCH TO SUPPRESS TRANSPORT PROGRAM DISTURB                                                                   |
| PCT/US2008/80636      | AF02531PCT                | WIPO    | 10/21/2008  |            | SELECTIVE SILICIDE FORMATION USING RESIST ETCHBACK                                                                                        |
| PCT/US2008/072161     | AF02559PCT                | WIPO    | 08/04/2008  |            | THE MANUFACTURING METHOD FOR A CHIP WHICH HAS A THROUGH-HOLE ELECTRODE                                                                    |
| PCT/US2008/063390     | AF02560PCT                | WIPO    | 05/12/2008  |            | DIE ATTACHMENT, DIE STACKING, AND WIRE EMBEDDING USING FILM                                                                               |
| PCT/US2008/85443      | AF02562PCT                | WIPO    | 12/03/2008  |            | FORMING METAL-SEMICONDUCTOR FILMS HAVING DIFFERENT THICKNESSES WITHIN DIFFERENT REGIONS OF AN ELECTRONIC DEVICE                           |
| PCT/US2008/079969     | AF02563PCT                | WIPO    | 10/15/2008  |            | NON-VOLATILE MEMORY ARRAY PARTITIONING ARCHITECTURE AND METHOD TO UTILIZE SINGLE LEVEL CELLS AND MULTI-LEVEL CELLS WITHIN THE SAME MEMORY |
| PCT/US2008/080317     | AF02566PCT                | WIPO    | 10/17/2008  |            | TAMPER REACTIVE MEMORY DEVICE TO SECURE DATA FROM TAMPER ATTACKS                                                                          |
| PCT/US2008/075731     | AF02572PCT                | WIPO    | 09/09/2008  |            | SECURE MODULAR EXPONENTIATION BY RANDOMIZATION OF EXPONENT SCANNING                                                                       |
| PCT/US2008/013441     | AF02584PCT                | WIPO    | 12/04/2008  |            | MIRRORBIT PROGRAM / REFRESH ALGORITHM                                                                                                     |
| PCT/US2000/001262     | AF02593PCT                | WIPO    | 01/18/2000  |            | SHARED MEMORY APPARATUS AND METHOD FOR MULTUPROCESSOR SYSTEMS                                                                             |
| PCT/US2009/000126     | AF02646PCT                | WIPO    | 01/08/2009  |            | SYSTEM CONTROL METHOD OF MODE REGISTER SET OF DRAM IN MCP                                                                                 |
| PCT/US2008/88208      | AF02681PCT                | WIPO    | 12/23/2008  |            | ARRAYED NEUTRON DETECTOR WITH MULTI SHIELDING ALLOWING FOR DISCRIMINATION BETWEEN RADIATION TYPES                                         |
| PCT/US2008/004833     | AF02691PCT                | WIPO    | 04/14/2008  |            | SELF-ALIGNED PATTERNING METHOD BY USING NON-CONFORMAL FILM AND ETCH BACK FOR FLASH MEMORY AND OTHER SEMICONDUCTOR APPLICATIONS            |
| PCT/US2009/30182      | AF02764PCT                | WIPO    | 01/06/2009  |            | NON-VOLATILE MEMORY DEVICE AND METHODS OF USING                                                                                           |
| PCT/US2008/074417     | AF02813PCT                | WIPO    | 08/27/2008  |            | MIRROR BIT MEMORY DEVICE HAVING TOP INSULATING FILM WITH HIGH ETCHING SELECTIVITY TO GATE OXIDE FILM                                      |

# **ASSIGNMENT SCHEDULE A**

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|-----------------------|---------------------------|---------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| PCT/US2008/087800     | AF02814PCT                | WIPO    | 12/19/2008  |            | EXTENDING FLASH MEMORY DATA RETENTION VIA REWRITE REFRESH                                                                                              |
| PCT/US2008/087763     | AF02823PCT                | WIPO    | 12/19/2008  |            | ELECTRONIC DEVICE INCLUDING A SILICON NITRIDE LAYER AND A PROCESS OF FORMING THE SAME                                                                  |
| PCT/US2008/084046     | AF02824PCT                | WIPO    | 11/19/2008  |            | A MEMORY BUFFERING SYSTEM THAT IMPROVES READ/WRITE PERFORMANCE AND PROVIDES LOW LATENCY FOR MOBILE SYSTEMS                                             |
| PCT/US2008/077762     | AF02827PCT                | WIPO    | 09/25/2008  |            | OPO MIRROR BIT MEMORY DEVICE HAVING SHALLOW TRENCH ISOLATION                                                                                           |
| PCT/US2008/011628     | AF02832PCT                | WIPO    | 10/08/2008  |            | FABRICATING METHOD OF OPO MIRROR BIT MEMORY DEVICE HAVING SHALLOW TRENCH ISOLATION                                                                     |
| PCT/US2008/013532     | AF02839PCT                | WIPO    | 12/09/2008  |            | CONTROL METHOD OF GBL AND LBL IN A READ                                                                                                                |
| PCT/US2008/79993      | AF02850PCT                | WIPO    | 10/15/2008  |            | CONTROLLED RAMP RATES FOR METAL BITLINES DURING WRITE OPERATIONS FROM HIGH VOLTAGE DRIVER FOR MEMORY APPLICATIONS                                      |
| PCT/US2008/86913      | AF02862PCT                | WIPO    | 12/17/2007  |            | HETERO-STRUCTURE VARIABLE SILICON RICHNESS NITRIDE FOR MLC FLASH MEMORY DEVICE                                                                         |
| PCT/US2008/073348     | AF02865US PCT             | WIPO    | 09/09/2008  |            | PROCESS OF FORMING AN ELECTRONIC DEVICE INCLUDING DEPOSITING LAYERS WITHIN OPENINGS                                                                    |
| PCT/US2008/013185     | AF02873PCT                | WIPO    | 11/26/2008  |            | A METHOD FOR SETTING PARAMETERS AND DETERMINING LATENCY IN A CHAINED DEVICE SYSTEM                                                                     |
| PCT/US2008/13194      | AF02874PCT                | WIPO    | 11/25/2008  |            | A METHOD FOR SETTING PARAMETERS AND DETERMINING LATENCY IN A CHAINED DEVICE SYSTEM                                                                     |
| PCT/US2008/013188     | AF02875PCT                | WIPO    | 11/25/2008  |            | A METHOD FOR SETTING PARAMETERS AND DETERMINING LATENCY IN A CHAINED DEVICE SYSTEM                                                                     |
| PCT/US2008/013186     | AF02876PCT                | WIPO    | 11/25/2008  |            | A METHOD FOR SETTING PARAMETERS AND DETERMINING LATENCY IN A CHAINED DEVICE SYSTEM                                                                     |
| PCT/US2008/086436     | AF02883PCT                | WIPO    | 12/11/2008  |            | REFERENCE-FREE SAMPLED SENSING                                                                                                                         |
| PCT/US2008/014115     | AF02892PCT                | WIPO    | 12/30/2008  |            | TABLE LOOKUP VOLTAGE COMPENSATION FOR MEMORY CELLS                                                                                                     |
| PCT/US2008/088658     | AF02907PCT                | WIPO    | 12/31/2008  |            | METHOD FOR PROTECTING DATA AGAINST DIFFERENTIAL FAULT ANALYSIS INVOLVED IN RSA USING THE CHINESE REMAINDER THEOREM                                     |
| PCT/US2008/013227     | AF02908PCT                | WIPO    | 11/26/2008  |            | SONOS-NAND DEVICE HAVING COMPLETELY SEPARATED STORAGE REGIONS                                                                                          |
| PCT/US2014/019105     | AF03137PCT                | WIPO    | 02/27/2014  |            | NON-VOLATILE MEMORY BASED SYSTEM RAM                                                                                                                   |
| PCT/US2011/047279     | AF03209US PCT             | WIPO    | 08/10/2011  |            | STITCH BUMP STACKING DESIGN FOR OVERALL PACKAGE SIZE REDUCTION FOR MULTIPLE STACK                                                                      |
| PCT/US2011/042396     | AF03219PCT                | WIPO    | 06/29/2011  |            | METHOD AND SYSTEM FOR THINK MULTI CHIP STACK PACKAGE WITH FILM ON WIRE AND COPPER WIRE                                                                 |
| PCT/US2009/059862     | AF04024                   | WIPO    | 10/07/2009  |            | REAL-TIME DATA PATTERN ANALYSIS SYSTEM AND METHOD OF OPERATION THEREOF                                                                                 |
| PCT/US2005/037985     | AF04031CN                 | WIPO    | 10/19/2005  |            | Non-volatile memory and pseudo-sram based on resonant tunneling concept                                                                                |
| PCT/US2012/070329     | AF04035PCT                | WIPO    | 12/18/2012  |            | ACOUSTIC PROCESSING UNIT INTERFACE                                                                                                                     |
| PCT/US2012/070332     | AF04036PCT                | WIPO    | 12/18/2012  |            | ARITHMETIC LOGIC UNIT ARCHITECTURE                                                                                                                     |
| PCT/US1996/17412      | B192PCT                   | WIPO    | 11/01/1996  |            | SOURCELESS FLOATING GATE MEMORY DEVICE AND METHOD OF STORING DATA                                                                                      |
| PCT/US1998/02330      | C144496PCT                | WIPO    | 02/05/1998  |            | HIGH VOLTAGE NMOS PASS GATE FOR INTEGRATED CIRCUIT WITH HIGH VOLTAGE GENERATOR AND FLASH NON-VOLATILE MEMORY DEVICE HAVING THE PASS GATE               |
| PCT/US1998/026850     | C369297WO                 | WIPO    | 12/18/1998  |            | BIASING METHOD AND STRUCTURE FOR REDUCING BAND-TO-BAND AND/OR AVALANCHE CURRENTS DURING THE ERASE OF FLASH MEMORY DEVICES                              |
| PCT/US1998/026848     | C627497WO                 | WIPO    | 12/18/1998  |            | FORMATION OF CONTROL AND FLOATING GATES OF SEMICONDUCTOR NON-VOLATILE MEMORIES                                                                         |
| PCT/US2000/24271      | C656497PCT                | WIPO    | 08/31/2000  |            | TUNGSTEN GATE MOS TRANSISTOR AND MEMORY CELL AND METHOD OF MAKING SAME                                                                                 |
| PCT/US2000/18019      | C695497PCT                | WIPO    | 06/29/2000  |            | THIN FLOATING GATE AND CONDUCTIVE SELECT GATE IN SITU                                                                                                  |
| PCT/US1999/21737      | C715497                   | WIPO    | 09/21/1999  |            | WORDLINE DRIVER FOR FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY MEMORY (EEPROM)                                                                 |
| PCT/US2000/21005      | C725497                   | WIPO    | 08/01/2000  |            | CIRCUIT IMPLEMENTATION TO QUENCH BIT LINE LEAKAGE CURRENT IN PROGRAM AND AUTO PROGRAM DISTURB MODE IN FLASH EPROM USING RESISTOR SOURCE LOAD           |
| PCT/US1999/23109      | D138                      | WIPO    | 10/05/1999  |            | SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON-VOLATILE MEMORY ARRAY                                                                                  |
| PCT/US1999/018762     | D139US                    | WIPO    | 08/16/1999  |            | BANK SELECTOR CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                                     |
| PCT/US1999/018678     | D168WO                    | WIPO    | 08/16/1999  |            | SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                                          |
| PCT/US1999/18495      | D169                      | WIPO    | 08/16/1999  |            | METHOD OF MAKING FLEXIBLY PARTITIONED METAL LINE SEGMENTS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE |
| PCT/US1999/18761      | D170                      | WIPO    | 08/16/1999  |            | MEMORY ADDRESS DECODING CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE                           |
| PCT/US2000/012343     | D832WO                    | WIPO    | 05/05/2000  |            | RAMPED OR STEPPED GATE CHANNEL ERASE FOR FLASH MEMORY APPLICATION                                                                                      |
| PCT/US2000/033044     | D853                      | WIPO    | 12/05/2000  |            | METHOD TO PROVIDE A REDUCED CONSTANT E-FIELD DURING ERASE OF EEPROMS FOR RELIABILITY IMPROVEMENT                                                       |
| PCT/US2000/26874      | D894PCT                   | WIPO    | 09/29/2000  |            | METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITH REDUCED ARC LOSS IN PERIPHERAL CIRCUITRY REGION                                                    |

# **ASSIGNMENT SCHEDULE A**

| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                                                                  |
|-----------------------|---------------------------|---------|-------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------|
| PCT/US2000/34213      | D958PCT                   | WIPO    | 12/13/2000  |            | NOVEL NITRIDATION BARRIERS FOR NITRIDATED TUNNEL OXIDE FOR CIRCUITRY FOR FLASH TECHNOLOGY AND FOR LOCOS/STI ISOLATION                                  |
| PCT/US2001/13855      | DA01011                   | WIPO    | 04/27/2001  |            | A SUBMICRON SEMICONDUCTOR DEVICE HAVING A SELF-ALIGNED CHANNEL STOP REGION AND A METHOD FOR FABRICATING THE SEMICONDUCTOR DEVICE USING A TRIM AND ETCH |
| PCT/US2000/19486      | DA01016PCT                | WIPO    | 07/14/2000  |            | METHOD FOR PROVIDING A DOPANT LEVEL FOR POLYSILICON FOR FLASH MEMORY DEVICES                                                                           |
| PCT/US2000/19571      | DA01023                   | WIPO    | 07/17/2000  |            | METHOD FOR CONTACT SIZE CONTROL FOR NAND TECHNOLOGY                                                                                                    |
| PCT/US2001/10922      | DA01025                   | WIPO    | 04/03/2001  |            | FLASH MEMORY ARRAY AND A METHOD AND SYSTEM OF FABRICATION THEREOF                                                                                      |
| PCT/US2001/08867      | DA01028                   | WIPO    | 03/20/2001  |            | METHOD AND SYSTEM FOR PROVIDING CONTACT TO A FIRST POLYSILICON LAYER IN A FLASH MEMORY DEVICE                                                          |
| PCT/US2000/17912      | E0197PCT                  | WIPO    | 06/29/2000  |            | NEW METHOD OF FORMING SELECT GATE TO IMPROVE RELIABILITY AND PERFORMANCE FOR NAND-TYPE FLASH MEMORY DEVICES                                            |
| PCT/US2000/19303      | E0251                     | WIPO    | 07/14/2000  |            | FLASH MEMORY ARCHITECTURE EMPLOYING THREE LAYER METAL INTERCONNECT                                                                                     |
| PCT/US2001/06364      | E0255                     | WIPO    | 02/27/2001  |            | CHARGE SHARING TO HELP BOOST THE WORDLINES DURING APDE VERIFY                                                                                          |
| PCT/US2001/04050      | E0264                     | WIPO    | 02/07/2001  |            | TRIMMING METHOD FOR WORDLINE BOOSTER TO MINIMIZE PROCESS VARIATION OF BOOSTED WORDLINE VOLTAGE                                                         |
| PCT/US2001/024679     | E0310US                   | WIPO    | 08/06/2001  |            | SELECT TRANSISTOR ARCHITECTURE FOR A VIRTUAL GROUND NON-VOLATILE MEMORY CELL ARRAY                                                                     |
| PCT/US2001/003876     | E0480PCT                  | WIPO    | 02/06/2001  |            | USER SELECTABLE CELL PROGRAMMING                                                                                                                       |
| PCT/US2001/003858     | E0484PCT                  | WIPO    | 02/06/2001  |            | MODE INDICATOR FOR MULTI-LEVEL MEMORY                                                                                                                  |
| PCT/US2001/003863     | E0485PCT                  | WIPO    | 02/06/2001  |            | INTERLACED MULTI-LEVEL MEMORY                                                                                                                          |
| PCT/US2000/034093     | E0584US                   | WIPO    | 12/15/2000  |            | CHAINED ARRAY OF SEQUENTIAL ACCESS MEMORIES ENABLING CONTINUOUS READ                                                                                   |
| PCT/US2001/003877     | E1021US                   | WIPO    | 02/06/2001  |            | VARIABLE PULSE WIDTH MEMORY PROGRAMMING                                                                                                                |
| PCT/US2001/049057     | F0259WO                   | WIPO    | 12/14/2001  |            | MODULATED CHARGE PUMP WHICH USES AN ANALOG TO DIGITAL CONVERTER TO COMPENSATE FOR SUPPLY VOLTAGE VARIATIONS                                            |
| PCT/US2002/030784     | F0283WO                   | WIPO    | 09/27/2002  |            | SALICIDED GATE FOR VIRTUAL GROUND ARRAYS                                                                                                               |
| PCT/US2001/032463     | F0919                     | WIPO    | 10/16/2001  |            | PROGRAMMING METHOD USING VOLTAGE PULSE WITH STEPPED PORTIONS FOR MULTI-LEVEL CELL FLASH MEMORIES                                                       |
| PCT/JP2006/319419     | FMA13-00307PCT            | WIPO    | 09/29/2006  |            | TRANSMITTING/RECEIVING SYSTEM, NODE AND COMMUNICATION METHOD                                                                                           |
| PCT/JP2006/319364     | FMA13-00309PCT            | WIPO    | 09/28/2006  |            | SIGNAL RECEIVER APPARATUS AND WAVEFORM SHAPING METHOD                                                                                                  |
| PCT/JP2007/056890     | FMA13-00331JP             | WIPO    | 03/29/2007  |            | DISPLAY CONTROL DEVICE, INFORMATION PROCESSOR, AND DISPLAY CONTROL PROGRAM                                                                             |
| PCT/JP2007/062590     | FMA13-00332PCT            | WIPO    | 06/22/2007  |            | PLL CONTROL CIRCUIT, PLL DEVICE, PLL CONTROL METHOD                                                                                                    |
| PCT/JP2007/055092     | FMA13-00335PCT            | WIPO    | 03/14/2007  |            | OUTPUT CIRCUIT                                                                                                                                         |
| PCT/JP2007/000183     | FMA13-00342PCT            | WIPO    | 03/08/2007  |            | SOFTWARE OPTIMIZATION DEVICE AND SOFTWARE OPTIMIZATION METHOD                                                                                          |
| PCT/JP2007/000274     | FMA13-00343JP DIV2        | WIPO    | 03/20/2007  |            | PROCESSOR SYSTEM OPTIMIZATION SUPPORTING APPARATUS AND SUPPORTING METHOD                                                                               |
| PCT/JP2007/067189     | FMA13-00352JP             | WIPO    | 09/04/2007  |            | CHARGING CIRCUIT                                                                                                                                       |
| PCT/JP2007/071430     | FMA13-00353KR             | WIPO    | 11/02/2007  |            | SIGNAL PROCESSOR AND COMMUNICATION DEVICE                                                                                                              |
| PCT/JP2008/070669     | FMA13-00408PCT            | WIPO    | 11/13/2008  |            | MICROCOMPUTER                                                                                                                                          |
| PCT/EP2008/065314     | FMA13-00472JP             | WIPO    | 11/11/2008  |            | METHOD OF DETECTING AN OPERATING CONDITION OF AN ELECTRIC STEPPER ...                                                                                  |
| PCT/JP2003/004968     | FMA13-00549JP             | WIPO    | 04/18/2003  |            | CONSTANT-VOLTAGE POWER SUPPLY CIRCUIT                                                                                                                  |
| PCT/IB2014/000998     | FMA13-00582PCT            | WIPO    | 03/19/2014  |            | SEMICONDUCTOR DEVICE AND ERASING METHOD THEREOF                                                                                                        |
| PCT/JP2000/005574     | FMA13-0093KR              | WIPO    | 08/18/2000  |            | FREQUENCY MEASUREMENT CIRCUIT                                                                                                                          |
| PCT/JP2002/013701     | FMA13-0172PCT             | WIPO    | 12/26/2002  |            | SIGMA DELTA MODULATOR FOR PLL CIRCUIT                                                                                                                  |
| PCT/JP2003/002443     | FMA13-0178KR              | WIPO    | 03/03/2003  |            | MOS VARIABLE CAPACITIVE DEVICE                                                                                                                         |
| PCT/JP2003/004571     | FMA13-0185JP              | WIPO    | 04/10/2003  |            | PULSE WIDTH MEASURING APPARATUS WITH AUTO-RANGE SETTING FUNCTION                                                                                       |
| PCT/JP2003/004794     | FMA13-0190JP DIV          | WIPO    | 04/15/2003  |            | CRYSTAL OSCILLATION CIRCUIT                                                                                                                            |
| PCT/JP2003/015215     | FMA13-0197WO              | WIPO    | 11/28/2003  |            | SIGMA-DELTA MODULATOR OF PLL CIRCUIT                                                                                                                   |
| PCT/2004/013041       | FMA13-0217KR              | WIPO    | 09/08/2004  |            | PLL FREQUENCY SYNTHESIZER                                                                                                                              |
| PCT/US2001/043730     | G0063WO                   | WIPO    | 11/14/2001  |            | ACCURATE VERIFY APPARATUS AND METHOD FOR NOR FLASH MEMORY CELLS IN THE PRESENCE OF HIGH COLUMN LEAKAGE                                                 |
| PCT/US2002/04779      | G0259PCT                  | WIPO    | 02/19/2002  |            | FLASH MEMORY DEVICE WITH INCREASE OF EFFICIENCY DURING AN APDE (AUTOMATIC PROGRAM DISTURB AFTER ERASE) PROCESS                                         |
| PCT/US2003/18309      | G0391WO                   | WIPO    | 06/10/2003  |            | BUILT-IN-SELF-TEST (BIST) OF FLASH MEMORY CELLS AND IMPLEMENTATION OF BIST INTERFACE                                                                   |
| PCT/US2003/004607     | G0861US                   | WIPO    | 02/14/2003  |            | IMPROVED ERASE METHOD FOR SINGLE SIDED MIRROR OPERATION                                                                                                |
| PCT/US2003/004606     | G0863US                   | WIPO    | 02/14/2003  |            | OVERERASE CORRECTION METHOD                                                                                                                            |
| PCT/US2003/21676      | G0878PCT                  | WIPO    | 07/10/2003  |            | A METHOD AND SYSTEM FOR ERASING A NITRIDE MEMORY DEVICE                                                                                                |
| PCT/US2003/003330     | G1255WO                   | WIPO    | 02/05/2003  |            | PARTIAL PAGE PROGRAMMING OF MULTI LEVEL FLASH                                                                                                          |
| PCT/US2005/043788     | H0290                     | WIPO    | 12/02/2005  |            | POLYMER-BASED TRANSISTOR DEVICES, METHODS, AND SYSTEMS                                                                                                 |
| PCT/US2003/021680     | H0297PCT                  | WIPO    | 07/10/2003  |            | CONTROL OF MEMORY ARRAYS UTILIZING ZENER DIODE-LIKE DEVICES                                                                                            |
| PCT/US2003/21669      | H0343PCT                  | WIPO    | 07/10/2003  |            | MOCVD FORMATION OF Cu2S                                                                                                                                |
| PCT/US2004/030511     | H0423PCT                  | WIPO    | 09/16/2004  |            | SELF ASSEMBLY OF CONDUCTING POLYMER FOR FORMATION OF POLYMER MEMORY CELL                                                                               |

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| PATENT OR APPL<br>NO. | SPANSION<br>REFERENCE NO. | COUNTRY | FILING DATE | ISSUE DATE | TITLE                                                                                                        |
|-----------------------|---------------------------|---------|-------------|------------|--------------------------------------------------------------------------------------------------------------|
| PCT/US2003/21679      | H0434PCT                  | WIPO    | 07/10/2003  |            | STACKED ORGANIC MEMORY DEVICES AND METHODS OF<br>OPERATING AND FABRICATING                                   |
| PCT/US2004/014696     | H0437PCT                  | WIPO    | 05/11/2004  |            | PLANAR POLYMER MEMORY DEVICE                                                                                 |
| PCT/US2006/039398     | H0439PCT                  | WIPO    | 10/06/2006  |            | SYSTEM AND METHOD FOR PROCESSING AN ORGANIC MEMORY<br>CELL                                                   |
| PCT/US2004/015945     | H0442                     | WIPO    | 05/21/2004  |            | ORGANIC MEMORY DEVICE AND METHODS OF USING AND MAKING<br>THE DEVICE                                          |
| PCT/US2004/011811     | H0443                     | WIPO    | 04/16/2004  |            | ERASING AND PROGRAMMING AN ORGANIC MEMORY DEVICE AND<br>METHODS OF OPERATING AND FABRICATING                 |
| PCT/US2003/030000     | H0496                     | WIPO    | 09/24/2003  |            | MEMORY DEVICE HAVING A P+ GATE AND THIN BOTTOM OXIDE AND<br>METHOD OF ERASING SAME                           |
| PCT/US2003/018447     | H0514                     | WIPO    | 06/10/2003  |            | NITROGEN OXIDATION TO REDUCE ENCROACHMENT                                                                    |
| PCT/US2004/022986     | H0541                     | WIPO    | 07/15/2004  |            | LOW POWER CHARGE PUMP                                                                                        |
| PCT/US2003/23085      | H0570                     | WIPO    | 07/24/2003  |            | IMPROVED SYSTEM FOR PROGRAMMING A NON-VOLATILE MEMORY<br>CELL                                                |
| PCT/US2003/023087     | H0575                     | WIPO    | 07/24/2003  |            | IMPROVED PRE-CHARGE METHOD FOR READING A NON-VOLATILE                                                        |
| PCT/US2003/21634      | H1203                     | WIPO    | 07/10/2003  |            | CASCADE AMPLIFIER CIRCUIT FOR PRODUCING A FAST, STABLE AND<br>ACCURATE BITLINE VOLTAGE                       |
| PCT/US2003/23083      | H1205                     | WIPO    | 07/24/2003  |            | CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS                                                                  |
| PCT/US2004/019664     | H1368PCT                  | WIPO    | 06/18/2004  |            | PECVD SILICON-RICH OXIDE LAYER FOR REDUCED UV CHARGING                                                       |
| PCT/RU2001/000334     | H1979PCT                  | WIPO    | 08/13/2001  |            | MEMORY CELL                                                                                                  |
| PCT/US2005/004583     | H1984US                   | WIPO    | 02/11/2005  |            | METHODS AND APPARATUS FOR WORDLINE PROTECTION IN FLASH<br>MEMORY DEVICES                                     |
| PCT/US2004/042855     | H1985PCT                  | WIPO    | 12/17/2004  |            | POCKET IMPLANT FOR COMPLEMENTARY BIT DISTURB<br>IMPROVEMENT AND CHARGING IMPROVEMENT OF SONOS MEMORY<br>CELL |
| PCT/US2005/015132     | H1990PCT                  | WIPO    | 04/29/2005  |            | METHOD OF FORMING NARROWLY SPACED FLASH MEMORY<br>CONTACT OPENINGS AND LITHOGRAPHY MASKS                     |
| PCT/US2005/004540     | H1993PCT                  | WIPO    | 02/11/2005  |            | BITLINE IMPLANT UTILIZING DUAL POLY                                                                          |
| PCT/US2006/012575     | H1998                     | WIPO    | 04/04/2006  |            | NON-CRITICAL COMPLEMENTARY MASKING METHOD FOR POLY-1<br>DEFINITION IN FLASH MEMORY DEVICE FABRICATION        |
| PCT/US2003/029985     | P072WO                    | WIPO    | 09/24/2003  |            | METHOD FOR REDUCING CONTACT DEFECTS IN SEMICONDUCTOR<br>CELLS                                                |
| PCT/US2002/039739     | P116WO                    | WIPO    | 12/11/2002  |            | METHOD FOR FORMING A SHALLOW TRENCH ISOLATION STRUCTURE<br>WITH IMPROVED CORNER ROUNDING                     |
| PCT/IL2001/000399     | P-2448WO                  | WIPO    | 05/03/2001  |            | PROGRAMMING OF NONVOLATILE MEMORY CELLS                                                                      |
| PCT/IL2002/000855     | P-4006WO                  | WIPO    | 10/24/2002  |            | METHOD FOR ERASING A MEMORY CELL                                                                             |
| PCT/IL2002/000922     | P-4007WO                  | WIPO    | 11/18/2002  |            | PROTECTIVE LAYER IN MEMORY DEVICE AND METHOD THEREFOR                                                        |
| PCT/IL2004/000981     | P-5484US                  | WIPO    | 10/27/2004  |            | METHOD SYSTEM AND CIRCUIT FOR PROGRAMMING A NON-VOLATILE<br>MEMORY ARRAY                                     |
| PCT/IL2004/000982     | P-5487-TW                 | WIPO    | 10/27/2004  |            | METHOD CIRCUIT AND SYSTEM FOR DETERMINING A REFERENCE<br>VOLTAGE                                             |
| PCT/IL2004/000983     | P-5487-TW1                | WIPO    | 10/27/2004  |            | METHOD FOR READ ERROR DETECTION IN A NON-VOLATILE MEMORY<br>ARRY                                             |
| PCT/US2003/007639     | SE0002WO                  | WIPO    | 03/11/2003  |            | SYSTEM AND METHOD OF ERASE VOLTAGE CONTROL DURING<br>MULTIPLE SECTOR ERASE OF A FLASH MEMORY DEVICE          |
| PCT/US2010/039585     | SP09-0001PCT              | WIPO    | 06/23/2010  |            | ELECTRONIC DEVICE HAVING A MOLDING COMPOUND INCLUDING A<br>COMPOSITE MATERIAL                                |
| PCT/US2013/063089     | SP09-0008PCT              | WIPO    | 10/02/2013  |            | IMPROVED SPACER DESIGN TO PREVENT TRAPPED ELECTRONS                                                          |
| PCT/US2008/000435     | SP09-0017.PCT             | WIPO    | 01/10/2008  |            | METHODS FOR FORMING A MEMORY CELL HAVING A TOP OXIDE<br>SPACER                                               |
| PCT/US2013/42673      | SP09-0030PCT              | WIPO    | 05/24/2013  |            | METHOD, APPARATUS, AND MANUFACTURE FOR FLASH MEMORY<br>ADAPTIVE ALGORITHM                                    |
| PCT/US2012/068467     | SP09-0056KR               | WIPO    | 12/07/2012  |            | HIGH SPEED SERIAL PERIPHERAL INTERFACE MEMORY SUBSYSTEM                                                      |
| PCT/US2013/52852      | SP09-0058PCT              | WIPO    | 07/31/2013  |            | POWER SAVINGS APPARATUS AND METHOD FOR MEMORY DEVICE<br>USING DELAY LOCKED LOOP                              |
| PCT/2014/071369       | SP10-0003PCT              | WIPO    | 12/19/2014  |            | CT-NOR DIFFERENTIAL BITLINE SENSING ARCHITECTURE                                                             |
| PCT/US2013/68289      | SP10-0006PCT              | WIPO    | 11/04/2013  |            | WEAR LEVELING IN FLASH MEMORY DEVICES WITH TRIM COMMANDS                                                     |
| PCT/US2011/065442     | SP10-0007WO               | WIPO    | 12/16/2011  |            | SELF-ALIGNED NAND FLASH SELECT-GATE WORDLINES FOR SPACER<br>DOUBLE PATTERNING                                |
| PCT/US2011/065930     | SP10-0008 PCT             | WIPO    | 12/19/2011  |            | EDGE ROUNDED FIELD EFFECT TRANSISTORS AND METHODS OF<br>MANUFACTURING                                        |
| PCT/US2011/065923     | SP10-0009WO               | WIPO    | 12/19/2011  |            | PROCESS MARGIN ENGINEERING IN CHARGE TRAPPING FIELD<br>EFFECT TRANSISTORS                                    |
| PCT/US2011/067905     | SP10-0012WO-PCT           | WIPO    | 12/29/2011  |            | MEMORY WITH EXTENDED CHARGE TRAPPING LAYER                                                                   |
| PCT/US2013/040904     | SP11-0015KR               | WIPO    | 05/14/2013  |            | SOFT ERROR RESISTANT CIRCUITRY                                                                               |
| PCT/US2013/025417     | SP11-0027KR               | WIPO    | 02/08/2013  |            | IMPROVING REDUNDANCY LOADING EFFICIENCY                                                                      |
| PCT/US13/049054       | SP11-0028US               | WIPO    | 07/02/2013  |            | APPARATUS AND METHOD FOR ROUNDED ONO FORMATION IN A<br>FLASH MEMORY DEVICE                                   |
| PCT/US2014/032704     | SP11-0030US               | WIPO    | 04/02/2014  |            | MODIFIED LOCAL SEGMENTED SELF-BOOSTING OF MEMORY CELL<br>CHANNELS                                            |
| PCT/US2014/010299     | SP11-0038PCT              | WIPO    | 01/06/2014  |            | MULTI-CHIP PACKAGE ASSEMBLY WITH IMPROVED BOND WIRE<br>SEPARATION                                            |
| PCT/US2013/070141     | SP11-0039US               | WIPO    | 11/14/2013  |            | METHOD AND SYSTEM FOR PROCESSING A WAFER                                                                     |
| PCT/US2013/076149     | SP11-0040PCT              | WIPO    | 12/18/2013  |            | PHONEME SCORE ACCELERATOR                                                                                    |
| PCT/US2012/069787     | SP11-0042PCT              | WIPO    | 12/14/2012  |            | ACOUSTIC PROCESSING UNIT                                                                                     |
| PCT/US2014/032678     | SP11-0043PCT              | WIPO    | 04/02/2014  |            | COMBINING OF RESULTS FROM MULTIPLE DECODERS                                                                  |
| PCT/US2013/037800     | SP11-0044PCT              | WIPO    | 04/23/2013  |            | POWER-EFFICIENT VOICE ACTIVATION                                                                             |
| PCT/US2013/070561     | SP12-0004PCT              | WIPO    | 11/18/2013  |            | DATA REFRESH IN NON-VOLATILE MEMORY                                                                          |
| PCT/US2013/076154     | SP12-0012PCT              | WIPO    | 12/18/2013  |            | CHIP POSITIONING IN MULTI-CHIP PACKAGE                                                                       |

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|-----------------------|---------------------------|---------|-------------|------------|-----------------------------------------------------------------------------------------------------|
| PCT/US2013/034778     | SP12-0013PCT              | WIPO    | 04/01/2013  |            | ADAPTIVELY PROGRAMMING OR ERASING FLASH MEMORY BLOCKS                                               |
| PCT/US2013/070579     | SP12-0016PCT              | WIPO    | 11/18/2013  |            | METHOD TO IMPROVE CHARGE TRAP FLASH MEMORY CORE CELL<br>PERFORMANCE AND RELIABILITY                 |
| PCT/US2013/49574      | SP12-0017PCT              | WIPO    | 07/08/2013  |            | LEAKAGE REDUCING WRITELINE CHARGE PROTECTION CIRCUIT                                                |
| PCT/US2013/52504      | SP12-0021PCT              | WIPO    | 07/29/2013  |            | BITLINE VOLTAGE REGULATION IN NON-VOLATILE MEMORY                                                   |
| PCT/US2014/032495     | SP12-0022PCT              | WIPO    | 04/01/2014  |            | ERASE VERIFICATION                                                                                  |
| PCT/US2014/013847     | SP12-0026PCT              | WIPO    | 01/30/2014  |            | NON-VOLATILE MEMORY WITH SILICIDED BIT LINE CONTACTS                                                |
| PCT/US2014/010489     | SP12-0027PCT              | WIPO    | 01/07/2014  |            | PROGRAMMABLE AND FLEXIBLE REFERENCE CELL SELECTION<br>METHOD FOR MEMORY DEVICES                     |
| PCT/US2013/071217     | SP12-0028PCT              | WIPO    | 11/21/2013  |            | FORMING CHARGE TRAP SEPARATION IN A FLASH MEMORY<br>SEMICONDUCTOR DEVICE                            |
| PCT/US2013/071214     | SP12-0029PCT              | WIPO    | 11/21/2013  |            | FORMING A SUBSTANTIALLY UNIFORM WING HEIGHT AMONG<br>ELEMENTS IN A CHARGE TRAP SEMICONDUCTOR DEVICE |
| PCT/US2013/076140     | SP12-0030PCT              | WIPO    | 12/18/2013  |            | MEMORY DEVICE WITH INTERNAL DATA PROCESSING LOGIC                                                   |
| PCT/US2013/068449     | SP12-0031PCT              | WIPO    | 11/05/2013  |            | SENONE SCORING FOR MULTIPLE INPUT STREAMS                                                           |
| PCT/IB2014/058829     | SP12-0032US               | WIPO    | 02/06/2014  |            | IMPROVED NON-VOLATILE MEMORY DEVICE                                                                 |
| PCT/US2013/075313     | SP12-0033PCT              | WIPO    | 12/16/2013  |            | HYBRID HASHING SCHEME FOR ACTIVE HMMS                                                               |
| PCT/US2013/063088     | SP12-0034PCT              | WIPO    | 10/02/2013  |            | SUPPLY POWER DEPENDENT CONTROLLABLE WRITE THROUGHPUT<br>FOR MEMORY APPLICATIONS                     |
| PCT/US2013/075309     | SP12-0036PCT              | WIPO    | 12/16/2013  |            | HISTOGRAM BASED PRE-PRUNING SCHEME FOR ACTIVE HMMS (as<br>amended)                                  |
| PCT/US2013/077835     | SP12-0037PCT              | WIPO    | 12/26/2013  |            | DESIGN FOR TEST (DFT) READ SPEED THROUGH TRANSITION<br>DETECTOR IN BUILT-IN SELF-TEST (BIST) SORT   |
| PCT/US2014/010301     | SP12-0041PCT              | WIPO    | 01/06/2014  |            | BURIED HARD MASK FOR EMBEDDED SEMICONDUCTOR DEVICE<br>PATTERNING                                    |
| PCT/US2013/068452     | SP12-0042PCT              | WIPO    | 11/05/2013  |            | RECOGNITION OF SPEECH WITH DIFFERENT ACCENTS                                                        |
| PCT/US2014/034367     | SP12-0043PCT              | WIPO    | 04/16/2014  |            | DIE SEAL LAYOUT FOR DUAL DAMASCENE IN A SEMICONDUCTOR<br>DEVICE                                     |
| PCT/US2013/070309     | SP12-0045PCT              | WIPO    | 11/15/2013  |            | INTER-LAYER INSULATOR FOR ELECTRONIC DEVICES AND<br>APPARATUS FOR FORMING SAME                      |
| PCT/US2013/070057     | SP12-0046PCT              | WIPO    | 11/14/2013  |            | DISTRIBUTION OF GAS OVER A SEMICONDUCTOR WAFER IN BATCH<br>PROCESSING                               |
| PCT/US2014/021255     | SP12-0051PCT              | WIPO    | 03/06/2014  |            | PIPELINING IN A MEMORY                                                                              |
| PCT/US2014/010514     | SP12-0054PCT              | WIPO    | 01/07/2014  |            | DISTRIBUTED SPEECH RECOGNITION SYSTEM                                                               |
| PCT/US2014/040677     | SP12-0060PCT              | WIPO    | 06/03/2014  |            | SCREENING FOR REFERENCE CELLS IN A MEMORY                                                           |
| PCT/US2014/034967     | SP12-0064PCT              | WIPO    | 04/22/2014  |            | CHARGE-TRAP NOR WITH SILICON-RICH NITRIDE AS A CHARGE TRAP<br>LAYER                                 |
| PCT/US2013/073327     | SP12-0067PCT              | WIPO    | 12/05/2013  |            | INTEGRATED CIRCUITS WITH NON-VOLATILE MEMORY AND METHODS<br>FOR MANUFACTURE                         |
| PCT/US2013/074651     | SP12-0068PCT              | WIPO    | 12/12/2013  |            | HIGH VOLTAGE GATE FORMATION                                                                         |
| PCT/US2013/074390     | SP12-0069PCT              | WIPO    | 12/11/2013  |            | MEMORY FIRST PROCESS FLOW AND DEVICE                                                                |
| PCT/US2013/074386     | SP12-0070PCT              | WIPO    | 12/11/2013  |            | CHARGE TRAPPING SPLIT GATE EMBEDDED FLASH MEMORY AND<br>ASSOCIATED METHODS                          |
| PCT/US2013/074652     | SP12-0071PCT              | WIPO    | 12/12/2013  |            | CHARGE TRAPPING DEVICE WITH IMPROVED SELECT GATE TO<br>MEMORY GATE ISOLATION                        |
| PCT/US2013/074713     | SP12-0072PCT              | WIPO    | 12/12/2013  |            | THREE DIMENSIONAL CAPACITOR                                                                         |
| PCT/US2013/074710     | SP12-0073PCT              | WIPO    | 12/12/2013  |            | USE DISPOSABLE GATE CAP TO FORM TRANSISTORS, AND SPLIT<br>GATE CHARGE TRAPPING MEMORY CELLS         |
| PCT/US2013/074732     | SP12-0074PCT              | WIPO    | 12/12/2013  |            | PROCESS CHARGING PROTECTION FOR SPLIT GATE CHARGE<br>TRAPPING FLASH                                 |
| PCT/US2013/074724     | SP12-0075PCT              | WIPO    | 12/12/2013  |            | CHARGE TRAPPING SPLIT GATE DEVICE AND METHOD OF<br>FABRICATING SAME                                 |
| PCT/US2013/074659     | SP12-0076PCT              | WIPO    | 12/12/2013  |            | MEMORY GATE LANDING PAD MADE FROM DUMMY FEATURES                                                    |
| PCT/US2014/060714     | SP12-0077PCT              | WIPO    | 10/15/2014  |            | THREE-DIMENSIONAL CHARGE TRAPPING NAND CELL WITH<br>DISCRETE CHARGE TRAPPING FILM                   |
| PCT/US2014/013853     | SP12-0079PCT              | WIPO    | 01/30/2014  |            | MANUFACTURING OF FET DEVICES HAVING LIGHTLY DOPED DRAIN<br>AND SOURCE REGIONS                       |
| PCT/US2014/032674     | SP12-0081PCT              | WIPO    | 04/02/2014  |            | AUTHENTICATION FOR RECOGNITION SYSTEMS                                                              |
| PCT/US2014/071524     | SP13-0008PCT              | WIPO    | 12/19/2014  |            | GATE FORMATION MEMORY BY PLANARIZATION                                                              |
| PCT/US2014/040873     | SP13-0009PCT              | WIPO    | 06/04/2014  |            | PROGRAMMABLE LATENCY COUNT TO ACHIEVE HIGHER MEMORY<br>BANDWIDTH                                    |