PATENT ASSIGNMENT COVER SHEET

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CONVEYING PARTY DATA

Name	Execution Date
WORLDWIDE SEMICONDUCTOR MANUFACTURING CORP.	06/01/2000

RECEIVING PARTY DATA

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ASSIGNMENT OF PATENTS AND PATENT APPLICATIONS

Worldwide Semiconductor Manufacturing Corp., A Taiwanese corporation having a place of business at No. 25, Li-Hsin Road, Science-Based Industrial Park, Hsinchu, Taiwan, R.O.C., (hereafter ASSIGNOR) has been assigned or otherwise has an ownership interest in certain new and useful improvements as set forth in the patents and patent applications listed in attached Appendix A.

For good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, ASSIGNOR hereby:

1) Sell(s), assign(s) and transfer(s) to Taiwan Semiconductor Manufacturing Co., Ltd., a Taiwanese corporation having a place of business at 121, Park Ave. III, Science-Based Industrial Park Hsin-Chu 300, Taiwan, R.O.C. (hereinafter referred to as "ASSIGNEE") the entire right, title and interest in any and all improvements and inventions disclosed in, application(s) based upon, and Patent(s) (including foreign parents) granted upon the information which is disclosed therein.

2) Authorize and request the Commissioner of Patents to issue any and all Letters Patents resulting from said application(s) or any division(s), continuation(s), substitute(s), re-examination(s) or reissue(s) thereof to the ASSIGNEE.

3) Agree to execute all papers and documents and, entirely at the ASSIGNEE's expense, perform any acts which are reasonably necessary in connection with the prosecution of said application(s), as well as any derivative and applications thereof, foreign applications based thereon, and/or the enforcement of patents resulting from such applications.

4) Agree that the terms, covenants and conditions of this assignment shall inure to the benefit of the ASSIGNEE, its successors, assigns and other legal representative(s), and shall be binding upon the inventor(s), as well as the inventor's heirs, legal representatives and assigns.

5) Warrant and represent that ASSIGNOR has not entered, and will not enter into any assignment, contract, or understanding that conflicts with this assignment.

Signed on the date(s) indicated beside my (our) signature(s).

Worldwide Semiconductor Manufacturing Corp.

By: _____ Date: June 1, 2000
Typed Name: Teyin Mark Liu
President
Worldwide Semiconductor Manufacturing Corp.

Witnesses:

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Appendix A

Title	Filing Date	Serial No.
Method for manufacturing interconnection plug	1997/12/5	08/985,698
Method for making a DRAM capacitor using a double layer of insitu doped polysilicon and undoped amorphous polysilicon with HSG polysilicon	1998/3/12	09/041,863
Method of making a DRAM cell with advantage of reduced aspect ratio for peripheral contact holes	1998/3/12	09/041,868
Method for automatically determing adjustments for stepping photolithography exposures	1998/3/30	09/050,740
Multi-level flash memory using triple well process and method of making	1998/3/30	09/050,741
Method for manufacturing a double crown capacitor for DRAM memory cell	1998/4/9	09/058,319
Dishing free process for shallow trench isolation	1998/4/15	09/060,771
Method for manufacturing split-gate flash memory cell	1998/4/16	09/061,618
Method of fabricating split-gate source side injection flash EEPROM array	1998/4/20	09/063,032
ROM structure and method of manufacture	1998/4/23	09/065,781
In situ plasma clean for tungsten etching back	1998/5/26	09/085,322
Method for forming a dual damascene contact and interconnect	1998/6/3	09/089,875
Interlayer dielectric planarization process	1998/6/12	09/096,901
Method of fabricating a split gate structure of a flash	1998/6/19	09/099,975
Method for reducing profile micro-loading during etching of nitride	1998/6/18	09/100,159
Method for forming a DRAM capacitor	1998/7/1	09/108,901
Low voltage flash memory cell and method of making	1998/7/8	09/111,656
Method for making a mushroom shaped DRAM capacitor	1998/7/17	09/118,170
Method for making a stacked DRAM capacitor	1998/7/22	09/121,021
Installation for improving chemical-mechanical polishing operation	1998/9/17	09/156,522
Method for forming planar intermetal or interlayer dielectric	1998/9/17	09/156,574
Dispensing tube design of chemical mechanical polishing station	1998/9/21	09/157,662
Installation for improving chemical-mechanical polishing operation	1998/9/21	09/157,716
Method for making a stack bottom storage node having reduced crystallization of amorphous polysilicon	1998/10/13	09/170,861
Single polysilicon DRAM cell with current gain and method of making	1998/10/13	09/170,863
Low voltage, low power n-channel flash memory cell using gate induced drain leakage current	1998/10/22	09/177,786
CMOS inverter using gate induced drain leakage current	1998/10/22	09/177,787
Method for manufacturing a self-aligned stacked storage node DRAM cell	1998/11/9	09/189,067
Method for making FIN-trench structured DRAM capacitor	1998/11/9	09/189,353
Installation for improving chemical-mechanical polishing operation	1998/11/25	09/200,072
Wafer cleaning device	1998/11/25	09/200,174
Installation for improving chemical-mechanical polishing operation	1998/11/25	09/200,364
Method for forming a crown capacitor	1998/11/30	09/201,280
Method for forming a planar intermetal dielectric using a barrier layer	1998/11/30	09/201,513
Method for forming a T-shaped plug having increased contact area	1998/11/30	09/201,581
Method for fabricating conducting lines with a high topography height	1998/12/7	09/206,780
Method of forming stacked capacitor	1998/12/7	09/206,807
Method for forming a crown capacitor	1998/12/9	09/209,047
Method for forming a borderless contact	1999/2/1	09/241,543
A method to reduce aspect ratio of DRAM peripheral contact	1999/2/9	09/246,919

Title	Filing Date	Serial No.
Method of planartzation	1999/2/9	09/247,749
Multi-exposure process	1999/2/16	09/250,786
A new SRAM cell structure using two single-transistor inverters	1999/2/19	09/253,322
Prediction based technique for high-speed memory built-in self test circuit	1999/3/3	09/261,800
Method to fabricate electrode for low-K dielectrics	1999/3/10	09/265,357
A new electron injection method for substrate-hot-electron program and erase VT tightening for ETOX cells in triple-well	1999/3/24	09/275,523
Method for forming tungsten plugs in interlayer dielectric using mixed mode deposition process	1999/3/26	09/277,451
Method for fabricating metal interconnect structure	1999/3/29	09/280,628
Method for planarizing polysilicon layer	1999/3/29	09/282,052
Method of fabricating shallow trench isolation structur	1999/4/5	09/286,014
Transistor and logic circuit on thin silicon-on-insulator wafers based on gate induce drain leakage currents	1999/4/8	09/286,946
Method for reducing capacitance depletion during hemispherical grain polysilicon synthesis for DRAM application	1999/4/7	09/287,959
High speed built-in self-test for DRAMs	1999/4/12	09/290,384
Method of fabricating read only memory	1999/4/16	09/293,435
DRAM capacitor and a method of fabricating the same	1999/4/19	09/293,973
Method of forming a tungsten plug	1999/4/19	09/293,974
A NOR architechture and operation methods for ETOX cells capable of full EEPROM functions	1999/4/20	09/295,017
Structurer and fabricating method of stacked capacitor	1999/4/26	09/299,956
Method for manufacturing stacked capacitor	1999/4/26	09/299,963
Method for forming a hard mask of half critical dimension	1999/4/28	09/301,481
Method of fabricating DRAM with novel landing pad process	1999/4/28	09/301,482
A built-in-self-test circuit for RAMBUS direct RDRAM	1999/4/30	09/303,770
Method for fabricating capacitor	1999/5/6	09/306,095
Bonding pad structure	1999/5/6	09/306,097
Method for planarizing oxide layer	1999/5/6	09/306,245
Method of manufacturing DRAM capacitor	1999/5/6	09/306,261
Method for fabricating metal plug	1999/5/6	09/306,341
Method for manufacturing metal plug	1999/5/6	09/306,342
Method of planarizing insulator laye	1999/5/6	09/306,346
Method of manufacturing Mask-Read-Only-Memory	1999/5/6	09/306,351
HDP-CVD method for spacer forming	1999/5/10	09/307,760
Novel method to form a poly connector	1999/5/10	09/307,761
Vertical thin film transistor as a load device in SRAM technology	1999/5/17	09/312,816
Movable multi-function maintenance apparatus	1999/5/17	09/313,169
Method for manufacturing bit lines in memory	1999/5/17	09/313,521
Method of manufacturing a capacitor for high density DRAMs	1999/5/19	09/314,018
Method of forming a vertical thin film transistor and the structure of the same	1999/5/19	09/314,623
Method of planarization	1999/5/21	09/316,664
Method for forming a DRAM capacitor	1999/5/24	09/317,132
Fabrication method of shallow trench isolation	1999/6/10	09/317,678

Appendix A

Title	Filing Date	Serial No.
Digitally tunable voltage reference using a neuron MOSFET	1999/6/4	09/326,166
A fabrication method of a twin-tub capacitor	1999/6/4	09/326,390
Method for fabrication a capacitor with a low resistance electrode structure in integrated circuit	1999/6/4	09/326,391
A high performance poly load SRAM device and a method of fabrication the same	1999/6/7	09/326,658
Method of making a MOSFET with self-aligned source and drain contacts	1999/6/4	09/327,093
Method for manufacturing DRAM capacitor	1999/6/9	09/328,755
Method for reducing contact resistance	1999/6/9	09/328,978
Method for forming buried contact	1999/6/9	09/328,979
Method of fabricating low voltage coefficient capacitor	1999/6/9	09/328,980
Method fo fabricamng landing pad	1999/6/9	09/328,981
ETOX cell having bipolar electron injection for substrate-hot-electron program	1999/6/18	09/334,080
Method for manufacturing stacked capacitor	1999/6/18	09/335,547
Method of fabricating copper damascene	1999/6/18	09/335,553
Method of manufacturing a DRAM capacitor	1999/6/18	09/335,631
Method of fabricating gate	1999/6/18	09/335,632
A method for fabricating a bonding pad structure for improving the bonding pad structure quality	1999/6/18	09/336,044
Method of planarizing inter-metal dielectric layer	1999/6/18	09/336,045
Apparatus for chemical-mechanical polishing	1999/6/29	09/342,414
Fabricating method of a capacitor	1999/6/29	09/342,569
Method of protecting tungsten plug from corroding	1999/6/29	09/342,570
A method of copper dual damascene	1999/6/29	09/342,708
Method of fabricating capacitor	1999/6/29	09/342,718
Method of fabricating shallow trench isolation	1999/6/29	09/343,053
Method for manufacturing gate dielectric layer	1999/6/29	09/343,137
Method for making a DRAM capacitor using a rotated photolithography mask	1999/7/2	09/346,324
Split gate flash memory cell	1999/7/2	09/347,203
Device and method for planarizing a thin film	1999/7/9	09/350,964
A method for forming gate oxide layer with multiple thickness	1999/7/9	09/350,981
Method for forming vertical thin film transistor and the structure of the same	1999/7/12	09/351,275
Method of reducing CMP dishing effect	1999/7/15	09/354,622
A method for forming a novel self-aligned offset thin film transistor and the structure of the same	1999/7/22	09/358,761
Method of forming a novel self-aligned offset thin film transistor and the structure of the same	1999/7/22	09/358,762
Method of forming dual damascene structures	1999/7/23	09/359,414
Method of forming shallow trench isolation	1999/7/23	09/359,415
Novel vertical poly load device in 4T SRAM technology	1999/7/26	09/360,809
Current source using merged vertical bipolar transistor on gate induced gate leakage current	1999/7/27	09/362,916
Electrostatic discharge protection device with resistive drain structure	1999/8/2	09/365,186
Vertical bipolar transistor based on gate induced drain leakage current	1999/8/2	09/365,436
EPROM cell structure and a method for forming the EPROM cell structure	1999/8/3	09/365,732
Method for forming a flash memory cell with improved drain erase performance	1999/8/3	09/365,733

Appendix A

Title	Filing Date	Serial No.
Method of preventing a conductive layer corrosion during forming a halogen-doped silicon glass	1999/8/3	09/365,878
Electrical overlay structure for monitoring multilayer alignment in a semiconductor wafer	1999/8/4	09/368,622
Structure and fabrication method for multiple crown capacitor	1999/8/10	09/371,728
Method for forming self-aligned contact	1999/8/10	09/371,734
Method for making a DRAM capacitor using a double layer of insitu doped silicon and undoped amorphous silicon with HSG polysilicon	1999/8/11	09/372,382
Self-aligned etching process	1999/8/12	09/373,318
Method to fabricate DRAM capacitor using damascene process	1999/8/17	09/375,519
Method to fabricate embedded DRAM with salicide logic cell structure	1999/8/8	09/376,481
Single poly cylindrical flash memory cell having high coupling ratio	1999/8/20	09/378,044
ETOX cell programmed by band-to-band tunneling induced substrate hot electron and read by gate induced drain leakage	1999/8/19	09/378,197
Source side injection flash EEPROM memory cell and operation	1999/8/20	09/378,271
A one transistor EEPROM cell using FERRO-ELECTRIC spacer	1999/8/19	09/378,558
Method for programming and erasing a triple-poly split-gate flash memory	1999/8/24	09/382,078
Method of fabricating reduced critical dimension for conductive line and space	1999/8/26	09/384,013
Method for forming inter-metal dielectric layers in metallizanon process	1999/9/1	09/387,306
Method for forming bottom anti-reflective coating (BARC)	1999/9/1	09/387,730
Method for forming salicide process by using double sidewall spacer	1999/9/7	09/390,696
Method for forming via and interconnect in dual damascene	1999/9/8	09/391,179
Method of forming tunable N and K of anti-reflective coatings	1999/9/8	09/391,495
Method for improving the thermal conductivity of metal line in integrated circuit	1999/9/8	09/391,496
Process of planarizing crown capacitor for integrated circuit	1999/9/8	09/392,158
Wafer surface protection method	1999/9/10	09/393,609
Method of fabricating bit lines	1999/9/10	09/393,610
Method to fabricate DRAM capacitor	1999/9/10	09/393,705
A fabrication method of a device isolation structure	1999/9/10	09/393,983
Method for fabricating a crown-shaped capacitor in a dynamic random access memory	1999/9/10	09/394,261
Method for manufacturing floating gate of stacked-gate nonvolatile memory unit	1999/9/10	09/394,270
Fabrication method of shallow trench isolation	1999/9/10	09/394,273
Method of fabricating landing plug with borderless contact	1999/9/10	09/394,806
Method for manufacturing stacked capacitor	1999/9/14	09/395,090
Method for forming pullback opening above shallow trench isolation structure	1999/9/14	09/395,108
Method of fabrication transistor	1999/9/14	09/395,109
Method of forming shallow trench isolation structure	1999/9/14	09/395,110
Method for forming contact plug	1999/9/14	09/395,111
Method of forming a DRAM crown capacitor	1999/9/14	09/395,187
Method for fabricating an embedded flash memory cell	1999/9/14	09/395,188
Method of fabricating shallow trench isolation	1999/9/14	09/395,428
Pull-back process in shallow trench isolation	1999/9/14	09/395,784
Fabrication method of landing pad	1999/9/14	09/395,897
Method for fabricating a nonvolatile memory cell with high coupling ratio	1999/9/21	09/400,370

Title	Filing Date	Serial No.
Interconnection lines for improving thermal conductivity in integrated circuits and method for fabricating the same	1999/9/20	09/400,626
Method for forming a capacitor of DRAM cell	1999/9/28	09/406,728
Method of forming salicide	1999/10/4	09/410,949
Wafer inspection and defect analysis method	1999/10/4	09/410,950
Method for forming flash memory of ETOX-cell programmed by band-to-band tunneling induced substrate hot electron and read by gate induced drain leakage current	1999/10/1	09/411,133
Fabrication method for a borderless via of a semiconductor device	1999/10/7	09/414,252
Method of forming self-aligned mask ROM	1999/10/7	09/414,281
Method of fabricating dual damascene structure	1999/10/8	09/414,817
Short channel effect free MOSFET and method of making	1999/10/13	09/416,906
Pre-treatment process for salicide process	1999/10/13	09/417,357
Method of fabricating a flash memory	1999/10/13	09/417,393
A single poly EPLD cell and its fabricating method	1999/10/15	09/418,833
Method for forming a crown capacitor having HSG for DRAM memory	1999/10/13	09/419,402
Method and apparatus for high speed analog to digital conversion of video graphic signals using interleaving	1999/10/14	09/419,616
Method of fabricating multi-level mask ROM	1999/10/20	09/422,024
Flash memory cell using N+/P-well diode with double poly floating gate	1999/10/20	09/422,050
Single polysilicon DRAM cell and array with current gain	1999/10/20	09/422,051
Multi-level flash memory using triple well process and method of making	1999/10/26	09/427,438
Method for forming interlayer dielectric layer	1999/10/28	09/429,190
Dual-damascene process	1999/10/28	09/429,601
Method for forming interlayer dielectric layer	1999/10/29	09/430,749
Self-aligned coding process for a mask read-only memory	1999/11/9	09/436,964
Dynamic random access memory with slanted active regions	1999/11/15	09/439,988
Nonvolatile memories with hith capacitive-coupling ratio	1999/11/15	09/440,138
Method of manufacturing crown-shaped DRAM capacitor	1999/11/16	09/440,902
Method of planarizing polysilicon plug	1999/11/16	09/440,904
Method to protect alignment mark in CMP process	1999/11/24	09/444,922
Method of manufacturing deep trench capacitor	1999/11/23	09/448,017
Method of forming shallow trench isolation structure	1999/11/23	09/448,018
Method for manufacturing stacked capacitor	1999/11/30	09/451,384
Method of forming dual layer anti-reflective coatings	1999/12/1	09/451,853
Fabrication method for a stacked capacitor	1999/12/3	09/454,387
Flash memory cell using P+/N-well with double poly floating gate	1999/12/2	09/454,490
Auto slurry deliver fine-tune system for chemical-mechanical-polishing process and method of using the system	1999/12/31	09/458,827
Method of forming the metal line and inter metal dielectric	1999/12/13	09/458,828
Method of forming shallow trench isolation structure	1999/12/13	09/460,359
Fabrication method for a metal interconnect	1999/12/13	09/460,667
Failure site addressable test for integrated circuit	1999/12/17	09/465,531
Low voltage flash memory cell	1999/11/10	09/465,531
Method of forming via	1999/12/17	09/465,905

Title	Filing Date	Serial No.
Method of manufacturing double-recess crown-shaped DRAM capacitor	1999/12/17	09/466,044
Self-aligned contact process	1999/12/21	09/468,196
Method to solve implant photo layer overlaying with layers thereon	1999/12/29	09/473,983
Process for forming a borderless via in a semiconductor device	2000/1/13	09/482,421
Method of manufacturing DRAM capacitor	2000/1/13	09/482,757
Single poly source side injection flash EEPROM memory cell and operation	2000/1/18	09/484,946
Method of forming crown-shaped capacitor	2000/1/21	09/488,955
Method of forming shallow trench isolation structure	2000/1/24	09/490,275
Method of forming pattern	2000/1/25	09/491,067
Method of fabricating a DRAM crown capacitor	2000/1/31	09/494,177
Slurry dilution system capable of in-situ adjustment of slurry concentration	2000/1/31	09/494,178
Self-aligned fabricating process and structure of source line of ETOX flash memory	2000/1/13	09/494,524
Method of fabricating integrated circuit	2000/2/4	09/498,329
Method of manufacturing well-controled sizes of HSG grain	2000/2/4	09/498,478
Method for forming gate oxide in various thickness	2000/2/7	09/498,641
Copper damascene manufacturing process	2000/2/4	09/499,067
Modified IC socket	2000/2/17	09/506,248
Method of forming T-shaped gate	2000/2/24	09/513,268
Method for forming an epitaxial silicon-germanium layer	2000/2/29	09/515,017
Method of fabricating capacitors and devices in mixed-signal integrated circuit	2000/2/29	09/515,119
Self-aligned process for forming source line of ETOX flash memory	2000/2/29	09/515,302
Method of fabricating a mask ROM	2000/2/29	09/515,953
Split-gate flash memory with self-aligned source line	2000/2/29	09/515,957
Method for predicting Ig-max for a PMOS transistor for use in reliability analysis	2000/3/10	09/517,132
Method of forming shallow trench isolation region	2000/3/3	09/518,022
Alignment mark configuration	2000/3/8	09/521,021
Damascene local interconnect process	2000/3/7	09/521,085
Multi-zone conditioner for chemical mechanical polishing system	2000/3/14	09/525,005
Method of fabricating interconnects	2000/3/20	09/528,645
Method for fabricating a small dimension trench structure	2000/3/20	09/531,907
ETOX-cell with multi-layer nano-Si-crystal dots as floating gate and method of making	2000/3/22	09/532,472
Method for forming an attenuated phase-shifting mask	2000/3/24	09/534,171
A method of fabricating copper damascene	2000/3/24	09/535,494
Quake-proof pad	2000/3/24	09/535,498
Bonding pad structure and manufacturing method thereof	2000/3/24	09/535,509
Process for fabricating capacitor	2000/5/4	09/538,911
Method for reading 2-bit ETOX-cells using gate induced drain leakage current	2000/4/7	09/545,038
Method of fabricating copper damascene	2000/4/10	09/546,423
CMOS transistor on thin silicon-on-insulator using accumulation as conduction mechanism	2000/4/18	09/551,717
Method of fabricating dual damascene structure	2000/4/25	09/557,510
Method of doing ESD protective device ion implantat without additional photo mask	2000/5/11	09/568,495

Title	Date of Patent	Patent No.
Method for forming a planar intermetal dielectric layer	1999/8/3	5,932,487
Method for erasing split-gate flash memory	1999/11/2	5,978,274
Improved method for forming a planar intermetal dielectric layer	2000/2/1	6,020,265
Reduction of optical proximity effect of bit line pattern in DRAM devices	2000/1/18	6,015,641
Method for forming barrier layer tungsten plugs in interlayer dielectrics	2000/2/8	6,022,800
Hot carrier injection programming and negative gate voltage channel erase flash EEPROM structure	2000/2/15	6,026,028
Method for manufacturing ETOX cell having damage-free source region	1999/12/7	5,998,262
Single poly cylindrical flash memory cell having high coupling ratio	1999/10/26	5,973,354
Method for making a flower shaped DRAM capacitor	2000/3/28	6,043,131
Method for manufacturing interconnection plug	1999/11/9	5,981,386
Method for making an 8-shaped storage node DRAM cell	2000/3/7	6,033,966
Method for making dual damascene contact	1999/6/29	5,916,823
Method for fabricating a stack capacitor	1999/12/21	6,004,859
Method of using silicon oxynitride to improve fabricating of DRAM contacts and landing pads	2000/2/8	6,022,776
Single poly EEPROM cell	2000/2/15	6,023,625
Method of fabricating a capacitor electrode structure in a dynamic random-access memory device	2000/3/14	6,037,217
Electrostatic discharge protection circuit employing MOSFETs having double ESD implantations	2000/3/21	6,040,603
Alignment-marker structure and method of forming the same in integrated circuit fabrication	2000/5/9	6,060,786