PATENT ASSIGNMENT COVER SHEET

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
ALLVIA, INC.	10/20/2011

RECEIVING PARTY DATA

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Property Type	Number
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DATE SIGNED:	08/12/2015

Total Attachments: 11
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Assignment

THIS DEED OF ASSIGNMENT ("**Assignment**"), EFFECTIVE AS OF OCTOBER 21, 2011, IS MADE BY AND BETWEEN

ALLVIA, Inc. (hereinafter "**ASSIGNOR**"), a corporation organized under the laws of the State of California with its principal place of business located at 657 N. Pastoria Ave., Sunnyvale, California 94085; and

INVENSAS CORPORATION (hereinafter "**INVENSAS**"), a Delaware corporation having a place of business at 2702 Orchard Parkway, San Jose, California 95134, United States.

WHEREAS:

A ASSIGNOR is the sole owner in respect of the patents and patent applications listed in the attached Appendix (hereinafter "the **PATENTS**"); and

B INVENSAS is desirous of acquiring all of the worldwide right, title and interest in and to the PATENTS and the inventions disclosed therein.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, **ASSIGNOR** has sold, assigned and transferred, and does hereby sell, assign and transfer to **INVENSAS** all of the worldwide right, title and interest in (i) the **PATENTS** and the inventions and improvements disclosed therein; (ii) all reissues, divisionals, continuations, continuations-in-part, extensions, renewals, reexaminations and foreign counterparts thereof, and other patents, patent applications, certificates of invention other governmental grants resulting from the **PATENTS**; (iii) all patents and applications which claim priority to or have common disclosure or common priority with any such patents or patent applications, and (iv) all rights corresponding to any of the foregoing throughout the world (including the right to claim the priority date of any of the **PATENTS** and the right to sue for and recover damages for any past, present or future infringement of the Patents), the same to be held and enjoyed by **INVENSAS** for its own use and enjoyment, and for the use and enjoyment of its successors, assigns and other legal representatives, to the end of the term or terms of such **PATENTS** granted or reissued or reexamined as fully and entirely as the same would have been held and enjoyed by **ASSIGNOR**, if this assignment and sale had not been made.

IN WITNESS WHEREOF, **ASSIGNOR** has caused these presents to be signed by its duly appointed trustee having full authority to convey its property; and **INVENSAS** has caused these presents to be signed by its duly appointed trustee.

And if the issue date and/or patent number of any of the **PATENTS** is unknown to **ASSIGNOR** and **INVENSAS** at the time this Assignment is executed, **ASSIGNOR** does hereby authorize its attorneys to insert on this Assignment the issue date and patent number of such any patent when known.

ASSIGNOR hereby declares that **INVENSAS** may take the steps for recordal of this assignment in the sole name of **INVENSAS.**

ASSIGNOR hereby undertakes that it shall, without further consideration, but at the expense of **INVENSAS**, execute all documents and do all such acts and things as **INVENSAS** may in its absolute discretion consider necessary or desirable to enable Letters Patent or any other form of protection to be issued in respect of any of such **PATENTS** and the inventions disclosed therein in any part of the world and to enable or to assist **INVENSAS** to defend oppositions thereto, to maintain the **PATENTS** and to prosecute for the infringement thereof.

SIGNED for and on behalf of

ASSIGNOR

by ______________________ on October 20, 2011
(Signature) (Date)

Sergey Savastiouk
(Print Name and Title)

State of California) SS:

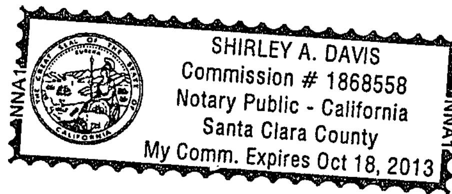
County of Santa Clara)

On this 20th day of October, 2011 before me, Shirley A. Davis, Notary Public, personally appeared Sergey Savastiouk, who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the instrument and acknowledged to me that he executed the same in his authorized capacity and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

____
(Notary Public)



SIGNED for and on behalf of

INVENSAS

by ______________________ on ______________________
(Signature) (Date)

____
(Print Name and Title)

State of California) SS:

County of ________________)

On this _____ day of ______________, 2011 before me, __________________________, personally appeared________________________________, who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the instrument and acknowledged to me that he/she executed the same in his/her authorized capacity, and that by his/her signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

____
(Notary Public)

APPENDIX

Listed Patents and Patent Applications

1. United States Listed Issued Patents and Pending Patent Applications

United States Listed Issued Patents

Patent Number	Filing Date	Application Number	Issue Date	Publication Number	Title
6095582	03/11/1998	09/041,284	08/01/2000	-	Article holders and holding methods
6139678	11/20/1997	08/975,403	10/31/2000	-	Plasma processing methods and apparatus
6184060	05/22/1998	09/083,927	02/06/2001	-	Integrated circuits and methods for their fabrication
6261375	07/17/2000	09/617,211	07/17/2001	-	Plasma processing methods and apparatus
6287976	05/19/1999	09/315,122	09/11/2001	-	Plasma processing methods and apparatus
6322903	12/06/1999	09/456,225	11/27/2001	-	Package of integrated circuits and vertical integration
6323134	03/07/2000	09/519,281	11/27/2001	-	Plasma processing methods and apparatus
6420209	03/29/2000	09/538,869	07/16/2002	-	Integrated circuits and methods for their fabrication
6423923	08/04/2000	09/632,485	07/23/2002	-	Monitoring and controlling separate plasma jets to achieve desired properties in a combined stream
6448153	12/28/2000	09/752,802	09/10/2002	-	Thinning and dicing of semiconductor wafers using dry etch, and obtaining semiconductor chips with rounded bottom edges and corners
6462300	08/02/2001	09/922,069	10/08/2002	US-2002-0017508	Monitoring and controlling separate plasma jets to achieve desired properties in a combined stream
6498074	06/06/2001	09/876,888	12/24/2002	US-2002-0013061	Thinning and dicing of semiconductor wafers using dry etch, and obtaining semiconductor chips with rounded bottom edges and corners
6498381	02/22/2001	09/792,311	12/24/2002	US-2002-0115290	Semiconductor structures having multiple conductive layers in an opening, and methods for fabricating same
6541729	08/02/2001	09/922,205	04/01/2003	US-2002-0014475	Monitoring and controlling separate plasma jets to achieve desired properties in a combined stream
6627039	04/03/2000	09/542,519	09/30/2003	-	Plasma processing methods and apparatus
6631935	08/04/2000	09/632,236	10/14/2003	-	Detection and handling of semiconductor wafer and wafer-like objects
6638004	07/13/2001	09/904,700	10/28/2003	US-2003-0012638	Article holders and article positioning methods

Patent Number	Filing Date	Application Number	Issue Date	Publication Number	Title
6639303	12/17/1999	09/466,535	10/28/2003	US-2002-0063311	Integrated circuits and methods for their fabrication
6664129	12/12/2002	09/318,833	12/16/2003	US-2003-0085460	Integrated circuits and methods for their fabrication
6665583	10/04/2002	10/265,056	12/16/2003	US-2003-0040837	Article holders with sensors detecting a type of article held by the holder
6667242	01/08/2001	09/757,242	12/23/2003	US-2001-0002613	Brim and gas escape for non-contact wafer holder
6688662	04/02/2002	10/116,462	02/10/2004	US- 2003-0052495	Detection and handling of semiconductor wafers and wafer-like objects
6693361	11/16/2000	09/716,092	02/17/2004	-	Packaging of integrated circuits and vertical integration
6717254	02/22/2001	09/791,977	04/06/2004	US-2002-0113321	Devices having substrates with opening passing through the substrates and conductors in the openings, and methods of manufacture
6730540	04/18/2002	10/127,144	05/04/2004	US-2003-0199123	Clock distribution networks and conductive lines in semiconductor integrated circuits
6740582	04/26/2002	10/133,595	05/25/2004	US-2002-0127868	Integrated circuits and methods for their fabrication
6753205	01/27/2003	10/352,607	06/22/2004	US-2003-0148552	Method for manufacturing a structure comprising a substrate with a cavity and a semiconductor integrated circuit bonded to a contact pad located in the cavity
6759341	04/09/2003	10/412,978	07/06/2004	-	Wafering method comprising a plasma etch with a gas emitting wafer holder
6844241	08/28/2001	09/941,447	01/18/2005	US-2002-0115260	Fabrication of semiconductor structures having multiple conductive layers in an opening
6882030	01/28/2002	10/059,898	04/19/2005	US-2002-0084513	Integrated circuit structures with a conductor formed in a through hole in a semiconductor substrate and protruding from a surface of the substrate
6897148	04/09/2003	10/410,929	05/24/2005	US-2004-0203224	Electroplating and electroless plating of conductive materials into openings, and structures obtained thereby
6958285	03/27/2002	10/109,233	10/25/2005	US-2002-0115234	Methods of manufacturing devices having substrates with opening passing through the substrates and conductors in the openings
7001825	12/16/2004	11/014,464	02/21/2006	US-2005-0106845	Semiconductor structures having multiple conductive layers in an opening, and methods for fabricating same
7034401	05/05/2005	11/123,532	04/25/2006	US-2005-0189636	Packaging substrates for integrated circuits and soldering methods

Patent Number	Filing Date	Application Number	Issue Date	Publication Number	Title
7049170	12/17/2003	10/739,788	05/23/2006	US-2005-0136634	Integrated circuits and packaging substrates with cavities, and attachment methods including insertion of protruding contact pads into cavities
7060601	12/17/2003	10/739,707	06/13/2006	US-2005-0133930	Packaging substrates for integrated circuits and soldering methods
7104579	01/12/2004	10/756,631	09/12/2006	US-2004-0150237	Detection and handling of semiconductor wafers and wafer-like objects
7173327	05/18/2005	11/131,711	02/06/2007	US-2005-0207238	Clock distribution networks and conductive lines in semiconductor integrated circuits
7179397	04/15/2003	10/414,603	02/20/2007	US-2003-0196754	Plasma processing methods and apparatus
7186586	10/19/2005	11/253,943	03/06/2007	US-2006-0035416	Integrated circuits and packaging substrates with cavities, and attachment methods including insertion of protruding contact pads into cavities
7241641	10/19/2005	11/253,492	07/10/2007	US-2006-0040423	Attachment of integrated circuit structures and other substrates to substrates with vias
7241675	03/10/2004	10/798,540	07/10/2007	US-2005-0136635	Attachment of integrated circuit structures and other substrates to substrates with vias
7510928	05/05/2006	11/418,801	03/31/2009	US-2007-0257367	Dielectric trenches, nickel/tantalum oxide structures, and chemical mechanical polishing techniques
7521360	10/10/2006	11/548,053	04/21/2009	US-2007-0128868	Electroplating and electroless plating of conductive materials into openings, and structures obtained thereby
7964508	08/21/2008	12/196,065	06/21/2011	US-2008-0311749	Dielectric trenches, nickel/tantalum oxide structures, and chemical mechanical polishing techniques

United States Listed Pending Patent Applications

Application Number	Filing Date	Publication Number	Title
11/744,046	05/03/2007	US-2008-0271995	Agitation of electrolytic solution in electrodeposition
11/866,186	10/02/2007	US-2008-0025009	Dielectric trenches, nickel/tantalum oxide structures, and chemical mechanical polishing techniques
13/042,186	03/07/2011	-	Substrates with through vias with conductive features for connection to integrated circuit elements, and methods for forming through vias in substrates
13/181,006	07/12/2011	-	Structures with through vias passing through a substrate comprising a planar insulating layer between semiconductor layers

2. Foreign Listed Issued Patents and Pending Patent Applications

Foreign Listed Issued Patents

Patent Number	Country	Filing Date	Application Number	Issue Date	Publication Number	Title
4397986	JP	11/16/1998	10-342346	10/30/2009	-	Plasma processing methods and apparatus
3537447	JP	10/27/1997	1998-520556	03/26/2004	-	Integrated circuits and methods for their fabrication
4063078	JP	02/22/2001	2002-576018	01/11/2008	2004-526321	The semiconductor structure by which several conductive layers were formed in opening, and its manufacturing method
587124	KR	05/20/2000	2000-7005527	05/29/2006	-	Plasma processing methods and apparatus
377033	KR	04/28/1999	1999-703711	03/10/2003	2000-052865	Integrated circuits and method for fabricating the same
509898	KR	02/20/2002	2003-7010999	08/17/2005	86594/2003	Semiconductor structures having multiple conductive layers in an opening, and methods for fabricating same

Foreign Listed Pending Patent Applications

Country	Filing Date	Application Number	Publication Number	Title
EP	10/27/1997	04021536.0	1503406	Back-side contact pads of a semiconductor chip
EP	10/27/1997	03017445.2	1387401	Integrated circuits and methods for their fabrication
EP	10/27/1997	97911823.9	948808	Integrated circuits and methods for their fabrication
EP	10/27/1997	10179553.2	2270845	Integrated circuits and methods for their fabrication
EP	10/27/1997	10179557.3	2270846	Integrated circuits and methods for their fabrication
EP	01/25/2001	01906698.4	1266399	Thinning and dicing of semiconductor wafers using dry etch, and obtaining semiconductor chips with rounded bottom edges and corners
EP	12/06/2000	00982464.0	1247294	Packaging of integrated circuits and vertical integration
EP	02/20/2002	02739087.1	1386355A2	Semiconductor structures having multiple conductive layers in an opening, and methods for fabricating same
KR	05/02/2007	2008-7029677	2009-0010227	Dielectric trenches, nickel/tantalum oxide structures, and chemical mechanical polishing techniques

3. United States and Foreign Listed Abandoned/Expired Patents and Pending Patent Applications

Patent Number	Country	Filing Date	Application Number	Issue Date	Publication Number	Title
6203661	US	12/07/1999	09/457,042	03/20/2001	-	Brim and gas escape for non-contact wafer holder
6427991	US	08/04/2000	09/633,086	08/06/2002	-	Non-contact workpiece holder using vortex chuck with central gas flow
6615113	US	07/13/2001	09/904,638	09/02/2003	US-2003-0018410	Articles holders with sensors detecting a type of article held by the holder
6749764	US	11/14/2000	09/713,137	06/15/2004	-	Plasma processing comprising three rotational motions of an article being processed
6787916	US	09/13/2001	09/952,263	09/07/2004	US-2003-0047798	Structures having a substrate with a cavity and having an integrated circuit bonded to a contact pad located in the cavity
7027894	US	09/09/2003	10/659,562	04/11/2006	US-2004-0049318	Article holders with sensors detecting a type of article held by the holder
7144056	US	03/25/2003	10/397,906	12/05/2006	US-2004-0012214	Detection and handling of semiconductor wafers and wafer-like objects
-	US	05/24/2005	11/136,799	-	US-2005-0212127	Integrated circuits and packaging substrates with cavities, and attachment methods including insertion of protruding contact pads into cavities
-	US	10/19/2005	11/253,490	-	US-2006-0076661	Attachment of integrated circuit structures and other substrates to substrates with vias
-	US	02/26/2003	10/375,218	-	US-2003-0197239	Clock distribution networks and conductive lines in semiconductor integrated circuits
-	US	10/01/2004	10/956,827	-	US-2005-0051887	Clock distribution networks and conductive lines in semiconductor integrated circuits
-	US	11/14/2006	11/559,805	-	US-2007-0069377	Clock distribution networks and conductive lines in semiconductor integrated circuits
-	US	02/10/2005	11/055,940	-	US-2005-0170647	Electroplating and electroless plating of conductive materials into openings, and structures obtained thereby
-	US	10/29/1996	60/030,425	-	-	Back-side contact pads of a semiconductor chip

Patent Number	Country	Filing Date	Application Number	Issue Date	Publication Number	Title
-	US	01/26/2000	09/491,456	-	-	Back-side contact pads of a semiconductor chip
-	US	02/06/2001	09/673,392	-	-	Back-side contact pads of a semiconductor chip
-	US	07/24/2003	10/627,038	-	US-2004-0016406	Plasma processing comprising three rotational motions of an article being processed

Patent Number	Country	Filing Date	Application Number	Issue Date	Publication Number	Title
-	AU	12/06/2000	2001-19493	-	1949301	Packaging of integrated circuits and vertical integration
-	AU	02/20/2002	2002-311762	-	31176202	Semiconductor chip having multiple conductive layers in an opening, and method for fabricating same
-	AU	01/31/2001	2001-34799	-	3479901	Detection and handling of semiconductor wafers and wafer-like objects
-	AU	02/20/2002	2002-306557	-	30655702	Devices having substrates with openings passing through the substrates and conductors in the openings, and methods of manufacture
-	AU	07/18/2001	2001-80628	02/18/2002	8062801	Monitoring and controlling separate plasma jets to achieve desired properties in a combined stream
-	AU	11/09/2001	2002-30692	-	3069202	Plasma processing comprising three rotational motions of an article being processed
60217372	DE	07/08/2002	02740020.9	01/03/2007	-	Gegenstandshalter mit sensoren zur bestimmung der art des artikels, welcher durch den halter gehalten wird
69838398	DE	11/06/1998	9896016.5	09/05/2007	-	Plasma processing methods and apparatus
69933368 .7	DE	01/08/1999	99900804.8	09/27/2006	-	Haltzungverfahren und vorrichtung fuer einen wafer
1030788	EP	11/06/1998	9896016.2	-	-	Plasma processing methods and apparatus
1062683	EP	01/08/1999	1999900804	09/27/2006	-	Holding method and apparatus for a wafer

Patent Number	Country	Filing Date	Application Number	Issue Date	Publication Number	Title
1430513	EP	07/08/2002	02740020.9	01/03/2007	-	Articles holders with sensors detecting a type of article held by the holder
-	EP	11/06/1998	0201102.9	-	1246224	Plasma processing methods and apparatus
-	EP	02/20/2002	2002-780735	-	1412283A2	Devices having substrates with openings passing through the substrates and conductors in the openings, and methods of manufacture

Patent Number	Country	Filing Date	Application Number	Issue Date	Publication Number	Title
1030788	FR	11/06/1998	9896016.2	09/05/2007	-	Plasma processing methods and apparatus
1430513	FR	07/08/2002	02740020.9	01/03/2007	-	Articles holders with sensors detecting a type of article held by the holder
1010788	GB	11/06/1998	9896016.2	09/05/2007	-	Plasma processing methods and apparatus
1010788	IT	11/06/1998	9896016.2	09/05/2007	-	Plasma processing methods and apparatus
-	JP	01/19/1999	1999-10210	-	1999-330203	Article Holder and Holding Method
-	JP	01/25/2001	2001-555120	-	2003-521120	Integrated circuits and methods for their fabrication
-	JP	12/18/2002	Unknown	-	-	Back-side contact pads of a semiconductor chip
-	JP	02/20/2002	2002-567846	-	2004-525778	Devices having substrates with openings passing through the substrates and conductors in the openings, and methods of manufacture
-	JP	11/09/2001	2002-543469	-	2004-514284	Plasma Plasma processing comprising three rotational motions of an article being processed

Patent Number	Country	Filing Date	Application Number	Issue Date	Publication Number	Title
-	WO	12/16/2004	PCT/US04/42228	-	WO 2005/059998	Integrated circuits and packaging substrates with cavities, and attachment methods including insertion of protruding contact pads into cavities
-	WO	12/15/2004	PCT/US04/42204	-	WO 2005/059993	Packaging substrates for integrated circuits and soldering methods
-	WO	01/08/1999	PCT/US99/00430	-	WO 1999/046806	Article Holder and Holding Methods
-	WO	11/06/1998	PCT/US98/23701	-	WO 1999/26796	Plasma processing methods and apparatus
-	WO	10/27/1997	PCT/US97/18979	-	WO 1998/019337	Integrated circuits and methods for their fabrication

Patent Number	Country	Filing Date	Application Number	Issue Date	Publication Number	Title
-	WO	01/25/2001	PCT/US01/02544	-	WO 2001/56063	Thinning and dicing of semiconductor wafers using dry etch, and obtaining semiconductor chips with rounded bottom edges and corners
-	WO	12/18/2002	PCT/US02/41029	-	WO2003065450	Integrated circuits with backside contacts and methods for their fabrication
-	WO	05/19/2000	PCT/US00/13976	-	WO 2000/70659	Plasma processing methods and apparatus
-	WO	12/06/2000	PCT/US00/33073	-	WO 2001/41207	Packaging of integrated circuits and vertical integration
-	WO	02/22/2001	PCT/US02/05371	-	WO 2002/078087	Semiconductor structures having multiple conductive layers in an opening, and methods for fabricating same
-	WO	07/08/2002	PCT/US02/21600	-	WO 2003/007345	Article holders with sensors detecting a type of article held by the holder
-	WO	01/31/2001	PCT/US01/03578	-	WO 2002/012098	Detection and handling of semiconductor wafers and wafer-like objects
-	WO	02/20/2002	PCT/US02/05175	-	WO 2002/068320	Methods of manufacturing devices having substrates with opening passing through the substrates and conductors in the openings

Patent Number	Country	Filing Date	Application Number	Issue Date	Publication Number	Title
-	WO	05/02/2007	PCT/US07/68051	-	WO 2007/131046	Dielectric trenches, nickel/tantalum oxide structures, and chemical mechanical polishing techniques
-	WO	09/10/2002	PCT/US02/28862	-	WO 2003/023856	Method for manufacturing a structure comprising a substrate with a cavity and a semiconductor integrated circuit bonded to a contact pad located in the cavity
-	WO	04/30/2008	PCT/US08/062027	-	WO 2008/137459	Agitation of electrolytic solution in electrodeposition
-	WO	07/18/2001	PCT/US01/22804	-	WO 2002/013584	Monitoring and controlling separate plasma jets to achieve desired properties in a combined stream
-	WO	11/09/2001	PCT/US01/47391	-	WO 2002/041355	Plasma Plasma processing comprising three rotational motions of an article being processed