PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
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EPAS ID: PAT3558407

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
CONTOUR SEMICONDUCTOR, INC.	05/15/2015

RECEIVING PARTY DATA

Name:	HGST, INC.
Street Address:	3403 YERBA BUENA ROAD
City:	SAN JOSE
State/Country:	CALIFORNIA
Postal Code:	95135

PROPERTY NUMBERS Total: 1

Property Type	Number
Patent Number:	7460384

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Email: cthomas@pattersonsheridan.com,
psdocketing@pattersonsheridan.com
Correspondent Name: STEVEN H. VERSTEEG
Address Line 1: 24 GREENWAY PLAZA
Address Line 2: SUITE 1600
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ATTORNEY DOCKET NUMBER:	HGST/0021US
NAME OF SUBMITTER:	STEVEN H. VERSTEEG
SIGNATURE:	/Steven H. VerSteeg/
DATE SIGNED:	10/06/2015

Total Attachments: 8
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PATENT AND PATENT APPLICATION ASSIGNMENT

This PATENT AND PATENT APPLICATION ASSIGNMENT (this "Assignment") is entered into as of May 15, 2015 by and between Contour Semiconductor, Inc., a Delaware corporation ("Assignor"), and HGST, Inc., a Delaware corporation ("Assignee"). Capitalized terms not defined herein shall have the meanings ascribed to such terms in the Purchase Agreement (as defined below).

WHEREAS, Assignor entered into that certain Asset Purchase Agreement, dated as of May 15, 2015, with Buyer (the "Purchase Agreement"); and

WHEREAS, pursuant to the terms and conditions set forth in the Purchase Agreement, effective as of the date hereof, Assignor has agreed to sell, transfer, convey, assign and deliver to Assignee, and Assignee has agreed to purchase from Assignor, the Patent Assets;

NOW, THEREFORE, in consideration of the mutual covenants and agreements set forth in this Assignment and the Purchase Agreement and for other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the parties do hereby agree as follows:

1. Assignment of Patent Assets.

a. Assignor hereby sells, assigns, transfers and sets over to Assignee, Assignor's entire right, title and interest for all countries in and to: (i) all of the Patent Assets, including each of the Patents in the Intellectual Property Assets and all Patent Family Rights therein, further including, but not limited to those patents and patent applications listed on Schedule 1 of this Assignment; (ii) all rights to sue and recover for, and all rights to, profits or damages due or accrued arising out of or in connection with any and all past, present, or future infringements of any or all of the Patent Assets or any Patents arising therefrom.

b. Assignor authorizes and requests the respective worldwide Patent, Letters Patent and Industrial Property Offices to issue to the Assignee, its successors, assigns and legal representatives, in accordance with this Assignment, any and all Patents, letters patent or industrial property on the inventions or any of them disclosed in any of the Patent Assets.

c. Assignor authorizes and agrees that the Assignee may apply for and receive Patents, letters patents, industrial property or rights of any other kind for the inventions disclosed in any of the Patent Assets; and may claim, in applications for said patents, letters patent, industrial property or other rights, the priority of the Patent Assets under the provisions of the International Convention of 1883 and later modifications thereof, under the Patent Cooperation Treaty, under the European Patent Convention or under any other available international agreement.

2. Interpretation. This Assignment is intended only to document and effectuate the sale, assignment, conveyance and transfer of the Patent Assets to Assignee, and the Purchase Agreement is the exclusive source of the agreement and understanding between Assignor and Assignee with respect to the Patent Assets. Nothing contained in this Assignment modifies or alters the representations, warranties, covenants and obligations contained in the Purchase Agreement.

3. Rights under Purchase Agreement; Conflicts. Each of Assignor and Assignee, by their execution of this Assignment, hereby acknowledge that the rights and remedies of each party under the Purchase Agreement will not be deemed to be enlarged, modified or altered in any way by such execution of this Assignment. To the extent the terms and provisions of this Assignment conflict with the Purchase Agreement, the terms of the Purchase Agreement shall govern.

4. Binding Effect. This Assignment shall be binding upon and inure to the benefit of and be enforceable by the successors and assigns of the parties hereto.

5. Governing Law. Except to the extent that federal law preempts state law with respect to the matters covered hereby, this Assignment shall be governed by and construed in accordance with the internal laws of the State of California, without giving effect to any principles of conflicts of law.

6. Counterparts. This Assignment may be executed in any number of counterparts, each of which will be deemed an original, but all of which together will constitute one and the same instrument. A signed copy of this Assignment delivered by facsimile, e-mail or other means of electronic transmission shall be deemed to have the same legal effect as delivery of an original signed copy of this Assignment.

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IN WITNESS WHEREOF, the parties hereto have caused this Assignment to be duly executed as of May 15, 2015.

ASSIGNOR:

CONTOUR SEMICONDUCTOR, INC.

By _____
Name: Saul Zales
Title: Chief Executive Officer

State of California

The ~~Commonwealth of Massachusetts~~)
) ss.:
County of Sacramento)

On this 13th day of May, 2015, before me, M. Dibaj notary public personally appeared Saul Zales, CEO of Contour Semiconductor, Inc., personally known to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity and that by his signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

Witness my hand and official seal.

_____
Notary Public

M. DIBAJ
COMM. # 2168023
NOTARY PUBLIC-CALIFORNIA
SACRAMENTO COUNTY
My Comm. Exp. Mar. 28, 2018

[Additional Signature Page Follows]

ASSIGNEE:

HGST, Inc.

By _____
Name: Chelsea Ferraro
Title: VP and HGST General Counsel

SCHEDULE 1

ISSUED PATENTS

Patent No.	Issue Date	Title
US5673218	9/30/1997	Dual-addressed rectifier storage device
US5889694	3/30/1999	Dual-addressed rectifier storage device
US6586327	7/1/2003	Fabrication of semiconductor devices
US6598164	7/22/2003	Device and method for reducing piracy of digitized information
US6956757	10/18/2005	Low cost high density rectifier matrix memory
US7149934	12/12/2006	Error correcting memory access means and method
US7183206	2/27/2007	Fabrication of semiconductor devices
US7376008	5/20/2008	Scr matrix storage device
US7460384	12/2/2008	Low cost high density rectifier matrix memory
US7507663	3/24/2009	Fabrication of semiconductor devices
US7548454	6/16/2009	Memory array with readout isolation
US7548453	6/16/2009	Memory array with readout isolation
US7593256	9/22/2009	Memory array with readout isolation
US7593246	9/22/2009	Low cost high density rectifier matrix memory
US7652916	1/26/2010	Scr matrix storage device
US7667996	2/23/2010	Nano-vacuum-tubes and their application in storage devices
US7682981	3/23/2010	Topography transfer method with aspect ratio scaling
USRE41733	9/21/2010	Dual-addressed rectifier storage device
US7813157	10/12/2010	Non-linear conductor memory
US7826244	11/2/2010	Low cost high density rectifier matrix memory

US7916530	3/29/2011	Scr matrix storage device
USRE42310	4/26/2011	Dual-addressed rectifier storage device
US7933133	4/26/2011	Low cost, high-density rectifier matrix memory
US8000129	8/16/2011	Field-emitter-based memory array with phase-change storage devices
US8035416	10/11/2011	Bipolar-mos driver circuit
US8108735	1/31/2012	Error correcting memory access means and method
US8116109	2/14/2012	Low-cost high-density rectifier matrix memory
US8325556	12/4/2012	Sequencing decoder circuit
US8325557	12/4/2012	Methods and apparatus for disabling a memory-array portion
US8351238	1/8/2013	Low-complexity electronic circuits and methods of forming the same
US8358526	1/22/2013	Diagonal connection storage array
US8358525	1/22/2013	Low cost high density rectifier matrix memory
US8378456	2/19/2013	Unified switch array for memory devices
US8451024	5/28/2013	Bipolar-mos driver circuit
US8455298	6/4/2013	Method for forming self-aligned phase-change semiconductor diode memory
US8526217	9/3/2013	Low-complexity electronic circuit and methods of forming the same
US8537618	9/17/2013	Ram memory device with nand type interface
US8635426	1/21/2014	Diagonally accessed memory array circuit
US8766227	7/1/2014	Pinched center resistive change memory cell
US8773881	7/8/2014	Vertical switch three-dimensional memory array
US8786023	7/22/2014	Embedded non-volatile memory
US8934293	1/13/2015	Means and method for operating a resistive array
US8980532	3/17/2015	Solid state devices having fine pitch structures

US9007801	4/14/2015	Bipolar-MOS Memory Circuit
ZL01819463X	11/19/2008	Fabrication of Semiconductor Devices

PENDING PATENT APPLICATIONS

U.S. Application Serial No.	Filing Date	Title
13/200909	10/4/2011	Multiple sector parallel access memory array with error correction
14/282444	5/20/2014	Vertical switch three-dimensional memory array
14/283714	5/21/2014	Pinched center resistive change memory cell
14/306801	6/17/2014	Embedded non-volatile memory
13/385371	2/15/2012	Current steering element formation for memory arrays
14/628925	2/23/2015	Bipolar-MOS Memory Circuit
14/576909	12/19/2014	Operating a Resistive Array
14/561679	12/5/2014	Multiple Bit Per Cell Dual-Alloy GST Memory Elements
62/006957	6/3/2014	4F2 SCR Memory Device
62/014868	6/20/2014	Variable Selectivity Silicon Growth Process
62/022941	7/10/2014	NMOS Regulated Voltage Reference
62/026657	7/20/2014	Incremental Error Detection and Correction for Memories
62/041306	8/25/2014	3-D Planes Memory Device
62/086359	12/2/2014	Deposition Method for Planar Surfaces
62/108643		Method for Forming PCM and RRAM 3-D Memory Cells
14/616128	2/6/2015	Solid State Devices Having Fine Pitch Structures
14/635532	3/2/2014	Controlling Coupling in Large Cross-Point Memory Arrays

62/022289	7/9/2014	Self-Aligned Memory Cell Contact