PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

EPAS ID: PAT3586156

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
TESSERA RESEARCH LLC	09/08/2011

RECEIVING PARTY DATA

Name:	TESSERA, INC.
Street Address:	3025 ORCHARD PARKWAY
City:	SAN JOSE
State/Country:	CALIFORNIA
Postal Code:	95134

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	14501915

CORRESPONDENCE DATA

Fax Number: (908)654-7866

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: (908) 518-6394
Email: assignment@lernerdavid.com
Correspondent Name: LDLK&M
Address Line 1: 600 SOUTH AVENUE WEST
Address Line 4: WESTFIELD, NEW JERSEY 07090

ATTORNEY DOCKET NUMBER:	TESSERA 3.0-642 DIV (E)
NAME OF SUBMITTER:	MELINDA C. CORMIER
SIGNATURE:	/Melinda C. Cormier/
DATE SIGNED:	10/26/2015

Total Attachments: 5
source=TESSERA 3#page1.tif
source=TESSERA 3#page2.tif
source=TESSERA 3#page3.tif
source=TESSERA 3#page4.tif
source=TESSERA 3#page5.tif

PATENT ASSIGNMENT

For good and valuable consideration, the receipt of which is hereby acknowledged, Tessera Research LLC, a limited liability company of the state of Delaware, US, having a place of business at 3025 Orchard Parkway, San Jose, California 95134, US (hereinafter "ASSIGNOR"), hereby sells, transfers and assigns to Tessera, Inc., a corporation of the state of Delaware, having a place of business at 3025 Orchard Parkway, San Jose, California 95134, US (hereinafter "ASSIGNEE"), all of ASSIGNOR'S right, title and interest in and to (i) the patents and patent applications identified in Exhibit A attached hereto, and (ii) patents that may issue or reissue from any of the foregoing (together with all extensions, reexaminations and substitutions of any of the foregoing), (hereinafter, all such patents and patent applications, collectively, "ASSIGNED PATENTS"), to have and to hold the same, unto ASSIGNEE and/or its successors and assigns, including all damages for infringement of any of the ASSIGNED PATENTS and the sole right to sue therefore under such ASSIGNED PATENTS, for the full term or terms of all such ASSIGNED PATENTS, subject to all rights previously granted under the ASSIGNED PATENTS to third parties.

ASSIGNOR hereby declares that ASSIGNEE may take the steps for recordal of this assignment in the sole name of ASSIGNEE.

IN WITNESS WHEREOF, ASSIGNOR has caused this Patent Assignment to be duly signed on its behalf and ASSIGNEE has caused this Patent Assignment to be duly signed on its behalf.

This Assignment may be executed in any number of counterparts, each of which shall be deemed an original, but all of which together shall constitute one instrument.

[Signatures follow on Page 2]

SIGNED for and on behalf of Tessera Research LLC:

Signature: _____ Date: 9-8, 2011
Name: Michael Anthofer
Title: Executive Vice President and Chief Financial Officer

State of California)
) S.S.
County of Santa Clara)

On September 8, 2011, before me, Karen A. Rogers, personally appeared Michael Anthofer, who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the entity upon behalf of which he acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

Notary Signature _____ (Seal)

KAREN A. ROGERS
Commission # 1890143
Notary Public - California
Santa Clara County
My Comm. Expires May 18, 2014

SIGNED for and on behalf of Tessera, Inc.:

Signature: _____ Date: 9-8, 2011
Name: Michael Anthofer
Title: Executive Vice President and Chief Financial Officer

State of California)
) S.S.
County of Santa Clara)

On September 8, 2011, before me, Karen A Rogers, personally appeared Michael Anthofer, who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the entity upon behalf of which he acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

Notary Signature _____ (Seal)

KAREN A. ROGERS
Commission # 1890143
Notary Public - California
Santa Clara County
My Comm. Expires May 18, 2014

1485786_1.doc

EXHIBIT A - ASSIGNMENT FROM TESSERA RESEARCH LLC TO TESSERA, INC.				
Country	Application Number	Patent Number	Title	Filename
China P.R.	200980122523.0		WAFER LEVEL EDGE STACKING	TESRCH 3.4-590 China
China P.R.	201010546210.2		MICROELECTRONIC ELEMENTS HAVING METALLIC PADS OVERLYING VIAS	TESRCH 3.0-611 China
China P.R.	201020606709.3		MICROELECTRONIC ELEMENTS HAVING METALLIC PADS OVERLYING VIAS	TESRCH 3.0-611 China UM
China P.R.	201010546793.9		METHODS OF FORMING SEMICONDUCTOR ELEMENTS USING MICRO-ABRASIVE PARTICLE STREAM	TESRCH 3.0-613 China
China P.R.	201020606686.6		METHODS OF FORMING SEMICONDUCTOR ELEMENTS USING MICRO-ABRASIVE PARTICLE STREAM	TESRCH 3.0-613 China UM
European Patent Convention	09767074.9		WAFER LEVEL EDGE STACKING	TESRCH 3.4-590 EP
Japan	2011-514614		WAFER LEVEL EDGE STACKING	TESRCH 3.4-590 Japan
Patent Cooperation Treaty	PCT/US10/27135		MICROELECTRONIC ASSEMBLY WITH IMPEDANCE CONTROLLED WIREBOND AND REFERENCE\nWIREBOND	TESRCH 3.4-589 III
Patent Cooperation Treaty	PCT/US10/03213		MICROELECTRONIC ASSEMBLY WITH JOINED BOND ELEMENTS HAVING LOWERED INDUCTANCE	TESRCH 3.4-594 II
Patent Cooperation Treaty	PCT/US10/52783		MICROELECTRONIC ELEMENTS HAVING METALLIC PADS OVERLYING VIAS	TESRCH 3.4-611
Patent Cooperation Treaty	PCT/US10/52458		MICROELECTRONIC ELEMENTS WITH REAR CONTACTS CONNECTED WITH VIA FIRST OR VIA\nMIDDLE STRUCTURES	TESRCH 3.4-612
Patent Cooperation Treaty	PCT/US10/52785		METHODS OF FORMING SEMI-CONDUCTOR ELEMENTS USING MICRO-ABRASIVE PARTICLE STREAM	TESRCH 3.4-613
Patent Cooperation Treaty	PCT/US10/52633		NON-LITHOGRAPHIC FORMATION OF THREE-DIMENSIONAL CONDUCTIVE ELEMENTS	TESRCH 3.4-614
Patent Cooperation Treaty	PCT/US10/52462		ACTIVE CHIP ON CARRIER OR LAMINATED CHIP HAVING MICROELECTRONIC ELEMENT EMBEDDED\nTHEREIN	TESRCH 3.4-615
Patent Cooperation Treaty	PCT/US10/52792		MICROELECTRONIC ELEMENTS WITH POST-ASSEMBLY PLANARIZATION	TESRCH 3.4-616
Patent Cooperation Treaty	PCT/US11/29394		STACKED MICROELECTRONIC ASSEMBLY WITH TSVS FORMED IN STAGES AND CARRIER ABOVE CHIP	TESRCH 3.4-619
Patent Cooperation Treaty	PCT/US11/31391		ENHANCED STACKED MICROELECTRONIC ASSEMBLIES WITH CENTRAL CONTACTS	TESRCH 3.4-630
Patent Cooperation Treaty	PCT/US11/29568		STACKED MICROELECTRONIC ASSEMBLY WITH TSVS FORMED IN STAGES WITH PLURAL ACTIVE CHIPS	TESRCH 3.4-632
Patent Cooperation Treaty	PCT/US11/30871		SIMULTANEOUS WAFER BONDING AND INTERCONNECT JOINING	TESRCH 3.4-635
Patent Cooperation Treaty	PCT/US11/24143		PIN ATTACHMENT	TESRCH 3.4-643
Patent Cooperation Treaty	PCT/US10/27141		MICROELECTRONIC ASSEMBLY WITH IMPEDANCE CONTROLLED WIREBOND AND CONDUCTIVE\nREFERENCE ELEMENT	TESSERA 3.4-589 II
Patent Cooperation Treaty	PCT/US11/44026		HIGH DENSITY THREE-DIMENSIONAL INTEGRATED CAPACITORS	TESSERA 3.4-639 CIP
South Korea	10-2009-0089470	10-0950511	MICROELECTRONIC ASSEMBLY WITH IMPEDANCE CONTROLLED WIREBOND AND CONDUCTIVE REFERENCE ELEMENT	TESRCH 3.0-589 II Korea
South Korea	10-2009-0089471	10-0935854	MICROELECTRONIC ASSEMBLY WITH IMPEDANCE CONTROLLED WIREBOND AND REFERENCE	TESRCH 3.0-589 III Korea
South Korea	10-2010-7028161		WAFER LEVEL EDGE STACKING	TESRCH 3.4-590 Korea
South Korea	10-2010-0040446	10-1003393	MICROELECTRONIC ASSEMBLY WITH JOINED BOND ELEMENTS HAVING LOWERED INDUCTANCE	TESRCH 3.0-594 II Korea
South Korea	10-2010-0104904	10-1061867	MICROELECTRONIC ELEMENTS HAVING METALLIC PADS OVERLYING VIAS	TESRCH 3.0-611 Korea
South Korea	10-2011-0015195		MICROELECTRONIC ELEMENTS HAVING METALLIC PADS OVERLYING VIAS	TESRCH 3.0-611 Korea DIV
South Korea	10-2011-0051406		MICROELECTRONIC ELEMENTS HAVING METALLIC PADS OVERLYING VIAS	TESRCH 3.0-611 Korea DIV II
South Korea	10-2010-0104905		METHODS OF FORMING SEMICONDUCTOR ELEMENTS USING MICRO-ABRASIVE PARTICLE STREAM	TESRCH 3.0-613 Korea
South Korea	10-2011-0024801		METHODS OF FORMING SEMICONDUCTOR ELEMENTS USING MICRO-ABRASIVE PARTICLE STREAM	TESRCH 3.0-613 Korea DIV I
South Korea	10-2011-0024802		METHODS OF FORMING SEMICONDUCTOR ELEMENTS USING MICRO-ABRASIVE PARTICLE STREAM	TESRCH 3.0-613 Korea DIV II
South Korea	10-2011-0027368		STACKED MICROELECTRONIC ASSEMBLY WITH TSVS FORMED IN STAGES AND CARRIER ABOVE CHIP	TESRCH 3.0-619 Korea
South Korea	10-2011-0069006		STACKED MICROELECTRONIC ASSEMBLY WITH TSVS FORMED IN STAGES AND CARRIER ABOVE CHIP	TESRCH 3.0-619 KR DIV
South Korea	10-2010-0113272	10-1059490	CONDUCTIVE PADS DEFINED BY EMBEDDED TRACES	TESRCH 3.0-621 Korea
South Korea	10-2010-0113271		MICROELECTRIC PACKAGE WITH TERMINALS ON DIELETRIC MASS	TESRCH 3.0-622 Korea
South Korea	10-2011-0020819		MICROELECTRIC PACKAGE WITH TERMINALS ON DIELETRIC MASS	TESRCH 3.0-622 Korea DIV

Country	Application Number	Patent Number	Title	Filename
South Korea	10-2010-0129888	10-1061531	ENHANCED STACKED MICROELECTRONIC ASSEMBLIES WITH CENTRAL CONTACTS AND IMPROVED GROUND OR POWER DISTRIBUTION	TESRCH 3.0-623 Korea
South Korea	10-2011-0035798		ENHANCED STACKED MICROELECTRONIC ASSEMBLIES WITH CENTRAL CONTACTS AND IMPROVED GROUN OR POWER DISTRIBUTION	TESRCH 3.0-623 Korea DIV I
South Korea	10-2011-0035799		ENHANCED STACKED MICROELECTRONIC ASSEMBLIES WITH CENTRAL CONTACTS AND IMPROVED GROUN OR POWER DISTRIBUTION	TESRCH 3.0-623 Korea DIV II
South Korea	10-2010-0129890		ENHANCED STACKED MICROELECTRONIC ASSEMBLIES WITH CENTAL CONTACTS	TESRCH 3.0-630 Korea
South Korea	10-2011-0024339		ENHANCED STACKED MICROELECTRONIC ASSEMBLIES WITH CENTAL CONTACTS	TESRCH 3.0-630 Korea DIV
South Korea	10-2011-0027369		STACKED MICROELECTORNIC ASSEMBLY WITH TSVS FORMED IN STAGES WITH PLURAL ACTIVE CHIPS	TESRCH 3.0-632 Korea
South Korea	10-2011-0069932		STACKED MICROELECTORNIC ASSEMBLY WITH TSVS FORMED IN STAGES WITH PLURAL ACTIVE CHIPS	TESRCH 3.0-632 KR DIV
South Korea	10-2011-0032044		SIMULTANEOUS WAFER BONDING AND INTERCONNECT JOINING	TESRCH 3.0-635 Korea
South Korea	10-2011-0061826		SIMULTANEOUS WAFER BONDING AND INTERCONNECT JOINING	TESRCH 3.0-635 KR DIV
South Korea	10-2011-0041843		PACKAGE-ON-PACKAGE ASSEMBLY WITH WIRE BONDS TO ENCAPULATION SURFACE	TESRCH 3.0-647 Korea
South Korea	10-2011-0026686		HIGH DENSITY THREE-DIMENSIONAL INTEGRATED CAPACITORS	TESSERA 3.0-639 KR
Taiwan	099107377		MICROELECTRONIC ASSEMBLY WITH IMPEDANCE CONTROLLED WIREBOND AND CONDUCTIVE REFERENCE ELEMENT	TESRCH 3.0-589 II Taiwan
Taiwan	099107375		MICROELECTRONIC ASSEMBLY WITH IMPEDANCE CONTROLLED WIREBOND AND REFERENCE WIREBOND	TESRCH 3.0-589 III Taiwan
Taiwan	098120145		WAFER LEVEL EDGE STACKING	TESRCH 3.0-590 Taiwan
Taiwan	099145382		MICROELECTRONIC ASSEMBLY WITH JOINED BOND ELEMENTS HAVING LOWERED INDUCTANCE	TESRCH 3.0-594 II Taiwan
Taiwan	099143374		MICROELECTRONIC ELEMENTS HAVING METALLIC PADS OVERLYING VIAS	TESRCH 3.0-611 Taiwan
Taiwan	099140226		MICROELECTRONIC ELEMENTS WITH REAR CONTACTS CONNECTED WITH VIA FIRST OR VIA MIDDLE STRUCTURES	TESRCH 3.0-612 Taiwan
Taiwan	099143358		METHODS OF FORMING SEMICONDUCTOR ELEMENTS USING MICRO-ABRASIVE PARTICLE STREAM	TESRCH 3.0-613 Taiwan
Taiwan	099140225		NON-LITHOGRAPHIC FORMATION OF THREE-DIMENSIONAL CONDUCTIVE ELEMENTS	TESRCH 3.0-614 Taiwan
Taiwan	099140224		ACTIVE CHIP ON CARRIER OR LAMINATED CHIP HAVING MICROELECTRONIC ELEMENT EMBEDDED THEREIN	TESRCH 3.0-615 Taiwan
Taiwan	099140235		MICROELECTRONIC ELEMENTS WITH POST-ASSEMBLY PLANARIZATION	TESRCH 3.0-616 Taiwan
Taiwan	100113585		CONDUCTIVE PADS DEFINED BY EMBEDDED TRACES	TESRCH 3.0-621 Taiwan
Taiwan	100125521		STACKABLE MOLDED MICROELECTRONIC PACKAGES	TESSERA 3.0-607 TW
Taiwan	100125522		STACKABLE MOLDED MICROELECTRONIC PACKAGES WITH AREA ARRAY UNIT CONNECTORS	TESSERA 3.0-608 TW
United States	61/210,063		IMPEDANCE CONTROLLED WIREBOND	TESRCH 3.8-589 I
United States	12/722,784	7,923,851	MICROELECTRONIC ASSEMBLY IWTH IMPEDANCE CONTROLLED WIREBOND AND CONDUCTIVE REFERENCE ELEMENT	TESRCH 3.0-589 II
United States	12/986,601		MICROELECTRONIC ASSEMBLY WITH IMPEDANCE CONTROLLED WIREBOND AND CONDUCTIVE REFERENCE ELEMENT	TESRCH 3.0-589 II DIV I
United States	12/986,556		MICROELECTRONIC ASSEMBLY WITH IMPEDANCE CONTROLLED WIREBOND AND CONDUCTIVE REFERENCE ELEMENT	TESRCH 3.0-589 II DIV II
United States	12/722,799		MICROELECTRONIC ASSEMBLY WITH IMPEDANCE CONTROLLED WIREBOND AND REFERENCED WIREBOND	TESRCH 3.0-589 III
United States	12/456,349		WAFER LEVEL EDGE STACKING	TESRCH 3.0-590
United States	61/268,488		CURABLE RESINS AND ARTICLES MADE THEREFROM	TESRCH 3.8-591
United States	61/229,654		3D INTERCONNECTS FOR HIGH DENSITY DIE STACK PACKAGES	TESRCH 3.8-593
United States	12/644,476		MICROELECTRONIC ASSEMBLY WITH BOND ELEMENTS HAVING LOWERED INDUCTANCE	TESRCH 3.0-594
United States	12/793,824	8,008,785	MICROELECTRONIC ASSEMBLY WITH JOINED BOND ELEMENTS HAVING LOWERED INDUCTANCE	TESRCH 3.0-594 II
United States	13/196,192		MICROELECTRONIC ASSEMBLY WITH JOINED BOND ELEMENTS HAVING LOWERED INDUCTANCE	TESRCH 3.0-594 II CON
United States	61/322,404		MICROELECTRONIC ASSEMBLY WITH JOINED BOND ELEMENTS HAVING LOWERED INDUCTANCE	TESRCH 3.8-594 II
United States	12/883,556		TSOP WITH IMPEDANCE CONTROL	TESRCH 3.0-606
United States	12/844,463		MICROELECTRONIC PACKAGES WITH NANOPARTICLE JOINING	TESRCH 3.0-610
United States	12/842,717		MICROELECTRONIC ELEMENTS HAVING METALLIC PADS OVERLYING VIAS	TESRCH 3.0-611

Country	Application Number	Patent Number	Title	Filename
United States	12/842,651		MICROELECTRONIC ELEMENTS WITH REAR CONTACTS CONNECTED WITH VIA FIRST OR VIA MIDDLE STRUCTURES	TESRCH 3.0-612
United States	12/842,612		METHODS OF FORMING SEMICONDUCTOR ELEMENTS USING MICRO-ABRASIVE PARTICLE STREAM	TESRCH 3.0-613
United States	12/842,669		NON-LITHOGRAPHIC FORMATION OF THREE-DIMENSIONAL CONDUCTIVE ELEMENTS	TESRCH 3.0-614
United States	12/842,692		ACTIVE CHIP ON CARRIER OR LAMINATED CHIP HAVING MICROELECTRONIC ELEMENT EMBEDDED THEREIN	TESRCH 3.0-615
United States	12/842,587		MICROELECTRONIC ELEMENTS WITH POST-ASSEMBLY PLANARIZATION	TESRCH 3.0-616
United States	12/883,421		CHIP ASSEMBLY HAVING VIA INTERCONNECTS JOINED BY PLATING	TESRCH 3.0-617
United States	12/884,649		STAGED VIA FORMATION FROM BOTH SIDES OF CHIP	TESRCH 3.0-618
United States	61/419,033		STACKED MICROELECTRONIC ASSEMBY WITH TSVS FORMED IN STAGES AND CARRIER ABOVE CHIP	TESRCH 3.8-619
United States	13/051,424		STACKED MICROELECTRONIC ASSEMBLY WITH TSVS FORMED IN STAGES AND CARRIER ABOVE CHIP	TESRCH 3.0-619
United States	12/884,695		MULTI-FUNCTION AND SHIELDED 3D INTERCONNECTS	TESRCH 3.0-620
United States	12/963,938		CONDUCTIVE PADS DEFINED BY EMBEDDED TRACES	TESRCH 3.0-621
United States	12/883,821		IMPEDANCE CONTROLLED PACKAGES WITH METAL SHEET OR 2-LAYER RDL	TESRCH 3.0-625
United States	12/883,811		METAL CAN IMPEDANCE CONTROL STRUCTURE	TESRCH 3.0-626
United States	12/938,068		NO FLOW UNDERFILL	TESRCH 3.0-627
United States	12/883,431		STACKED CHIP ASSEMBLY HAVING VERTICAL VIAS	TESRCH 3.0-628
United States	12/907,522		ENHANCED STACKED MICROELECTRONIC ASSEMBLIES WITH CENTRAL CONTACTS AND IMPROVED THERMAL CHARACTERISTICS	TESRCH 3.0-629
United States	13/080,876		ENHANCED STACKED MICROELECTRONIC ASSEMBLIES WITH CENTRAL CONTACTS	TESRCH 3.0-630
United States	12/953,994		ENHANCED STACKED MICROELECTRONIC ASSEMBLIES WITH CENTRAL CONTACTS WITH VIAS CONNECTED TO THE CENTRAL CONTACTS	TESRCH 3.0-631
United States	61/419,037		STACKED MICROELECTRONIC ASSEMBY WITH TSVS FORMED IN STAGES WITH PLURAL ACTIVE CHIPS	TESRCH 3.8-632
United States	13/051,414		STACKED MICROELECTRONIC ASSEMBLY WITH TSVS FORMED IN STAGES WITH PLURAL ACTIVE CHIPS	TESRCH 3.0-632
United States	12/958,866		STACKED MICROELECTRONIC ASSEMBLY HAVING INTERPOSER CONNECTING ACTIVE CHIPS	TESRCH 3.0-633
United States	61/424,906		SIMULTANEOUS WAFER BONDING AND INTERCONNECT JOINING	TESRCH 3.8-635
United States	13/076,969		SIMULTANEOUS WAFER BONDING AND INTERCONNECT JOINING	TESRCH 3.0-635
United States	12/962,806		COMPLIANT INTERCONNECTS IN WAFERS	TESRCH 3.0-636
United States	12/965,192		INTERCONNECT STRUCTURE	TESRCH 3.0-642
United States	12/966,225		PIN ATTACHMENT	TESRCH 3.0-643
United States	61/416,779		LEAD STRUCTURES WITH VERTICAL OFFSETS	TESRCH 3.8-644
United States	13/092,495		VIAS IN POROUS SUBSTRATES	TESRCH 3.0-650
United States	13/091,800		INTERPOSER HAVING MOLDED LOW CTE DIELECTRIC	TESRCH 3.0-655
United States	61/477,820		STACKED CHIP-ON-BOARD MODULE WITH EDGE CONNECTOR	TESRCH 3.8-656
United States	12/839,038		STACKABLE MOLDED MICROELECTRONIC PACKAGES WITH AREA ARRAY UNIT CONNECTORS	TESSERA 3.0-608
United States	12/964,049		HIGH DENSITY THREE-DIMENSIONAL INTEGRATED CAPACITORS	TESSERA 3.0-639
United States	13/092,376		MULTI-CHIP MODULE WITH STACKED FACE-DOWN CONNECTED DIES	TESSERA 3.0-651
1485720				