PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
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EPAS ID: PAT3590943

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
JEFFERIES FINANCE LLC	10/28/2015

RECEIVING PARTY DATA

Name:	LATTICE SEMICONDUCTOR CORPORATION
Street Address:	111 SW 5TH AVENUE
Internal Address:	7TH FLOOR
City:	PORTLAND
State/Country:	OREGON
Postal Code:	97204

PROPERTY NUMBERS Total: 34

Property Type	Number
Patent Number:	5969552
Patent Number:	6219747
Patent Number:	6326826
Patent Number:	6385692
Patent Number:	6393505
Patent Number:	7231009
Patent Number:	7257129
Patent Number:	7340558
Patent Number:	7639561
Patent Number:	7777652
Patent Number:	7831778
Patent Number:	7849339
Patent Number:	7903684
Patent Number:	7908501
Patent Number:	7949863
Patent Number:	8001334
Patent Number:	8036248
Patent Number:	8160192
Patent Number:	8386867

Property Type	Number
Patent Number:	8510487
Patent Number:	8543873
Patent Number:	8667354
Patent Number:	8751709
Patent Number:	8760188
Patent Number:	8839058
Patent Number:	8924805
Patent Number:	6976201
Patent Number:	7039121
Patent Number:	7113507
Patent Number:	7154905
Patent Number:	7746798
Patent Number:	6771192
Patent Number:	7978099
Application Number:	14300166

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

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NAME OF SUBMITTER:	MICHAEL GARRABRANTS
SIGNATURE:	/michael s. garrabrants/
DATE SIGNED:	10/28/2015

Total Attachments: 5
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RELEASE OF A SECURITY INTEREST -- PATENTS

October 28, 2015

WHEREAS, pursuant to that certain Grant of Security Interest in United States Patents, dated as of March 10, 2015, recorded in the United States Patent and Trademark Office at Reel 035220, Frame 0226, LATTICE SEMICONDUCTOR CORPORATION, a Delaware corporation (the "Releasee"), inter alia, granted to JEFFERIES FINANCE LLC, as Administrative Agent for the ratable benefit of the Secured Creditors ("Releasor"), a continuing security interest in all right, title and interest of the Releasee in, to and under United States Patents listed on the attached Schedule A (the "Patents"), and all Proceeds in respect thereof (with all of the Releasee's rights listed above being collectively referred to as the "Collateral") to secure the payment, performance and observance of the Obligations; and

WHEREAS, the Releasee has requested and Releasor has agreed to provide a document suitable for recording in the United States Patent and Trademark Office evidencing and effecting the release, relinquishment and discharge of its security interest in the Collateral.

NOW, THEREFORE, in consideration of and in exchange for good and valuable consideration, Releasor hereby agrees as follows:

1. Defined Terms. All capitalized terms used but not otherwise defined herein have the meanings given to them in the Grant of Security Interest in United States Patents.

2. Release of Security Interest. Releasor hereby, without any representation and warranty and without any recourse to Releasor, releases, relinquishes and discharges all of its security interest in the Collateral.

[Signature Page Follows]

IN WITNESS WHEREOF, the undersigned has executed and delivered this Release as of the date first written above.

JEFFERIES FINANCE LLC,
as Administrative Agent

By: _____
Name: J. Paul McDonnell
Title: Managing Director

SCHEDULE A

App. No.	Patent No.	Jurisdiction	Title	Status	Record Owner
09/007,707	5969552	United States	Dual loop delay-locked loop	Issued	Lattice Semiconductor Corporation
09/226,776	6219747	United States	Methods and apparatus for variable length sd-ram transfers	Issued	Lattice Semiconductor Corporation
9/805,588	6385692	United States	Methods and apparatus for variable length sd-ram transfers	Issued	Lattice Semiconductor Corporation
09/227,502	6393505	United States	Methods and apparatus for data bus arbitration	Issued	Lattice Semiconductor Corporation
10/045,600	6771192	United States	Method and system for dc-balancing at the physical layer	Issued	Lattice Semiconductor Corporation
10/036,794	6976201	United States	Method and system for host handling of communications errors	Issued	Lattice Semiconductor Corporation
10/045,393	7039121	United States	Method and system for transition-controlled selective block inversion communications	Issued	Lattice Semiconductor Corporation
10/053,461	7113507	United States	Method and system for communicating control information via out-of-band symbols	Issued	Lattice Semiconductor Corporation
10/035,911	7154905	United States	Method and system for nesting of communications packets	Issued	Lattice Semiconductor Corporation
10/371,220	7231009	United States	Data synchronization across an asynchronous boundary using, for example, multi-phase clocks	Issued	Lattice Semiconductor Corporation

10/045,297	7257129	United States	Memory architecture with multiple serial communications ports	Issued	Lattice Semiconductor Corporation
10/045,601	7340558	United States	Multi-section memory bank system	Issued	Lattice Semiconductor Corporation
11/697,813	7639561	United States	Multi-port memory device having variable port speeds	Issued	Lattice Semiconductor Corporation
10/045,625	7746798	United States	Method and system for integrating packet type information with synchronization symbols	Issued	Lattice Semiconductor Corporation
12/260,972	7777652	United States	Coding system for memory systems employing high-speed serial links	Issued	Lattice Semiconductor Corporation
11/690,629	7831778	United States	Shared nonvolatile memory architecture	Issued	Lattice Semiconductor Corporation
11/690,659	7849339	United States	Power-saving clocking technique	Issued	Lattice Semiconductor Corporation
11/828,286	7903684	United States	Communications architecture for transmission of data between memory bank caches and ports	Issued	Lattice Semiconductor Corporation
11/690,642	7908501	United States	Progressive power control of a multi-port memory device	Issued	Lattice Semiconductor Corporation
11/694,819	7949863	United States	Inter-port communication in a multi-port memory device	Issued	Lattice Semiconductor Corporation
12/847,416	7978099	United States	17b/20b coding system	Issued	Lattice Semiconductor Corporation
11/952,052	8001334	United States	Bank sharing and refresh in a shared multi-port memory device	Issued	Lattice Semiconductor Corporation
12/260,970	8036248	United States	Method, apparatus, and system for automatic data aligner for multiple serial	Issued	Lattice Semiconductor Corporation

			receivers		
11/861,175	8160192	United States	Signal interleaving for serial clock and data recovery	Issued	Lattice Semiconductor Corporation
12/497,391	8386867	United States	Computer memory test structure	Issued	Lattice Semiconductor Corporation
12/704,417	8510487	United States	Hybrid interface for serial and parallel communication	Issued	Lattice Semiconductor Corporation
12/683,365	8543873	United States	Multi-Site testing of computer memory devices and Serial IO Port	Issued	Lattice Semiconductor Corporation
13/776,508	8667354	United States	Computer memory test structure	Issued	Lattice Semiconductor Corporation
13/934,147	8751709	United States	Hybrid interface for serial and parallel communication	Issued	Lattice Semiconductor Corporation
13/174,616	8760188	United States	Configurable multi-dimensional driver and receiver	Issued	Lattice Semiconductor Corporation
14/035,795	8839058	United States	Multi-Site testing of computer memory devices and Serial IO Port	Issued	Lattice Semiconductor Corporation
14/145,751	8924805	United States	Computer memory test structure	Issued	Lattice Semiconductor Corporation
[redacted]					
09/574571	6326826	United States	Wide frequency range delay-locked loop circuit	Issued	Lattice Semiconductor Corporation
14/300,166		United States	Configurable multi-dimensional driver and receiver	Pending	Lattice Semiconductor Corporation