PATENT ASSIGNMENT COVER SHEET

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE OF SECURITY INTEREST

CONVEYING PARTY DATA

Name	Execution Date
COMERICA BANK	12/11/2015

RECEIVING PARTY DATA

Name:	GCT SEMICONDUCTOR, INC.
Street Address:	2121 RINGWOOD AVENUE
City:	SAN JOSE
State/Country:	CALIFORNIA
Postal Code:	95131

PROPERTY NUMBERS Total: 51

Property Type	Number
Patent Number:	8243579
Patent Number:	8229028
Patent Number:	8018990
Patent Number:	7995645
Patent Number:	7953192
Patent Number:	7952442
Patent Number:	7952435
Patent Number:	7949324
Patent Number:	7945208
Patent Number:	7812672
Patent Number:	7768097
Patent Number:	7606293
Patent Number:	7560960
Patent Number:	7535977
Patent Number:	7515662
Patent Number:	7512390
Patent Number:	7436265
Patent Number:	7202741
Patent Number:	7190236
Patent Number:	7071535

Property Type	Number
Patent Number:	7035351
Patent Number:	7003265
Patent Number:	7002410
Patent Number:	6963620
Patent Number:	6952125
Patent Number:	6876266
Patent Number:	6850748
Patent Number:	6781424
Patent Number:	6756828
Patent Number:	6754478
Patent Number:	6704383
Patent Number:	6657498
Patent Number:	6553089
Patent Number:	6538498
Patent Number:	6512408
Patent Number:	6510185
Patent Number:	6498927
Patent Number:	6483355
Patent Number:	6424222
Patent Number:	6424192
Patent Number:	6404277
Patent Number:	6335952
Patent Number:	6313688
Patent Number:	6194947
Patent Number:	7831215
Patent Number:	7925217
Application Number:	11878937
Application Number:	11878938
Application Number:	11878939
Application Number:	11976910
Application Number:	13272779

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SIGNATURE:	/Philip Nulud/
DATE SIGNED:	12/17/2015

Total Attachments: 4
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RELEASE AND REASSIGNMENT OF PATENTS AND PATENT APPLICATIONS

December 11, 2015

Reference is hereby made to that certain Intellectual Property Security Agreement (the "Agreement"), dated as of March 13, 2013, executed by GCT Semiconductor, Inc., a Delaware corporation ("Grantor"), whose address is 2121 Ringwood Avenue, San Jose, California 95131, in favor of Comerica Bank ("Secured Party"), whose address is 39200 Six Mile Road, Mail Code 7578, Livonia, Michigan 48152, which was recorded in the United States Patent and Trademark Office on March 29, 2013, at Reel 030112 Frame 0447, and pursuant to which the Grantor assigned and granted to Secured Party, a security interest in and to all of Grantor's right, title and interest in and to certain patents, including those patents specifically listed on Schedule 1 attached hereto (the "Patents"); and

WHEREAS, Secured Party wishes to terminate the Agreement and release, retransfer and reassign to Grantor, without representation or warranty, all of Secured Party's right, title and interest in and to the Patents.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, Secured Party hereby terminates the Agreement and releases, retransfers and reassigns to Grantor, without representation or warranty, all of Secured Party's right, title and interest in and to the Patents.

IN WITNESS WHEREOF, Secured Party has executed this Release and Reassignment of Patents and Patent Applications as of the date first above written.

COMERICA BANK
("Secured Party")

By: _____
Name: MELANIE DURANO
Title: FIRST VICE PRESIDENT

Schedule 1
Patents

Description	Publication No./ Application No.	Publication Date/ Application File Date
OFDM receiving circuit having multiple demodulation paths using oversampling analog-to-digital converter	8243579	8/14/2012
Apparatus for measuring IQ imbalance	8229028	7/24/2012
Apparatus for measuring in-phase and quadrature (IQ) imbalance	8018990	9/13/2011
Apparatus for measuring in-phase and quadrature (IQ) imbalance	7995645	8/9/2011
Receiver with fast gain control and digital signal processing unit with transient signal compensation	7953192	5/31/2011
Integrated circuit package having inductance loop formed from same-pin-to-same-bonding-pad structure	7952442	05/31/2011
Phase locked loop and method for compensating temperature thereof	7952435	5/31/2011
Method for compensating transmission carrier leakage and transceiving circuit embodying the same	7949324	5/24/2011
Radio frequency integrated circuit	7945208	5/17/2011
Low noise amplifier having improved linearity	7812672	10/12/2010
Integrated circuit package having an inductance loop formed from a multi-loop configuration	7768097	8/3/2010
Bidirectional turbo ISI canceller-based DSSS receiver for high-speed wireless LAN	7606293	10/20/2009
Frequency synthesizer using two phase locked loops	7560960	7/14/2009
Sigma-delta based phase lock loop	7535977	5/19/2009
Method for compensating for gain ripple and group delay characteristics of filter and receiving circuit embodying the same	7515662	4/7/2009
System and method for tuning a frequency generator using an LC oscillator	7512390	3/31/2009
Clock generator and clock generating method using delay locked loop	7436265	10/14/2008
Highly linear variable gain amplifier	7202741	4/10/2007
Apparatus and method of oscillating wideband frequency	7190236	3/13/2007
Integrated circuit package having inductance loop formed from a bridge interconnect	7071535	7/4/2006

Description	Publication No./ Application No.	Publication Date/ Application File Date
Automatic gain control loop apparatus	7035351	4/25/2006
System and method for filtering signals in a transceiver	7003265	2/21/2006
Adaptive linearization technique for communication building block	7002410	2/21/2006
Communication transmitter using offset phase-locked-loop	6963620	11/8/2005
System and method for suppressing noise in a phase-locked loop circuit	6952125	10/4/2005
LC oscillator with wide tuning range and low phase noise	6876266	4/5/2005
RF front end with reduced carrier leakage	6850748	2/1/2005
Single chip CMOS transmitter/receiver and method of using same	6781424	8/24/2004
Phase lock loop (PLL) apparatus and method	6756828	6/29/2004
CMOS low noise amplifier	6754478	6/22/2004
Sample and hold type fractional-N frequency synthesizer	6704383	3/9/2004
Variable gain low-noise amplifier for a wireless terminal	6657498	12/2/2003
Fractional-N frequency synthesizer with fractional compensation method	6553089	4/22/2003
Gm-C tuning circuit with filter configuration	6538498	3/25/2003
Mixer structure and method for using same	6512408	1/28/2003
Single chip CMOS transmitter/receiver	6510185	1/21/2003
Automatic gain control method for highly integrated communication receiver	6498927	12/24/2002
Single chip CMOS transmitter/receiver and method of using same	6483355	11/19/2002
Variable gain low noise amplifier for a wireless terminal	6424222	7/23/2002
Phase lock loop (PLL) apparatus and method	6424192	7/23/2002
Gm-C tuning circuit with filter configuration	6404277	6/11/2002
Single chip CMOS transmitter/receiver	6335952	1/1/2002

Description	Publication No./ Application No.	Publication Date/ Application File Date
Mixer structure and method of using same	6313688	11/6/2001
VCO-mixer structure	6194947	2/27/2001
Tranceiver circuit for compensating IQ mismatch and carrier leakage and method for controlling the same	7831215	11/9/2010
Receiving circuit and method for compensating IQ mismatch	7925217	4/12/2011
Method for performing handoff from WIBRO (WIMAX) service to wireless LAN service and terminal apparatus using the same title	11878937	7/27/2007
Method and system for transmitting voice data by using wireless LAN and Bluetooth	11878938	7/27/2007
Method and system for transmitting voice data by using wireless LAN and Bluetooth	11878939	7/27/2007
OFDM receiving circuit having multiple demodulation paths	11976910	10/29/2007
Receiver for estimating and compensating for in-phase/quadrature mismatch	13272779	10/13/2011