PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1 Stylesheet Version v1.2 EPAS ID: PAT3727486

SUBMISSION TYPE:	NEW ASSIGNMENT		
NATURE OF CONVEYANCE:	ASSIGNMENT		

CONVEYING PARTY DATA

Name	Execution Date
DAVID R. CHERITON	01/25/2016

RECEIVING PARTY DATA

Name:	INTEL CORPORATION
Street Address:	2200 MISSION COLLEGE BOULEVARD
City:	SANTA CLARA
State/Country:	CALIFORNIA
Postal Code:	95054

PROPERTY NUMBERS Total: 40

Property Type	Number
Patent Number:	8407428
Patent Number:	8504791
Application Number:	12842958
Application Number:	61273179
Patent Number:	7650460
Application Number:	60897773
Patent Number:	8065476
Patent Number:	8230168
Patent Number:	8612673
Patent Number:	8938580
Application Number:	14569007
Patent Number:	9047334
Application Number:	61273178
Application Number:	14697938
Patent Number:	8838656
Application Number:	61273177
Application Number:	14457046
Application Number:	14997104
Application Number:	12890471
Application Number:	61279380
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PATENT REEL: 037668 FRAME: 0654

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Property Type	Number
Patent Number:	8370458
Application Number:	61008657
Application Number:	61281417
Application Number:	13541396
Application Number:	61504669
Patent Number:	9208082
Application Number:	61615103
Application Number:	14880248
Application Number:	13829527
Application Number:	61615102
Patent Number:	8316276
Application Number:	14058919
Application Number:	61738887
Application Number:	14178038
Application Number:	61775041
Application Number:	14479676
Application Number:	61876115
Application Number:	14596113
Application Number:	61927914
Application Number:	14178130

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ATTORNEY DOCKET NUMBER:	HICAMP
NAME OF SUBMITTER:	ANGELA MILLER
SIGNATURE:	/Angela Miller/
DATE SIGNED:	02/04/2016

Total Attachments: 7

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Patent Assignment

David R. Cheriton, an individual with an address of 131 Cowper St., Palo Alto, CA 94301, ("<u>Assignor</u>") is the sole owner of the patents and patent applications listed in <u>Schedule A</u> hereto (collectively the "<u>Patents</u>"); and

Intel Corporation, a Delaware Corporation, with an office at 2200 Mission College Boulevard, Santa Clara, California, 95054, ("Buyer") desires to acquire all right, title and interest in the Patents and the related rights described below.

For good and valuable consideration, the receipt of which is hereby acknowledged, Assignor does hereby sell, assign, transfer and convey to Buyer and its successors and assigns all right, title and interest that may exist today and in the future to any and all:

- (1) Patents;
- (2) patents and patent applications to which any of the patents or patent applications listed in <u>Schedule A</u> directly or indirectly claims, or forms the basis for, priority anywhere in the world;
- (3) reissues, reexaminations, extensions, continuations, continuations-in-part, continuing prosecution applications and divisions of any of the items listed in (1) or (2) of this Assignment;
- (4) foreign counterparts to any of the items listed in (1), (2) or (3) of this Assignment, including utility models, inventors' certificates, industrial design protection and any other form of governmental grants or issuances for the protection of inventions, designs or discoveries;
- inventions, invention disclosures, designs and discoveries described in the items listed in (1) through (4) of this Assignment;
- (6) patents that issue from any of the items listed in (1) through (5) of this Assignment;
- claims, causes of action and enforcement rights of any kind, whether currently pending, filed or otherwise, and whether known or unknown, under or arising from any of the items listed in (1) through (6) of this Assignment, including all rights to pursue and collect damages, costs, injunctive relief and other remedies for past, current or future infringement of the Patents and including rights afforded under 35 U.S.C. § 154(d);
- (8) royalties, income and other payments due as of the date hereof or hereafter under or arising from any of the items listed in (1) through (7) of this Assignment; and
- (9) rights to apply for, file, register, maintain, extend and renew in any or all countries of the world patents, certificates of invention, utility models, industrial design protection, design patent protection and other governmental grants or issuances of

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any kind related to any of the items listed in (1) through (9) of this Assignment.

Assignor shall execute and deliver any instruments, and do and perform any other acts and things as may be reasonably necessary or desirable for effecting and evidencing the assignments contemplated hereby, including the execution, acknowledgment and recordation of any instruments.

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks and any other patent office to issue any and all patents, utility models or other governmental grants or issuances pertaining to any of the items assigned hereunder in the name of Buyer.

This Assignment will inure to the benefit of Buyer and its successors, assigns and other legal representatives and is binding upon Assignor and its successors, assigns, heirs and legal representatives.

Assignor, by its duly authorized representative, has executed this Assignment on the date set forth below.

DATE: <u>//// (24 //</u>), 2016

By: David R. Cheriton

Signature

STATE OF CALIFORNIA COUNTY OF SAN MATEO

On Amulum 25 2016, before me, Vertica the Month of Notary Public, personally appeared and Notary Who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument the person executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal. (Seal)

VERONICA T. PULA
Commission # 1965828
Notary Public - California #
Santa Clara County
My Comm. Expires Feb 3, 2016

Signature

Print Name

evonica

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ACCEPTED:	
DATE: <u>31</u> ,20 <u>16</u>	Intel Corporation By: Tiffany Silva Title: Assistant Secretary
	7.100. 7.100.000.000.000.000.000.000.000.000.00

Case Number	Application No.	Filing Date	Patent Number	Issue Date	Title
CHERP001	12/784,268	5/20/2010	8,407,428	3/26/2013	Title: STRUCTURED MEMORY COPROCESSOR
CHERP001C1	13/629,183	9/27/2012	8,504,791	8/6/2013	Title: HIERARCHICAL IMMUTABLE CONTENT- ADDRESSABLE MEMORY COPROCESSOR
CHERP002	12/842,958	7/23/2010	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		Title: ITERATOR REGISTER FOR STRUCTURED MEMORY
CHERP002+	61/273,179	7/31/2009			Title: ITERATOR REGISTER FOR EFFICIENT STRUCTURED MEMORY ACCESS
CHERP003	12/011,311	1/25/2008	7,650,460	1/19/2010	Title: HIERARCHICAL IMMUTABLE CONTENT- ADDRESSABLE MEMORY PROCESSOR
CHERP003+	60/897,773	1/26/2007			Title: HIERARCHICAL IMMUTABLE CONTENT- ADDRESSABLE MEMORY PROCESSOR
CHERP003C1	12/653,889	12/17/2009	8,065,476	11/22/2011	Title: HIERARCHICAL IMMUTABLE CONTENT- ADDRESSABLE MEMORY PROCESSOR
CHERP003C2	13/271,137	10/11/2011	8,230,168	7/24/2012	Title: HIERARCHICAL IMMUTABLE CONTENT- ADDRESSABLE MEMORY PROCESSOR
CHERP003C3	13/533,125	6/26/2012	8,612,673	12/17/2013	Title: HIERARCHICAL IMMUTABLE CONTENT- ADDRESSABLE MEMORY PROCESSOR
CHERP003C4	14/062,301	10/24/2013	8,938,580	1/20/2015	Title: HIERARCHICAL IMMUTABLE CONTENT- ADDRESSABLE MEMORY PROCESSOR
CHERP003C5	14/569,007	12/12/2014		4, 10, 10, 10, 10, 10, 10, 10, 10, 10, 10	Title: HIERARCHICAL IMMUTABLE CONTENT- ADDRESSABLE MEMORY PROCESSOR
CHERP004	12/804,901	7/29/2010	9,047,334	6/2/2015	Title: MERGE-UPDATE FOR EFFICIENT ATOMIC MEMORY MODIFICATION IN CONCURRENT COMPUTER SYSTEMS
CHERP004+	61/273,178	7/31/2009			Title: MERGE-UPDATE FOR EFFICIENT ATOMIC MEMORY MODIFICATION IN CONCURRENT COMPUTER SYSTEMS

Case Number	Application No.	Filing Date	Patent Number	Issue Date	Title
CHERP004C1	14/697,938	4/28/2015			Title: MERGE-UPDATE FOR EFFICIENT ATOMIC MEMORY MODIFICATION IN CONCURRENT COMPUTER SYSTEMS
CHERP005	12/804,900	7/29/2010	8,838,656	9/16/2014	Title: HARDWARE-PROTECTED REFERENCE COUNT-BASED MEMORY MANAGEMENT USING WEAK REFERENCES
CHERP005+	61/273,177	7/31/2009			Title: WEAK REFERENCE MANAGEMENT FOR HARDWARE-PROTECTED CYCLE-FREE REFERENCE COUNT-BASED MEMORY RECLAMATION
CHERP005C1	14/457,046	8/11/2014			Title: HARDWARE-PROTECTED REFERENCE COUNT-BASED MEMORY MANAGEMENT USING WEAK REFERENCES
CHERP005C2	14/997,104	1/15/2016			Title: HARDWARE-PROTECTED REFERENCE COUNT-BASED MEMORY MANAGEMENT USING WEAK REFERENCES
CHERP006	12/890,471	9/24/2010			Title: COMPACT INSTRUCTION EXECUTION USING REGISTER TAG STATE
CHERP006+	61/279,380	10/19/2009			Title: METHOD OF COMPACT INSTRUCTION REPRESENTATION USING DYNAMIC TAG STATE
CHERP007	12/317,375	12/19/2008	8,370,458	2/5/2013	Title: HIERARCHICAL BLOCK- IDENTIFIED DATA COMMUNICATION FOR UNIFIED HANDLING OF STRUCTURED DATA AND DATA COMPRESSION
CHERP007+	61/008,657	12/21/2007			Title: HIERARCHICAL BLOCK- IDENTIFIED DATA COMMUNICATION FOR UNIFIED HANDLING OF STRUCTURED DATA AND DATA COMPRESSION
CHERP008+	61/281,417	11/16/2009			Title: HICAMP: A MEMORY ARCHITECTURE FOR FAULT- TOLERANT CONCURRENCY- SAFE SHARED STRUCTURED DATA ACCESS
CHERP009	13/541,396	7/3/2012			Title: MEMORY SHARING AND PAGE DEDUPLICATION USING INDIRECT LINES

Case Number	Application No.	Filing Date	Patent Number	Issue Date	Title
CHERP009+	61/504,669	7/5/2011			Title: MEMORY COMPACTION BY INDIRECT SHARED DATA LINES AND SOFTWARE PAGE DEDUPLICATION
CHERP010	13/712,878	12/12/2012	9,208,082	12/8/2015	Title: HARDWARE-SUPPORTED PER-PROCESS METADATA TAGS
CHERP010+	61/615,103	3/23/2012			Title: HARDWARE-SUPPORTED PER-PROCESS METADATA TAGS
CHERP010C1	14/880,248	10/11/2015			Title: HARDWARE-SUPPORTED PER-PROCESS METADATA TAGS
CHERP011	13/829,527	3/14/2013	44,074		Title: SPECIAL MEMORY ACCESS PATH WITH SEGMENT-OFFSET ADDRESSING
CHERP011+	61/615,102	3/23/2012			Title: SPECIAL MEMORY ACCESS PATH WITH SEGMENT-OFFSET ADDRESSING
CHERP012	12/137,919	6/12/2008	8,316,276	11/20/2012	Title: UPPER LAYER PROTOCOL (ULP) OFFLOADING FOR INTERNET SMALL COMPUTER SYSTEM INTERFACE (ISCSI) WITHOUT TCP OFFLOAD ENGINE (TOE)
CHERP013	14/058,919	10/21/2013			Title: FINE GRAINED ONLINE REMAPPING TO HANDLE MEMORY ERRORS
CHERP013+	61/738,887	12/18/2012			Title: FINE-GRAINED ONLINE REMAPPING TO HANDLE MEMORY ERRORS
CHERP014	14/178,038	2/11/2014			Title: HAREWARE-SUPPORTED MEMORY TEMPORAL COPY
CHERP014+	61/775,041	3/8/2013			Title: HARDWARE-SUPPORTED MEMORY TEMPORAL COPY AND LOGGING
CHERP015	14/479,676	9/8/2014			Title: HYBRID MAIN MEMORY USING A FINE-GRAIN LEVEL OF REMAPPING
CHERP015+	61/876,115	9/10/2013			Title: HYBRID MAIN MEMORY USING A FINE-GRAIN LEVEL OF REMAPPING
CHERP016	14/596,113	1/13/2015			Title: DEDUPLICATION-BASED DATA SECURITY

Case Number	Application No.	Filing Date	Patent Number	Issue Date	Title
CHERP016+	61/927,914	1/15/2014			Title: DEDUPLICATION-BASED MEMORY ENCRYPTION
CHERP017	14/178,130	2/11/2014			Title: HARDWARE SUPPORTED MEMORY LOGGING

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